



**1996
NEW RELEASES
DATA BOOK
Volume V**

Featuring:

- *Product Selection Tables and Trees*
- *Data Sheets*
- *Free Sample Request Cards*

Other Data Books Available from Maxim:

- *New Product Selector Guide*
- *1993 to 1995 New Releases Data Books, Volumes I through IV*
- *1994 Evaluation Kits Data Book*
- *Notebook Computer Applications Data Book*
- *High-Reliability Products Data Book*
- *High-Frequency ASIC Development Handbook*

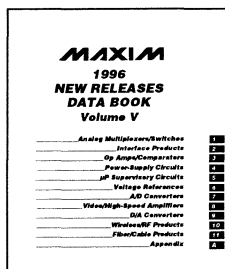
HOW TO USE THE 1996 NEW RELEASES DATA BOOK

Maxim's 1996 *New Releases Data Book* (Vol. V) brings together 177 new devices from 11 product families in a single, easy-to-use "Design Guide" format. Each section contains: (1) data sheets for all new products in that family of parts, (2) product-family selection tables and trees.

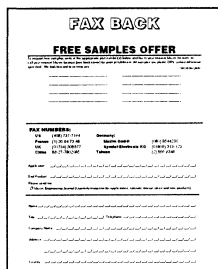
If you need samples for further evaluation, simply fill out one of the sample request cards and fax it to the nearest Maxim office, or call the nearest Maxim office (see back cover) for prompt fulfillment.

We've provided a variety of reference guides to help you locate a specific product or product family:

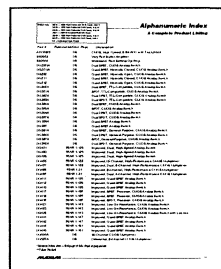
1	Analog Multiplexers/Switches
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5	μ P Supervisory Circuits
6	Voltage References
7	A/D Converters
8	Video/High-Speed Amplifiers
9	D/A Converters
10	Wireless/RF Products
11	Fiber/Cable Products



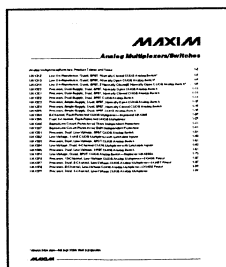
PRODUCT-FAMILY SECTIONS, INDICATED BY TAB NUMBER



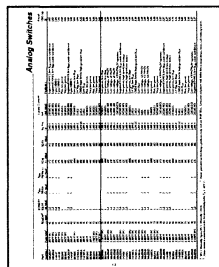
FREE SAMPLE REQUEST CARDS



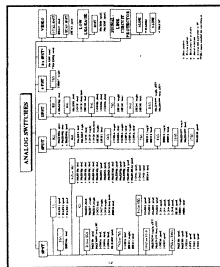
COMPLETE ALPHANUMERIC INDEX OF PART NUMBERS, CROSS REFERENCED TO OTHER MAXIM DATA BOOKS



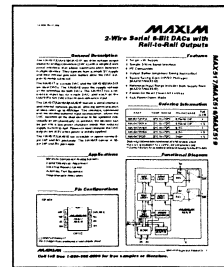
SECTION TABLES OF CONTENTS, SORTED BY PRODUCT FAMILY



PRODUCT-FAMILY SELECTION TABLES WITH SPECIFICATIONS, FEATURES, AND PRICING



PRODUCT-FAMILY SELECTION TREES



DATA SHEETS



1996
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Introduction

Maxim Integrated Products designs, develops, manufactures, and markets a broad range of linear and mixed-signal integrated circuits (ICs) for use in a variety of electronic products. These ICs "connect" the real (analog) world to the digital world. They detect, measure, amplify, and convert real-world signals—such as temperature, pressure, or sound—into digital signals a computer can process. Over the past 12 years, Maxim has introduced over 850 analog ICs—more than any other company.

Maxim is committed to meeting the needs of the industry through aggressive product development and superior quality. Our product lines include the following: micro-processor supervisory circuits, data converters, references, RS-232 interface circuits, amplifiers, power-control circuits, timers and counters, display circuits, multiplexers, switches, voltage detectors, and analog filters. In addition, the acquisition of Tektronix Integrated Circuits has expanded our product line to include high-frequency circuits.

Recognizing the growing demand for BiCMOS technology, Maxim has focused increasingly on CMOS- and BiCMOS-based products. These circuits are marketed worldwide, principally through distributors and independent sales representatives, and are available in several different packages and temperature ranges to meet varying customer requirements.

World Wide Web

Our full line of data sheets will be available on the World Wide Web. Look for our new *Product Selector Guide* in the Fall of 1995.

Customer Service

To request free samples and literature, call or fax your nearest Maxim location. Plus, evaluation kits or a small quantity of parts can be ordered using VISA or MasterCard by calling U.S. Headquarters at (800) 998-8800 extension 6380 (U.S. residents only) or (408) 737-7600 extension 6380.

Customer service representatives are available during normal business hours to provide information on orders placed directly with the factory or with any of our franchised distributors. Please see the back cover for a list of domestic and international sales representatives and distributors.

Technical Support

In order to provide full technical support, Maxim has a large, highly qualified group of senior applications engineers available to help you. Simply call U.S. headquarters (408) 737-7600 extension 4000, or fax your questions to (408) 732-8159.

Maxim also offers a wide variety of technical publications, including the new *Product Selector Guide* (available October 1995), *Maxim Engineering Journal* (a quarterly magazine explaining the application of our new products), *High-Reliability Products Data Book*, *New Releases Data Books*, *1994 Evaluation Kits Data Book*, *Notebook Computer Applications Data Book*, Design Guides for each product family, and the *High-Frequency ASIC Development Handbook*. Call your nearest Maxim location for any literature you may need.

Reliability

Maxim's mission is to provide reliable, innovative analog ICs that solve customer problems. Our programs offering complete lot traceability, life test, and humidity life qualification are unique in the industry.

ISO 9001/9002 Certification

In November 1993, the wafer fab at Maxim's Sunnyvale headquarters received formal ISO 9001 certification, validating that our quality system meets the worldwide standard. The wafer fab at our Beaverton, Oregon facility is also 9001 certified, as of July 1994. ISO 9001 is the most stringent of the 9000 series of specifications, because it includes review of design, test, manufacturing, and shipment processes.

In May 1995, ISO 9002 certification was granted to Maxim UK.

Information furnished by Maxim Integrated Products is believed to be accurate and reliable. However, the company cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product; nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Maxim Integrated Products. Maxim reserves the right to change the circuitry and specifications without notice.

Life Support Policy: Maxim does not authorize any Maxim product for use in life support devices and/or systems without the express written approval of an officer of Maxim Integrated Products, Inc. Life support devices or systems are devices or systems which, (i) are intended for surgical implant into the body or (ii) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

Products in this book may be covered by one or more of the patents listed below. Additional patents are pending.

4,700,286, 4,679,134, 4,636,930, 4,859,963, 4,857,778, 4,897,774, 4,797,899, 4,806,875, 4,847,522, 4,812,891, 4,809,152, 4,801,888, 4,797,569, 4,777,580, 4,777,577, 4,999,761, 4,752,700, 5,142,242, 5,055,796, 4,819,147, 5,027,165, 4,217,599, 4,261,761, 4,228,447, 4,229,756, 4,260,425, 4,435,655, 4,622,736, 4,628,406, 4,701,694, 4,714,872, 4,732,865, 4,733,218, 4,767,946, 4,769,619, 4,774,497, 4,774,478, 4,786,856, 4,819,049, 4,823,028, 4,862,096, 4,876,214, 4,902,640, 4,994,400, 4,994,694, 5,017,814, 5,209,117, 5,151,775, 5,247,468, 5,268,315.

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Part #	Publication/Doc. Page	Description
ADC0820	DS	CMOS, High-Speed, 8-Bit ADC with Track/Hold
BB3553	DS	Very Fast Buffer Amplifier
BB3554	DS	Wideband, Fast-Settling Op Amp
DG200/A	DS	Dual SPST, CMOS Analog Switch
DG201/A	DS	Quad SPST, Normally Closed, CMOS Analog Switch
DG202	DS	Quad SPST, Normally Open, CMOS Analog Switch
DG211	DS	Quad SPST, Normally Closed, CMOS Analog Switch
DG212	DS	Quad SPST, Normally Open, CMOS Analog Switch
DG300A	DS	Dual SPST, TTL-Compatible, CMOS Analog Switch
DG301A	DS	SPDT, TTL-Compatible, CMOS Analog Switch
DG302A	DS	Dual DPST, TTL-Compatible, CMOS Analog Switch
DG303A	DS	Dual SPDT, TTL-Compatible, CMOS Analog Switch
DG304A	DS	Dual SPST, CMOS Analog Switch
DG305A	DS	SPDT, CMOS Analog Switch
DG306A	DS	Dual DPST, CMOS Analog Switch
DG307A	DS	Dual SPDT, CMOS Analog Switch
DG308A	DS	Quad SPST Analog Switch
DG309	DS	Quad SPST Analog Switch
DG381A	DS	Dual SPST, General-Purpose, CMOS Analog Switch
DG384A	DS	Dual DPST, General-Purpose, CMOS Analog Switch
DG387A	DS	SPDT, General-Purpose, CMOS Analog Switch
DG390A	DS	Dual SPDT, General-Purpose, CMOS Analog Switch
DG401	95NR 1-125	Improved, Dual, High-Speed Analog Switch
DG403	95NR 1-125	Improved, Dual, High-Speed Analog Switch
DG405	95NR 1-125	Improved, Dual, High-Speed Analog Switch
DG406	95NR 1-128	Improved, 16-Channel, High-Performance CMOS Multiplexer
DG407	95NR 1-128	Improved, Dual, 8-Channel, High-Performance CMOS Multiplexer
DG408	93NR 1-31	Improved, 8-Channel, High-Performance CMOS Multiplexer
DG409	93NR 1-31	Improved, Dual, 4-Channel, High-Performance CMOS Multiplexer
DG411	95NR 1-135	Improved, Quad SPST Analog Switch
DG412	95NR 1-135	Improved, Quad SPST Analog Switch
DG413	95NR 1-135	Improved, Quad SPST Analog Switch
DG417	95NR 1-139	Improved, SPST, Precision, CMOS Analog Switch
DG418	95NR 1-139	Improved, SPST, Precision, CMOS Analog Switch
DG419	95NR 1-139	Improved, SPDT, Precision, CMOS Analog Switch
DG421	95NR 1-143	Improved, Low On-Resistance, CMOS Analog Switch
DG423	95NR 1-143	Improved, Low On-Resistance, CMOS Analog Switch
DG425	95NR 1-143	Improved, Low On-Resistance, CMOS Analog Switch with Latches
DG441	95NR 1-147	Improved, Quad SPST Analog Switch
DG442	95NR 1-147	Improved, Quad SPST Analog Switch
DG444	95NR 1-151	Improved, Quad SPST Analog Switch
DG445	95NR 1-151	Improved, Quad SPST Analog Switch
DG506A	DS	16-Channel CMOS Multiplexer
DG507A	DS	Differential, 8-Channel CMOS Multiplexer

*Advance Information—first page of data sheet in preparation.

**Future Product.

Alphanumeric Index

A Complete Product Listing

Part #	Publication/Doc. Page	Description
DG508A	DS	8-Channel CMOS Multiplexer
DG509A	DS	Differential, 4-Channel CMOS Multiplexer
DG528	DS	8-Channel, Latchable Multiplexer
DG529	DS	Differential, 4-Channel, Latchable Multiplexer
HI-201	DS	Quad SPST, CMOS Analog Switch
HI-201HS	DS	High-Speed, Quad SPST, CMOS Analog Switch
HI-508A	92NR 1-25	Fault-Protected, 8-Channel Multiplexer
HI-509A	92NR 1-25	Fault-Protected, Differential 4-Channel Multiplexer
ICL7106	DS	3 1/2-Digit ADC with Direct LCD Drivers
ICL7107	DS	3 1/2-Digit ADC with Direct LCD Drivers
ICL7109	DS	12-Bit ADC with Three-State Binary Outputs
ICL7116	DS	3 1/2-Digit ADC with Direct LCD Display Hold
ICL7117	DS	3 1/2-Digit ADC with Direct LED Display Hold
ICL7126	DS	Low-Power, 3 1/2-Digit ADC with Direct LCD Drivers
ICL7129A	DS	Low-Noise, 4 1/2-Digit, Single-Chip ADC with Multiplexed LCD Drivers
ICL7135	DS	4 1/2-Digit ADC with Multiplexed BCD Outputs
ICL7136	DS	Low-Power, 3 1/2-Digit ADC with Direct LCD Drivers
ICL7137	DS	Low-Power, 3 1/2-Digit ADC with Direct LED Drivers
ICL7611	DS	Low-Power Op Amp
ICL7612	DS	Low-Power Op Amp
ICL7614	DS	Low-Power Op Amp
ICL7616	DS	Low-Power Op Amp
ICL7621	DS	Dual, Low-Power Op Amp
ICL7622	DS	Dual, Low-Power Op Amp
ICL7631	DS	Triple, Low-Power Op Amp
ICL7632	DS	Triple, Low-Power Op Amp
ICL7641	DS	Quad, Low-Power Op Amp
ICL7642	DS	Quad, Low-Power Op Amp
ICL7650/B	DS	Chopper-Stabilized Op Amp
ICL7652/B	DS	Chopper-Stabilized Op Amp
ICL7660	93NR 4-141	10µA Charge-Pump Voltage Converter
ICL7662	DS	CMOS, Switched-Capacitor Voltage Converter (Up to 20V Input)
ICL7663	DS	Low-Power, Adjustable-Output, Positive-Voltage Linear Regulator
ICL7664	DS	Low-Power, Adjustable-Output, Negative-Voltage Linear Regulator
ICL7665	DS	µP Voltage Monitor with Dual Over/Undervoltage Detection
ICL7667	DS	Dual-Power MOSFET Driver (Inverting)
ICL8069	DS	1.2V Voltage Reference
ICM7211	DS	4-Digit, LCD Decoder/Driver
ICM7212	DS	4-Digit, LED Decoder/Driver
ICM7217	DS	4-Digit, Presetable, LED Up/Down Counter
ICM7218	DS	8-Digit, Multiplexed, LED Decoder/Driver
ICM7224	DS	4 1/2-Digit, LCD, High-Speed Counter/Decoder/Driver
ICM7225	DS	4 1/2-Digit, LED, High-Speed Counter/Decoder/Driver
ICM7228	DS	8-Digit, LED Display Driver

*Advance Information—first page of data sheet in preparation.

**Future Product.

Alphanumeric Index

A Complete Product Listing

Part #	Publication/Doc. Page	Description
ICM7240	DS	8-Bit Binary, Programmable, RC Timer/Counter
ICM7242	DS	7-Bit Binary, Fixed, RC Timer/Counter
ICM7250	DS	Two-Digit BCD, Programmable, RC Timer/Counter
ICM7260	DS	Module-60, Programmable, RC Timer/Counter
ICM7555	DS	Low-Power, General-Purpose Timer
ICM7556	DS	Low-Power, General-Purpose Dual Timer
IH5040	DS	SPST, Normally Open, CMOS Analog Switch
IH5041	DS	Dual SPST, Normally Open, CMOS Analog Switch
IH5042	DS	SPDT, CMOS Analog Switch
IH5043	DS	Dual SPDT, CMOS Analog Switch
IH5044	DS	DPST, Normally Open, CMOS Analog Switch
IH5045	DS	Dual DPST, Normally Open, CMOS Analog Switch
IH5047	DS	SPST, 5Ω, High-Level, CMOS Analog Switch
IH5048	DS	Dual SPST, Low Charge Injection Analog Switch
IH5048A	DS	Dual SPST, Low On-Resistance, Low Charge Injection Analog Switch
IH5049	DS	Dual DPST, Low Charge Injection Analog Switch
IH5050	DS	SPDT, Low Charge Injection Analog Switch
IH5051	DS	Dual SPDT, Low Charge Injection Analog Switch
IH5108	92NR 1-25	See MAX358
IH5140	DS	Low-Power, SPST, Fast, CMOS Analog Switch
IH5141	DS	Dual SPST, Low-Power, Fast, CMOS Analog Switch
IH5142	DS	SPDT, Low-Power, Fast, CMOS Analog Switch
IH5143	DS	Dual SPDT, Low-Power, Fast, CMOS Analog Switch
IH5144	DS	DPST, Low-Power, Fast, CMOS Analog Switch
IH5145	DS	Dual DPST, Low-Power, Fast, CMOS Analog Switch
IH5208	92NR 1-25	See MAX359
IH5341	DS	Dual SPST, RF/Video Switch
IH5352	DS	Quad SPST, RF/Video Switch
IH6108	DS	See DG508A
IH6116	DS	See DG506A
IH6208	DS	See DG509A
IH6216	DS	See DG507A
LH0033/A	DS	Fast Buffer Amplifier
LH0063	DS	Very Fast Buffer Amplifier
LH0101	DS	Power Op Amp
MAX038	95NR 10-3	High-Frequency Waveform Generator
MAX038EVKIT	DS	Evaluation Kit for the MAX038
MAX100	96NR 7-9	250Msps, 8-Bit ADC with Track/Hold
MAX100EVKIT	DS	Evaluation Kit for the MAX100
MAX101	96NR 7-25	500Msps, 8-Bit ADC with Track/Hold
MAX101EVKIT	DS	Evaluation Kit for the MAX101
MAX104	96NR 7-41*	1Gsps, 8-Bit ADC with Track/Hold
MAX1044	DS	10μA Charge-Pump Voltage Converter
MAX110	96NR 7-43	±5V, Low-Cost, 2-Channel, Serial ±14-Bit ADC

*Advance Information—first page of data sheet in preparation.

**Future Product.

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A Complete Product Listing

Part #	Publication/Doc. Page	Description
MAX110EVKIT	DS	Evaluation Kit for the MAX110/MAX111
MAX111	96NR 7-43	5V, Low-Cost, 2-Channel, Serial ± 14-Bit ADC
MAX120	95NR 7-15	500ksps, Sampling, 12-Bit ADC with Track/Hold and Reference
MAX120EVKIT	DS	Evaluation Kit for the MAX120
MAX121	DS	308ksps ADC with DSP Interface and 78dB SINAD
MAX121EVKIT	DS	Evaluation Kit for the MAX121
MAX122	95NR 7-15	333ksps, Sampling, 12-Bit ADC with Track/Hold and Reference
MAX1232	92NR 5-11	μ P Monitor
MAX1259	DS	Battery Manager
MAX130	DS	3 1/2-Digit ADC with Bandgap Reference
MAX131	DS	3 1/2-Digit ADC with Bandgap Reference
MAX132	93NR 7-15	± 18 -Bit, Low-Power ADC with Serial Interface
MAX132EVKIT	DS	Evaluation Kit for the MAX132
MAX133	DS	9V, 3 3/4-Digit DMM Circuit
MAX134	DS	± 5 V, 3 3/4-Digit DMM Circuit
MAX134EVBDR	DS	PC-Based Evaluation System for the MAX134
MAX135	93NR 7-15	± 15 -Bit, Low-Power ADC with Parallel Interface
MAX136	DS	Low-Power, 3 1/2-Digit ADC with Display Hold and Direct LCD Drivers
MAX138	DS	3 1/2-Digit ADC with Reference, Charge-Pump and Direct LED Drivers
MAX139	DS	3 1/2-Digit ADC with Reference, Charge-Pump and Direct LCD Drivers
MAX140	DS	3 1/2-Digit ADC with Reference, Charge-Pump and Low-Current LED Drivers
MAX146	96NR 7-65*	3V, Low-Power, 8-Channel, Serial 12-Bit DAS
MAX1480A	DS	Complete, 2.5Mbps, Isolated RS-485/RS-422 Data Interface
MAX1480B	95NR 2-7	Complete, 250kbps, Isolated RS-485/RS-422 Data Interface
MAX1482	96NR 2-7	20μA, 1/8-Unit-Load, Slew-Rate-Limited, Full-Duplex RS-485 Transceiver
MAX1483	96NR 2-7	20μA, 1/8-Unit-Load, Slew-Rate-Limited, Half-Duplex RS-485 Transceiver
MAX1487	DS	1/4-Unit Load, Half-Duplex RS-485/RS-422 Transceiver
MAX1487E**	96NR 2-19	2.5Mbps, ± 15kV ESD-Protected, Low-Power, RS-485/RS-422 Transceiver
MAX1488E	96NR 2-31*	± 15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver
MAX1489E	96NR 2-33*	± 15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver
MAX149	96NR 7-67*	3V, Low-Power, 8-Channel, Serial 10-Bit DAS
MAX150	DS	CMOS, 1.3 μ s, 8-Bit ADC with Voltage Reference and Track/Hold
MAX151	92NR 7-21	300kHz, 10-Bit ADC with Reference and Track/Hold
MAX152	DS	3V, 8-Bit ADC with 1 μ A Power-Down
MAX152EVKIT	DS	Evaluation Kit for the MAX152
MAX153	DS	1Msps, μ P-Compatible, 8-Bit ADC with 1 μ A Power-Down
MAX154	DS	CMOS, High-Speed, 8-Bit ADC with Multiplexer and Reference
MAX155	93NR 7-33	High-Speed, 8-Channel, 8-Bit ADC with Simultaneous Track/Holds and Reference
MAX155EVKIT	DS	Evaluation Kit for the MAX155
MAX156	93NR 7-33	High-Speed, 4-Channel, 8-Bit ADC with Simultaneous Track/Holds and Reference
MAX158	DS	CMOS, High-Speed, 8-Bit ADC with Multiplexer and Reference
MAX160	DS	CMOS, μ P-Compatible, 4 μ s, 8-Bit ADC

*Advance Information—first page of data sheet in preparation.

**Future Product.

Edition Key: **96NR** – 1996 New Releases Data Book, Vol. V
 95NR – 1995 New Releases Data Book, Vol. IV
 94NR – 1994 New Releases Data Book, Vol. III
 94EV – 1994 Evaluation Kits Data Book
 93NR – 1993 New Releases Data Book, Vol. II
 92NR – 1992 New Releases Data Book, Vol. I
 DS – Individual Data Sheet

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A Complete Product Listing

Part #	Publication/Doc. Page	Description
MAX1600	96NR 4-11*	Dual-Channel Cardbus and PCMCIA Vcc/Vpp Power-Switching Network
MAX1601	96NR 4-19*	Dual-Channel Cardbus and PCMCIA Power-Switch with SMBus™ Serial Interface
MAX161	DS	CMOS, 20μs, 8-Bit, 8-Channel Data-Acquisition System
MAX1610	96NR 4-31*	Digitally Controlled CCFL Backlight Power Supply
MAX1611	96NR 4-31*	Digitally Controlled CCFL Backlight Power Supply w/SMBus™ Interface
MAX162	92NR 7-37	CMOS, 3μs, 12-Bit ADC with Reference
MAX1620	96NR 4-33*	Digitally Adjustable LCD Bias Supply
MAX1621	96NR 4-33*	Digitally Adjustable LCD Bias Supply
MAX1622	96NR 4-33*	Digitally Adjustable LCD Bias Supply
MAX1626	96NR 4-35*	100% Duty Cycle, PFM, 5V or 3.3V, Pin-Selectable, Step-Down DC-DC Controller
MAX1627	96NR 4-35*	100% Duty Cycle, PFM, 1.3V to Input Adjustable, Step-Down DC-DC Controller
MAX163	92NR 7-53	CMOS, 5V-Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX164	92NR 7-53	CMOS, 5V-Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX1649	96NR 4-37	5V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller
MAX165	93NR 7-53	5μs, 8-Bit ADC with Track/Hold and Reference
MAX1651	96NR 4-37	3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller
MAX166	93NR 7-53	Differential Input, 5μs, 8-Bit ADC with Track/Hold and Reference
MAX167	92NR 7-53	CMOS, ±2.5V Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX168	93NR 7-65	14-Bit, 250ksps ADC with Track/Hold and Reference
MAX1691	96NR 5-5	Integrated μP Supervisory Module with Lithium Backup Battery
MAX170	DS	Serial-Output, 5.6μs, 12-Bit ADC with Reference
MAX171	92NR 7-67	Opto-Isolated, Serial-Output, 5.8μs, 12-Bit ADC
MAX172	92NR 7-77	CMOS, 10μs, 12-Bit ADC with Reference
MAX173	DS	CMOS, 5μs, 10-Bit ADC with Reference
MAX1732	94NR 4-15	12V, 120mA Flash Memory Programmer Module
MAX1738	94NR 4-23	See MAX738 Data Sheet
MAX174	DS	Industry-Standard, 12-Bit ADC with Reference
MAX1743	94NR 4-27	See MAX743 Data Sheet
MAX176	94NR 7-73	Serial-Output, 250ksps, 12-Bit ADC with Track/Hold and Reference
MAX176EVKIT	DS	Evaluation Kit for the MAX176
MAX177	DS	CMOS, 12-Bit ADC with Track/Hold and Reference
MAX1771	DS	12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller
MAX1771EVKIT	DS	Evaluation Kit for the MAX1771
MAX178	92NR 7-99	Calibrated, 12-Bit ADC with Track/Hold and Reference
MAX180	92NR 7-111	Complete, 100ksps, 8-Channel, 12-Bit Data-Acquisition System
MAX180EVKIT	DS	Evaluation Kit for the MAX180
MAX181	92NR 7-111	Complete, 100ksps, 6-Channel, 12-Bit Data-Acquisition System
MAX182	92NR 7-131	Calibrated, 4-Channel, 12-Bit ADC with Track/Hold and Reference
MAX183	92NR 7-143	3μs, 12-Bit ADC

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX184	92NR 7-143	5 μ s, 12-Bit ADC
MAX185	92NR 7-143	10 μ s, 12-Bit ADC
MAX186	DS	Low-Power, 8-Channel, 133ksps, Serial 12-Bit ADC with Track/Hold and Reference
MAX186EVKIT	DS	Evaluation Kit for the MAX186
MAX187	95NR 7-43	Low-Power, Serial 12-Bit ADC with Track/Hold and Reference (8-Pin)
MAX187EVKIT	DS	Evaluation Kit for the MAX187
MAX188	DS	Low-Power, 8-Channel, 133ksps, Serial 12-Bit ADC with Track/Hold and Reference
MAX189	95NR 7-43	Low-Power, Serial 12-Bit, ADC with Track/Hold and Reference (8-Pin)
MAX190	DS	75ksps, 5V, 12-Bit ADC with Track/Hold and Reference
MAX190EVKIT	DS	Evaluation Kit for the MAX190
MAX191	94NR 7-113	Low-Power, Sampling, 12-Bit ADC with Reference and Power-Down
MAX191EVKIT	DS	Evaluation Kit for the MAX191
MAX192	95NR 7-61	Low-Power, 8-Channel, Serial, 10-Bit ADC
MAX194	96NR 7-69	85ksps, Serial 14-Bit ADC with 10μA Shutdown
MAX194EVC16	DS	Evaluation System for the MAX194/MAX195
MAX194EVKIT	DS	Evaluation Kit for the MAX194/MAX195
MAX195	96NR 7-93	16-Bit, 85ksps ADC with 10μA Shutdown
MAX195EVKIT	DS	Evaluation Kit for the MAX195
MAX196	96NR 7-119*	8-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection
MAX197	96NR 7-121	8-Channel, Multi-Range, 5V, 12-Bit DAS with 8+4 Bus Interface and Fault Protection
MAX197EVKIT	DS	Evaluation Kit for the MAX197
MAX198	96NR 7-119*	8-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection
MAX199	96NR 7-137	8-Channel, Multi-Range, 5V, 12-Bit DAS with 8+4 Bus Interface and Fault Protection
MAX200	95NR 2-23	5V, 5-Channel RS-232 Transmitter with 0.1 μ F External Capacitors
MAX2003	96NR 4-49	NiCd/NiMH Battery Fast-Charge Controller
MAX2003A	96NR 4-49	NiCd/NiMH Battery Fast-Charge Controller with Pulse Trickle
MAX2003EVKIT	DS	Evaluation Kit for the MAX2003
MAX201	95NR 2-23	5V/9V to 13.2V, Dual RS-232 Transceiver with 0.1 μ F External Capacitors
MAX202	95NR 2-23	5V, Dual RS-232 Transceiver with 0.1 μ F External Capacitors
MAX202E	95NR 2-43	$\pm$ 15kV ESD-Protected, 5V RS-232 Transceiver
MAX203	95NR 2-43	Complete, 5V, Dual RS-232 Transceiver
MAX203E	96NR 2-35*	$\pm$15kV ESD-Protected, Complete, 5V, Dual RS-232 Transceiver
MAX204	95NR 2-23	5V, Quad RS-232 Transmitter with 0.1 μ F External Capacitors
MAX205	95NR 2-23	Complete, 5V, 5-Channel RS-232 Transceiver
MAX206	95NR 2-23	5V RS-232 Transceiver with 0.1 μ F External Capacitors
MAX207	95NR 2-23	5V RS-232 Transceiver with 0.1 μ F External Capacitors
MAX208	95NR 2-23	5V, Quad RS-232 Transceiver with 0.1 μ F External Capacitors
MAX209	95NR 2-23	5V RS-232 Transceiver with 0.1 μ F External Capacitors

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX2100 Cells	96NR 10-3	Quadrature Digitizer Circuits
MAX2101	96NR 10-11	6-Bit Quadrature Digitizer
MAX2101EVKIT	DS	Evaluation Kit for the MAX2101
MAX211	95NR 2-23	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX211E	95NR 2-43	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX212	95NR 2-57	3V, 3-Driver/5-Receiver, True RS-232 Serial Port
MAX213	95NR 2-23	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX213E	95NR 2-43	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX214	95NR 2-65	5V, Programmable, DTE/DCE RS-232 Transceiver
MAX216	94NR 2-45	Low-Power, Appletalk™ Interface Transceiver
MAX218	DS	1.8V to 4.25V V _{IN} , Dual RS-232 Transceiver
MAX220	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX222	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX223	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX225	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX230	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX231	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX232	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX232A	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX232E	95NR 2-43	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX233	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX233A	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX234	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX235	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX236	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX237	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX238	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX239	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX240	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX2402	96NR 10-33	800MHz to 1000MHz Spread-Spectrum Transmitter
MAX2402EVKIT	DS	Evaluation Kit for the MAX2402
MAX241	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX241E	95NR 2-43	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX242	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX243	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX2430	96NR 10-39*	900MHz, 100mW/250mW Power Amplifier
MAX244	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX245	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX2450	96NR 10-41*	70MHz Modulator/Demodulator
MAX2451	96NR 10-43*	70MHz Demodulator
MAX2452	96NR 10-45*	70MHz Modulator
MAX246	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX247	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX248	DS	5V, Multi-Channel RS-232 Driver/Receiver

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX249	DS	5V, Multi-Channel RS-232 Driver/Receiver
MAX250	92NR 2-57	5V, Isolated, RS-232 Driver/Receiver
MAX251	92NR 2-57	5V, Isolated, RS-232 Driver/Receiver
MAX252	DS	Complete, 5V, Isolated, Dual RS-232 Transceiver Module
MAX253	95NR 2-121	Isolated RS-485 Power Driver
MAX260	92NR 6-13	μP-Programmable, Universal Switched-Capacitor Filter
MAX261	92NR 6-13	μP-Programmable, Universal Switched-Capacitor Filter
MAX262	92NR 6-13	μP-Programmable, Universal Switched-Capacitor Filter
MAX263	92NR 6-37	Pin-Programmable, Universal Switched-Capacitor Filter
MAX264	92NR 6-37	Pin-Programmable, Universal Switched-Capacitor Filter
MAX265	DS	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter
MAX266	DS	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter
MAX267	92NR 6-37	Pin-Programmable, Bandpass Switched-Capacitor Filter
MAX268	92NR 6-37	Pin-Programmable, Bandpass Switched-Capacitor Filter
MAX270	92NR 6-61	Digitally Programmable, Dual, 2nd-Order, Continuous Lowpass Filter
MAX271	92NR 6-61	Digitally Programmable, Dual, 2nd-Order, Continuous Lowpass Filter with Track/Hold
MAX274	93NR 6-3	8th-Order, Continuous Analog Filter
MAX274/5SOFT	94EV 2-3	Filter Design Software for the MAX274/MAX275
MAX274EVKIT	94EV 2-3	Evaluation Kit for the MAX274
MAX275	93NR 2-3	4th-Order, Continuous Analog Filter
MAX280	DS	5th-Order, Zero-Error, Butterworth, Switched-Capacitor Lowpass Filter
MAX281	92NR 6-91	5th-Order, Zero-Error, Bessel, Switched-Capacitor Lowpass Filter
MAX291	93NR 6-31	8th-Order, Butterworth, Clock-Tunable, 100:1 Lowpass Filter
MAX292	93NR 6-31	8th-Order, Bessel, Clock-Tunable, 100:1 Lowpass Filter
MAX293	93NR 6-39	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX294	93NR 6-39	8th-Order, Elliptic, 1.2 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX295	93NR 6-31	8th-Order, Butterworth, Clock-Tunable, 50:1 Lowpass Filter
MAX296	93NR 6-31	8th-Order, Bessel, Clock-Tunable, 50:1 Lowpass Filter
MAX297	93NR 6-39	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 50:1 Lowpass Filter
MAX301	95NR 1-9	Low-On Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX303	95NR 1-9	Low-On Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX305	95NR 1-9	Low-On Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX306	95NR 1-17	Precision, 16-Channel, High-Performance, CMOS Analog Multiplexer
MAX307	95NR 1-17	Precision, 8-Channel, High-Performance, CMOS Analog Multiplexer
MAX308	95NR 1-29	Precision, 8-Channel, High-Performance, CMOS Analog Multiplexer
MAX309	95NR 1-29	Precision, Dual, 4-Channel, High-Performance, CMOS Analog Multiplexer
MAX310	92NR 8-17	8-Channel, CMOS RF/Video Multiplexer
MAX311	92NR 8-17	Differential 4-Channel, CMOS RF/Video Multiplexer
MAX312	96NR 1-9*	Low-On Resistance, Quad, SPST, Normally Closed, CMOS Analog Switch
MAX313	96NR 1-9*	Low-On Resistance, Quad, SPST, Normally Open, CMOS Analog Switch
MAX314	96NR 1-9*	Low-On Resistance, Quad, SPST, 2 Normally Open/2 Normally Closed, CMOS Analog Switch
MAX317	DS	Precision, SPST, CMOS Analog Switch

*Advance Information—first page of data sheet in preparation.

**Future Product.

Edition Key: 96NR – 1996 New Releases Data Book, Vol. V
 95NR – 1995 New Releases Data Book, Vol. IV
 94NR – 1994 New Releases Data Book, Vol. III
 94EV – 1994 Evaluation Kits Data Book
 93NR – 1993 New Releases Data Book, Vol. II
 92NR – 1992 New Releases Data Book, Vol. I
 DS – Individual Data Sheet

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Part #	Publication/Doc. Page	Description
MAX318	DS	Precision, SPST, CMOS Analog Switch
MAX319	DS	Precision, SPST, CMOS Analog Switch
MAX320	96NR 1-11	Precision, Dual-Supply, Dual, SPST, Normally Open CMOS Analog Switch
MAX321	96NR 1-11	Precision, Dual-Supply, Dual SPST, Normally Closed CMOS Analog Switch
MAX3212	96NR 2-37	1μA, 2.7V to 3.6V, 3-Driver/5-Receiver, True RS-232 Transceiver
MAX3218	96NR 2-49	1μA, 1.8V to 4.25V RS-232 Transceiver with AutoShutdown™
MAX322	96NR 1-11	Precision, Dual-Supply, Dual, SPST CMOS Analog Switch
MAX3222	96NR 2-61	300μA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1μF Capacitors
MAX3223	96NR 2-73	1μA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown™
MAX323	96NR 1-19	Precision, Single-Supply, SPST, Normally Open Analog Switch
MAX3232	96NR 2-61	300μA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1μF Capacitors
MAX324	96NR 1-19	Precision, Single-Supply, SPST, Normally Closed Analog Switch
MAX3241	96NR 2-61	300μA, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1μF Capacitors
MAX3243	96NR 2-73	1μA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown™
MAX325	96NR 1-19	Precision, Single-Supply, SPST, Analog Switch
MAX326	DS	Quad SPST, Ultra-Low-Leakage, CMOS Analog Switch
MAX3260	96NR 11-3	1GHz Transimpedance Preamplifier with 25dB Dynamic Range
MAX3261	96NR 11-7	Single 5V, Fully Integrated, 1.2Gbps Laser Diode Driver
MAX3262	96NR 11-19	1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection
MAX3263	96NR 11-27*	Single 5V, Fully Integrated, 155 Mbps Laser Diode Driver
MAX327	DS	Quad SPST, Ultra-Low-Leakage, CMOS Analog Switch
MAX3270	96NR 11-29	155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector
MAX328	DS	Ultra-Low-Leakage, Single-Ended, Monolithic, CMOS Analog Multiplexer
MAX329	DS	Ultra-Low-Leakage, Differential, Monolithic, CMOS Analog Multiplexer
MAX331	DS	Quad, SPST, Normally Closed, CMOS Analog Switch
MAX332	DS	Quad, SPST, Normally Open, CMOS Analog Switch
MAX333	DS	Quad, SPDT, CMOS Analog Switch
MAX333A	95NR 1-51	Improved, Quad, SPDT, CMOS Analog Switch
MAX334	DS	Quad, SPST, High-Speed, Break-Before-Make Analog Switch
MAX335	95NR 1-59	Serial-Controlled, Octal SPST Analog Switch
MAX338	95NR 1-69	8-Channel, Low-Leakage, CMOS Analog Multiplexer
MAX339	95NR 1-69	Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexer
MAX341	DS	Dual, SPST, High-Voltage, CMOS/DMOS Analog Switch
MAX343	DS	Dual, SPDT, High-Voltage, CMOS/DMOS Analog Switch
MAX345	DS	Dual, DPST, High-Voltage, CMOS/DMOS Analog Switch
MAX348	DS	Low On-Resistance, Dual, SPST, High-Voltage, CMOS/DMOS Analog Switch
MAX3483	96NR 2-87	3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver
MAX3485	96NR 2-87	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3486	96NR 2-87	3.3V, 2.5Mbps, True RS-485/RS-422 Transceiver

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX3488	96NR 2-87	3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver
MAX3490	96NR 2-87	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3491	96NR 2-87	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX351	95NR 1-81	Precision, Quad, SPST Analog Switch
MAX352	95NR 1-81	Precision, Quad, SPST Analog Switch
MAX353	95NR 1-81	Precision, Quad, Normally Closed, SPST Analog Switch
MAX354	96NR 1-29	Single, 8-Channel, Fault-Protected CMOS Multiplexer—Improved MAX358
MAX355	96NR 1-29	Dual, 4-Channel, Fault-Protected CMOS Multiplexer
MAX358	92NR 1-25	8-Channel, Fault-Protected Multiplexer
MAX359	92NR 1-25	Differential 4-Channel, Fault-Protected Multiplexer
MAX361	95NR 1-91	Precision, Quad, SPST Analog Switch
MAX362	95NR 1-91	Precision, Quad, SPST Analog Switch
MAX364	95NR 1-99	Precision, Quad, SPST Analog Switch
MAX365	95NR 1-99	Precision, Quad, SPST Analog Switch
MAX366	96NR 1-41	Signal-Line Circuit Protector with Three Independent Protectors
MAX367	96NR 1-41	Signal-Line Circuit Protector with Eight Independent Protectors
MAX368	92NR 1-37	8-Channel, Fault-Protected, Latched Multiplexer
MAX369	92NR 1-37	Differential 4-Channel, Fault-Protected, Latched Multiplexer
MAX378	DS	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX379	DS	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX381	96NR 1-51	Precision, Dual, Low-Voltage, SPST CMOS Analog Switch
MAX382	96NR 1-63	Low-Voltage, 1-of-8 CMOS Multiplexer with Latchable Inputs
MAX383	96NR 1-51	Precision, Dual, Low-Voltage, SPDT CMOS Analog Switch
MAX384	96NR 1-63	Low-Voltage, Dual, 4-Channel CMOS Multiplexer with Latchable Inputs
MAX385	96NR 1-51	Precision, Dual, Low-Voltage, DPST CMOS Analog Switch
MAX388	DS	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX389	DS	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX391	95NR 1-133	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX392	95NR 1-133	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX393	95NR 1-133	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX394	96NR 1-75	Low-Voltage, Quad, SPDT, CMOS Analog Switch—Replaces MAX333A
MAX396	96NR 1-87	Precision, 16-Channel, Low-Voltage, CMOS Analog Multiplexer— DG406 Pinout
MAX397	96NR 1-87	Precision, Dual, 8-Channel, Low-Voltage, CMOS Analog Multiplexer— DG407 Pinout
MAX398	96NR 1-99	Precision, 8-Channel, Low-Voltage, CMOS Analog Multiplexer— DG408 Pinout
MAX399	96NR 1-99	Precision, Dual, 4-Channel, Low-Voltage, CMOS Analog Multiplexer
MAX400	DS	Ultra-Low-Offset Op Amp
MAX400S	96NR 8-5	950MHz FET-Input Buffer with 75Ω Output
MAX402	DS	High-Speed, Low-Voltage, Micropower Op Amp
MAX403	DS	High-Speed, Low-Voltage, Micropower Op Amp
MAX404	92NR 8-25	Video Op Amp
MAX405	92NR 8-29	Precision Video Buffer Amplifier

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX406	94NR 3-19	1.2μA Max, Single-Supply Op Amp
MAX407	94NR 3-19	1.2μA Max, Dual, Single-Supply Op Amp
MAX408	DS	High-Speed, High Output Current Op Amp
MAX409	94NR 3-19	1.2μA Max, 150kHz, Single-Supply Op Amp
MAX410	94NR 3-33	Single, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX4100	96NR 8-9*	600MHz, High-Speed, Low-Power Op Amp
MAX4101	96NR 8-9*	750MHz, High-Speed, Low-Power Op Amp
MAX4102	96NR 8-11*	300MHz, High-Speed, Low-Power Video Op Amp
MAX4103	96NR 8-11*	450MHz, High-Speed, Low-Power Video Op Amp
MAX4104	96NR 8-13*	750MHz, Ultra-High-Speed, Low-Noise Op Amp
MAX4105	96NR 8-13*	750MHz, Ultra-High-Speed, Low-Noise Op Amp
MAX4106	96NR 8-15*	550MHz, High-Speed, Ultra-Low-Noise Op Amp
MAX4107	96NR 8-15*	500MHz, High-Speed, Ultra-Low-Noise Op Amp
MAX4108	96NR 8-17*	550MHz, High-Speed, Low-Distortion Op Amp
MAX4109	96NR 8-17*	500MHz, High-Speed, Low-Distortion Op Amp
MAX4111	96NR 8-19	330MHz Buffered Video Switch/Crosspoint Building Block
MAX4112	96NR 8-31*	500MHz, High-Speed, Current-Mode Feedback Op Amp
MAX4113	96NR 8-31*	375MHz, High-Speed, Current-Mode Feedback Op Amp
MAX412	94NR 3-33	Dual, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX4121	96NR 8-19	330MHz Buffered Video Switch/Crosspoint Building Block
MAX414	94NR 3-33	Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX4141	96NR 8-33	330MHz Buffered Video Switch/Crosspoint Building Block
MAX417	94NR 3-19	Dual, 1.2μA Max, Single-Supply Op Amp
MAX4177	96NR 8-41*	380MHz, Gain of +1, High-Speed Buffer
MAX418	94NR 3-19	Quad, 1.2μA Max, Single-Supply Op Amp
MAX419	94NR 3-19	Quad, 1.2μA Max, Single-Supply Op Amp
MAX4193	92NR 4-45	CMOS, Micropower, Step-Up Switching Regulator
MAX420	DS	±15V Chopper-Stabilized Op Amp
MAX421	DS	±15V Chopper-Stabilized Op Amp
MAX422	DS	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX4221	96NR 8-19	330MHz Buffered Video Switch/Crosspoint Building Block
MAX423	DS	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX427	94NR 3-45	Low-Noise, High-Precision Op Amp
MAX4277	96NR 8-41*	350MHz, Gain of +2, High-Speed Buffer
MAX428	DS	Dual, High-Speed, High Output Current Op Amp
MAX430	DS	±15V Chopper-Stabilized Op Amp
MAX432	DS	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX435	94NR 8-5	250MHz Wideband Transconductance Amplifier with Differential Output
MAX436	94NR 8-5	250MHz Wideband Transconductance Amplifier with Single-Ended Output
MAX437	94NR 3-45	Low-Noise, High-Precision Op Amp
MAX438	DS	High-Speed, Low-Voltage, Micropower Op Amp
MAX439	DS	High-Speed, Low-Voltage, Micropower Op Amp
MAX4391	92NR 4-65	CMOS, Micropower, Inverting Switching Regulator
MAX440	DS	8-Channel, High-Speed, Video Multiplexer/Amplifier

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX441	DS	4-Channel, High-Speed, Video Multiplexer/Amplifier
MAX442	DS	2-Channel, 140MHz, Video Multiplexer/Amplifier
MAX4420	94NR 4-31	High-Speed, 6A MOSFET Driver (Noninverting)
MAX4426	DS	Dual, High-Speed, 1.5A MOSFET Driver (Inverting)
MAX4427	DS	Dual, High-Speed, 1.5A MOSFET Driver (Noninverting)
MAX4428	DS	Dual, High-Speed, 1.5A MOSFET Driver (Inverting & Noninverting)
MAX4429	94NR 4-31	High-Speed, 6A MOSFET Driver (Inverting)
MAX445	DS	Low-Cost, High-Resolution, 200MHz Video CRT Driver
MAX445EVKIT	DS	Evaluation Kit for the MAX445
MAX448	DS	Quad, High-Speed, High Output Current Op Amp
MAX450	DS	10MHz Video Amplifier
MAX451	DS	Low-Bias-Current, 10MHz Video Amplifier
MAX452	92NR 8-37	50MHz Video Amplifier
MAX453	92NR 8-37	2-Channel, 50MHz Video Multiplexer/Amplifier
MAX454	92NR 8-37	4-Channel, 50MHz Video Multiplexer/Amplifier
MAX455	92NR 8-37	8-Channel, 50MHz Video Multiplexer/Amplifier
MAX456	DS	8x8 Crosspoint Video Switch
MAX457	92NR 8-47	Dual, 70MHz Video Amplifier
MAX458	DS	8x4 Video Crosspoint Switches with Buffers
MAX459	DS	8x4 Video Crosspoint Switches with Buffers
MAX459EVKIT	DS	Evaluation Kit for the MAX459
MAX460	DS	High-Accuracy Fast Buffer
MAX463	95NR 8-23	100MHz, Triple RGB Video Switch with Buffer
MAX464	95NR 8-23	100MHz, Quad RGB Video Switch with Buffer
MAX464EVKIT	DS	Evaluation Kit for the MAX464
MAX465	95NR 8-23	100MHz, Triple RGB Video Switch with $A_v = 2V/V$ Buffer
MAX466	95NR 8-23	100MHz, Quad RGB Video Switch with $A_v = 2V/V$ Buffer
MAX466EVKIT	DS	Evaluation Kit for the MAX466
MAX467	95NR 8-23	100MHz, Triple RGB Video Buffer
MAX468	95NR 8-23	100MHz, Quad Video Buffer
MAX469	95NR 8-23	100MHz, Triple RGB Video Buffer ($A_v = 2V/V$)
MAX470	95NR 8-23	100MHz, Quad Video Buffer ($A_v = 2V/V$)
MAX471	96NR 3-7	Precision, High-Side Current-Sense Amplifier
MAX472	96NR 3-7	Precision, High-Side Current-Sense Amplifier
MAX473	96NR 3-19	Single, 10MHz, Single-Supply Op Amp
MAX474	96NR 3-19	Dual, 10MHz, Single-Supply Op Amp
MAX475	96NR 3-19	Quad, 10MHz, Single-Supply Op Amp
MAX476	96NR 8-43*	325MHz High-Speed Op Amp
MAX477	DS	425MHz High-Speed Amplifier and Buffer
MAX478	94NR 3-59	17 μ A Max, Dual, Single-Supply, Precision Op Amp
MAX479	94NR 3-59	17 μ A Max, Quad, Single-Supply, Precision Op Amp
MAX480	DS	High-Precision, Low-Voltage, Micropower Op Amp
MAX481	DS	500 μ A RS-485 Transceiver with Low-Power Shutdown
MAX481E**	96NR 2-19	2.5Mbps, ± 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver

*Advance Information—first page of data sheet in preparation.

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MAX483	DS	Slew-Rate-Limited, 350µA RS-485 Transceiver with Low-Power Shutdown
MAX483E**	96NR 2-19	250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with Shutdown
MAX485	DS	500µA, RS-485 Transceiver—Direct LTC485 Replacement
MAX485E**	96NR 2-19	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver
MAX487	DS	Slew-Rated-Limited, 350µA RS-485 Transceiver with 1/4-Unit Load
MAX487E**	96NR 2-19	250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with 1/4-Unit Load
MAX488	DS	Slew-Rated-Limited, 350µA, Full-Duplex RS-485 Transceiver
MAX488E**	96NR 2-19	250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver
MAX489	DS	Slew-Rated-Limited, 350µA, Full-Duplex RS-485 Transceiver
MAX489E**	96NR 2-19	250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver
MAX490	DS	500µA, Full-Duplex RS-485 Transceiver
MAX490E**	96NR 2-19	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver
MAX491	DS	500µA, Full-Duplex RS-485 Transceiver
MAX491E	96NR 2-19	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver
MAX492	96NR 3-31	Dual, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp
MAX494	96NR 3-31	Quad, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp
MAX495	96NR 3-31	Single, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp
MAX496	96NR 8-45*	430MHz Quad Video Buffer
MAX497	96NR 8-45*	375MHz Quad Video Buffer
MAX498	96NR 8-47*	Two-Channel, Quad RGB Video Switch with Gain of +2 Buffers
MAX499	96NR 8-47*	Two-Channel, Triple RGB Video Switch with Gain of +2 Buffers
MAX500	DS	CMOS, Quad, Serial 8-Bit DAC
MAX501	93NR 9-5	Voltage-Output, Multiplying, 12-Bit DAC with 8+4 Interface
MAX502	93NR 9-5	Voltage-Output, Multiplying, 12-Bit DAC with 12-Bit Interface
MAX503	96NR 9-7	5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC
MAX504	96NR 9-23	5V, Low-Power, Voltage-Output, Serial, 10-Bit DAC with Internal Reference
MAX505	DS	Quad, 8-Bit DAC with Rail-to-Rail Outputs
MAX506	DS	Quad, 8-Bit DAC with Rail-to-Rail Output
MAX507	93NR 9-33	Voltage-Output, 12-Bit DAC with Internal Reference and 12-Bit Interface
MAX508	93NR 9-33	Voltage-Output, 12-Bit DAC with Internal Reference and 8+4 Interface
MAX509	DS	Quad, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX510	DS	Quad, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX512	DS	5V, Triple, Voltage-Output, Serial, 8-Bit DAC
MAX513	DS	3V, Triple, Voltage-Output, Serial, 8-Bit DAC
MAX514	93NR 9-45	Quad, CMOS, Serial, Multiplying, 12-Bit DAC
MAX515	96NR 9-23	5V, Low-Power, Voltage-Output, Serial, 10-Bit DAC
MAX516	92NR 9-21	Quad, DAC-Programmed, CMOS Comparator
MAX517	96NR 9-37	Single, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX518	96NR 9-37	Dual, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX519	96NR 9-37	Dual, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX520	96NR 9-53*	Quad, 2-Wire, Serial, 8-Bit DAC with Unbuffered Outputs
MAX521	96NR 9-55	Octal, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Output
MAX522	96NR 9-69	Dual, Voltage-Output, Serial, 8-Bit DAC in 8-Pin Package
MAX526	DS	Calibrated, Quad, Voltage-Output, 12-Bit DAC
MAX527	DS	±5V, Calibrated, Quad, Voltage-Output, 12-Bit DAC
MAX528	93NR 9-69	Octal, Serial, 8-Bit DAC with Output Buffers
MAX529	93NR 9-69	±5V, Octal, Serial, 8-Bit DAC with Output Buffers
MAX530	DS	5V, Low-Power, Voltage-Output, Parallel, 12-Bit DAC with Reference
MAX531	DS	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC with Reference
MAX532	95NR 9-53	Dual, Serial-Input, Voltage-Output, Multiplying, 12-Bit DAC
MAX536	95NR 9-67	Quad, Serial, Voltage-Output, -5V/12V/15V, 12-Bit DAC
MAX537	95NR 9-67	Quad, Serial, Voltage-Output, ±5V, 12-Bit DAC
MAX538	DS	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC, 0V to 2.5V Output
MAX539	DS	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC, 0V to 2.5V Output
MAX543	DS	Serial, CMOS, Multiplying, 12-Bit DAC in 8-Pin Package
MAX547	DS	Octal, Voltage-Output, 13-Bit DAC with Parallel Interface
MAX555	96NR 9-81	300Mps, 12-Bit DAC with Complementary Voltage Outputs
MAX555EVKIT	DS	Evaluation Kit for the MAX555
MAX560	93NR 2-53	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX561	93NR 2-53	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX562	95NR 2-175	2.7V to 5.25V, High-Speed RS-232 Serial Port
MAX563	95NR 2-183	3.3V, Dual EIA/TIA-562 Transceiver
MAX600	DS	Low-Cost AC-DC Regulator (110/220VAC to 5VDC—Full Wave)
MAX601	DS	Low-Cost AC-DC Regulator (110/220VAC to 5VDC—Half Wave)
MAX602	DS	Low-Cost AC-DC Regulator (8VRMS to 5VDC—Full Wave)
MAX603	96NR 4-69	5V or Adjustable, Low-Dropout, Low IQ, 500mA Linear Regulator
MAX604	96NR 4-69	3.3V or Adjustable, Low-Dropout, Low IQ, 500mA Linear Regulator
MAX606	96NR 4-79*	Low-Profile, 0.8MHz, Step-Up DC-DC Converter for Type 1 Flash Memory/PCMCIA Cards
MAX607	96NR 4-79*	Low-Profile, 0.4MHz, Step-Up DC-DC Converter for Type 2 and 3 Flash Memory/PCMCIA Cards
MAX608	96NR 4-81*	Low Input Voltage, High-Efficiency, Step-Up DC-DC Controller
MAX610	DS	AC-DC Regulator (110/220VAC to 5VDC—Full Wave)
MAX611	DS	AC-DC Regulator (110/220VAC to 5VDC—Half Wave)
MAX612	DS	AC-DC Regulator (8VRMS to 5VDC—Full Wave)
MAX6120	96NR 6-5*	Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference
MAX613	95NR 4-31	Dual-Slot, PCMCIA Analog Power Controller
MAX614	95NR 4-31	Dual-Slot, PCMCIA Analog Power Controller
MAX619	95NR 4-39	Regulated 5V Charge-Pump DC-DC Converter
MAX619EVKIT	DS	Evaluation Kit for the MAX619
MAX620	DS	Quad, High-Side MOSFET Driver
MAX621	DS	Quad, High-Side MOSFET Driver with Internal Capacitors
MAX622	92NR 4-31	High-Side Power Supply
MAX623	92NR 4-31	High-Side Power Supply with Internal Capacitors

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX624	96NR 4-83	Dual-Output, 1MHz, DC-DC Boost Converter for PCMCIA Applications
MAX625	93NR 4-7	Quad, High-Side Power Switch with Internal FETs and Capacitors
MAX626	DS	Dual-Power MOSFET Driver (Inverting)
MAX627	DS	Dual-Power MOSFET Driver (Noninverting)
MAX628	DS	Dual-Power MOSFET Driver (Inverting & Noninverting)
MAX630	92NR 4-45	CMOS, Micropower, Step-Up Switching Regulator
MAX631	92NR 4-57	5V/Adjustable, Step-Up Switching Regulator
MAX632	92NR 4-57	12V/Adjustable, CMOS, Step-Up Switching Regulator
MAX633	92NR 4-57	15V/Adjustable, CMOS, Step-Up Switching Regulator
MAX634	92NR 4-65	CMOS, Micropower, Inverting Switching Regulator
MAX635	92NR 4-77	-5V/Adjustable, CMOS, Inverting Switching Regulator
MAX636	92NR 4-77	-12V/Adjustable, CMOS, Inverting Switching Regulator
MAX637	92NR 4-77	-15V/Adjustable, CMOS, Inverting Switching Regulator
MAX638	92NR 4-85	5V/Adjustable, CMOS, Step-Down Switching Regulator
MAX639	95NR 4-47	5V/Adjustable, High-Efficiency, Low Iq, Step-Down DC-DC Converter
MAX639EVKIT	DS	Evaluation Kit for the MAX639
MAX640	95NR 4-47	3.3V/Adjustable, High-Efficiency, Low Iq, Step-Down DC-DC Converter
MAX641	92NR 4-93	5V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX642	92NR 4-93	12V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX643	92NR 4-93	15V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX644	–	Replaced by MAX654
MAX645	–	Replaced by MAX655
MAX646	–	Replaced by MAX656
MAX647	–	Replaced by MAX657
MAX649	DS	5V/Adjustable, High-Efficiency, Low Iq, Step-Down DC-DC Controller
MAX649EVKIT	DS	Evaluation Kit for the MAX649/651/652
MAX650	DS	-48V Input to 5V, Switching DC-DC Converter
MAX651	DS	3.3V/Adjustable, High-Efficiency, Low Iq, Step-Down DC-DC Controller
MAX652	DS	3V/Adjustable, High-Efficiency, Low Iq, Step-Down DC-DC Controller
MAX653	95NR 4-47	3V/Adjustable, High-Efficiency, Low Iq, Step-Down DC-DC Converter
MAX654	92NR 4-105	Low-Voltage, 5V, Step-Up DC-DC Converter
MAX655	92NR 4-105	Low-Voltage, 5V, Step-Up DC-DC Converter
MAX655EVKIT	DS	Evaluation Kit for the MAX655
MAX656	92NR 4-105	Low-Voltage, 5V, Step-Up DC-DC Converter with External FET
MAX657	92NR 4-105	Low-Voltage, 3V, Step-Up DC-DC Converter
MAX658	92NR 4-105	Low-Voltage, 5V, Step-Up DC-DC Converter with External FET
MAX660	92NR 4-117	100mA, Charge-Pump Voltage Converter
MAX661	–	Replaced by MAX662
MAX662	94NR 4-43	12V, 30mA Flash Memory Programming Supply Charge Pump
MAX662A	95NR 4-75	12V, 30mA Flash Memory Programming Supply
MAX662EVKIT	DS	Evaluation Kit for the MAX662
MAX663	92NR 4-125	CMOS, 5V/Adjustable, Micropower, Positive Linear Regulator
MAX664	92NR 4-125	CMOS, -5V/Adjustable, Micropower, Negative Linear Regulator
MAX665	93NR 4-25	100mA, 1.5 to 8V, CMOS, Switched-Capacitor Voltage Converter

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX666	92NR 4-125	5V/Adjustable, Micropower, Positive Linear Regulator with Low-Battery Detect
MAX667	95NR 4-81	5V/Programmable, Low-Dropout Voltage Regulator
MAX670	DS	Precision, 10V Kelvin-Sensed Reference -3 ppm/°C
MAX671	DS	Precision, 10V Kelvin-Sensed Reference -1 ppm/°C
MAX672	—	Replaced by MAX674
MAX673	—	Replaced by MAX675
MAX674	92NR 3-1	Precision, 10V Voltage Reference
MAX675	92NR 3-5	Precision, 5V Voltage Reference
MAX676	DS	Calibrated, Low-Drift, 4.096V Precision Voltage Reference
MAX677	DS	Calibrated, Low-Drift, 5V Precision Voltage Reference
MAX678	DS	Calibrated, Low-Drift, 10V Precision Voltage Reference
MAX680	92NR 4-141	5V to ±10V, Switched-Capacitor Voltage Converter
MAX681	92NR 4-141	5V to ±10V, Switched-Capacitor Voltage Converter with Internal Capacitors
MAX687	96NR 4-99	3.3V, Low-Noise, Linear Regulator Controller with Automatic Shutdown
MAX687EVKIT	DS	Evaluation Kit for the MAX687
MAX688	96NR 4-99	3.3V, Low-Noise, Linear Regulator Controller
MAX688EVKIT	DS	Evaluation Kit for the MAX688
MAX688EVKIT-4A	DS	Evaluation Kit for the MAX688/689 IOUT
MAX689	96NR 4-99	3V, Low-Noise, Linear Regulator Controller
MAX689EVKIT	DS	Evaluation Kit for the MAX689
MAX690	DS	µP Reset IC with Watchdog and Battery Switchover
MAX690A	95NR 5-9	µP Reset IC with Watchdog and Battery Switchover
MAX690R/S/T	95NR 5-19	µP Reset IC with Watchdog and Battery Switchover
MAX691	DS	µP Reset IC with Watchdog and Battery Switchover
MAX691A	DS	µP Reset IC with Watchdog, Chip Enable, and Battery Backup
MAX692	DS	µP Reset IC with Watchdog and Battery Switchover
MAX692A	95NR 5-9	µP Reset IC with Watchdog and Battery Switchover
MAX693	DS	µP Reset IC with Watchdog and Battery Switchover
MAX693A	DS	µP Reset IC with Watchdog, Chip Enable, and Battery Backup
MAX694	DS	µP Reset IC with Watchdog and Battery Switchover
MAX695	DS	µP Reset IC with Watchdog and Battery Switchover
MAX696	92NR 5-33	µP Supervisor with Battery Switchover and Programmable Reset
MAX697	92NR 5-33	µP Supervisor with Programmable Reset
MAX698	92NR 5-45	Low-Cost Power-On Reset IC
MAX699	92NR 5-45	Low-Cost Power-On Reset IC with Watchdog Controller
MAX700	92NR 5-49	Adjustable-Threshold Power-Supply Monitor with Reset
MAX701	92NR 5-49	Power-Supply Monitor with Reset
MAX702	92NR 5-49	Power-Supply Monitor with Reset
MAX703	94NR 5-35	µP Reset IC with Battery Backup
MAX704	94NR 5-35	µP Reset IC with Battery Backup
MAX704R/S/T	95NR 5-19	3V µP Reset IC with Battery Backup
MAX705	DS	µP Reset IC with Watchdog
MAX706	DS	µP Reset IC with Watchdog
MAX706P/R/S/T	95NR 5-57	3V µP Reset IC with Watchdog

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX707	DS	µP Reset IC with Power-Fail Warning
MAX708	DS	µP Reset IC with Power-Fail Warning
MAX708R/S/T	95NR 5-57	3V µP Reset IC with Power-Fail Warning
MAX709L	94NR 5-67	Power-Supply Monitor with 4.65V Reset Threshold
MAX709M	94NR 5-67	Power-Supply Monitor with 4.40V Reset Threshold
MAX709R	94NR 5-67	Power-Supply Monitor with 2.63V Reset Threshold
MAX709S	94NR 5-67	Power-Supply Monitor with 2.93V Reset Threshold
MAX709T	94NR 5-67	Power-Supply Monitor with 3.08V Reset Threshold
MAX712	DS	Battery Fast-Charge Controller (NiMH)
MAX712EVKIT	DS	Evaluation Kit for the MAX712
MAX713	DS	Battery Fast-Charge Controller (NiCd)
MAX713SWEVKIT	DS	Evaluation Kit for the MAX713 (Switching Applications)
MAX714	DS	3-Output, Battery-Powered Supply System
MAX715	DS	6-Output, Battery-Powered Supply System
MAX716	DS	7-Output, Battery-Powered Supply System
MAX716EVKIT	DS	Evaluation Kit for the MAX716
MAX717	94NR 4-67	3.3V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718	94NR 4-67	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718EVKIT	DS	Evaluation Kit for the MAX718
MAX719	94NR 4-67	3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX720	94NR 4-67	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX721	94NR 4-67	3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX7219	DS	Serially Interfaced, 8-Digit, LED Display Driver
MAX722	93NR 4-49	3.3/5V Palmtop Computer and LCD Power-Supply Regulator
MAX722EVKIT	93NR 4-49	Evaluation Kit for the MAX722
MAX723	93NR 4-49	3V Palmtop Computer and LCD Power-Supply Regulator
MAX7231	DS	8-Digit, Triplexed LCD Decoder/Driver
MAX7232	DS	10-Digit, Triplexed LCD Decoder/Driver
MAX7233	DS	4-Character, Triplexed LCD Decoder/Driver
MAX7234	DS	5-Character, Triplexed LCD Decoder/Driver
MAX724	DS	5A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX726	DS	2A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX727	DS	2A, 5V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX728	DS	2A, 3.3V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX729	DS	2A, 3V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX730	94NR 4-69	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX730A	95NR 4-85	5V, Step-Down, Current-Mode PWM DC-DC Converter
MAX731	DS	5V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX731EVKIT	DS	Evaluation Kit for the MAX731
MAX732	93NR 4-93	12V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX732EVKIT	DS	Evaluation Kit for the MAX732
MAX733	93NR 4-93	15V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX734	94NR 4-103	12V, 120mA Flash Memory Programming Supply
MAX734EVKIT	DS	Evaluation Kit for the MAX734

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX735	94NR 4-111	-5V, Inverting, PWM DC-DC Converter
MAX736	DS	-12V, Inverting, PWM, Current-Mode DC-DC Converter
MAX737	DS	-15V, Inverting, PWM, Current-Mode DC-DC Converter
MAX738	93NR 4-69	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX738A	95NR 4-85	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX739	93NR 4-117	-5V, Inverting, PWM, Current-Mode DC-DC Converter
MAX739EVKIT	DS	Evaluation Kit for the MAX739
MAX741	DS	Pin-Programmed, Low-Voltage, PWM Current-Mode Controller
MAX741EVKIT	DS	Evaluation Kit for the MAX741
MAX742	DS	Switch-Mode Regulator with 5V to ± 1 or ± 15 V Dual Output
MAX742EVKIT	DS	Evaluation Kit for the MAX742
MAX743	DS	Dual-Output, PWM Switch-Mode Regulator (5V to ± 15 V or ± 12 V)
MAX743EVKIT	92NR 4-169	Evaluation Kit for the MAX743
MAX744A	95NR 4-85	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX746	DS	High-Efficiency, PWM, Step-Down, N-Channel DC-DC Controller
MAX747	94NR 4-135	High-Efficiency, PWM, Step-Down Controller (External P-Channel Driver)
MAX747EVKIT	DS	Evaluation Kit for the MAX747
MAX748A	95NR 4-87	3.3V, PWM, Step-Down DC-DC Converter
MAX749	DS	Digitally Adjustable LCD Bias Supply
MAX749EVKIT	DS	Evaluation Kit for the MAX749
MAX750	93NR 4-69	Adjustable, PWM, Step-Down DC-DC Converter
MAX750A	DS	Adjustable, PWM, Step-Down Regulator
MAX751	94NR 4-161	5V, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752	93NR 4-81	Adjustable, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752EVKIT	DS	Evaluation Kit for the MAX752
MAX753	DS	CCFT Backlight and LCD Negative Contrast Controller
MAX754	DS	CCFT Backlight and LCD Positive Contrast Controller
MAX755	94NR 4-111	Adjustable, PWM, Inverting DC-DC Converter
MAX756	DS	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX756EVKIT	DS	Evaluation Kit for the MAX756/MAX757
MAX757	DS	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX758	93NR 4-69	Adjustable, Step-Down, PWM, Current-Mode DC-DC Converter
MAX758A	DS	Adjustable, PWM, Step-Down DC-DC Converter
MAX759	DS	Adjustable, Inverting, PWM, Current-Mode DC-DC Converter
MAX759LCDEVKIT	DS	Evaluation Kit for the MAX759
MAX761	95NR 4-101	12V/Adjustable, High-Efficiency, Low Iq, Step-Up DC-DC Converter
MAX761EVKIT	DS	Evaluation Kit for the MAX761
MAX762	95NR 4-101	15V/Adjustable, High-Efficiency, Low Iq, Step-Up DC-DC Converter
MAX7624	DS	Improved MX7524
MAX763A	95NR 4-87	3.3V, PWM, Step-Down DC-DC Converter
MAX764	95NR 4-113	-5V/Adjustable, High-Efficiency, Low Iq, Inverting DC-DC Converter
MAX7645	DS	Improved MX7545
MAX764EVKIT	DS	Evaluation Kit for the MAX764–MAX766
MAX765	95NR 4-113	-12V/Adjustable, High-Efficiency, Low Iq, Inverting DC-DC Converter

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX766	95NR 4-113	-15V/Adjustable, High-Efficiency, Low I _Q , Inverting DC-DC Converter
MAX767	95NR 4-125	5V Supply to 3.3V Output, Synchronous, Step-Down Power-Supply Controller
MAX767EVKIT	DS	Evaluation Kit for the MAX767
MAX770	95NR 4-141	5V/Adjustable, High-Efficiency, Low I _Q , Step-Up DC-DC Controller
MAX7705	DS	µP Power-Supply Monitor with Reset
MAX770EVKIT	DS	Evaluation Kit for the MAX770
MAX771	95NR 4-141	12V/Adjustable, High-Efficiency, Low I _Q , Step-Up DC-DC Controller
MAX772	95NR 4-141	15V/Adjustable, High-Efficiency, Low I _Q , Step-Up DC-DC Controller
MAX773	95NR 4-141	5V/12V/15V/Adjustable, High-Voltage, High-Efficiency, Low I _Q , Step-Up DC-DC Controller
MAX774	95NR 4-161	-5V or Adjustable, High-Efficiency, Low I _Q , Inverting DC-DC Controller
MAX774EVKIT	DS	Evaluation Kit for the MAX774
MAX775	95NR 4-161	-12V or Adjustable, High-Efficiency, Low I _Q , Inverting DC-DC Controller
MAX776	95NR 4-161	-15V or Adjustable, High-Efficiency, Low I _Q , Inverting DC-DC Controller
MAX777	95NR 4-177	1V-Input, 5V-Output, Step-Up DC-DC Converter
MAX778	95NR 4-177	1V-Input, 3V/3.3V-Output, Step-Up DC-DC Converter
MAX778EVKIT	DS	Evaluation Kit for the MAX778
MAX779	95NR 4-177	1V-Input, Adjustable-Output, Step-Up DC-DC Converter
MAX780	DS	Dual-Slot, PCMCIA Analog Power Controller
MAX781	DS	PDA/Hand-Held Computer Power Controller
MAX781EVKIT	DS	Evaluation Kit for the MAX781
MAX782	DS	Triple-Output Power-Supply Controller for Notebook Computers
MAX783	DS	3.3V/5V Notebook Computer Power Supply, Dual PCMCIA Vpp Outputs (6-Cell Input)
MAX783EVKIT	DS	Evaluation Kit for the MAX783
MAX786	95NR 4-189	3.3V/5V Notebook Computer Power Supply with 25µA Shutdown
MAX786EVKIT	DS	Evaluation Kit for the MAX786
MAX787	DS	5V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX788	DS	3.3V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX789	DS	3V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX791	DS	µP Supervisory Circuit
MAX792	DS	µP and Non-Volatile Memory Supervisory Circuit
MAX793	96NR 5-21	3V/3.3V Adjustable, µP Supervisory Circuit
MAX794	96NR 5-21	3V/3.3V Adjustable, µP Supervisory Circuit
MAX795	96NR 5-21	3V/3.3V Adjustable, µP Supervisory Circuit
MAX796	96NR 4-109	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Positive Secondary
MAX796EVKIT	DS	Evaluation Kit for the MAX796
MAX797	96NR 4-109	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Low-Noise Pin
MAX797EVKIT	DS	Evaluation Kit for the MAX797
MAX799	96NR 4-109	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Negative Secondary
MAX799EVKIT	DS	Evaluation Kit for the MAX799

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX800L/M	DS	µP Reset IC with Watchdog, Battery Switchover, and ±2% Power-Fail Accuracy
MAX802L/M	95NR 5-9	High-Accuracy µP Reset IC with Watchdog and Battery Backup
MAX802R/S/T	95NR 5-19	3V, High-Accuracy µP Reset IC with Watchdog and Battery Backup
MAX804R/S/T	95NR 5-19	3V, High-Accuracy µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX805L	95NR 5-9	µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX805R/S/T	95NR 5-19	3V µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX806R/S/T	95NR 5-19	3V, High-Accuracy µP Reset IC with Battery Backup
MAX807L/M/N	96NR 5-41*	µP Supervisory Circuit with ±1.5% Reset Accuracy
MAX808L/M/R/S/T	DS	3-Pin µP Reset Circuit
MAX809L/M/R/S/T	96NR 5-43	3-Pin µP Reset Circuit
MAX810L/M/R/S/T	96NR 5-43	3-Pin µP Reset Circuit
MAX811L/M/R/S/T	96NR 5-49	4-Pin µP Voltage Monitor with Manual RESET Output
MAX812L/M/R/S/T**	96NR 5-49	4-Pin µP Voltage Monitor with Manual RESET Output
MAX813L	DS	µP Reset IC (asserted high) with Watchdog
MAX814	96NR 5-57	High-Accuracy, 1%, Low-Power, 3V and 5V µP Supervisory Circuit
MAX815	96NR 5-57	High-Accuracy, 1%, Low-Power, 3V and 5V µP Supervisory Circuit
MAX816	96NR 5-57	High-Accuracy, 1%, Low-Power, 3V and 5V µP Supervisory Circuit
MAX820	DS	µP and Non-Volatile Memory Supervisory Circuit
MAX8211	DS	µP Voltage Monitor with Programmable Voltage Detection
MAX8212	DS	µP Voltage Monitor with Programmable Voltage Detection
MAX8213	DS	Five Universal Voltage Monitors, Complete µP Voltage Monitoring
MAX8214	DS	Five Universal Voltage Monitors with Active Pull-Ups
MAX8215	DS	±5V, ±12V Dedicated µP Voltage Monitor
MAX8216	DS	±5V, ±12V Dedicated µP Voltage Monitor
MAX830	96NR 4-141	1A, Adjustable V_{OUT}, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX831	96NR 4-141	1A, 5V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX831EVKIT	DS	Evaluation Kit for the MAX830–MAX833
MAX832**	96NR 4-141	1A, 3.3V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX833**	96NR 4-141	1A, 3V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX840	96NR 4-147	Low-Noise, Regulated, -2V GaAsFET Bias
MAX840EVKIT	DS	Evaluation Kit for the MAX840
MAX843	96NR 4-147	Low-Noise, Regulated, -2V GaAsFET Bias with Adjustable Reference
MAX844	96NR 4-147	Low-Noise, Regulated, -2V GaAsFET Bias with LCD Output
MAX845	96NR 4-157	750mW Isolated Transformer Driver for PCMCIA Applications
MAX845EVKIT	DS	Evaluation Kit for the MAX845
MAX848	96NR 4-173*	1 to 3 Cell, High Power, Low-Noise, Step-Up DC-DC Converter with 0.5A MOSFET Power Switch
MAX849	96NR 4-173*	1 to 3 Cell, High Power, Low-Noise, Step-Up DC-DC Converter with 1A MOSFET Power Switch
MAX850	95NR 4-215	-4.1V/Adjustable, GaAsFET Bias Supply
MAX850EVKIT	DS	Evaluation Kit for the MAX850–853
MAX851	95NR 4-215	-4.1V/Adjustable, GaAsFET Bias Supply

*Advance Information—first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX852	95NR 4-215	-4.1V/Adjustable, GaAsFET Bias Supply with Adjustable Oscillator
MAX853	95NR 4-215	Adjustable-Output, GaAsFET Bias Supply and Adjustable Reference Level
MAX856	DS	3.3V/5V, High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX856EVKIT	DS	Evaluation Kit for the MAX856
MAX857	DS	Adjustable-Output, High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX858	DS	3.3V/5V, High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX859	DS	Adjustable-Output, High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX860	95NR 4-235	50mA, Frequency-Selectable, Switched-Capacitor Voltage Converter
MAX861	95NR 4-235	50mA, Frequency-Selectable, Switched-Capacitor Voltage Converter
MAX863	96NR 4-175*	Dual-Output, PFM, Step-Up DC-DC Controller
MAX864	96NR 4-177*	Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter with Shutdown
MAX865	96NR 4-179*	Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter in μMAX
MAX866	96NR 4-181	3.3V/5V-Output, Single-Cell DC-DC Converter for Pagers
MAX866EVKIT	DS	Evaluation Kit for the MAX866
MAX867	96NR 4-181	Adjustable-Output, Single-Cell DC-DC Converter for Pagers
MAX872	94NR 6-7	10 μ A, Low-Dropout, 2.5V Precision Voltage Reference
MAX873	94NR 6-15	Low-Power, Low-Drift, 2.5V Precision Voltage Reference
MAX874	94NR 6-7	10 μ A, Low-Dropout, 4.096V Precision Voltage Reference
MAX875	94NR 6-15	Low-Power, Low-Drift, 5V Precision Voltage Reference
MAX876	94NR 6-15	Low-Power, Low-Drift, 10V Precision Voltage Reference
MAX877	95NR 4-243	5V-Output, 1.8V to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX877EVKIT	DS	Evaluation Kit for the MAX877/878
MAX878	95NR 4-243	3.3V/3V-Output, 1.8V to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX879	95NR 4-243	Adjustable-Output, 1.8V to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX882	96NR 4-193	3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulator with Standby Mode
MAX883	96NR 4-193	5V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulator with Shutdown Mode
MAX884	96NR 4-193	3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulator with Shutdown Mode
MAX887	DS	Low-Noise, Adjustable-Output, Step-Down DC-DC Converter with Synching Capability
MAX900	92NR 8-51	Quad, High-Speed, Low-Power Voltage Comparator
MAX901	92NR 8-51	Quad, High-Speed, Low-Power Voltage Comparator
MAX902	92NR 8-51	Dual, High-Speed, Low-Power Voltage Comparator
MAX903	92NR 8-51	High-Speed, Low-Power Voltage Comparator
MAX905	93NR 3-41	High-Speed, Clocked, D Flip-Flop, ECL Voltage Comparator
MAX906	93NR 3-41	Dual, High-Speed, Clocked, D Flip-Flop, ECL Voltage Comparator
MAX907	DS	Dual, High-Speed, Ultra-Low-Power, Single 5V TTL Comparator
MAX908	DS	Quad, High-Speed, Ultra-Low-Power, Single 5V TTL Comparator
MAX909	DS	Single, High-Speed, Ultra-Low-Power, Single 5V TTL Comparator
MAX910	93NR 3-57	High-Speed, Threshold-Programmable Voltage Comparator
MAX911	93NR 3-57	High-Speed, Threshold-Programmable Voltage Comparator

*Advance Information—first page of data sheet in preparation.

**Future Product.

Alphanumeric Index

A Complete Product Listing

Part #	Publication/Doc. Page	Description
MAX912	95NR 3-39	Dual, Ultra-Fast, Low-Power, Precision TTL Comparator
MAX913	95NR 3-39	Single, Ultra-Fast, Low-Power, Precision TTL Comparator
MAX915	DS	Ultra-High-Speed, TTL Comparator
MAX916	DS	Master/Slave, Dual, Ultra-High-Speed, TTL Comparator
MAX921	DS	Ultra-Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX922	DS	Dual, Ultra-Low-Power, Single-Supply Comparator
MAX923	DS	Dual, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX924	DS	Quad, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX931	95NR 3-47	Ultra-Low-Power, Low-Cost Comparator with 2%-Accurate Reference
MAX932	95NR 3-47	Dual, Ultra-Low-Power, Low-Cost Comparator with 2%-Accurate Reference
MAX933	95NR 3-47	Dual, Ultra-Low-Power, Low-Cost Comparator with 2%-Accurate Reference
MAX934	95NR 3-47	Quad, Ultra-Low-Power, Low-Cost Comparator with 2%-Accurate Reference
MAX941	DS	3V and 5V, 75ns, Rail-to-Rail Input Comparator
MAX942	DS	Dual, 3V and 5V, 75ns, Rail-to-Rail Input Comparator
MAX944	DS	Quad, 3V and 5V, 75ns, Rail-to-Rail Input Comparator
MAX951	96NR 3-47*	6μA 1V/V, Single-Supply Op Amp + Comparator + Reference
MAX952	96NR 3-47*	6μA 10V/V, Single-Supply Op Amp + Comparator + Reference
MAX953	96NR 3-47*	4μA 1V/V, Single-Supply Op Amp + Comparator
MAX954	96NR 3-47*	4μA 10V/V, Single-Supply Op Amp + Comparator
MAX9685	DS	Ultra-Fast ECL-Output Comparator with Latch Enable
MAX9686	DS	Very Fast TTL-Latched Output Comparator
MAX9687	DS	Dual, Ultra-Fast ECL-Output Comparator
MAX9690	DS	Ultra-Fast ECL-Output Comparator
MAX9698	DS	Dual, Very Fast, TTL-Latched Output Comparator
MAXC001	DS	150 μ F, Low-ESR Aluminum Electrolytic Capacitor
MAXL001	92NR 4-185	100 μ H Toroid Inductor
MF10	DS	Dual, Second-Order, Universal Switched-Capacitor Filter
MM74C945	DS	4-Digit, Up/Down Counter/Decoder/Driver
MM74C947	DS	4-Digit, Up/Down Counter/Decoder/Driver
MX2700	DS	Precision, 3ppm/ $^{\circ}$ C, 10V Reference
MX2701	DS	Precision, 3ppm/ $^{\circ}$ C, -10V Reference
MX2710	DS	Precision, 1ppm/ $^{\circ}$ C, 10V Reference
MX3554	DS	Wideband, Fast-Setting Op Amp
MX390	DS	Quad, CMOS 12-Bit DAC
MX536A	DS	True RMS-to-DC Converter
MX565A	DS	High-Speed, 12-Bit, Monolithic DAC with Voltage Reference
MX566A	DS	High-Speed, 12-Bit, Monolithic DAC
MX574A	DS	Industry-Standard, Complete 12-Bit ADC
MX578	DS	High-Speed, 3 μ s 12-Bit ADC
MX580	DS	Precision 2.5V Voltage Reference
MX581	DS	Precision 10V Voltage Reference
MX584	DS	Pin-Programmable 10V, 7.5V, 5V, 2.5V, Precision Voltage Reference

*Advance Information—first page of data sheet in preparation.

**Future Product.

Alphanumeric Index

A Complete Product Listing

Part #	Publication/Doc. Page	Description
MX636	DS	True RMS-to-DC Converter
MX674A	DS	Industry-Standard, Complete 12-Bit ADC
MX7224	DS	CMOS, Double-Buffered, 8-Bit DAC with Voltage-Output Amplifier
MX7225	DS	CMOS, Quad, 8-Bit DAC with Voltage-Output Amplifier Latches
MX7226	DS	CMOS, Quad, 8-Bit DAC with Voltage-Output Amplifier
MX7228	DS	CMOS, Octal, 8-Bit DAC
MX7245	DS	Complete, 12-Bit, Voltage-Output Multiplying DAC
MX7248	DS	Complete, 12-Bit, Voltage-Output Multiplying DAC
MX7501	DS	8-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7502	DS	Differential, 4-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7503	DS	8-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7506	DS	Monolithic CMOS Multiplexer
MX7507	DS	Monolithic CMOS Multiplexer
MX7520	DS	CMOS, 10-Bit Multiplying DAC
MX7521	DS	CMOS, 12-Bit Multiplying DAC
MX7523	DS	CMOS, 8-Bit Multiplying DAC
MX7524	DS	CMOS, Buffered, 8-Bit Multiplying DAC
MX7528	DS	CMOS, Dual, Buffered, 8-Bit Multiplying DAC
MX7530	DS	CMOS, 10-Bit Multiplying DAC
MX7531	DS	CMOS, 12-Bit Multiplying DAC
MX7533	DS	CMOS, Low-Cost, 10-Bit Multiplying DAC
MX7534	DS	μP-Compatible, 14-Bit DAC
MX7535	DS	μP-Compatible, 14-Bit DAC
MX7536	DS	μP-Compatible, 14-Bit DAC
MX7537	DS	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7538	DS	CMOS, μP-Compatible, 14-Bit DAC
MX7541	DS	CMOS, 12-Bit Multiplying DAC
MX7541A	DS	CMOS, 12-Bit Multiplying DAC
MX7542	DS	CMOS, 12-Bit, μP-Compatible DAC
MX7543	DS	CMOS, 12-Bit, Serial-Input DAC
MX7545	DS	CMOS, Buffered, 12-Bit Multiplying DAC
MX7545A	DS	CMOS, Buffered, 12-Bit Multiplying DAC
MX7547	DS	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7548	DS	CMOS, 8-Bit-Compatible, 12-Bit DAC
MX7549	DS	CMOS, Dual, Double-Buffered, 12-Bit, μP-Compatible DAC
MX7572	92NR 7-37	CMOS, Complete, High-Speed, 12-Bit ADC
MX7574	DS	CMOS, μP-Compatible, 8-Bit ADC
MX7575	DS	CMOS, μP-Compatible, 5μs, 8-Bit ADC
MX7576	DS	CMOS, μP-Compatible, 10μs, 8-Bit ADC
MX7578	DS	Calibrated 12-Bit ADC
MX7581	DS	CMOS, 8-Bit, 8-Channel Data-Acquisition System
MX7582	DS	Calibrated, 4-Channel, 12-Bit ADC
MX7628	DS	CMOS, Dual, Buffered, 8-Bit, Multiplying DAC
MX7672	DS	High-Speed 12-Bit ADC with External Reference Input

*Advance Information—first page of data sheet in preparation.

**Future Product.

Alphanumeric Index

A Complete Product Listing

Part #	Publication/Doc. Page	Description
MX7820	DS	CMOS, 1.3 μ s, 8-Bit ADC with Track/Hold
MX7821	92NR 7-157	μ P-Compatible, 660ns, 8-Bit ADC with Track/Hold
MX7824	DS	CMOS, High-Speed, 8-Bit ADC with 4-Channel Multiplexer
MX7828	DS	CMOS, High-Speed, 8-Bit ADC with 8-Channel Multiplexer
MX7837	DS	Complete, Dual, 12-Bit Multiplying DAC with 8-Bit Bus Interface
MX7845	DS	Complete, 12-Bit Multiplying DAC
MX7847	DS	Complete, Dual, 12-Bit Multiplying DAC with 12-Bit Bus Interface
MXD1000	94NR 10-5	5-Tap Silicon Delay Line
MXD1013	94NR 10-7	3-in-1 Silicon Delay Line
MXD1210	DS	Nonvolatile RAM Controller
MXL1001	DS	Low-Offset Op Amp
MXL1007	DS	Low-Noise, Precision Op Amp
MXL1013	DS	Dual, Precision Op Amp
MXL1014	DS	Dual, Precision Op Amp
MXL1016	DS	Ultra-Fast, Precision TTL Comparator
MXL1028	DS	Ultra-Low-Noise, High-Speed, Precision Op Amp
MXL1062	DS	5th-Order, Zero-Error, Butterworth, Switched-Capacitor Lowpass Filter
MXL1074	DS	5A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1076	DS	2A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1116	DS	Ultra-Fast, Single-Supply, Precision TTL Comparator
MXL1178	DS	17 μ A Max, Dual, Single-Supply, Precision Op Amp
MXL1179	DS	17 μ A Max, Quad, Single-Supply, Precision Op Amp
MXT429	DS	High-Speed, 6A MOSFET Driver (Inverting)
OP07	DS	Precision Op Amp
OP27	DS	Low-Noise, Precision Op Amp
OP37	DS	Low-Noise, Precision Op Amp
OP90	DS	Precision, Low-Voltage, Micropower Op Amp
PGA100	DS	Programmable Gain Amplifier
REF01	DS	Precision, 10V Voltage Reference
REF02	DS	Precision, 5V Voltage Reference
Si7661	DS	CMOS, Switched-Capacitor Voltage Converter (Up to 20V Input)
TSC426	DS	Dual-Power MOSFET Driver (Inverting)
TSC427	DS	Dual-Power MOSFET Driver (Noninverting)
TSC428	DS	Dual-Power MOSFET Driver (Inverting and Noninverting)

*Advance Information—first page of data sheet in preparation.

**Future Product.

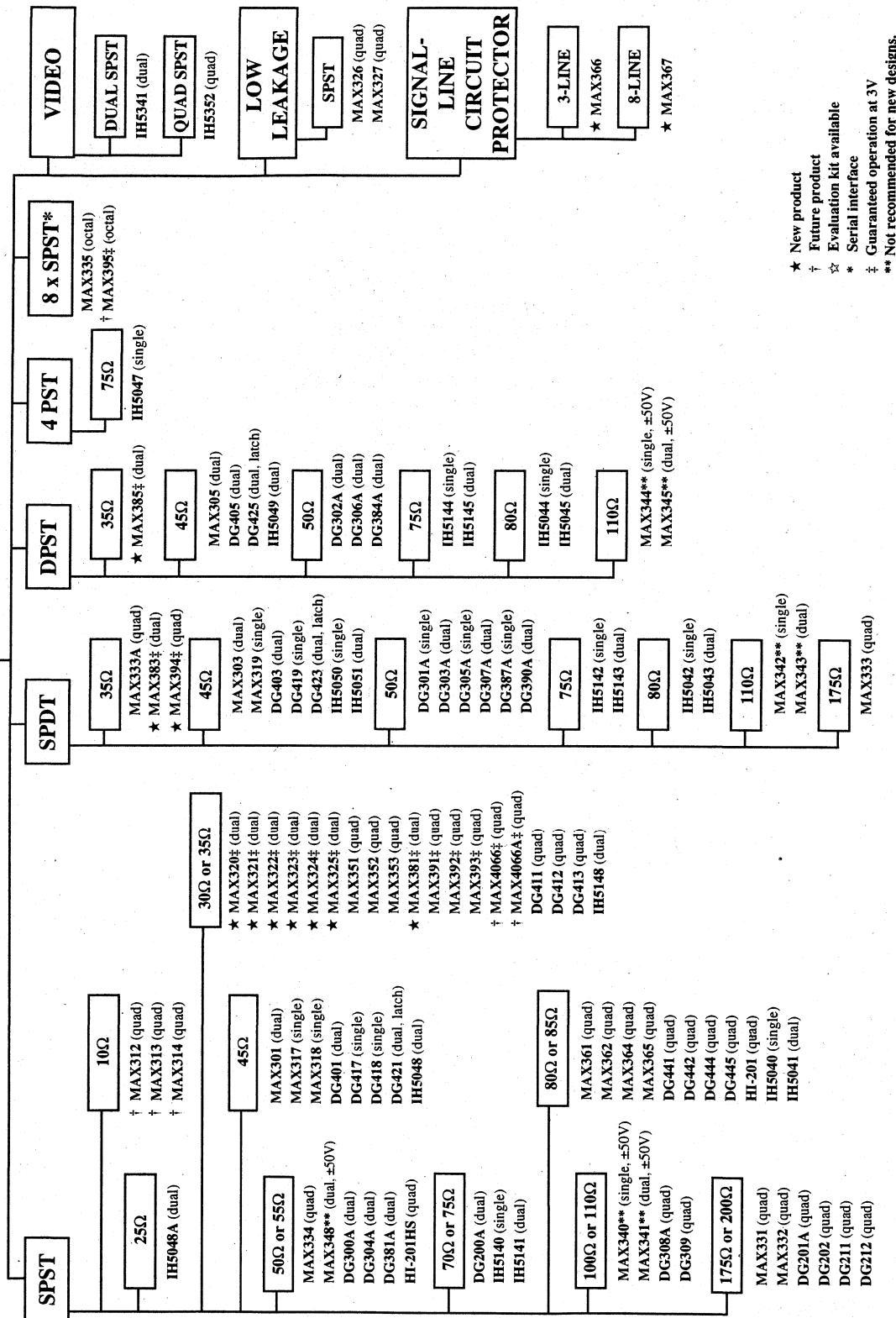


Analog Multiplexers/Switches

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MAX312 Low On-Resistance, Quad, SPST, Normally Closed CMOS Analog Switch*	1-9
MAX313 Low On-Resistance, Quad, SPST, Normally Open CMOS Analog Switch*	1-9
MAX314 Low On-Resistance, Quad, SPST, 2 Normally Closed/2 Normally Open CMOS Analog Switch*	1-9
MAX320 Precision, Dual-Supply, Dual, SPST, Normally Open CMOS Analog Switch	1-11
MAX321 Precision, Dual-Supply, Dual, SPST, Normally Closed CMOS Analog Switch	1-11
MAX322 Precision, Dual-Supply, Dual, SPST CMOS Analog Switch	1-11
MAX323 Precision, Single-Supply, Dual, SPST, Normally Open CMOS Analog Switch	1-19
MAX324 Precision, Single-Supply, Dual, SPST, Normally Closed CMOS Analog Switch	1-19
MAX325 Precision, Single-Supply, Dual, SPST CMOS Analog Switch	1-19
MAX354 8-Channel, Fault-Protected CMOS Multiplexer—Improved MAX358	1-29
MAX355 Dual, 4-Channel, Fault-Protected CMOS Multiplexer	1-29
MAX366 Signal-Line Circuit Protector w/ Three Independent Protectors	1-41
MAX367 Signal-Line Circuit Protector w/ Eight Independent Protectors	1-41
MAX381 Precision, Dual, Low-Voltage, SPST CMOS Analog Switch	1-51
MAX382 Low-Voltage, 1-of-8 CMOS Multiplexer with Latchable Inputs	1-63
MAX383 Precision, Dual, Low-Voltage, SPDT CMOS Analog Switch	1-51
MAX384 Low-Voltage, Dual, 4-Channel CMOS Multiplexer with Latchable Inputs	1-63
MAX385 Precision, Dual, Low-Voltage, DPST CMOS Analog Switch	1-51
MAX394 Low-Voltage, Quad, SPDT CMOS Analog Switch—Replaces MAX333A	1-75
MAX396 Precision, 16-Channel, Low-Voltage CMOS Analog Multiplexer—DG406 Pinout	1-87
MAX397 Precision, Dual, 8-Channel, Low-Voltage CMOS Analog Multiplexer—DG407 Pinout	1-87
MAX398 Precision, 8-Channel, Low-Voltage CMOS Analog Multiplexer—DG408 Pinout	1-99
MAX399 Precision, Dual, 4-Channel, Low-Voltage CMOS Analog Multiplexer	1-99

*Advance Information—first page of data sheet in preparation.

ANALOG SWITCHES



- ★ New product
- † Future product
- ☆ Evaluation kit available
- * Serial interface
- ‡ Guaranteed operation at 3V
- ** Not recommended for new designs.

Analog Switches

Part Number	Function ¹	RDS(ON) ² (Ω max)	ICOM(OFF) I _O (OFF) (nA max)	Ron Match (Ω max)	Ron Flatness (Ω max)	t _{ON} (ns max)	t _{OFF} (ns max)	V _{IL} /V _{IH} (V)	Supply Current I ₊ /I ₋ (mA max)	Features	Price [†] 1000-up (\$)
MAX317	SPST NC	45	0.25	—	3	175	145	0.82,4	0.001/0.001	Improved DG417, low Ron match and flatness	1.05
MAX318	SPST NO	45	0.25	—	3	175	145	0.82,4	0.001/0.001	Improved DG418, low Ron match and flatness	1.05
DG417	SPST NC	45	0.25	—	4	175	145	0.82,4	0.001/0.001	8-pin DIP/SO	0.96
DG418	SPST NO	45	0.25	—	4	175	145	0.82,4	0.001/0.001	8-pin DIP/SO	0.96
IH5140	SPST NO	75	1	—	150	150	125	0.82,4	0.01/0.01	Fast, low power	2.89
IH5040	SPST NO	80	5	—	400	200	200	0.82,4	0.01/0.01	Very low power	2.06
MAX319	SPST	45	0.25	2	3	175	145	0.82,4	0.001/0.001	Improved DG419, low Ron match and flatness	1.39
DG419	SPDT	45	0.25	3	4	175	145	0.82,4	0.001/0.001	8-pin DIP/SO	1.32
IH5050	SPDT NO	45	5	—	1000	500	500	0.82,4	0.01/0.01	Low power, low Ron	3.94
DG301A	SPDT	50	1	—	300	250	250	0.84,0	0.1/0.1	2.4 V _{IH} , low Ron	1.94
DG305A	SPDT	50	1	—	250	150	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low Ron	2.55
DG387A	SPDT	50	1	—	300	250	250	0.84,0	0.1/0.1	Low Ron	2.08
IH5142	SPDT	75	1	—	200	125	125	0.82,4	0.01/0.01	Fast, low power	3.23
IH5042	SPDT	80	5	—	400	200	200	0.82,4	0.01/0.01	Very low power	1.84
IH5144	DPST NO	75	1	—	200	125	125	0.82,4	0.01/0.01	Fast, low power	3.23
IH5044	DPST NO	80	5	—	400	200	200	0.82,4	0.01/0.01	Very low power	2.29
IH5047	4PST NC	75	1	—	400	200	200	0.82,4	0.001/0.001	Very low power	2.44
IH5048A	2 SPST NO	25	5	—	1000	500	500	0.82,4	0.01/0.01	Low power, low Ron	4.49
IH5148	2 SPST	30	1	—	1000	500	500	0.82,4	0.01/0.01	Low power, low Ron	4.94
MAX320	2 SPST NO	35	0.1	2	4	150	100	2.5/3.5	0.125/0.125	Low voltage, ±3V/±5V	0.89
MAX321	2 SPST NC	35	0.1	2	4	150	100	2.5/3.5	0.125/0.125	Low voltage, ±3V/±5V	0.89
MAX322	2 SPST	35	0.1	2	4	150	100	2.5/3.5	0.125/0.125	Low voltage, ±3V/±5V	0.89
MAX381	2 SPST	35	0.1	2	4	175	100	0.82,4	-0.001/0.001	Low voltage, +3V/+5V/±5V operation	1.23
MAX301	2 SPST NO	45	0.25	2	3	150	100	0.82,4	-0.001/0.001	Improved DG401, low Ron match and flatness	1.23
DG401	2 SPST NO	45	0.5	2	3	150	100	0.82,4	0.001/0.001	Low power, high speed, low leakage	1.23
DG421	2 SPST	45	0.25	3	4	250	200	0.82,4	0.001/0.001	Low power, high speed, has latches	1.59
IH5048	2 SPST NO	45	5	—	1000	500	500	0.82,4	0.01/0.01	Low power, low Ron	4.49
DG300A	2 SPST NC	50	1	—	300	250	250	0.84,0	0.5/0.1	2.4 V _{IH} , low Ron	1.94
DG304A	2 SPST NC	50	1	—	250	150	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low Ron	2.18
DG381A	2 SPST NO	50	1	—	300	250	250	0.84,0	0.1/0.1	Low Ron	2.08
MAX323	2 SPST NO	60	0.1	2	6	150	100	0.82,4	0.001	Low voltage, +2.7V/+5V	0.89
MAX324	2 SPST NC	60	0.1	2	6	150	100	0.82,4	0.001	Low voltage, +2.7V/+5V	0.89
MAX325	2 SPST	60	0.1	2	6	150	100	0.82,4	0.001	Low voltage, +2.7V/+5V	0.93
DG200A	2 SPST NC	70	2	—	1000	500	500	0.82,4	0.3/0.01	Low power	3.23
IH5141	2 SPST NO	75	1	—	150	150	125	0.82,4	0.01/0.01	Fast, low power	1.84
IH5041	2 SPST NC	80	1	—	400	200	200	0.82,4	0.001/0.001	Very low power	2.57
MAX383	2 SPST	35	0.1	2	4	175	100	0.82,4	-0.001/0.001	Low voltage, +3V/+5V/±5V operation	1.84
MAX303	2 SPDT	45	0.25	2	3	150	100	0.82,4	0.001/0.001	Improved DG403, low Ron match and flatness	2.57
DG403	2 SPDT	45	0.5	2	3	150	100	0.82,4	0.001/0.001	Low power, high speed, low leakage	2.57
DG423	2 SPDT	45	5	3	4	250	200	0.82,4	0.001/0.001	Low power, high speed, has latches	3.30
IH5051	2 SPDT	45	5	—	1000	500	500	0.82,4	0.01/0.01	Low power, low Ron	4.73
DG303A	2 SPDT	50	1	—	300	250	250	0.84,0	0.1/0.1	2.4 V _{IH} , low Ron	2.36
DG307A	2 SPDT	50	1	—	250	150	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low Ron	2.36
DG390A	2 SPDT	50	1	—	300	250	250	0.84,0	0.1/0.1	Low Ron	2.60
IH5143	2 SPDT	75	1	—	200	125	125	0.82,4	0.01/0.01	Fast, low power	3.49
IH5043	2 SPDT	80	1	—	400	200	200	0.82,4	0.001/0.001	Very low power	2.36
MAX385	2 DPST	35	0.1	2	4	175	100	0.82,4	-0.001/0.001	Low voltage, +3V/+5V/±5V operation	2.57
MAX305	2 DPST NO	45	0.25	2	3	150	100	0.82,4	0.001/0.001	Improved DG405, low Ron match and flatness	2.57

1 NO = Normally Open, NC = Normally Closed.
 2 Drain-source on-resistance is for the commercial grade, T_A = +25°C.
 † Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Analog Switches (continued)

Part Number	Function ¹	ROS(ON) ² (Ω max)	ICOM(OFF)/ ID(OFF) (nA max)	RON Match (Ω max)	RON Flatness (Ω max)	t(ON) (ns max)	t(OFF) (ns max)	V _{IL} /V _{IH} (V)	Supply Current I _{SL} - (mA max)	Features	Price [†] 1000-up (\$)
DG405	2 DPST NO	45	0.25	2	3	150	100	0.8/2.4	0.01/0.001	Low power, high speed, low leakage	2.57
DG425	2 DPST	45	0.25	2	3	250	200	0.8/2.4	0.01/0.001	Low power, high speed, has latches	3.30
IH5049	2 DPST NO	45	5			1000	500	0.8/2.4	0.01/0.01	Low power, low RON	5.35
DG302A	2 DPST NC	50	1			300	250	0.8/4.0	0.10/1	2.4 V _{IH} , low RON	2.50
DG306A	2 DPST NC	50	1			250	150	3.5/11.0	0.10/1	CMOS logic levels, high speed, low RON	2.53
DG384A	2 DPST NC	50	1			300	250	0.8/4.0	0.10/1	Low RON	2.92
IH5145	2 DPST NO	75	1			200	125	0.8/2.4	0.01/0.01	Fast, low power	3.82
IH5045	2 DPST NC	80	1			400	200	0.8/2.4	0.01/0.001	Very low power	2.44
MAX312	4 SPST NC	10	0.25	2	4	175	145	0.8/2.4	0.01/0.001	Low voltage, high speed, low leakage	††
MAX313	4 SPST NO	10	0.25	2	4	175	145	0.8/2.4	0.01/0.001	Low voltage, high speed, low leakage	††
MAX314	4 SPST	10	0.25	2	4	175	145	0.8/2.4	0.01/0.001	Low voltage, high speed, low leakage	††
MAX351	4 SPST NC	35	0.25	2	3	175	145	0.8/2.4	0.01/0.001	Improved DG411, low RON match and flatness	1.76
MAX352	4 SPST NO	35	0.25	2	3	175	145	0.8/2.4	0.01/0.001	Improved DG412, low RON match and flatness	1.76
MAX353	4 SPST	35	0.25	2	3	175	145	0.8/2.4	0.01/0.001	Improved DG413, low RON match and flatness	1.76
MAX391	4 SPST NC	35	0.1	2	4	130	75	0.8/2.4	0.01/0.001	Low voltage, +3V/+5V/±5V operation	1.87
MAX392	4 SPST NO	35	0.1	2	4	130	75	0.8/2.4	0.01/0.001	Low voltage, +3V/+5V/±5V operation	1.87
MAX393	4 SPST	35	0.1	2	4	130	75	0.8/2.4	0.01/0.001	Low voltage, +3V/+5V/±5V operation	1.87
MAX4066A	4 SPST NC	35	0.1	2	4	130	75	0.8/2.4	0.01/0.001	Low voltage, +2.7V	††
DG411	4 SPST NC	35	0.25	2	4	175	145	0.8/2.4	0.01/0.001	Low power, high speed, low leakage	1.85
DG412	4 SPST NO	35	0.25	2	4	175	145	0.8/2.4	0.01/0.001	Low power, high speed, low leakage	1.85
DG413	4 SPST	35	0.25	3	4	175	145	0.8/2.4	0.01/0.001	Low power, high speed, low leakage	1.85
MAX4066	4 SPST	45	1	4	6	130	75	0.8/2.4	0.01/0.001	Improved 74HC4066, low voltage, +2.7V	††
MAX334	4 SPST NC	50	1			100	50	0.8/3.0	4.5/3.5	Most switches per package, high speed with break-before-make	2.88
HI-201HS	4 SPST NC	50	1			50	50	0.8/3.0	4.0/1.5	Low RON, high speed	2.64
HI-201	4 SPST NC	80	5			400	300	0.8/2.4	0.30/1	Low RON, quad SPST	2.00
MAX361	4 SPST NC	85	0.5	2	5	250	120	0.8/2.4	0.10/0.01	Improved DG441, low RON match and flatness	1.29
MAX362	4 SPST NO	85	0.5	2	5	250	120	0.8/2.4	0.10/0.01	Improved DG442, low RON match and flatness	1.29
MAX364	4 SPST NC	85	0.5	2	5	250	120	0.8/2.4	0.01/0.001	Improved DG444, low RON match and flatness	1.14
MAX365	4 SPST NO	85	0.5	2	5	250	120	0.8/2.4	0.01/0.001	Improved DG445, low RON match and flatness	1.14
DG441	4 SPST NC	85	0.5	4	9	250	120	0.8/2.4	0.10/0.01	Low power, low leakage	1.29
DG442	4 SPST NO	85	0.5	4	9	250	120	0.8/2.4	0.10/0.01	Low power, low leakage	1.29
DG444	4 SPST NC	85	0.5	4	9	250	120	0.8/2.4	0.01/0.001	Low cost, quad SPST	1.03
DG445	4 SPST NO	85	0.5	4	9	250	120	0.8/2.4	0.01/0.001	Low cost, quad SPST	1.03
DG308A	4 SPST NO	100	1			200	150	3.1/11.0	0.10/1	CMOS logic levels, high speed, low RON	0.95
DG309	4 SPST NC	100	1			200	150	3.5/11.0	0.10/1	CMOS logic levels, high speed, low RON	0.95
MAX331	4 SPST NC	175	1			600	450	0.8/2.4	0.01/0.01	Improved DG201	3.37
MAX332	4 SPST NO	175	1			600	450	0.8/2.4	0.01/0.01	Improved DG201	3.37
DG211	4 SPST NC	175	5			1000	500	0.8/2.4	0.10/1	No V _{LOC} supply	0.91
DG212	4 SPST NO	175	5			1000	500	0.8/2.4	0.10/1	Normally open	0.91
DG201A	4 SPST NC	200	1			600	450	0.8/2.4	0.10/1	Low power	0.95
DG202	4 SPST NO	200	1			600	450	0.8/2.4	0.10/1	Low power	0.95
MAX326	4 SPST NC	3500	0.01			1000	500	0.8/2.4	0.25/0.1	Ultra-low leakage, 10pA max	2.78
MAX327	4 SPST NO	3500	0.01			1000	500	0.8/2.4	0.25/0.1	Ultra-low leakage, 10pA max	2.78
MAX333A	4 SPDT	35	0.25	2	3	175	145	0.8/2.4	0.01/0.001	Improved MAX333, low RON	3.60
MAX334	4 SPDT	35	0.25	2	3	175	145	0.8/2.4	0.01/0.001	MAX333A replacement, low-voltage, +2.7V	3.19
MAX333	8 SPDT	175	5			1000	500	0.8/2.4	0.25/0.25	Serial interface with break-before-make	2.87
MAX335	8 SPST	175	1			400	400	0.8/2.4	0.30/0.1	Low voltage, serial interface with break-before-make	2.84
MAX395	8 SPST	100	1	4		400	400	0.8/2.4	0.30/0.1	Low voltage, serial interface with break-before-make	††

1 NO = Normally Open, NC = Normally Closed.

2 Drain-source on-resistance is for the commercial grade, T_A = +25°C.

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

High-Voltage Analog Switches

Part Number	Function ¹	R _{DS(ON)} ² (Ω max)	I _{D(OFF)} (nA max)	t _(ON) (μs max)	t _(OFF) (ns max)	V _{IL/V_{IH}} (V)	Supply Current I _q /I _{qH} (mA max)	Features	Price [†] 1000-up (\$)
MAX340*	SPST NO	110	60	1000	750	3.5/12	0.3/0.02	↑ High-voltage, ±50V operation with ±50 analog signal range ↓	6.27
MAX342*	SPDT	110	60	1000	750	3.5/12	0.3/0.02		6.31
MAX344*	DPST NO	110	60	1000	750	3.5/12	0.3/0.02		5.21
MAX348*	2 SPST NO	55	60	1000	750	3.5/12	0.3/0.02		7.83
MAX341*	2 SPST NO	110	60	1000	750	3.5/12	0.3/0.02		6.27
MAX343*	2 SPDT	110	60	1000	750	3.5/12	0.3/0.02		8.71
MAX345*	2 DPST NO	110	60	1000	750	3.5/12	0.3/0.02		8.71

Video Switches

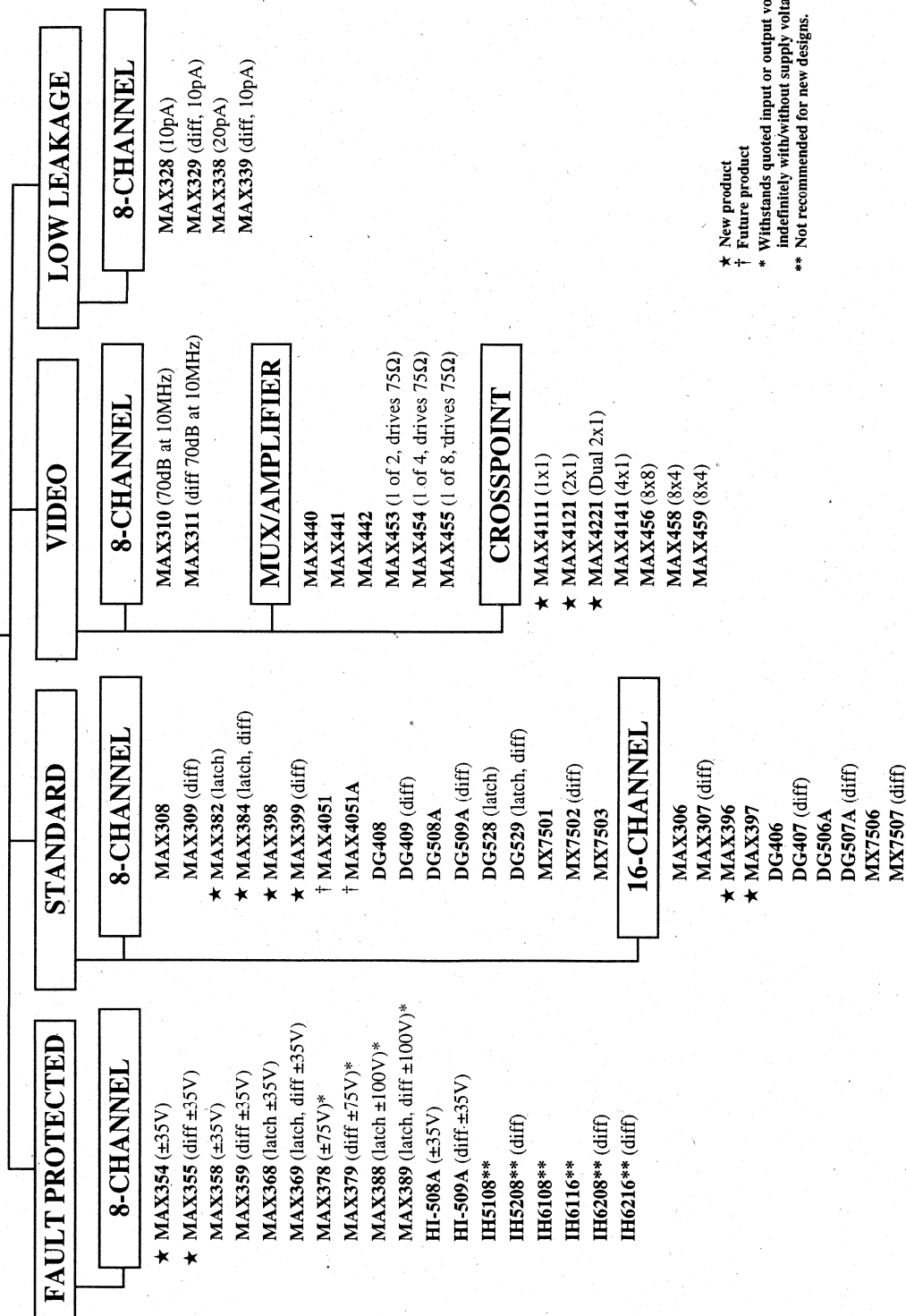
Part Number	Function ¹	R _{DS(ON)} ² (Ω max)	I _{D(OFF)} (nA max)	t _(ON) (μs max)	t _(OFF) (ns max)	V _{IL/V_{IH}} (V)	Analog-Signal Voltage Range (V)	Features	Price [†] 1000-up (\$)
IH5341	2 SPST NO	75	0.5	0.300	0.300	0.8/2.4	±10	70dB isolation at 10MHz	2.48
IH5352	4 SPST NO	75	0.5	0.300	0.300	0.8/2.4	±10	70dB isolation at 10MHz	4.30

Signal-Line Circuit Protectors

Part Number	Function	R _{DS(ON)} ² (Ω max)	I _{D(OFF)} (nA max)	Analog-Signal Voltage Range (V)	Features	Price [†] 1000-up (\$)
MAX366†	3-line	100	1.0	-12.5 to 13.5	±35V overvoltage protected	1.42
MAX367†	8-line	100	1.0	-12.5 to 13.5	±35V overvoltage protected	2.43

* Not recommended for new designs
 1 NO = Normally Open, NC = Normally Closed
 2 Drain-source on resistance is for the commercial grade, T_A = + 25°C.
 † Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
 ‡ No control required. Switches are always on when power is on.

ANALOG MULTIPLEXERS



★ New product
 † Future product
 * Withstands quoted input or output voltage indefinitely with/without supply voltage present
 ** Not recommended for new designs.

Analog Multiplexers

Part Number	Function	RDS(ON)* (Ω max)	I _D (OFF)/I _D (OFF) (nA max)	R _{ON} Match (Ω max)	t _{ON} (t _{OFF}) (μ s max)	Analog-Signal Voltage Range (V)	Features	Price [†] 1000-up (\$)
MAX308	1-of-8	100	0.75	5	0.225/0.150	± 15	Improved DG408, guaranteed R _{ON} match and flatness	2.59
MAX382	1-of-8	100	0.2	4	0.15/0.15	± 5	Low-voltage +3V/+5V/ ± 5 V operation, latchable address inputs	3.00
MAX398	1-of-8	100	0.1	4	0.15/0.15	+3, -5, ± 5	Low-voltage +3V/+5V/ ± 5 V operation, DG408 pinout	2.59
MAX4051A	1-of-8	100	0.1	4	0.15/0.15	± 5	Improved 74HC4051, low voltage, improved R _{ON}	††
DG408	1-of-8	100	1		0.225/0.150	± 15	Industry standard	2.59
MAX4051	1-of-8	125	1	10	0.15/0.15	± 5	Low voltage, improved R _{ON}	††
MAX354	1-of-8	350	0.5	12	0.25/0.20	± 15	Improved MAX358, improved R _{ON} , ± 35 V fault protection	2.45
DG508A	1-of-8	350	2		1.0/1.7	± 15	Industry standard	2.39
MX7501	1-of-8	350	5		1.5/1.0	± 15	Industry standard	5.58
MX7503	1-of-8	350	5		1.5/1.0	± 15	Industry standard	5.58
MAX338	1-of-8	400	0.02	10	0.50/0.50	± 15	Improved DG508A, low-leakage upgrade	2.39
DG528	1-of-8	450	10		1.5	± 15	Industry standard with latches	2.28
MAX358	1-of-8	1800	1		0.5	-12.5 to +13.5	Fault protected to ± 35 V	2.45
MAX368	1-of-8	1800	2		1.5/1.0	-12.5 to +13.5	Fault protected with latches to ± 35 V	3.50
HI-508A	1-of-8	1800	2		0.5	-12.5 to +13.5	Overvoltage	2.75
MAX378	1-of-8	3500	1		0.75/0.5	-12.5 to +13.5	Fault protected to ± 75 V	3.50
MAX388	1-of-8	3000	1		1	-12.5 to +13.5	Fault protected with latches to ± 100 V	4.50
MAX328	1-of-8	5000	0.02		1	± 15	Ultra-low leakage	3.61
IH5108	Use MAX358 (pin-for-pin compatible upgrade)							—
Use DG508A (pin-for-pin compatible upgrade)								
MAX309	2-of-8	100	1	5	0.225/0.150	± 15	Improved DG409, guaranteed R _{ON} match and flatness	2.59
MAX384	2-of-8	100	0.2	4	0.15/0.15	± 5	Low-voltage +3V/+5V/ ± 5 V operation, latchable address inputs	3.00
MAX399	2-of-8	100	0.1	4	0.15/0.15	+3, -5, ± 5	Low-voltage +3V/+5V/ ± 5 V operation, DG409 pinout	2.59
DG409	2-of-8	100	1		0.225/0.150	± 15	Industry standard	2.59
MAX355	2-of-8	350	0.5	12	0.25/0.20	± 15	Improved MAX359, improved R _{ON} , ± 35 V fault protection	2.45
DG509A	2-of-8	350	2		1.0/1.7	± 15	Industry standard	2.39
MX7502	2-of-8	350	3		1.5/1.0	± 15	Industry standard	5.58
MAX339	2-of-8	400	0.02	10	0.50/0.50	± 15	Improved DG509A, low-leakage upgrade	2.39
DG529	2-of-8	450	10		1.5	± 15	Industry standard with latches	2.28
MAX359	2-of-8	1800	1		0.5	-12.5 to +13.5	Fault protected to ± 35 V	2.45
MAX369	2-of-8	1800	1		1.5/1.0	-12.5 to +13.5	Fault protected with latches to ± 35 V	3.50
HI-509A	2-of-8	1800	2		0.5	-12.5 to +13.5	Overvoltage	2.75
MAX379	2-of-8	3500	1		0.75/0.5	-12.5 to +13.5	Fault protected to ± 75 V	3.50
MAX389	2-of-8	3000	1		1	-12.5 to +13.5	Fault protected with latches to ± 100 V	4.50
MAX329	2-of-8	5000	0.02		1	± 15	Ultra-low leakage	3.61
IH5208	Use MAX359 (pin-for-pin compatible upgrade)							—
Use DG509A (pin-for-pin compatible upgrade)								
MAX306	1-of-16	100	2	5	0.2/0.15	± 15	Improved DG406, guaranteed R _{ON} match and flatness	3.87
MAX396	1-of-16	100	0.1	4	0.15/0.15	+3, -5, ± 5	Low-voltage +3V/+5V/ ± 5 V operation, DG406 pinout	4.04
DG406	1-of-16	100	2		0.2/0.15	± 15	Industry standard	4.53
DG506A	1-of-16	450	5		1.0/0.4(typ)	± 15	Industry standard	3.68
MX7506	1-of-16	450	5		1.5/1.0	± 15	Industry standard	10.25
IH6116	Use MAX306A (pin-for-pin compatible upgrade)							—
MAX307	2-of-16	100	2	5	0.2/0.15	± 15	Improved DG407, guaranteed R _{ON} match and flatness	3.87
MAX397	1-of-16	100	0.1	4	0.15/0.15	+3, -5, ± 5	Low-voltage +3V/+5V/ ± 5 V operation, DG407 pinout	4.04
DG407	2-of-16	100	2		0.2/0.15	± 15	Industry standard	4.53
MX7507	2-of-16	450	5		1.5/1.0	± 15	Industry standard	10.25
DG507A	2-of-16	450	5		1.0/0.4(typ)	± 15	Industry standard	3.68
IH6216	Use DG507A (pin-for-pin compatible upgrade)							—

* Drain-source on-resistance is for the commercial grade, T_A = +25°C.

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Video Multiplexers

Part Number	Unity GBW (MHz)	Slew Rate (V/ μ s)	DP/DG (degrees/%)	Output Current (mA max)	Supply Voltage (V)	Supply Current (mA)	Features	Price [†] 1000-up (\$)
MAX440	160	370	0.03/0.04	35	± 5	40	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain error, 15ns switch time, high-Z output state	8.95
MAX441	160	370	0.03/0.04	35	± 5	40	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain error, 15ns switch time	5.90
MAX442	140	250	0.03/0.04	35	± 5	40	Video amp with 4-channel mux, 15ns switch time, 8-pin DIP/SO	4.45

Part Number	Function ¹	RDS(ON) ² (Ω max)	I _B (OFF) (nA max)	t _{ON} (μ s max)	V _{IL} /V _{IH} (V)	Analog-Signal Voltage Range (V)	Features	Price [†] 1000-up (\$)
MAX453	1-of-2 mux	Buffered output	10	0.12	0.8/2.4	± 2	On-chip output amp	3.94
MAX454	1-of-4 mux	Buffered output	10	0.12	0.8/2.4	± 2	On-chip output amp	5.25
MAX455	1-of-8 mux	Buffered output	10	0.12	0.8/2.4	± 2	On-chip output amp	8.75
MAX310	1-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	5.18
MAX311	2-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	7.20

Part Number	Unity GBW (MHz)	Slew Rate (V/ μ s)	DP/DG (degrees/%)	Off Isolation (dB typ)	Crosstalk (dB typ)	EV Kit	Features	Price [†] 1000-up (\$)
VIDEO CROSSPOINT SWITCHES								
MAX4111	330	700	0.01/0.01	74 (30MHz)	N/A	Yes	1x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	1.70
MAX4121	330	700	0.01/0.01	74 (30MHz)	66	Yes	2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.10
MAX4221	330	700	0.01/0.01	74 (30MHz)	66	Yes	Dual 2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50
MAX4141	330	700	0.01/0.01	74 (30MHz)	66	Yes	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50
MAX456	35	250	1/0.5	80 (5MHz)	70 (5MHz)		8x8 crosspoint switch array with eight output buffers, high-Z output capability	19.98
MAX458/459	100/90	300	0.05/0.01	60 (10MHz)	55 (10MHz)	Yes	8x4 crosspoint switch array with four 75 Ω cable drivers, high-Z output capability	21.85

¹ NO = Normally Open, NC = Normally Closed

² Drain-source on resistance is for the commercial grade, T_A = + 25°C.

[†] Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

10 Ω , Quad, SPST, CMOS Analog Switches

General Description

Maxim's MAX312/MAX313/MAX314 analog switches feature low on-resistance (10 Ω max) and 2 Ω on-resistance matching between channels. These switches conduct equally well in either direction. They offer low leakage over temperature (20nA at +85°C). Low power consumption and ESD tolerance greater than 2000V per Method 3015.7 are guaranteed.

The MAX312/MAX313/MAX314 are quad, single-pole/single-throw (SPST) analog switches. The MAX312 is normally closed (NC), and the MAX313 is normally open (NO). The MAX314 has two NC switches and two NO switches. All three devices operate from a single supply of +4.5V to +30V or from dual supplies of $\pm$ 4.5V to $\pm$ 20V.

Applications

Test Equipment
Communication Systems
PBX, PABX Systems
Audio Signal Routing
Avionics
Sample-and-Hold Circuits
Data Acquisition Systems

Features

- ◆ Pin Compatible with DG411/DG412/DG413
- ◆ Low On-Resistance (7 Ω typical)
- ◆ Guaranteed RON Match Between Channels (2 Ω max)
- ◆ Guaranteed RON Flatness over Specified Signal Range (3 Ω max)
- ◆ Guaranteed ESD Protection > 2000V per Method 3015.7
- ◆ Crosstalk > 96dB at 20kHz
- ◆ Single-Supply Operation: +4.5V to +30V
Dual-Supply Operation: $\pm$ 4.5V to $\pm$ 20V
- ◆ Rail-to-Rail Signal Handling

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX312CPE	0°C to +70°C	16 Plastic DIP
MAX312CSE	0°C to +70°C	16 Narrow SO
MAX312C/D	0°C to +70°C	Dice*
MAX312EPE	-40°C to +85°C	16 Plastic DIP
MAX312ESE	-40°C to +85°C	16 Narrow SO
MAX312MJE	-55°C to +125°C	16 CERDIP**

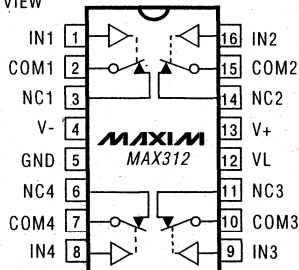
Ordering Information continued on last page.

* Contact factory for dice specifications.

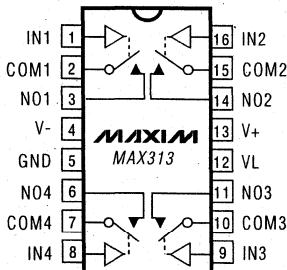
**Contact factory for availability.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

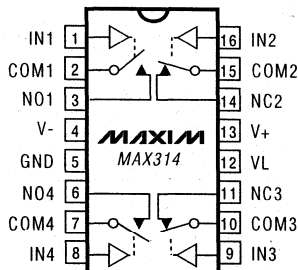


DIP/SO MAX312	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO MAX313	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT



DIP/SO MAX314		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

MAX312/MAX313/MAX314

MAXIM

Maxim Integrated Products 1-9

Call toll free 1-800-998-8800 for free samples or literature.

10 Ω , Quad, SPST, CMOS Analog Switches

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX313CPE	0°C to +70°C	16 Plastic DIP
MAX313CSE	0°C to +70°C	16 Narrow SO
MAX313C/D	0°C to +70°C	Dice*
MAX313EPE	-40°C to +85°C	16 Plastic DIP
MAX313ESE	-40°C to +85°C	16 Narrow SO
MAX313MJE	-55°C to +125°C	16 CERDIP**
MAX314CPE	0°C to +70°C	16 Plastic DIP
MAX314CSE	0°C to +70°C	16 Narrow SO
MAX314C/D	0°C to +70°C	Dice*
MAX314EPE	-40°C to +85°C	16 Plastic DIP
MAX314ESE	-40°C to +85°C	16 Narrow SO
MAX314MJE	-55°C to +125°C	16 CERDIP**

* Contact factory for dice specifications.

**Contact factory for availability.

MAXIM

Precision, Dual-Supply, SPST Analog Switches

General Description

The MAX320/MAX321/MAX322 are precision, dual, SPST analog switches designed to operate from $\pm 3V$ to $\pm 8V$ dual supplies. The MAX320 has two normally open (NO) switches and the MAX321 has two normally closed (NC) switches. The MAX322 has one NO and one NC switch. Low power consumption (1.25mW) makes these parts ideal for battery-powered equipment. They offer low leakage currents (100pA max) and fast switching speeds ($t_{ON} = 150ns$ max, $t_{OFF} = 100ns$ max).

The MAX320 series, powered from $\pm 5V$ supplies, offers 35 Ω max on-resistance (R_{ON}), 2 Ω max matching between channels, and 4 Ω max R_{ON} flatness.

These switches also offer 5pC max charge injection and a minimum of 2000V ESD protection per Method 3015.7.

For equivalent devices specified for single-supply operation, see the MAX323/MAX324/MAX325 data sheet. For quad versions of these switches, see the MAX391/MAX392/MAX393 data sheet.

Applications

Battery-Operated Systems	Sample-and-Hold Circuits
Heads-Up Displays	Guidance and Control Systems
Audio and Video Switching	Military Radios
Test Equipment	Communications Systems
$\pm 5V$ DACs and ADCs	PBX, PABX

Features

- ♦ Low On-Resistance, 35 Ω max (16 Ω typical)
- ♦ R_{ON} Matching Between Channels <2 Ω
- ♦ R_{ON} Flatness <4 Ω
- ♦ Guaranteed Charge Injection <5pC
- ♦ Bipolar Supply Operation ($\pm 3V$ to $\pm 8V$)
- ♦ Low Power Consumption, <1.25mW
- ♦ Low Leakage Current Over Temperature, <2.5nA at +85°C
- ♦ Fast Switching, $t_{ON} < 150ns$, $t_{OFF} < 100ns$
- ♦ Guaranteed Break-Before-Make (MAX322 only)

Ordering Information

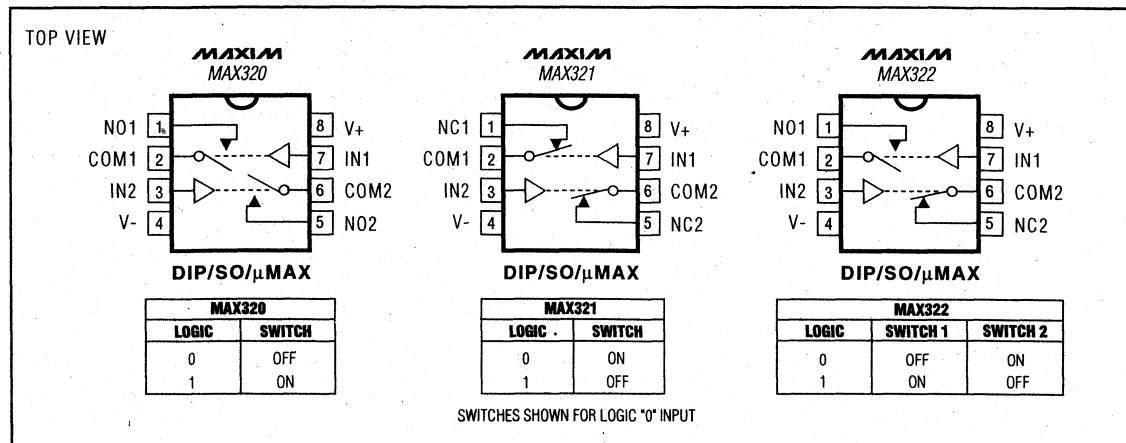
PART	TEMP. RANGE	PIN-PACKAGE
MAX320CPA	0°C to +70°C	8 Plastic DIP
MAX320CSA	0°C to +70°C	8 SO
MAX320CUA	0°C to +70°C	8 μ MAX
MAX320C/D	0°C to +70°C	Dice*
MAX320EPA	-40°C to +85°C	8 Plastic DIP
MAX320ESA	-40°C to +85°C	8 SO
MAX320EJA	-40°C to +85°C	8 Cerdip**
MAX320MJA	-55°C to +125°C	8 Cerdip**

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

** Contact factory for availability.

Pin Configurations/Functional Diagrams/Truth Tables



Precision, Dual-Supply, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
 V+(V- - 0.3V) to +17V
 IN₋, COM₋, NC₋, NO₋ (Note 1)(V- - 0.3V) to (V+ + 0.3V)
 Continuous Current (any terminal)30mA
 Peak Current, COM₋, NO₋, NC₋
 (pulsed at 1ms, 10% duty cycle max)100mA
 ESD per Method 3015.7>2000V
 Continuous Power Dissipation
 Plastic DIP (derate 9.09mW/°C above +70°C)727mW
 Narrow SO (derate 5.88mW/°C above +70°C)471mW

μMAX (derate 4.10mW/°C above +70°C)330mW
 CERDIP (derate 8.00mW/°C above +70°C)640mW
 Operating Temperature Ranges
 MAX32_C0°C to +70°C
 MAX32_E-40°C to +85°C
 MAX32_MJA-55°C to +125°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on NC₋, NO₋, COM₋, or IN₋ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V ±10%, V- = -5V ±10%, VINH = 3.5V, VINL = 2.5V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}	(Note 3)			V-		V+	V
On-Resistance	R _{ON}	V+ = 4.5V, V- = -4.5V, I _{COM} = 1.0mA, V _{NO} or V _{NC} = ±3.5V	TA = +25°C	C, E	16		35	Ω
				M	16		30	
			TA = T _{MIN} to T _{MAX}		45			
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V+ = 5V, V- = -5V, I _{COM} = 1.0mA, V _{NO} or V _{NC} = ±3V	TA = +25°C		0.3		2	Ω
			TA = T _{MIN} to T _{MAX}		4			
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	V+ = 5V, V- = -5V, I _{COM} = 1.0mA, V _{NO} or V _{NC} = ±3V	TA = +25°C		1		4	Ω
			TA = T _{MIN} to T _{MAX}		6			
NO or NC Off Leakage Current (Note 6)	I _{NO(OFF)} or I _{NC(OFF)}	V+ = 5.5V, V- = -5.5V, V _{COM} = ±4.5V, V _{NO} or V _{NC} = ±4.5V	TA = +25°C		-0.1	0.01	0.1	nA
			TA = T _{MIN} to T _{MAX}	C, E	-5		5	
				M	-40		40	
COM Off Leakage Current (Note 6)	I _{COM(OFF)}	V+ = 5.5V, V- = -5.5V, V _{COM} = ±4.5V, V _{NO} or V _{NC} = ±4.5V	TA = +25°C		-0.1	0.01	0.1	nA
			TA = T _{MIN} to T _{MAX}	C, E	-5		5	
				M	-40		40	
COM On Leakage Current (Note 6)	I _{COM(ON)}	V+ = 5.5V, V- = -5.5V, V _{COM} = ±4.5V, V _{NO} or V _{NC} = ±4.5V	TA = +25°C		-0.2	0.05	0.2	nA
			TA = T _{MIN} to T _{MAX}	C, E	-10		10	
				M	-50		50	

Precision, Dual-Supply, SPST Analog Switches

ELECTRICAL CHARACTERISTICS

(V+ = +5V ±10%, V- = -5V ±10%, VINH = 3.5V, VINL = 2.5V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
Input Current with Input Voltage High	I _{INH}			-0.5	0.005	0.5	μA
Input Current with Input Voltage Low	I _{INL}			-0.5	0.005	0.5	μA
Input Voltage High	V _{INH}	V+ = 5V ±10%, V- ≤ 0V		3.5			V
		3V < V+ < 8V, V- ≤ 0V			V+ - 1.5		
Input Voltage Low	V _{INL}	V+ = 5V ±10%, V- ≤ 0V				2.5	V
		3V < V+ < 8V, V- ≤ 0V			V+ - 2.5		
DYNAMIC							
Turn-On Time	t _{ON}	V _{COM} = ±3V, Figure 2	T _A = +25°C	65	150	ns	
			T _A = T _{MIN} to T _{MAX}		175		
Turn-Off Time	t _{OFF}	V _{COM} = ±3V, Figure 2	T _A = +25°C	35	100	ns	
			T _A = T _{MIN} to T _{MAX}		150		
Break-Before-Make Time Delay (Note 3)	t _D	MAX322 only, R _L = 300Ω, C _L = 35pF, Figure 3		2	5	ns	
Charge Injection (Note 3)	Q	C _L = 1.0nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 4	T _A = +25°C	2	5	pC	
Off Isolation (Note 7)	OIRR	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 5	T _A = +25°C	72		dB	
Crosstalk (Note 8)		R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 6	T _A = +25°C	85		dB	
NC or NO Capacitance	C _(OFF)	f = 1MHz, Figure 7	T _A = +25°C	9		pF	
COM Off Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 7	T _A = +25°C	9		pF	
COM On Capacitance	C _{COM(ON)}	f = 1MHz, Figure 8	T _A = +25°C	22		pF	
SUPPLY							
Power-Supply Range				±2.7	±8	V	
Positive Supply Current	I+	V+ = 5.5V, V- = -5.5V, V _{IN} = 0V or V+, all channels on or off	T _A = +25°C	-125	80	125	μA
			T _A = T _{MIN} to T _{MAX}	-200		200	
Negative Supply Current	I-	V+ = 5.5V, V- = -5.5V, V _{IN} = 0V or V+, all channels on or off	T _A = +25°C	-125	80	125	μA
			T _A = T _{MIN} to T _{MAX}	-200		200	

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔRON = ΔRON max - ΔRON min.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 6: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.

Note 7: Off Isolation = 20 log10 [VCOM / (VNC or VNO)]. VCOM = output, VNC or VNO = input to off switch.

Note 8: Between any two switches.

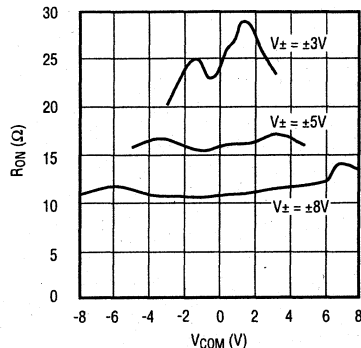
MAX320/MAX321/MAX322

Precision, Dual-Supply, SPST Analog Switches

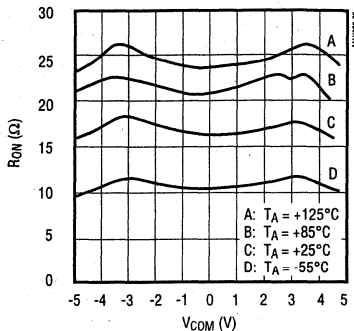
Typical Operating Characteristics

($V_+ = +5V$, $V_- = -5V$, $T_A = +25^\circ C$, unless otherwise noted.)

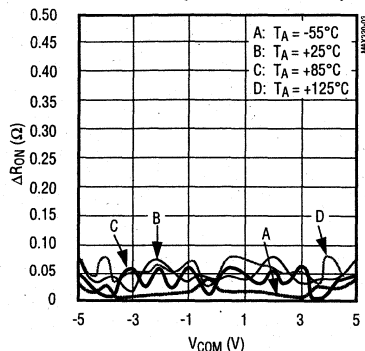
ON-RESISTANCE vs. VOLTAGE AT COM PIN



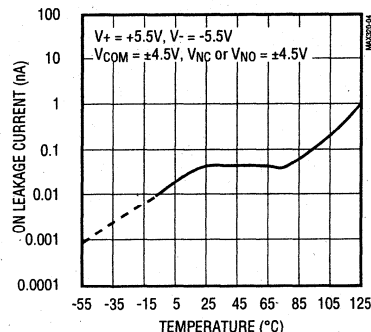
ON-RESISTANCE vs. VOLTAGE AT COM PIN (OVER TEMPERATURE)



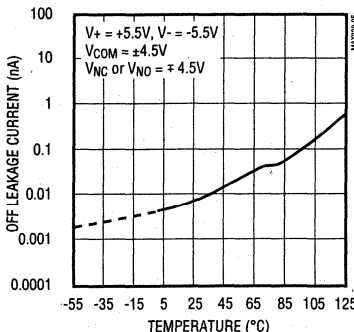
ON-RESISTANCE MATCH vs. VOLTAGE AT COM PIN (OVER TEMPERATURE)



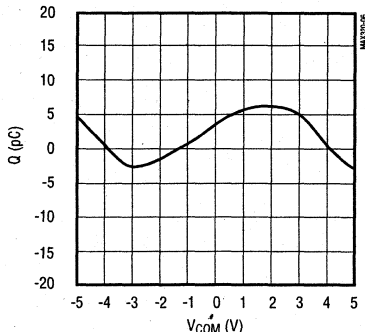
ON LEAKAGE CURRENT vs. TEMPERATURE



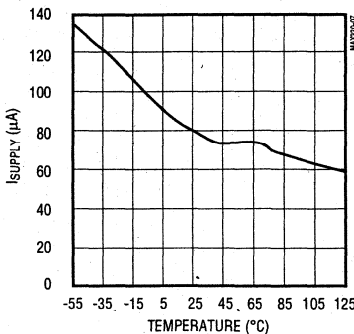
OFF LEAKAGE CURRENT vs. TEMPERATURE



CHARGE INJECTION vs. VOLTAGE AT COM PIN



SUPPLY CURRENT vs. TEMPERATURE



Precision, Dual-Supply, SPST Analog Switches

Pin Description

PIN	NAME	FUNCTION
1	NO1 (MAX320/MAX322)	Normally Open Analog Switch Terminal
	NC1 (MAX321)	Normally Closed Analog Switch Terminal
2, 6	COM1, COM2	Analog Switch Common Terminals
3, 7	IN2, IN1	Logic Inputs
4	V-	Negative Supply
5	NO2 (MAX320)	Normally Open Analog Switch Terminal
	NC2 (MAX321/MAX322)	Normally Closed Analog Switch Terminal
8	V+	Positive Supply

Applications Information

Logic Levels

Calculate the logic thresholds typically as follows: $V_{IH} = (V+ - 1.5V)$ and $V_{IL} = (V+ - 2.5V)$.

Power-supply consumption is minimized when IN1 and IN2 are driven with logic-high levels equal to V+ and logic-low levels well below the calculated V_{IL} of $(V+ - 2.5V)$. IN1 and IN2 can be driven to V- without damage.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V- to V+) can be switched, with very little change in on-resistance over the entire voltage range (see *Typical Operating Characteristics*). All switches are bidirectional, so NO_, NC_, and COM_ pins can be used as either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+, followed by V-, before applying analog signals or logic inputs, especially if the analog or logic signals are not current-limited. If

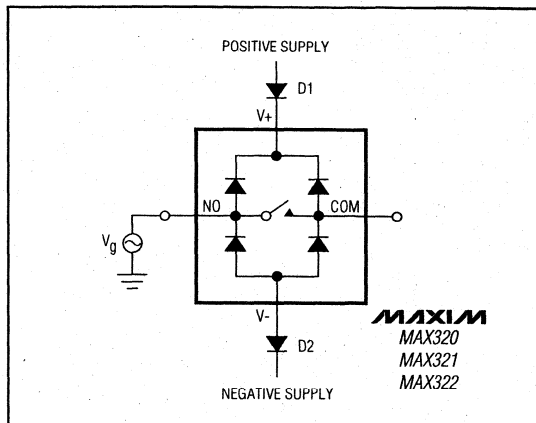


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

this sequencing is not possible, and if the analog or logic inputs are not current-limited to $<30mA$, add two small signal diodes (D1, D2) as shown in Figure 1. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ for D1, and a diode drop above V- for D2. Leakage is not affected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V- to V+) must not exceed 17V.

Adding protection diode D1 causes the logic thresholds to be shifted relative to the positive power-supply rail. This can be significant when low positive supply voltages (+5V or less) are used. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin or a diode drop lower than the V- pin) is always acceptable.

The protection diodes D1 and D2 also protect against some overvoltage situations. With the circuit of Figure 1, if the supply voltage is below the absolute maximum rating and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result. For example, with $\pm 5V$ supplies, analog signals up to $\pm 8.5V$ will not damage the circuit of Figure 1. If only a single fault signal is present, the fault voltage can rise to +12V or to -12V without damage.

MAX320/MAX321/MAX322

Precision, Dual-Supply, SPST Analog Switches

Test Circuits/Timing Diagrams

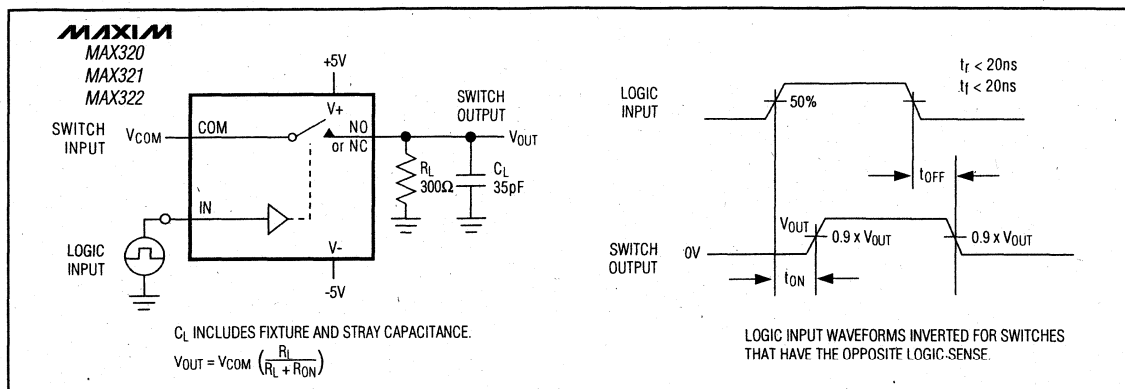


Figure 2. Switching Time

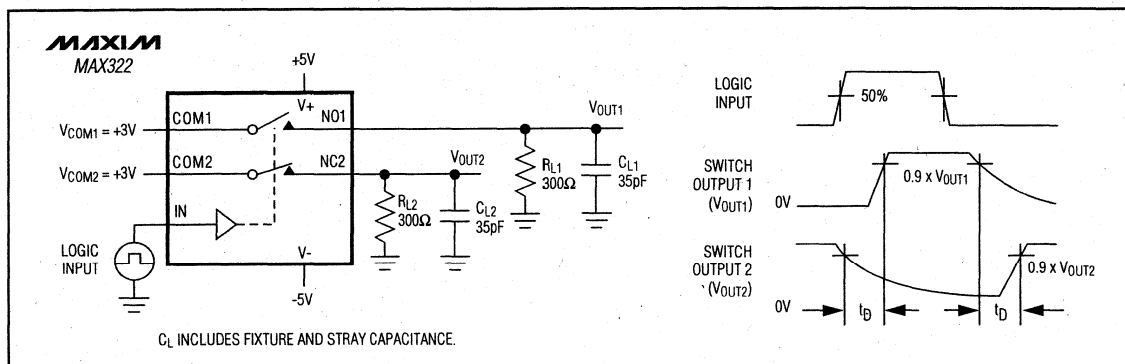


Figure 3. Break-Before-Make Interval (MAX322 only)

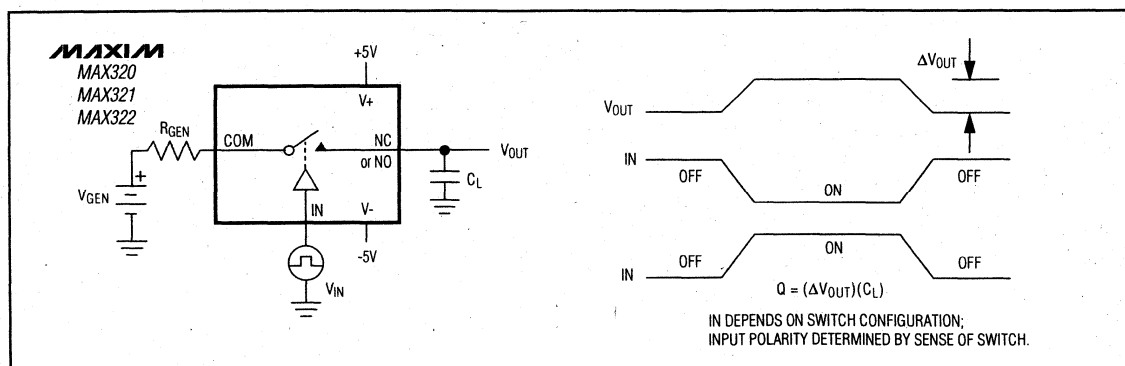


Figure 4. Charge Injection

Precision, Dual-Supply, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

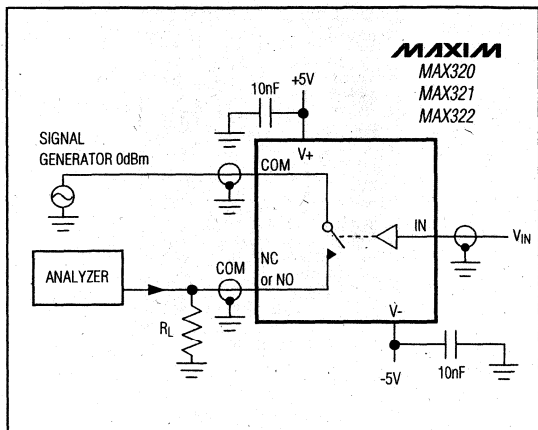


Figure 5. Off Isolation

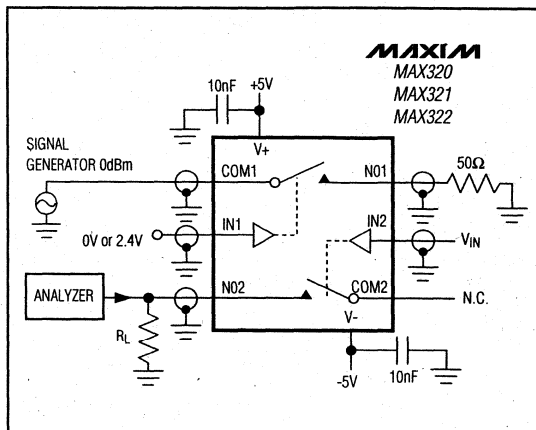


Figure 6. Crosstalk

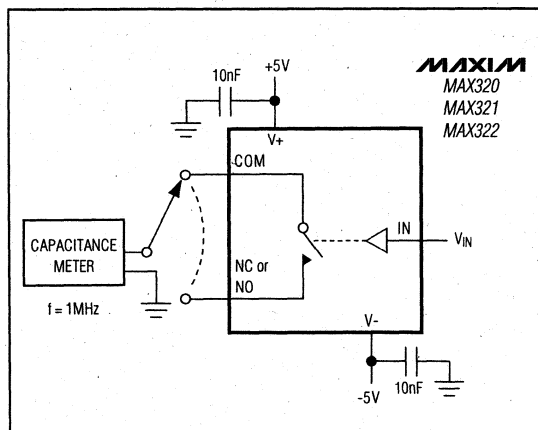


Figure 7. Channel-Off Capacitance

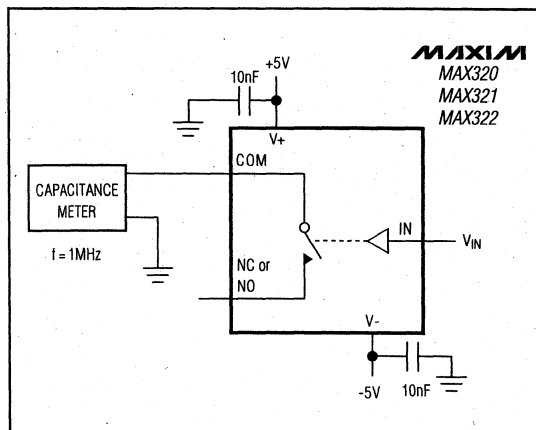


Figure 8. Channel-On Capacitance

MAX320/MAX321/MAX322

Precision, Dual-Supply, SPST Analog Switches

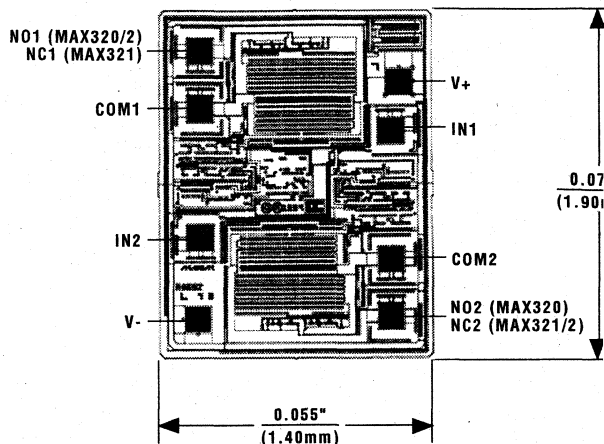
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX321CPA	0°C to +70°C	8 Plastic DIP
MAX321CSA	0°C to +70°C	8 SO
MAX321CUA	0°C to +70°C	8 μ MAX
MAX321C/D	0°C to +70°C	Dice*
MAX321EPA	-40°C to +85°C	8 Plastic DIP
MAX321ESA	-40°C to +85°C	8 SO
MAX321EJA	-40°C to +85°C	8 Cerdip**
MAX321MJA	-55°C to +125°C	8 Cerdip**
MAX322CPA	0°C to +70°C	8 Plastic DIP
MAX322CSA	0°C to +70°C	8 SO
MAX322CUA	0°C to +70°C	8 μ MAX
MAX322C/D	0°C to +70°C	Dice*
MAX322EPA	-40°C to +85°C	8 Plastic DIP
MAX322ESA	-40°C to +85°C	8 SO
MAX322EJA	-40°C to +85°C	8 Cerdip**
MAX322MJA	-55°C to +125°C	8 Cerdip**

* Contact factory for dice specifications.

** Contact factory for availability.

Chip Topography



TRANSISTOR COUNT: 91
SUBSTRATE CONNECTED TO V+

MAXIM

Precision, Single-Supply, SPST Analog Switches

General Description

The MAX323/MAX324/MAX325 are precision, dual, SPST analog switches. They are single-supply devices designed to operate from +2.7V to +16V. The MAX323 has two normally open (NO) switches, and the MAX324 has two normally closed (NC) switches. The MAX325 has one NO and one NC switch. Low power consumption (5 μ W) makes these parts ideal for battery-powered equipment. These switches offer low leakage currents (100pA max) and fast switching speeds (t_{ON} = 150ns max, t_{OFF} = 100ns max).

When powered from a 5V supply, the MAX323 series offers 2 Ω max matching between channels, 60 Ω max on-resistance, and 6 Ω max R_{ON} flatness.

These switches also offer 5pC max charge injection, and a minimum of 2000V ESD per Method 3015.7.

For equivalent devices specified for dual-supply operation, see the MAX320/MAX321/MAX322 data sheet. For quad versions of the MAX320 series, see MAX391/MAX392/MAX393 data sheet.

Applications

Battery-Operated Systems	Sample-and-Hold Circuits
Heads-Up Displays	Guidance and Control Systems
Audio and Video Switching	Military Radios
Test Equipment	Communications Systems
+3V, +5V DACs and ADCs	PBX, PABX

Features

- ◆ Low On-Resistance (R_{ON}), 60 Ω max (33 Ω typ)
- ◆ R_{ON} Matching Between Channels <2 Ω
- ◆ R_{ON} Flatness <6 Ω Max
- ◆ Guaranteed Charge Injection <5pC
- ◆ Single-Supply Operation (+2.7V to +16V)
- ◆ Low Power Consumption, <5 μ W
- ◆ Low Leakage Current Over Temperature, <2.5nA at +85°C
- ◆ Fast Switching: t_{ON} <150ns, t_{OFF} <100ns
- ◆ Guaranteed Break-Before-Make (MAX325 only)
- ◆ TTL/CMOS Logic Compatible

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX323CPA	0°C to +70°C	8 Plastic DIP
MAX323CUA	0°C to +70°C	8 μ MAX
MAX323CSA	0°C to +70°C	8 SO
MAX323C/D	0°C to +70°C	Dice*
MAX323EPA	-40°C to +85°C	8 Plastic DIP
MAX323ESA	-40°C to +85°C	8 SO
MAX323EJA	-40°C to +85°C	8 CERDIP**
MAX323MJA	-55°C to +125°C	8 CERDIP**

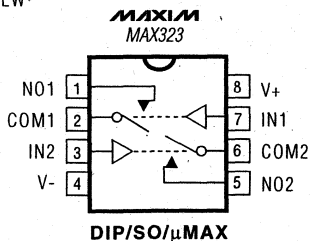
Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

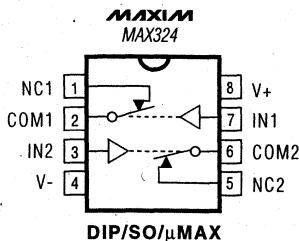
** Contact factory for availability.

Pin Configurations/Functional Diagrams/Truth Tables

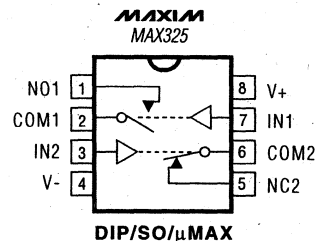
TOP VIEW



MAX323	
LOGIC	SWITCH
0	OFF
1	ON



MAX324	
LOGIC	SWITCH
0	ON
1	OFF



MAX325		
LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

MAX323/MAX324/MAX325

Precision, Single-Supply, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND

V+	-0.3V to +17V
IN ₋ , COM ₋ , NC ₋ , NO ₋ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current (any terminal)	30mA
Peak Current, COM ₋ , NO ₋ , NC ₋ (pulsed at 1ms, 10% duty cycle max)	100mA
ESD per Method 3015.7	>2000V
Continuous Power Dissipation Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
Narrow SO (derate 5.88mW/°C above +70°C)	471mW

CERDIP (derate 8.00mW/°C above +70°C)	640mW
μMAX (derate 4.10mW/°C above +70°C)	330mW
Operating Temperature Ranges	
MAX32_C_	0°C to +70°C
MAX32_E_	-40°C to +85°C
MAX32_MJA	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
ANALOG SWITCH								
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}	(Note 3)		0		V+	V	
On-Resistance	R _{ON}	V+ = 4.5V, I _{COM} = 1.0mA, V _{NO} or V _{NC} = 3.5V	T _A = +25°C	33		60	Ω	
			T _A = T _{MIN} to T _{MAX}			75		
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V+ = 5V, I _{COM} = 1.0mA, V _{NO} or V _{NC} = 3V	T _A = +25°C	0.8		2	Ω	
			T _A = T _{MIN} to T _{MAX}			4		
On-Resistance Flatness (Notes 3, 5)	R _{FLAT(ON)}	V+ = 5V, I _{COM} = 1.0mA, V _{NO} or V _{NC} = 1V, 2V, 3V	T _A = +25°C	2		6	Ω	
			T _A = T _{MIN} to T _{MAX}			8		
NO or NC Off Leakage Current (Note 6)	I _{NO(OFF)} or I _{NC(OFF)}	V+ = 5.5V, V _{COM} = 1V, V _{NO} or V _{NC} = 4.5V	T _A = +25°C	-0.1	0.01	0.1	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-5			5
				M	-40			40
COM Off Leakage Current (Note 6)	I _{COM(OFF)}	V+ = 5.5V, V _{COM} = 4.5V, V _{NO} or V _{NC} = 1V	T _A = +25°C	-0.1		0.1	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-5			5
				M	-40			40
COM On Leakage Current (Note 6)	I _{COM(ON)}	V+ = 5.5V, V _{COM} = 5V, or V _{NO} or V _{NC} = 5V	T _A = +25°C	-0.2		0.2	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-10			10
				M	-50			50

Precision, Single-Supply, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = 5V ±10%, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 3V	T _A = +25°C	85	150	ns	
			T _A = T _{MIN} to T _{MAX}		240		
Turn-Off Time	t _{OFF}	V _{NO} or V _{NC} = 3V	T _A = +25°C	25	100	ns	
			T _A = T _{MIN} to T _{MAX}		150		
Break-Before-Make Time Delay (Note 3)	t _D	MAX325 only, R _L = 300Ω, C _L = 35pF		2		ns	
Charge Injection (Note 3)	Q	C _L = 1.0nF, V _{GEN} = 0V, R _{GEN} = 0V, Figure 4	T _A = +25°C	1	5	pC	
Off Isolation (Note 7)	OIRR	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 5	T _A = +25°C	72		dB	
Crosstalk (Note 8)		R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 6	T _A = +25°C	85		dB	
NC or NO Capacitance	C _{OFF}	f = 1MHz, Figure 7	T _A = +25°C	9		pF	
COM Off Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 7	T _A = +25°C	9		pF	
COM On Capacitance	C _{COM(ON)}	f = 1MHz, Figure 8	T _A = +25°C	22		pF	
SUPPLY							
Power-Supply Range				2.7		16	V
Positive Supply Current	I ₊	V ₊ = 5.5V, V _{IN} = 0V or V ₊ , all channels on or off		-1	0.0001	1	μA
LOGIC INPUT							
Input Voltage Low	V _{INL}					0.8	V
Input Voltage High	V _{INH}			2.4			V

MAX323/MAX324/MAX325

Precision, Single-Supply, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

($V_+ = 3.0V$ to $3.6V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}	(Note 3)		0		V+	V
Channel On-Resistance	R _{ON}	V+ = 3V, I _{COM} = 1.0mA, V _{NO} or V _{NC} = 1.5V	TA = +25°C	83	175		Ω
			TA = T _{MIN} to T _{MAX}		275		
DYNAMIC							
Turn-On Time (Note 3)	t _{ON}	V _{NO} or V _{NC} = 1.5V	TA = +25°C	160	400		ns
			TA = T _{MIN} to T _{MAX}		500		
Turn-Off Time (Note 3)	t _{OFF}	V _{NO} or V _{NC} = 1.5V	TA = +25°C	40	125		ns
			TA = T _{MIN} to T _{MAX}		175		
Break-Before-Make Time Delay (Note 3)	t _D	MAX325 only, RL = 300Ω, CL = 35pF	TA = +25°C	2	5		ns
Charge Injection (Note 3)	Q	CL = 1.0nF, VGEN = 0V, RGEN = 0V	TA = +25°C		1	5	pC
SUPPLY							
Positive Supply Current	I+	V+ = 3.6V, VIN = 0V or V+, all channels on or off		-1		1	μA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON \text{ max}} - \Delta R_{ON \text{ min}}$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 6: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at $+25^\circ C$.

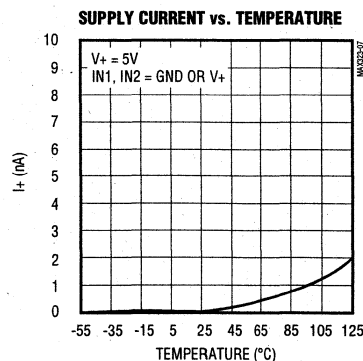
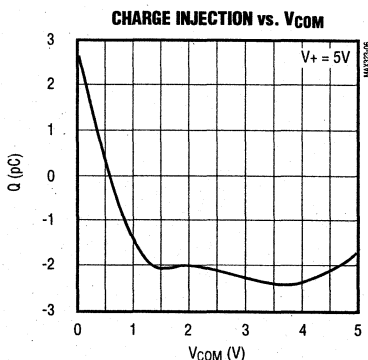
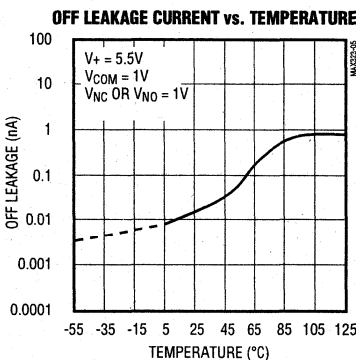
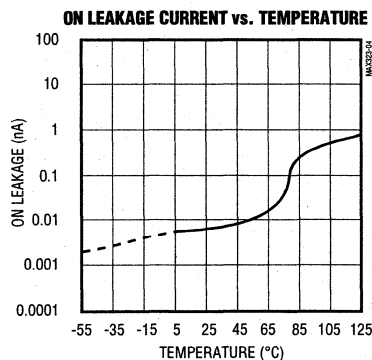
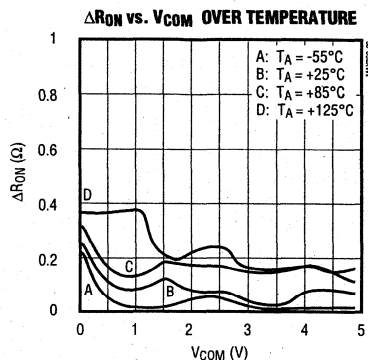
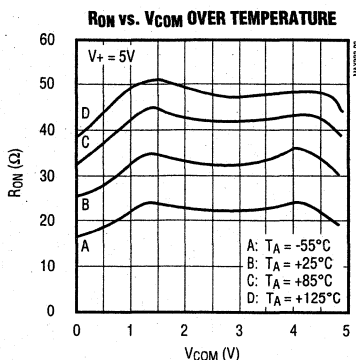
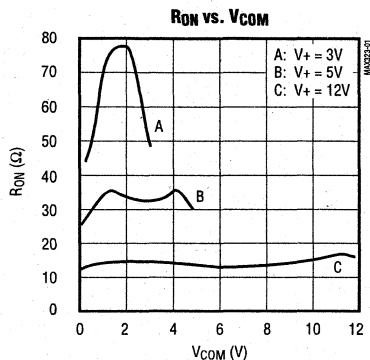
Note 7: Off Isolation = $20 \log_{10} [V_{COM} / (V_{NC} \text{ or } V_{NO})]$, V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

Note 8: Between any two switches.

Precision, Single-Supply, SPST Analog Switches

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



MAX323/MAX324/MAX325

Precision, Single-Supply, SPST Analog Switches

Pin Description

PIN	NAME	FUNCTION
1	NO1	Normally Open Analog Switch Terminal (MAX323/MAX325)
	NC1	Normally Closed Analog Switch Terminal (MAX324 only)
2, 6	COM1, COM2	Analog Switch Common Terminal
3, 7	IN2, IN1	Logic Inputs
4	GND	Ground
5	NO2	Normally Open Analog Switch Terminal (MAX323 only)
	NC2	Normally Closed Analog Switch Terminal (MAX324/MAX325)
8	V+	Positive Supply

Applications Information

Logic Levels

The MAX323/MAX324/MAX325 are TTL compatible when powered from a single +5V supply. When powered from other supply voltages, TTL compatibility is not guaranteed, and the logic inputs should be driven from rail to rail. For example, with a 15V supply, IN1 and IN2 should be driven low to 0V and high to 15V. Similarly, with a 3.3V supply, IN1 and IN2 should be driven low to 0V and high to 3.3V.

Driving IN1 and IN2 rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be switched with very little change in on-resistance over the entire voltage range (see *Typical Operating Characteristics*). All the switches are bidirectional, so NO_, NC_, and COM_ pins can be used as either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals or logic inputs, especially if the analog

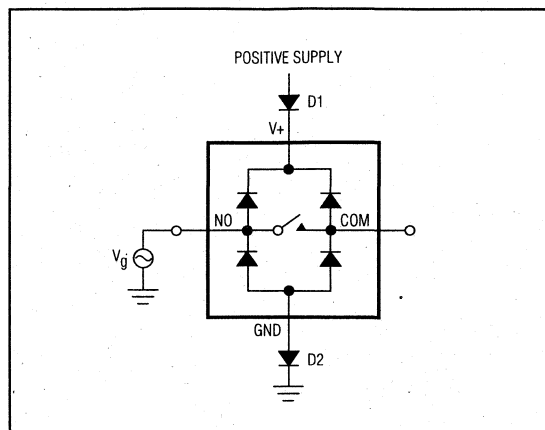


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

or logic signals are not current-limited. If this sequencing is not possible, and if the analog or logic inputs are not current-limited to <30mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode-drop (about 0.7V) below V+ (for D1), and to a diode-drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V+) must not exceed 17V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. This can be significant when low supply voltages (5V or less) are used. With a 5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e. to a diode-drop higher than the V+ pin, or to a diode-drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result. For example, with a +5V supply, analog signals up to $\pm 8V$ will not damage the circuit of Figure 1. If only a single fault signal is present, the fault voltage can rise to +17V or to -12V without damage occurring.

Precision, Single-Supply, SPST Analog Switches

Test Circuits/Timing Diagrams

MAX323/MAX324/MAX325

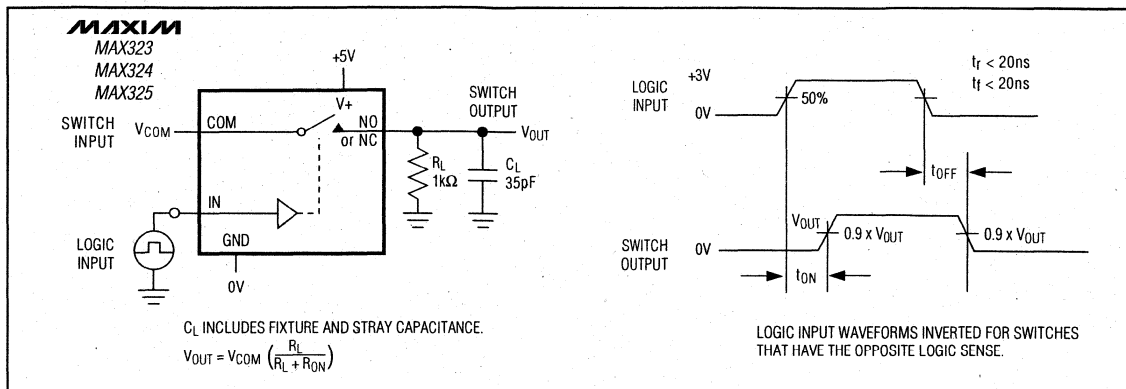


Figure 2. Switching Time

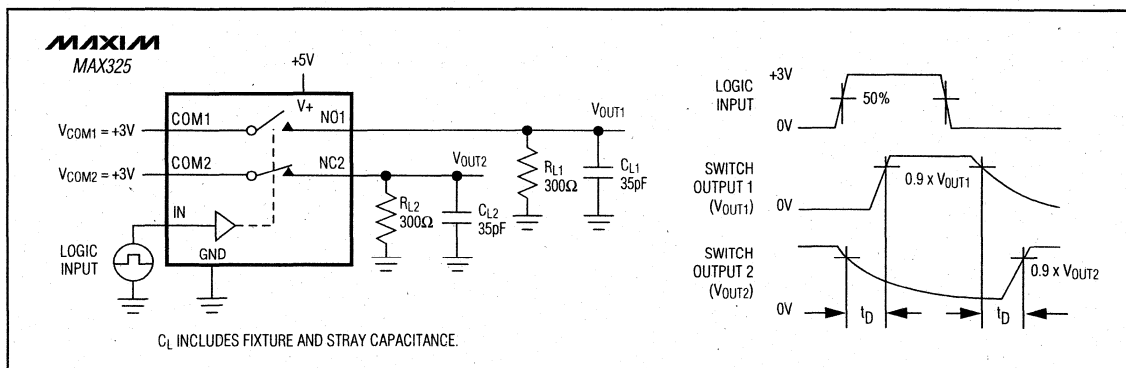


Figure 3. Break-Before-Make Interval (MAX325 only)

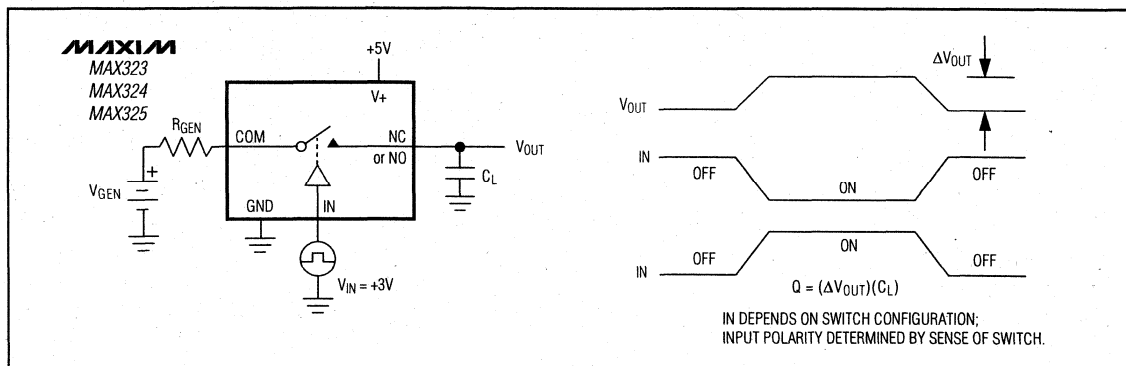


Figure 4. Charge Injection

Precision, Single-Supply, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

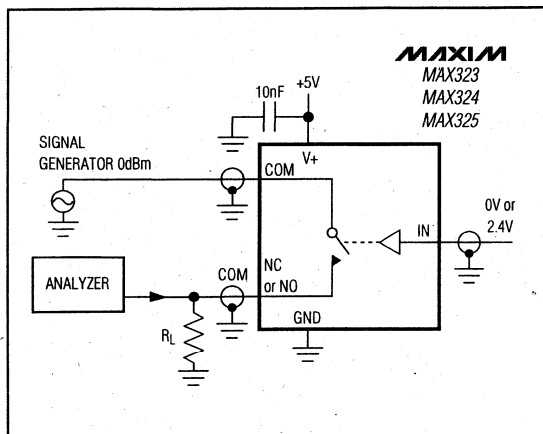


Figure 5. Off Isolation

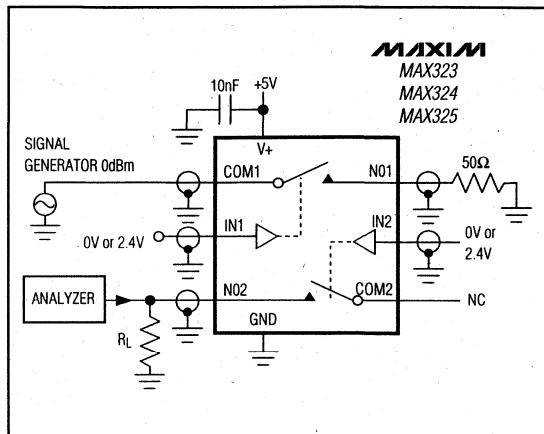


Figure 6. Crosstalk

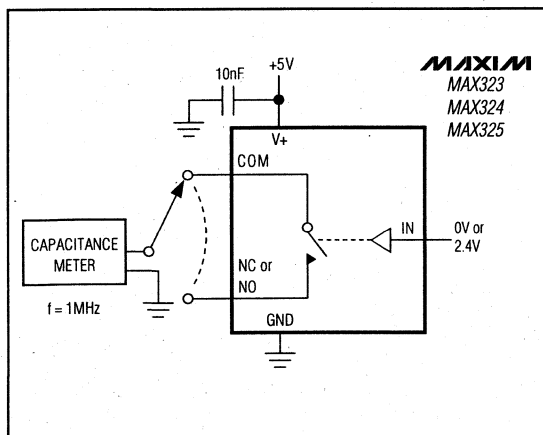


Figure 7. Channel-Off Capacitance

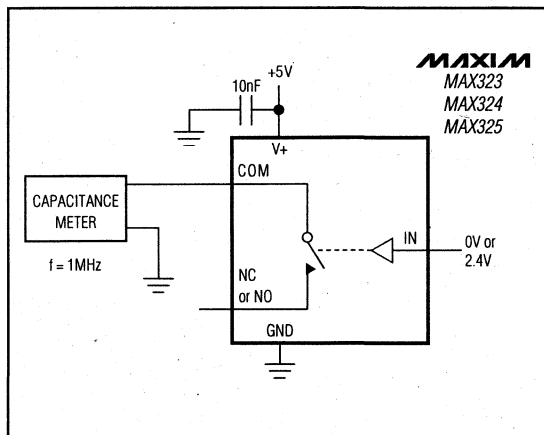


Figure 8. Channel-On Capacitance

Precision, Single-Supply, SPST Analog Switches

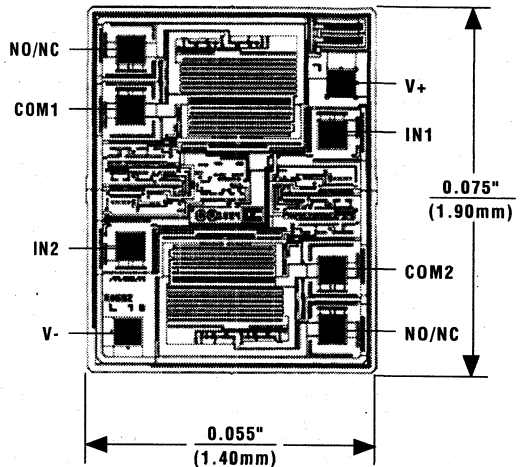
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX324CPA	0°C to +70°C	8 Plastic DIP
MAX324CUA	0°C to +70°C	8 μ MAX
MAX324CSA	0°C to +70°C	8 SO
MAX324C/D	0°C to +70°C	Dice*
MAX324EPA	-40°C to +85°C	8 Plastic DIP
MAX324ESA	-40°C to +85°C	8 SO
MAX324EJA	-40°C to +85°C	8 CERDIP**
MAX324MJA	-55°C to +125°C	8 CERDIP**
MAX325CPA	0°C to +70°C	8 Plastic DIP
MAX325CUA	0°C to +70°C	8 μ MAX
MAX325CSA	0°C to +70°C	8 SO
MAX325C/D	0°C to +70°C	Dice*
MAX325EPA	-40°C to +85°C	8 Plastic DIP
MAX325ESA	-40°C to +85°C	8 SO
MAX325EJA	-40°C to +85°C	8 CERDIP**
MAX325MJA	-55°C to +125°C	8 CERDIP**

* Contact factory for dice specifications.

** Contact factory for availability.

Chip Topography



MAX323/MAX324/MAX325

TRANSISTOR COUNT: 91
SUBSTRATE IS CONNECTED TO V+



Fault-Protected Analog Multiplexers

General Description

The MAX354/MAX355 fault-protected multiplexers (muxes) use a series N-channel, P-channel, N-channel structure that protects the devices from overvoltage up to 40V beyond the supply rails during power-up, power-down, and fault conditions. The MAX354/MAX355 also protect sensitive circuit components against voltages near or beyond the normal supplies.

The MAX354 single 8-channel mux and the MAX355 dual 4-channel mux protect analog signals while operating from a single 4.5V to 36V supply or $\pm 4.5V$ to $\pm 18V$ dual supplies. These muxes have 350 Ω on-resistance and can be used for demultiplexing as well as multiplexing. Input leakage current is less than 0.5nA at +25°C and less than 5nA at +85°C.

All digital inputs have 0.8V and 2.4V logic thresholds, ensuring both TTL and CMOS logic compatibility without pull-up resistors. Break-before-make operation is guaranteed and power consumption is less than 1.5mW.

Applications

Data-Acquisition Systems
Industrial and Process Control
Avionics
ATE Equipment
Signal Routing
Redundant/Backup Systems

Features

- ◆ 350 Ω Max On-Resistance
- ◆ Improved 2nd Source for MAX358/MAX359 and DG458/DG459
- ◆ Pin Compatible with ADG508F/ADG509F
- ◆ All Switches Off with Supplies Off
- ◆ On Switch Turns Off with Overvoltage
- ◆ Output Clamps at 1.5V Below Supply Rails
- ◆ 0.5nA Max Input Leakage at +25°C (5nA at +85°C)
- ◆ No Power-Up Sequencing Required
- ◆ TTL and CMOS-Logic Compatibility

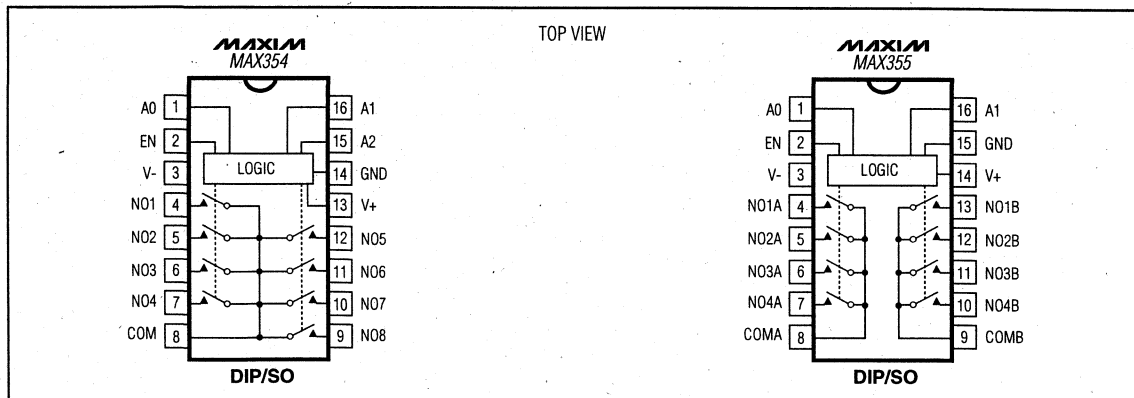
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX354CPE	0°C to +70°C	16 Plastic DIP
MAX354CWE	0°C to +70°C	16 Wide SO
MAX354C/D	0°C to +70°C	Dice*
MAX354EPE	-40°C to +85°C	16 Plastic DIP
MAX354EWE	-40°C to +85°C	16 Wide SO
MAX354MJE	-55°C to +125°C	16 Cerdip**
MAX355CPE	0°C to +70°C	16 Plastic DIP
MAX355CWE	0°C to +70°C	16 Wide SO
MAX355C/D	0°C to +70°C	Dice*
MAX355EPE	-40°C to +85°C	16 Plastic DIP
MAX355EWE	-40°C to +85°C	16 Wide SO
MAX355MJE	-55°C to +125°C	16 Cerdip**

* Dice are tested at $T_A = +25^\circ\text{C}$ only.

** Contact factory for availability.

Pin Configurations



Fault-Protected Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND, unless otherwise noted.)

V+	-0.3V to +44V
V-	+0.3V to -44V
V+ to V-	-0.3V to +44V
Digital Inputs	(V+ + 0.3V) to (V- - 0.3V)
Input Overvoltage with Mux Power On	
V+ = +15V	+25V
V- = -15V	-25V
Input Overvoltage with Mux Power Off	
V+ = 0V	+40V
V- = 0V	-40V
Continuous Current into Any terminal	±30mA

Peak Current into Any Terminal	±50mA
Continuous Power Dissipation (TA = +70°C)	
Plastic DIP (derate 10.53mW/°C above +70°C)	842mW
Wide SO (derate 9.52mW/°C above +70°C)	762mW
CERDIP (derate 10.00mW/°C above +70°C)	800mW
Operating Temperature Ranges	
MAX35_C_	0°C to +70°C
MAX35_E_	-40°C to +85°C
MAX35_M_	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +15V, V- = -15V, GND = 0V, VAH = VENH = 2.4V, VAL = VENL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS	
SWITCH										
Analog Signal Range	V _{COM} , V _{NO}	(Note 1)				(V+ - 40)		(V- + 40)		
Fault-Free Analog Signal Range		V+ = +15V, V- = -15V (Note 1)				-12		12		
On-Resistance (Note 2)	R _{ON}	I _{NO} = 1.0mA, V _{COM} = ±10V	T _A = +25°C		285		350		Ω	
			T _A = T _{MIN} to T _{MAX}	C, E	400					
				M	475					
On-Resistance Matching Between Channels	ΔR _{ON}	I _{NO} = 1.0mA, V _{COM} = ±10V (Note 3)	T _A = +25°C		7		12		Ω	
			T _A = T _{MIN} to T _{MAX}		15					
NO-Off Leakage Current (Note 4)	I _{NO} (OFF)	V _{COM} = ±10V, V _{NO} = ±10V, V _{EN} = 0V	T _A = +25°C		-0.5	0.01	0.5		nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-5.0		5.0			
				M	-50		50			
COM-Off Leakage Current (Note 4)	I _{COM} (OFF)	V _{COM} = ±10V, V _{NO} = ±10V, V _{EN} = 0V	MAX354	T _A = +25°C		-0.5	0.02	0.5		nA
				T _A = T _{MIN} to T _{MAX}	C, E	-25		25		
					M	-100		100		
		V _{COM} = ±10V, V _{NO} = ±10V, V _{EN} = 0V	MAX355	T _A = +25°C		-0.5	0.02	0.5		
				T _A = T _{MIN} to T _{MAX}	C, E	-15		15		
					M	-50		50		
COM-On Leakage Current (Note 4)	I _{COM} (ON)	V _{COM} = ±10V, V _{NO} = ±10V, sequence each switch on	MAX354	T _A = +25°C		-0.5	0.02	0.5		nA
				T _A = T _{MIN} to T _{MAX}	C, E	-30		30		
					M	-200		200		
			MAX355	T _A = +25°C		-0.5	0.02	0.5		
				T _A = T _{MIN} to T _{MAX}	C, E	-15		15		
					M	-100		100		

Fault-Protected Analog Multiplexers

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT							
Output Leakage Current (with Overvoltage)		V _D = 0V, analog overvoltage = ±33V	T _A = +25°C	-5	0.01	5	nA
			T _A = T _{MIN} to T _{MAX}	-2		2	μA
Input Leakage Current (with Overvoltage)		V _{IN} = ±25V, V _O = ±10V	T _A = +25°C	-0.1	0.001	0.1	μA
			T _A = T _{MIN} to T _{MAX}	-2		2	
Input Leakage Current (with Power Supplies Off)		V _{IN} = ±25V, V _{EN} = V _O = 0V, V _{A0} = V _{A1} = V _{A2} = 0V or 5V	T _A = +25°C	-0.1	0.001	0.1	μA
			T _A = T _{MIN} to T _{MAX}	-2		2	
DIGITAL LOGIC INPUT							
Logic High Input Voltage	V _{A,H} , V _{ENH}		T _A = T _{MIN} to T _{MAX}	2.4			V
Logic Low Input Voltage	V _{A,L} , V _{ENL}		T _A = T _{MIN} to T _{MAX}			0.8	V
Input Current with Input Voltage High	I _{A,H} , I _{ENH}	V _A = V _{EN} = 2.4V	T _A = +25°C	-1		1	μA
			T _A = T _{MIN} to T _{MAX}	-5		5	
Input Current with Input Voltage Low	I _{A,L} , I _{ENL}	V _A = V _{EN} = 0.8V	T _A = +25°C	-1		1	μA
			T _A = T _{MIN} to T _{MAX}	-5		5	
SUPPLY							
Power-Supply Range				±4.5		±18	V
Positive Supply Current	I+	V _{EN} = V _A = 5V	T _A = +25°C	-100		100	μA
			T _A = T _{MIN} to T _{MAX}	-200		200	
Negative Supply Current	I-	V _{EN} = V _A = 0V	T _A = +25°C	-1		1	μA
			T _A = T _{MIN} to T _{MAX}	-100		100	
DYNAMIC							
Transition Time	t _{TRANS}	Figure 1	T _A = +25°C		180	250	ns
			T _A = T _{MIN} to T _{MAX}			400	
Enable Turn-On Time	t _{ON(EN)}	Figure 2	T _A = +25°C		160	250	ns
			T _A = T _{MIN} to T _{MAX}			400	
Enable Turn-Off Time	t _{OFF(EN)}	Figure 2	T _A = +25°C		80	200	ns
			T _A = T _{MIN} to T _{MAX}			300	
Break-Before-Make Interval	t _{OPEN}	Figure 3	T _A = +25°C	50	100		ns
Charge Injection	V _{CTE}	C _L = 10nF, V _S = 0V, R _S = 0Ω, Figure 4	T _A = +25°C		80		pC
Off Isolation	V _{ISO}	V _{EN} = 0V, R _L = 1kΩ, f = 100kHz, Figure 5	T _A = +25°C		100		dB
Crosstalk Between Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{p-p} , R _L = 1kΩ, Figure 6	T _A = +25°C		92		dB
Logic Input Capacitance	C _{IN}	f = 1MHz, Figure 7	T _A = +25°C		2.5		pF
NO-Off Capacitance	C _{NO(OFF)}	f = 1MHz, V _{EN} = V _D = 0V	T _A = +25°C		1.6		pF

Fault-Protected Analog Multiplexers

ELECTRICAL CHARACTERISTICS (continued)

($V_+ = +15V$, $V_- = -15V$, $GND = 0V$, $V_{AH} = V_{ENH} = 2.4V$, $V_{AL} = V_{ENL} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC (cont'd)						
COM-Off Capacitance	$C_{COM(OFF)}$	$f = 1MHz$, Figure 7, $V_{EN} = V_D = 0V$	MAX354 MAX355	$T_A = +25^\circ C$	11	pF
					5	
COM-On Capacitance	$C_{COM(ON)}$	$f = 1MHz$, Figure 7, $V_{EN} = V_D = 0V$	MAX354 MAX355	$T_A = +25^\circ C$	28	pF
					14	
Setting Time (Note 5)	t_{SETT}	0.1% 0.01%		$T_A = +25^\circ C$	1	μs
					2.5	

Note 1: When the analog signal exceeds $+13.5V$ or $-13.5V$, the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow, and the channel on-resistance rises to infinity (see *Typical Operating Characteristics*).

Note 2: Electrical characteristics such as on-resistance will change when power supplies other than $\pm 15V$ are used.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$

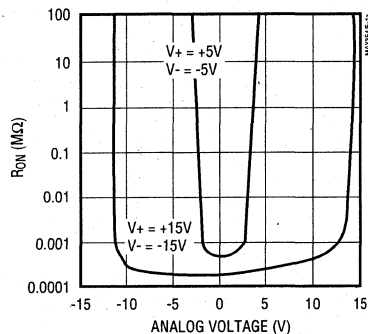
Note 4: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at $+25^\circ C$.

Note 5: Guaranteed by design.

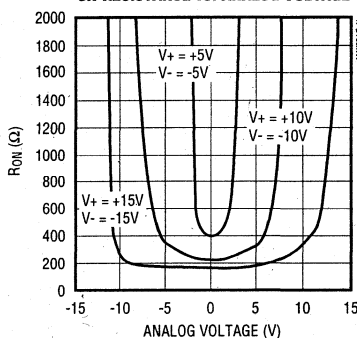
Typical Operating Characteristics

($T_A = +25^\circ C$, unless otherwise noted.)

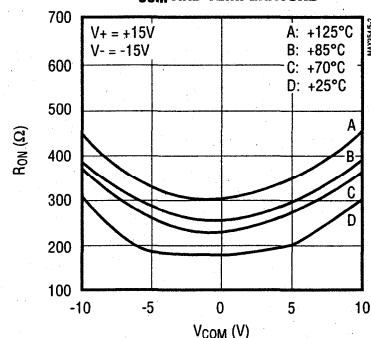
ON-RESISTANCE vs. ANALOG VOLTAGE



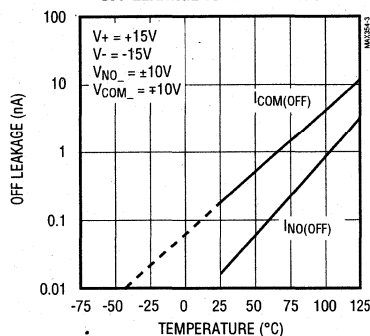
ON-RESISTANCE vs. ANALOG VOLTAGE



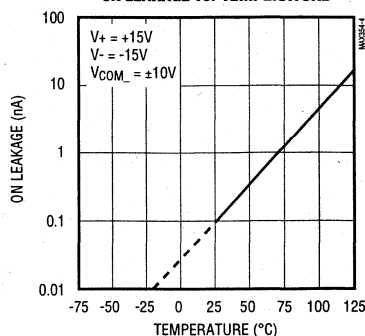
ON-RESISTANCE vs. VCOM AND TEMPERATURE



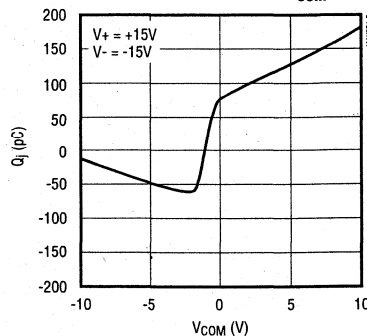
OFF LEAKAGE vs. TEMPERATURE



ON LEAKAGE vs. TEMPERATURE



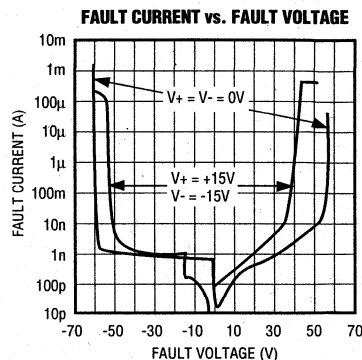
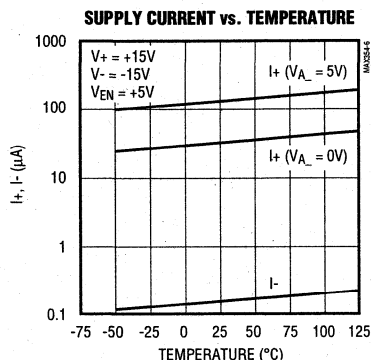
CHARGE INJECTION vs. VCOM



Fault-Protected Analog Multiplexers

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
MAX354	MAX355		
1, 15, 16	—	A0, A2, A1	Address Logic Inputs
—	1, 16	A0, A1	Address Logic Inputs
2	2	EN	Enable Logic Input. See truth tables
3	3	V-	Negative Supply Voltage Input. Connect to GND for single supply operation.
4–7	—	NO1–NO4	Analog Inputs—bidirectional
—	4–7	NO1A–NO4A	Analog Inputs—bidirectional “A” switch
8	—	COM	Analog Output—bidirectional
—	8, 9	COMA, COMB	Analog Outputs—bidirectional
9–12	—	NO8–NO5	Analog Inputs—bidirectional
—	10–13	NO4B–NO1B	Analog Inputs—bidirectional “B” switch
13	14	V+	Positive Supply Voltage Input
14	15	GND	Ground

Note: Analog inputs and outputs are electrically identical and completely interchangeable.

Fault-Protected Analog Multiplexers

Test Circuits/Timing Diagrams

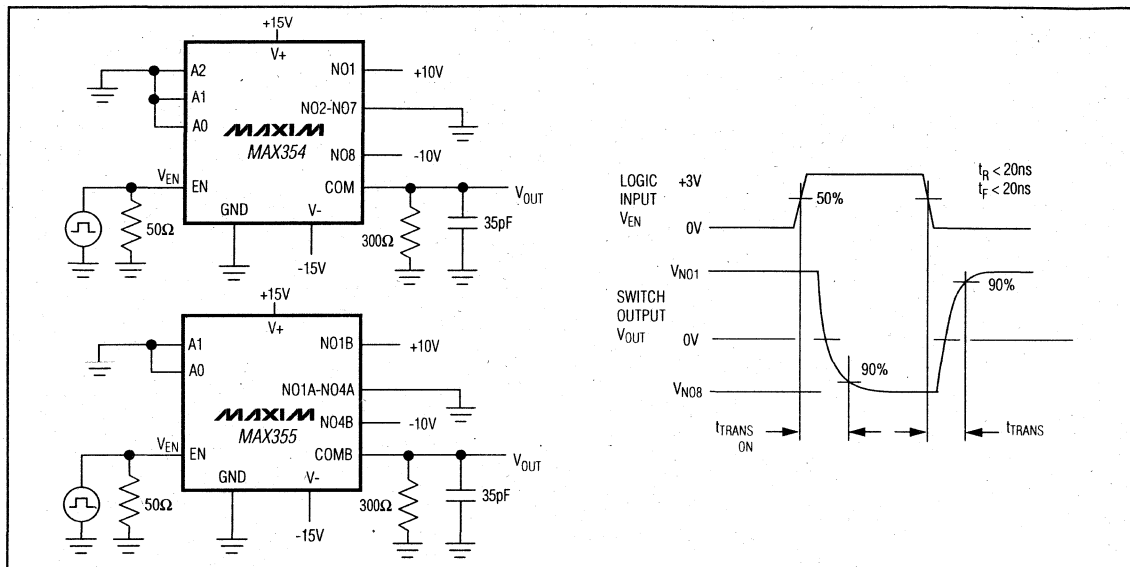


Figure 1. Transition Time

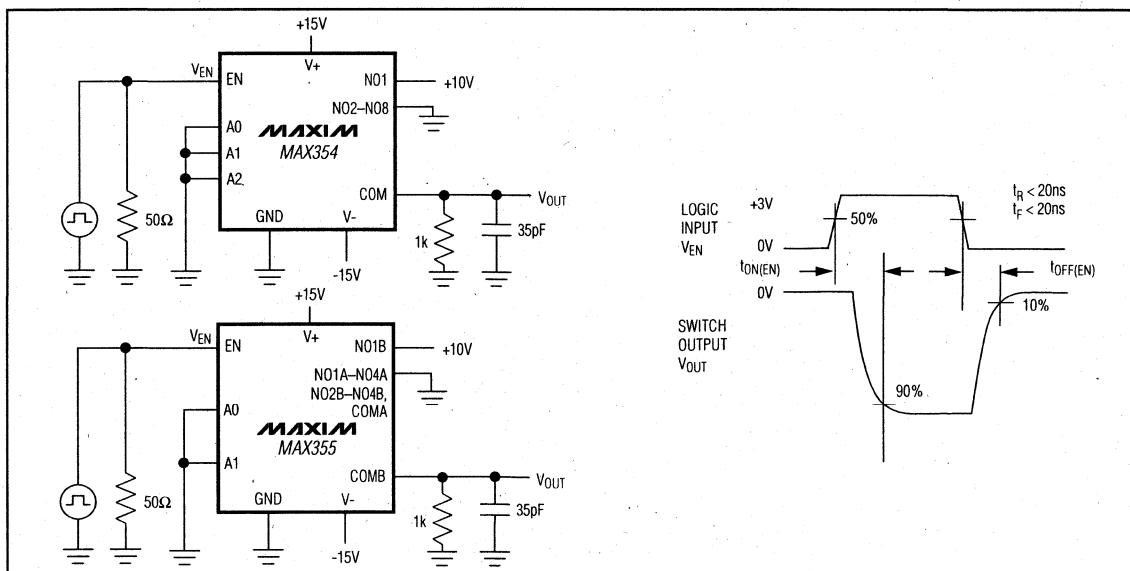


Figure 2. Enable Switching Time

Fault-Protected Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

MAX354/MAX355

1

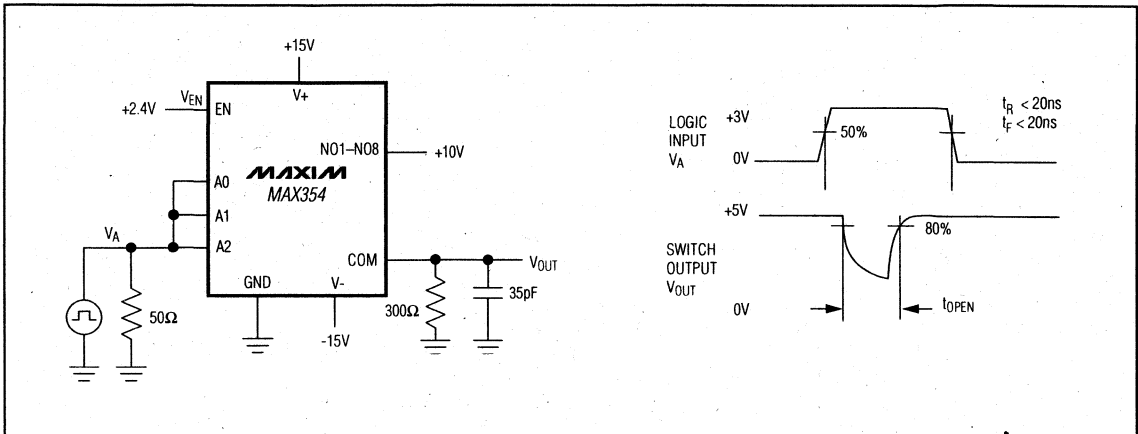


Figure 3. Break-Before-Make Interval

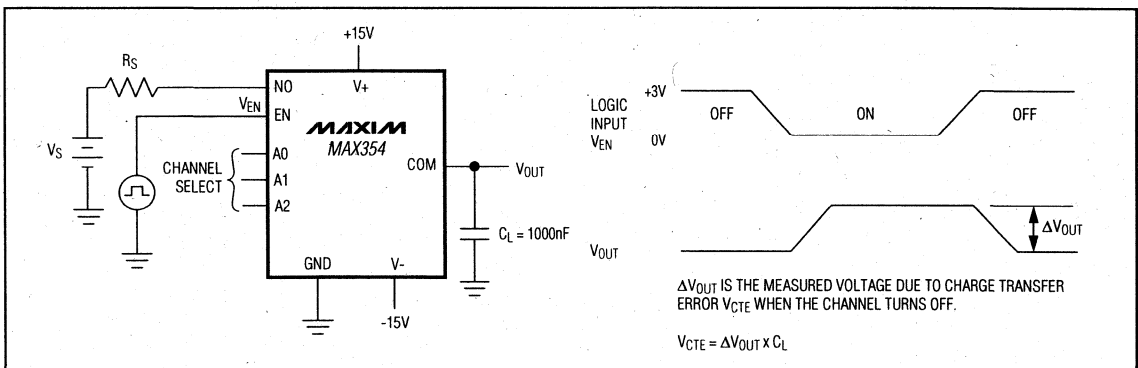


Figure 4. Charge Injection

Fault-Protected Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

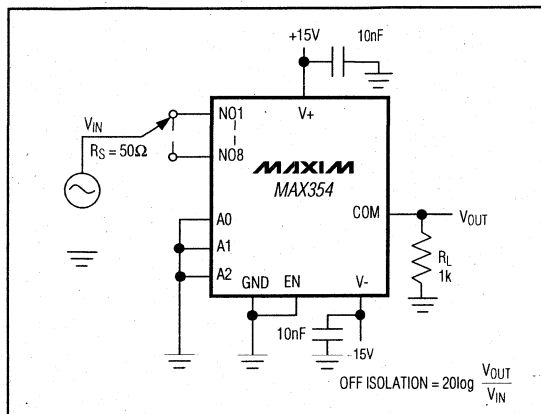


Figure 5. Off Isolation

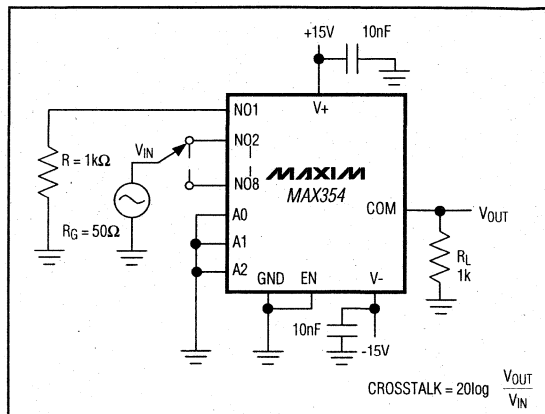


Figure 6. Crosstalk

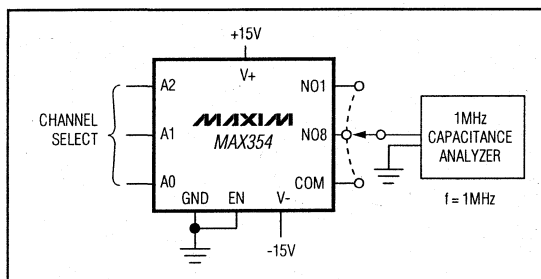


Figure 7. NO/COM Capacitance

Detailed Description

Fault-Protection Circuitry

Maxim's MAX354/MAX355 are fully fault protected for continuous input voltages up to $\pm 40V$, whether or not the $V+$ and $V-$ power supplies are present. These devices use a "series FET" protection scheme that not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels. When signal voltages exceed or are within approximately 1.5V of the supply rails, on-resistance increases. This greater on-resistance limits fault currents and output voltage, protecting sensitive circuits and components. The protected output clamps at approximately

1.5V below the supply rails and maintains the correct polarity. There are no glitches or polarity reversals going into or coming out of a fault condition.

Figures 8 and 9 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -25V input, N-channel FET Q1 is turned on by the +25V gate-to-source voltage. The P-channel device (Q2), however, has +25V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +25V, Q1 has a negative V_{GS} , which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any voltage will turn off either Q1 or Q2.

Fault-Protected Analog Multiplexers

Figure 10 shows the condition of an off channel with V_+ and V_- present. As with Figures 8 and 9, either an N-channel or a P-channel device will be off for any input voltage from $-40V$ to $+40V$. The leakage current with negative overvoltages will immediately drop to a few nanoamps at $+25^\circ C$. For positive overvoltages, that fault current will initially be $10\mu A$ or $20\mu A$, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault-protection scheme.

Figure 11 shows the condition of the on channel with V_+ and V_- present. With input voltages less than $\pm 10V$, all three FETs are on and the input signal appears at the output. If the input voltage exceeds V_+ minus the N-channel threshold voltage (V_{TN}), the N-channel FET will turn off. For voltages more negative than V_- minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically $1.5V$ and V_{TP} is typically $3V$, the multiplexer's output swing is limited to about $-12V$ to $+13.5V$ with $\pm 15V$ supplies.

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels versus power-supply voltages and analog input voltage. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

Table 1. MAX354 Charge Injection

Supply Voltage	Analog Input Level	Injected Charge
$\pm 5V$	$+2V$	$52pC$
	$0V$	$35pC$
	$-2V$	$16pC$
$\pm 10V$	$+5V$	$105pC$
	$0V$	$65pC$
	$-5V$	$25pC$
$\pm 15V$	$+10V$	$180pC$
	$0V$	$80pC$
	$-10V$	$15pC$

Test Conditions: $C_L = 1000pF$ on mux output; the tabulated analog input level is applied to channel 1; channels 2–8 inputs are open circuited. $EN = +5V$, $V_{A1} = V_{A2} = 0V$, V_O is toggled at a $2kHz$ rate between $0V$ and $3V$. $+100pC$ of charge creates a $+100mV$ step when injected into a $1000pF$ load capacitance.

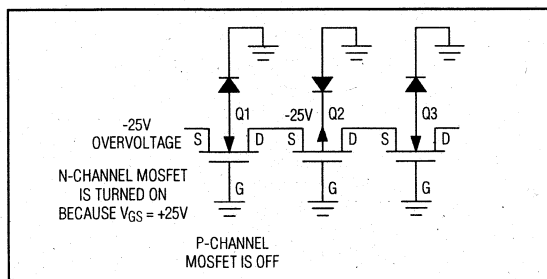


Figure 8. $-25V$ Overvoltage with Multiplexer Power Off

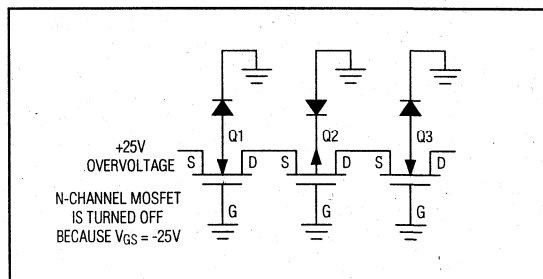


Figure 9. $+25V$ Overvoltage with Multiplexer Power Off

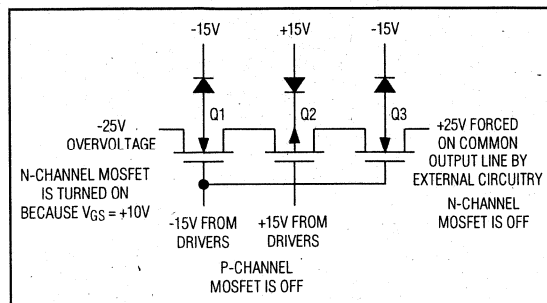


Figure 10. $-25V$ Overvoltage on an Off Channel with Multiplexer Power Supply On

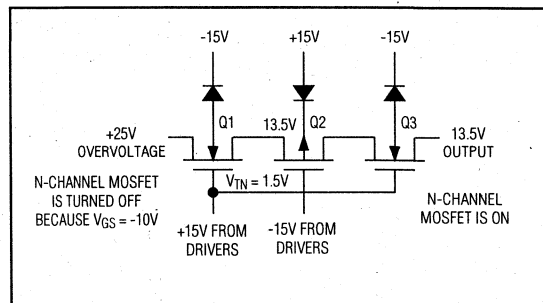


Figure 11. $+25V$ Overvoltage Input to the On Channel

Fault-Protected Analog Multiplexers

The channel-to-channel switching time is typically 180ns, with about 100ns of break-before-make delay. This 100ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system, the dominant delay is not the switching time of multiplexer, but is the settling time of the amplifiers and S/H. Another limiting factor is the RC time constant of the multiplexer R_{ON} plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output will approximately double the settling time to 0.01% accuracy.

Operation with Supply Voltages Other than $\pm 15V$

The main effect of supply voltages other than $\pm 15V$ is the reduction in output signal range. The MAX354 limits the output voltage to about 1.5V below $V+$ and about 3V above $V-$. In other words, the output swing is limited to +3.5V to -2V when operating from $\pm 5V$. The *Typical Operating Characteristics* show R_{ON} for +15V and $\pm 5V$ power supplies. Maxim tests and guarantees the MAX354/MAX355 for operation from $\pm 4.5V$ to $\pm 18V$ supplies. The switching delays are increased by about a factor of 2 at $\pm 5V$, but break-before-make action is preserved.

The MAX354/MAX355 can operate with a single +4.5V to +30V supply, as well as asymmetrical power supplies such as +15V and -5V. The digital threshold remains approximately 1.6V above the GND pin, and the analog characteristics, such as R_{ON} , are determined by the total voltage difference between $V+$ and $V-$. Connect $V-$ to 0V when operating with a +4.5V to +30V single supply.

The MAX354 digital threshold is relatively independent of the power-supply voltages, going from 1.6V typical when $V+$ is 15V to 1.5V typical when $V+$ is 5V. This means that the MAX354/MAX355 operate with standard TTL-logic levels, even with $\pm 5V$ power supplies. In all cases, the threshold of the enable (EN) pin is the same as the other logic inputs.

Digital Interface Levels

The typical digital threshold of both the address lines and the enable pin is 1.6V, with a temperature coefficient of about $-3mV/^{\circ}C$. This ensures compatibility with 0.8V to 2.4V TTL-logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from $\pm 15V$ to $\pm 5V$. In all cases, the digital threshold is referenced to the GND pin.

The digital inputs can also be driven with CMOS-logic levels swinging from either $V+$ to $V-$ or from $V+$ to ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1 μA .

Operation as a Demultiplexer

The MAX354/MAX355 function as demultiplexers where the input is applied to the output pin, and the input pins are used as outputs. The MAX354/MAX355 provide both break-before-make action and full fault protection when operated as demultiplexers, unlike earlier generations of fault-protected muxes.

Channel-to-Channel Crosstalk, Off-Isolation, and Digital Feedthrough

At DC and low frequencies the channel-to-channel crosstalk is caused by variations in output leakage currents as the off-channel input voltages are varied. The MAX354 output leakage varies only a few picoamps as all seven off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX354 output, which is R_{ON} plus the input signal source resistance in most cases, since the load driven by the MAX354 is usually high impedance. For a signal source impedance of 10k Ω or lower, the DC crosstalk exceeds 120dB.

Tables 2a and 2b show typical AC crosstalk and off-isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled. When the output is disabled, the digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the GND and $V-$ pins. The ground plane formed by these lines is continued onto the MAX354/MAX355 die to provide over 100dB isolation between the digital and analog sections.

Fault-Protected Analog Multiplexers

Table 2a. Typical Off-Isolation Rejection Ratio

Frequency	100kHz	1MHz
One Channel Driven	100dB	80dB

Test Conditions: $V_{IN} = 20V_{p-p}$ at the tabulated frequency, $R_L = 1.5k\Omega$ between OUT and ground, $EN = 0V$.

$$V_{ISO} = 20 \log \frac{20V_{p-p}}{V_{OUT} (p-p)}$$

Table 2b. Typical Crosstalk Rejection Ratio

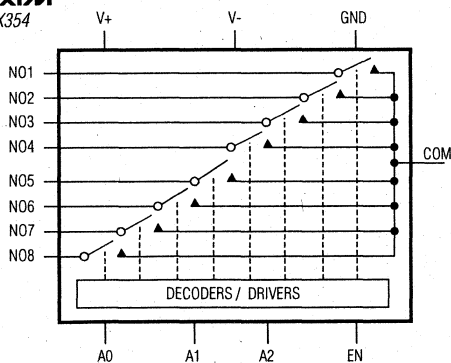
Frequency	100kHz	1MHz
$R_L = 1.5k\Omega$	92dB	72dB
$R_L = 10k\Omega$	76dB	56dB

Test Conditions: Specified R_L connected from OUT to ground, $EN = +5V$, $A_0 = A_1 = A_2 = +5V$ (Channel 1 selected). $20V_{p-p}$ at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

Functional Diagrams/Truth Tables

1

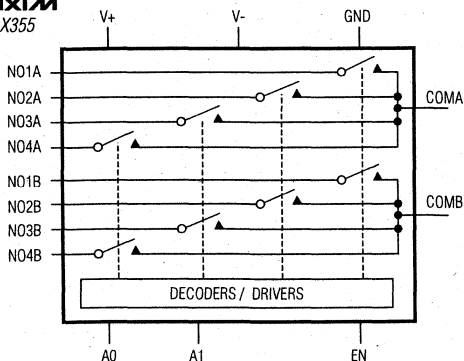
MAXIM
MAX354



MAX354				
A0	A1	A2	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "0" $V_{AL} \leq +0.8V$, LOGIC "1" $V_{AH} \geq +2.4V$

MAXIM
MAX355

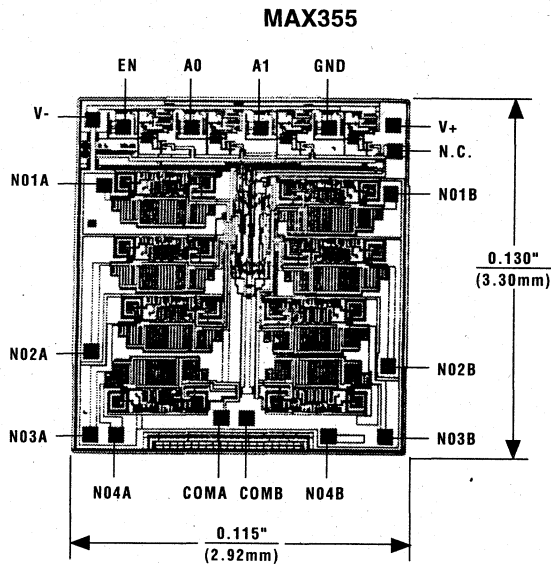
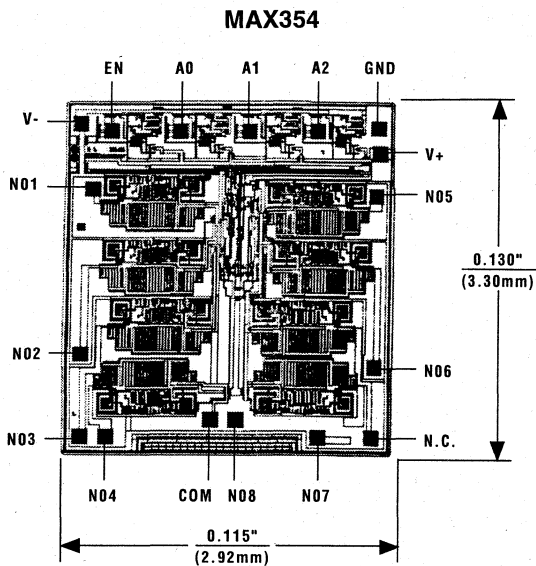


MAX355			
A0	A1	A2	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

LOGIC "0" $V_{AL} \leq +0.8V$, LOGIC "1" $V_{AH} \geq +2.4V$

Fault-Protected Analog Multiplexers

Chip Topographies



TRANSISTOR COUNT: 256
SUBSTRATE CONNECTED TO V+

MAXIM

Signal-Line Circuit Protectors

General Description

The MAX366 and MAX367 are multiple, two-terminal circuit protectors. Placed in series with signal lines, each two-terminal device guards sensitive circuit components against voltages near and beyond the normal supply voltages. These devices are used at interfaces where sensitive circuits are connected to the external world and could encounter damaging voltages (up to 35V beyond the supply rails) during power-up, power-down, or fault conditions.

The MAX366 contains three independent protectors and the MAX367 contains eight. They can protect analog signals using either unipolar (4.5V to 36V) or bipolar ($\pm 2.25V$ to $\pm 18V$) power supplies. Each protector is symmetrical. Input and output terminals may be freely interchanged.

These devices are voltage-sensitive MOSFET transistor arrays that are normally on when power is applied and normally open circuit when power is off. With $\pm 10V$ supplies, on-resistance is 100Ω max and leakage is less than $1nA$ at $+25^\circ C$.

When signal voltages exceed or are within approximately $1.5V$ of either power-supply voltage (including when power is off), the two-terminal resistance increases dramatically, limiting fault current as well as output voltage to sensitive circuits. The protected side of the switch maintains the correct polarity and clamps approximately $1.5V$ below the supply rail. There are no "glitches" or polarity reversals going into or coming out of a fault condition.

Applications

Process Control Systems Redundant/Backup Systems
Hot-Insertion Boards/Systems ATE Equipment
Data-Acquisition Systems Sensitive Instruments

Features

- ◆ $\pm 40V$ Overvoltage Protection
- ◆ Open Signal Paths with Power Off
- ◆ 100Ω Signal Paths with Power On
- ◆ $1nA$ Max Path Leakage at $+25^\circ C$
- ◆ $44V$ Maximum Supply Voltage Rating
- ◆ Automatic Protection; No Programming or Controls

Ordering Information

PART [†]	TEMP. RANGE	PIN-PACKAGE
MAX366CPA	$0^\circ C$ to $+70^\circ C$	8 Plastic DIP
MAX366CSA	$0^\circ C$ to $+70^\circ C$	8 SO
MAX366C/D	$0^\circ C$ to $+70^\circ C$	Dice*
MAX366EPA	$-40^\circ C$ to $+85^\circ C$	8 Plastic DIP
MAX366ESA	$-40^\circ C$ to $+85^\circ C$	8 SO
MAX366MJA	$-55^\circ C$ to $+125^\circ C$	8 Cerdip**
MAX367CPN	$0^\circ C$ to $+70^\circ C$	18 Plastic DIP
MAX367CWN	$0^\circ C$ to $+70^\circ C$	18 Wide SO
MAX367C/D	$0^\circ C$ to $+70^\circ C$	Dice*
MAX367EPN	$-40^\circ C$ to $+85^\circ C$	18 Plastic DIP
MAX367EWN	$-40^\circ C$ to $+85^\circ C$	18 Wide SO
MAX367MJN	$-55^\circ C$ to $+125^\circ C$	18 Cerdip**

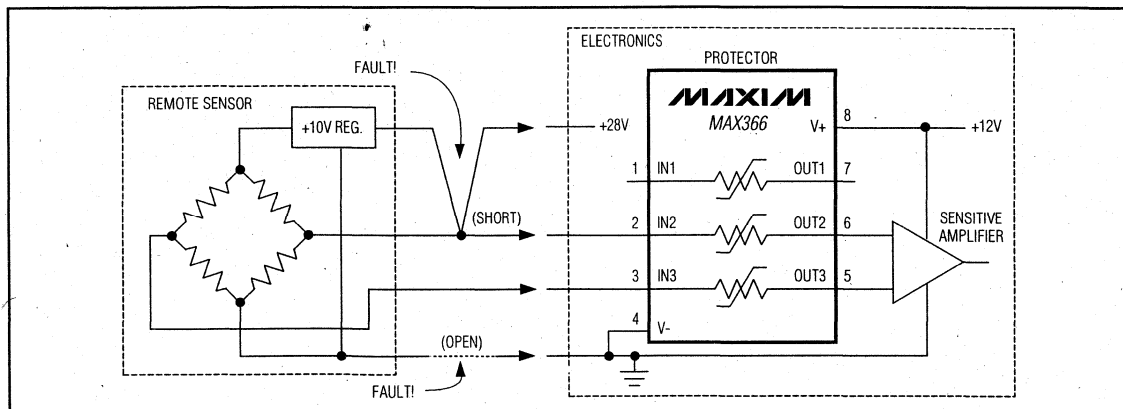
[†] MAX367 available after January 1, 1995.

* Dice are tested at $T_A = +25^\circ C$ only.

** Contact factory for availability.

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



MAXIM

Maxim Integrated Products 1-41

Call toll free 1-800-998-8800 for free samples or literature.

MAX366/MAX367

1

Signal-Line Circuit Protectors

ABSOLUTE MAXIMUM RATINGS

V+ to V- -0.3V, +44V
 IN-, OUT- (V- + 44V), (V+ - 44V)
 Continuous Current into Any Terminal ± 30 mA
 Peak Current into Any Terminal
 (pulsed at 1ms, 10% duty cycle) ± 70 mA
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 8-Pin Plastic DIP (derate 9.09mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 727mW
 8-Pin SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 471mW
 8-Pin Cerdip (derate 8.00mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 640mW

18-Pin Plastic DIP (derate 11.11mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 889mW
 18-Pin Wide SO (derate 9.52mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 762mW
 18-Pin Cerdip (derate 10.53mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 842mW
 Operating Temperature Ranges
 MAX36_C 0°C to $+70^\circ\text{C}$
 MAX36_E -40°C to $+85^\circ\text{C}$
 MAX36_M -55°C to $+125^\circ\text{C}$
 Storage Temperature Range -65°C to $+150^\circ\text{C}$
 Lead Temperature (soldering, 10sec) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +15V, V- = -15V, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP	MAX	UNITS
Analog Signal Range	V _{IN} , V _{OUT}	(Note 1)	All	(V+ - 40)		(V- + 40)	V
Fault-Free Analog Signal Range	V _{IN} , V _{OUT}	V+ = 15V, V- = -15V (Note 2)	All	-11		11	V
Analog-Signal Output Range (Fault)	V _{OUT}	V _{IN} = V+ or V-, 100kΩ < R _{OUT} < 1000MΩ (Note 1)	All	(V- + 3)		(V+ - 1.5)	V
Analog-Signal-Path Resistance	R _(IN-OUT)	V+ = 15V, V- = -15V, V _{IN} = ±10V, I _{OUT} = 1mA	+25°C		62	85	Ω
			C, E			100	
			M			125	
		V+ = 10V, V- = -10V, V _{IN} = ±5V, I _{OUT} = 1mA	+25°C		62	100	
			C, E			125	
			M			150	
		V+ = 5V, V- = -5V, V _{IN} = ±2V, I _{OUT} = 1mA	+25°C		140	350	
			C, E, M			400	
Signal-Path Resistance Match	ΔR _(IN-OUT)	V _{IN} = ±10V, I _{OUT} = 1mA	+25°C			7	Ω
		C, E, M			10		
Signal-Path Leakage (Power Off)	I _{IN(OFF)}	V+ = V- = 0V, V _{IN} = ±35V, V _{OUT} = open circuit	+25°C	-10		10	nA
			C, E, M	-1000		1000	
Signal-Path Leakage (without Fault Condition)	I _{OUT(ON)}	V _{IN} = V _{OUT} = ±10V	+25°C	-1		1	nA
			C, E, M	-100		100	
Signal-Path Leakage (with Fault Condition)	I _{IN(ON)}	V _{IN} = ±25V, V _{OUT} = open circuit	+25°C	-10		10	nA
			C, E, M	-1000		1000	
Signal-Path Leakage (with Overvoltage)	I _{IN(OFF)}	V+ = V- = 0V, V _{OUT} = 0V, V _{IN} = ±35V	+25°C	-10		10	nA
			C, E, M	-1000		1000	
POWER SUPPLY							
Power-Supply Range	V+, V-		+25°C, C, E, M	0		±18	V
Power-Supply Range (without Fault Condition)	V+, V-	R _(IN-OUT) < 1000Ω (Note 2)	+25°C, C, E, M	±2.25		±18	V
Power-Supply Current	I+, I-		+25°C	-1		1	μA
			C, E, M	-10		10	

Note 1: Guaranteed, but not tested.

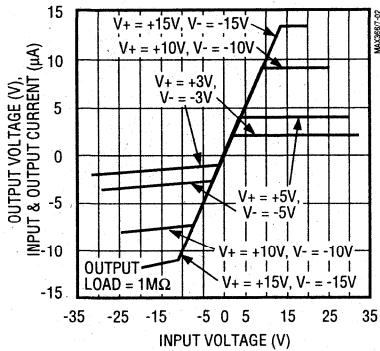
Note 2: See *Typical Operating Characteristics* curves for fault-free analog signal range at various supply voltages.

Signal-Line Circuit Protectors

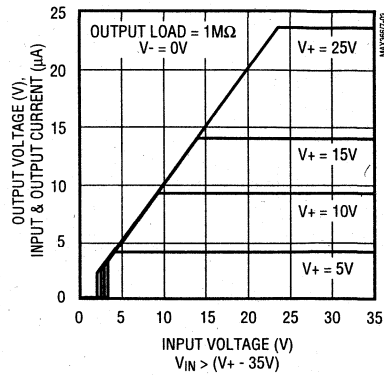
Typical Operating Characteristics

($V_+ = +15V$, $V_- = -15V$, $T_A = +25^\circ C$, unless otherwise noted.)

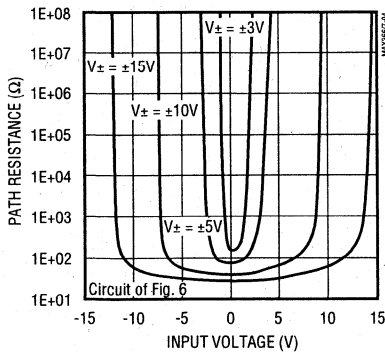
**TRANSFER CHARACTERISTICS
(BIPOLAR SUPPLIES)**



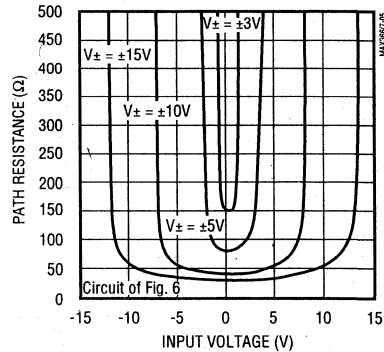
**TRANSFER CHARACTERISTICS
(SINGLE SUPPLY)**



**PATH RESISTANCE vs. INPUT VOLTAGE
(BIPOLAR SUPPLIES)**



**PATH RESISTANCE vs. INPUT VOLTAGE
(BIPOLAR SUPPLIES)**



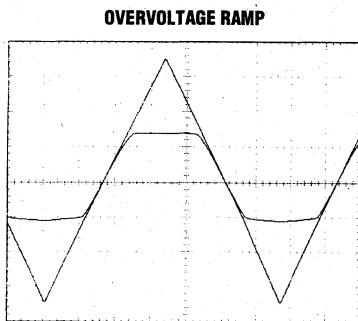
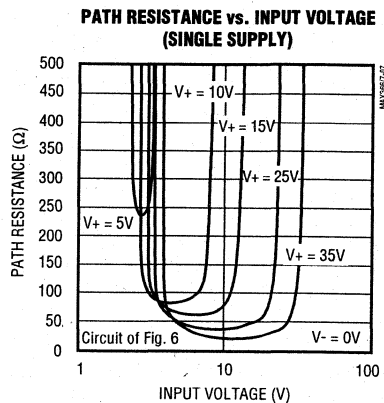
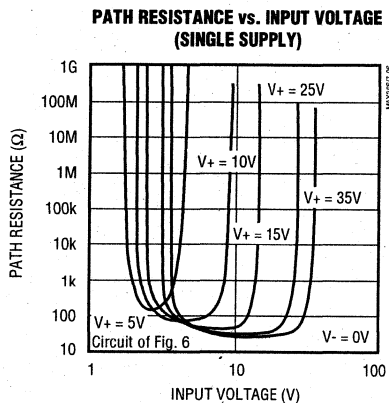
MAX366/MAX367

1

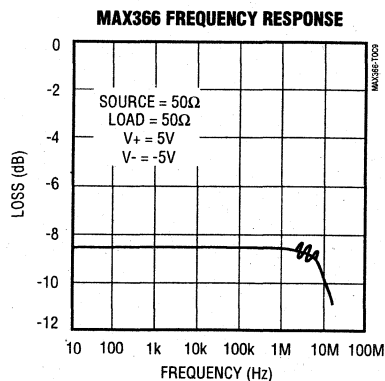
Signal-Line Circuit Protectors

Typical Operating Characteristics (continued)

($V_+ = +15V$, $V_- = -15V$, $T_A = +25^\circ C$, unless otherwise noted.)



$V_+ = 5V$, $V_- = -5V$
 CHAN 1: INPUT OVERVOLTAGE RAMP $\pm 7V$, 2V/div
 CHAN 2: OUTPUT; OUTPUT LOAD = 1000 Ω , 2V/div



Signal-Line Circuit Protectors

Pin Description

PIN		NAME*	FUNCTION
MAX366	MAX367		
1, 2, 3	1, 2, 3	IN1, IN2, IN3	Signal Inputs 1, 2, 3
–	4–8	IN4–IN8	Signal Inputs 4–8
4	9	V–	Negative Supply Voltage Input
–	10–14	OUT8–OUT4	Signal Outputs 4–8
5, 6, 7	15, 16, 17	OUT3, OUT2, OUT1	Signal Outputs 1, 2, 3
8	18	V+	Positive Supply Voltage Input

* Inputs and outputs are names for convenience only; inputs and outputs are identical and interchangeable.

Background Information

When a voltage outside the supply range is applied to most integrated circuits, there is a strong possibility they will be damaged or "latch up" (that is, fail to operate properly even after the offending voltage is removed). If an IC's input or output pin is supplied with a voltage when the IC's power is off, and power is subsequently applied, the device may act as an SCR and destroy itself and/or other circuitry. Such "faults" are commonly encountered in modular control systems where power and signals to interconnected modules may be interrupted and re-established at random. They can happen during production testing, maintenance, start-up, or a power "brownout."

The MAX366/MAX367 are designed to protect delicate input and output circuitry from overvoltage faults up to $\pm 40V$ (with or without power applied), in devices such as op amps, analog-to-digital/digital-to-analog converters, and voltage references. These circuit protectors automatically limit signal voltages and currents to safe levels without degrading normal signal performance, even in very high-impedance circuits. They are powered by the power supply of the protected circuit and inserted into the signal lines. There are no control lines, programming pins, or adjustments.

Unlike shunt diode networks, these devices are low-impedance FETs that become high impedance during a fault condition, so fault current and power dissipation are extremely low. Equally important, leakage current during normal and fault conditions is extremely low. In addition, unlike most discrete networks, these parts protect circuits both when power is off and during power transitions.

Detailed Description

Internal Construction

Figure 1 shows the simplified internal construction of each protector inside the MAX366/MAX367. Each circuit consists of two N-channel FETs and one P-channel FET. All the FETs are enhancement types; that is, the N channels must have approximately 1.3V of positive gate voltage in order to conduct, and the P channel must have approximately 2V of negative gate voltage in order to conduct.

During normal operation, V+ is connected to a positive potential and V– is connected to a negative potential. Since their gates are tied to V+, transistors Q1 and Q3 conduct as long as their sources are at least 1.3V below V+ (the N-channel gate threshold.) Transistor Q2's gate is tied to V–, so it conducts as long as its source is 2V or more above V– (the P-channel gate threshold.)

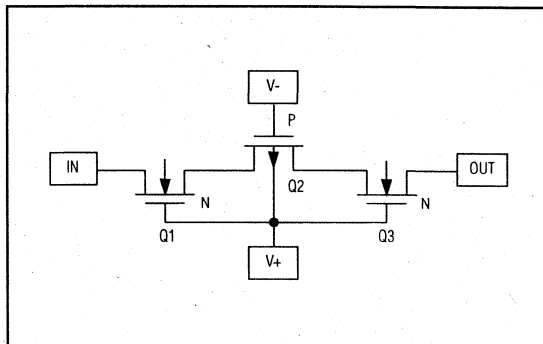


Figure 1. Simplified Internal Structure

MAX366/MAX367

1

Signal-Line Circuit Protectors

As long as the signal is within these limits, all three transistors conduct and a low-resistance path is maintained from the IN to OUT pin. (Note that, since the device is symmetrical, IN and OUT pins can be interchanged.) When the signal is beyond the gate threshold of either Q2 or Q1/Q3, the path resistance rises dramatically. When power is off, none of the transistors have gate bias, so the circuit from IN to OUT is open.

Normal Operation

In normal operation, the protector is placed in series with the signal line and the power supplies are connected to V+ and V- (see Figure 2). V- is ground when operating with a single supply. When power is applied, each protector acts as a resistor in the signal path. Any voltage source on the "input" side of the switch will be conducted through the protector to the output. (Note that, since the protector is symmetrical, IN and OUT pins can be interchanged.)

If the output load is resistive, it will draw current, and a voltage divider will be formed with the internal resistance so the output voltage will be lower than the input voltage. Since the internal resistance is typically less than 100Ω, high-impedance loads will be relatively unaffected by the presence of the protector. The protector's path resistance is a function of the supply voltage and the signal voltage (see *Typical Operating Characteristics*).

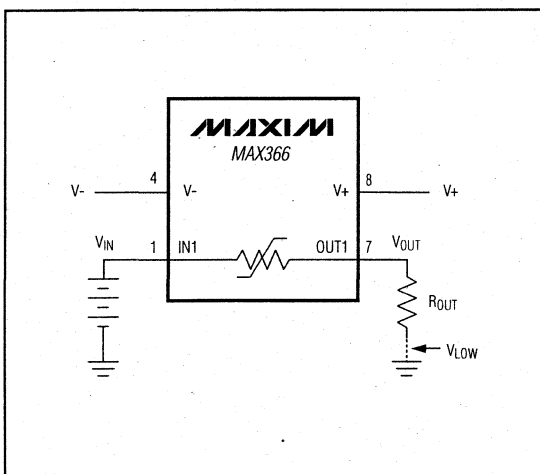


Figure 2. Application Circuit

Power Off

When power is off (i.e., $V+ = V- = 0V$), the protector is a virtual open circuit, and all voltages on each side are isolated from each other up to $\pm 40V$. With $\pm 40V$ applied to the input pin, the output pin will be 0V, regardless of its resistance to ground.

Fault Conditions

A fault condition exists when the voltage on either signal pin is within about 1.5V of either supply rail or exceeds either supply rail. This definition is valid when power is applied and when it is off, as well as during all the states as power ramps up or down.

During a fault, the protector acts as a variable resistor, conducting only enough to sustain the other side of the switch within about 1.5V of the supply rail. This voltage is known as the "fault knee voltage," and is not symmetrical. It is approximately 1.3V down from the positive supply (V+ pin) or approximately 2.0V up from the negative supply (V- pin). Each fault knee voltage varies slightly with supply voltage, with output current, and from device to device.

During a fault condition, all the fault current flows from one signal pin through the protector and out the other signal pin. No fault current flows through either supply pin. (There will be a few pico-amps of leakage current from each signal pin to each supply pin, but this is independent of fault current.)

During the fault condition, enough current will flow to maintain the output voltage at the fault knee voltage, so the fault current is a function of the output resistance and the supply voltage. **The output voltage and current have the same polarity as the fault.**

The maximum input fault voltage is 40V from the "opposite-polarity supply rail." This means the input can go to $\pm 35V$ with $\pm 5V$ supplies or to $\pm 25V$ with $\pm 15V$ supplies. The fault voltage is highest ($\pm 40V$) when the supplies are off ($V+ = V- = 0V$).

Using the circuit of Figure 2, the approximate fault currents are as follows:

- 1) For positive faults:

$$I(F) \approx (V+ - 1.3V - V_{LOW}) \div R_{OUT}$$

- 2) For negative faults:

$$I(F) \approx (V- + 2V + V_{LOW}) \div R_{OUT}$$

where V_{LOW} is the terminating voltage at the far end of R_{OUT} . $V_{LOW} = 0V$ when R_{OUT} is grounded.

Signal-Line Circuit Protectors

MAX366/MAX367

1

The current through each protector should never exceed 30mA. Always calculate the power dissipated by all the protectors in worst-case conditions (maximum voltage and current through each protector) to ensure the package dissipation limit is not reached.

With single-supply operation, grounded loads will have zero voltage (and current) whenever the input voltage is below approximately 2V. In effect, both the IN and OUT pins are in fault condition.

A special case arises when power is off: The part is in a perpetual fault condition but no fault current flows because all the internal FETs are off.

Single-Supply Output Operation

Single-supply operation is a special case. Signals cannot go to ground, since from 0V to approximately +2V is a fault condition.

Extremely Low-Current Operation

Figure 3 shows the typical high-impedance transfer characteristics with a 100M Ω load. Compared to the transfer characteristic at 1M Ω (see *Typical Operating Characteristics*), the two knees are closer to the supply voltages and the slopes of the flat portions of the curve (fault conditions) are steeper. As the load resistance is increased even further, the positive and negative knees increase, and the slopes in fault conditions increase even more. Eventually, at some extremely high output resistance (e.g., Tera ohms), the output voltage can exceed the supply voltage during fault conditions. This is due to extremely low leakage currents from the input to output.

When the protector's output side is connected to very high-resistance, very low-current loads (such as op-amp inputs), a small leakage current flows from the input to the output during fault conditions. This current is typically below a nano-ampere ($<10^{-9}$ A) but, if the output resistance is high enough, it can cause the output voltage to exceed the supply voltages during fault conditions.

This condition can be self-correcting, however, if the high-resistance load has protection diodes to the supply rails (either external or internal to the op amp). These diodes conduct the leakage current to the supply rails and safely limit the output voltage. An alternative is to add a high-value resistor to ground in parallel with the load. This resistor may be as low as 1000M Ω ; its value must be determined experimentally at the highest anticipated operational temperature.

The fault protectors will not normally be used with high-impedance FET-input amplifiers that lack input protection diodes. Such amplifiers are fragile and are normally

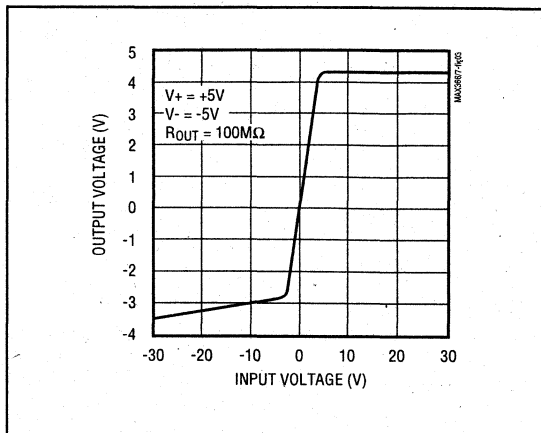


Figure 3. High-Impedance Transfer Characteristic

reserved for use when ultra-low leakage (pA) is needed. The MAX366/MAX367 have nano-amperes of leakage, which would negate the low leakage of the unprotected amplifier.

Low-Voltage Operation

The MAX366/MAX367 "operate" with supply voltages all the way down to 0V, but what they do to the signal is not obvious. With a total supply voltage of 3.5V, the protector is in a fault condition with nearly any input that is not close to 2.0V. Below 3.5V (including power off), the protector is perpetually in a fault condition (i.e., high impedance).

When the supply voltage(s) ramps up (and/or down) from zero, the signal path is initially in a fault condition (open), until the supply voltage passes the input voltage. The output starts at zero and is delayed from reaching the input voltage as the part comes out of the fault condition. If the supply voltage exceeds about 3.5V, but never exceeds the input voltage, the output will follow the supply, always remaining about 1.3V below the positive supply voltage or 2V above the negative supply voltage. If the input voltage subsequently comes out of the fault condition, the output returns to the input value. This set of conditions is exactly reversed when power ramps down to zero.

Since the input and output pins are identical and interchangeable, predicting whether or not the part is in a fault condition is easy: If either IN or OUT exceeds V+ or V-, a fault condition exists and the current that flows will be just enough to cause the other signal pin (OUT or IN) to approach the appropriate supply rail.

Signal-Line Circuit Protectors

Bipolar Faults

The MAX366/MAX367 V+ and V- pins are normally connected to a circuit's most positive and most negative power supplies. When a circuit has multiple power supplies (such as $\pm 5V$ and $\pm 12V$) and the MAX366/MAX367 V+ and V- pins are connected to the lower supply, it is possible to have fault conditions on both sides of the signal path at once, if both sides of the switch have paths to higher voltages. If the polarity of these faults is the same, the signal path will be open and there is no conflict.

If the IN and OUT pins are driven in opposite polarities from low-impedance sources, the lower of the two impedances will overcome the higher impedance, just as if the protector were not present. (Make sure the current does not exceed the 30mA absolute maximum rating.) As the lower impedance source approaches and exceeds the fault knee voltage, the protector will conduct enough current to maintain the other signal pin near the fault knee voltage. This means when the fault knee voltage is reached, the current through the protector shifts from the higher current capability of the lower impedance source to the lower current capability of the higher impedance source.

Typical Applications

Driven Switches

The MAX366/MAX367 have low supply currents ($<1\mu A$), which allows the supply pins to be driven directly by other active circuitry, instead of connected directly to the power sources. In this configuration, the parts can be used as driven fault-protected switches with V+ or V- pins used as the control pins. For example, if the V- pin is grounded, you can turn the V+ pin on and off by driving it with the output of a CMOS gate. This effectively connects and disconnects three or eight separate signal lines at once. (If bipolar signals or signals that go to ground are being switched, the V- pin must be driven simultaneously to a negative potential.) Always ensure that the driving source(s) does not drive the V+ pin more negative than the V- pin.

Figure 4 shows a simple turn-on delay that takes advantage of the MAX366's low power consumption. The two RC networks cause gradual application of power to the MAX366, which in turn applies the input signals smoothly after the amplifier has stabilized. The two diodes discharge the two capacitors rapidly when power is turned off.

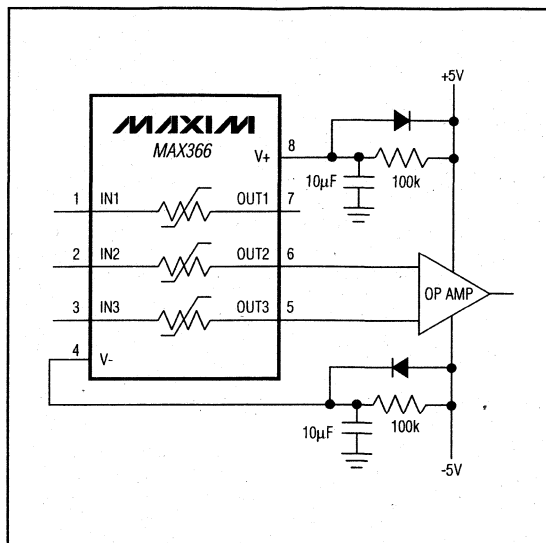


Figure 4. Turn-On Delay

This circuit can be tailored to nearly any rate of turn-on by selecting the RC time constants in the V+ and V- pins, without affecting the time constant of the measuring circuit.

Protectors as Circuit Elements

Any of the individual protectors in a MAX366 or MAX367 may be used as a switched resistor, independent of the functions of other elements in the same package. For example, Figure 5 shows a MAX366 with two of the protectors used to protect the input of an op amp, and the third element used to sequence a power supply. Combining the circuits of Figures 4 and 5 produces a delayed action on the switched +5V, as well as smooth application of signals to the amplifier input.

Testing Circuit Protectors

Measuring Path Resistance

Measuring path resistance requires special techniques, since path resistance varies dramatically with the IN and OUT voltages relative to the supply voltages. Conventional ohmmeters should not be used, for two reasons: 1) the applied voltage and currents are usually not predictable, and 2) the true resistance is a function of the applied voltage, which is dramatically altered by the ohmmeter itself. Autoranging ohmmeters are particularly unreliable.

Signal-Line Circuit Protectors

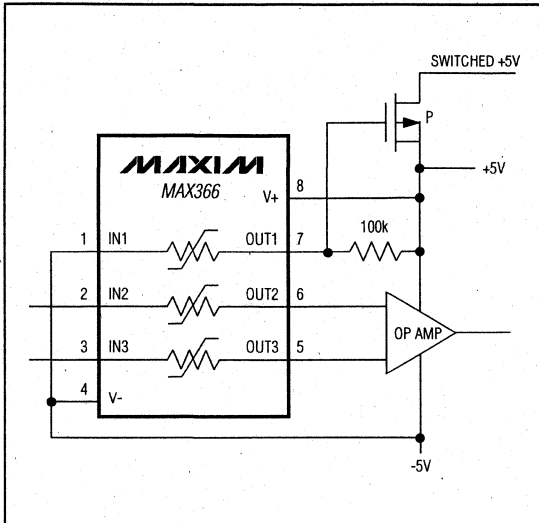


Figure 5. Power-Supply Sequencing

Figure 6 shows a circuit that can give reliable results. This circuit uses a 100mV voltage source and a low-voltage-drop ammeter as the measuring circuit, and an adjustable supply to sweep the analog voltage across its whole range. The ammeter must have a voltage drop of less than one millivolt (at any current) for accurate results. (A Keithley Model 617 Electrometer has a suitable ammeter circuit, appropriate ranges, and a built-in voltage source designed for this type of measurement.) Measurements are made by setting the analog voltage, measuring the current, and calculating the path resistance. The procedure is repeated at each analog voltage and supply voltage.

It is important to use a voltage source of 100mV or less. As shown in Figure 4, this voltage is added to the V_{IN} voltage to form the V_{OUT} voltage. Using a higher voltage could cause the OUT pin to go into a fault condition prematurely.

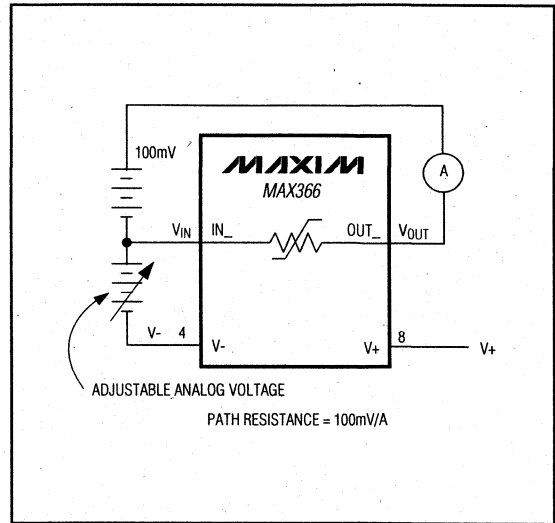


Figure 6. Path-Resistance Measuring Circuit

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to several megahertz (see *Typical Operating Characteristics*). Above 5MHz, the response has several minor peaks, which are highly layout dependent. Because the path resistance is dependent on the supply voltage and signal amplitude, the impedance is not controlled. Adjacent channel attenuation up to 5MHz is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Pulse response is reasonable, but because the impedance changes rapidly, fast rise times may induce ringing as the signal approaches the fault voltage. At very high amplitudes (such as noise spikes), the capacitive coupling across the signal pins will transfer considerable energy, despite the fact that the DC path is a virtual open circuit.

Signal-Line Circuit Protectors

High-Voltage Surge Suppression

These devices are not high-voltage arresters, nor are they substitutes for surge suppressors. In systems that use these forms of protection, however, the MAX366/MAX367 can fill a vital gap. Figure 7 shows a typical circuit. Although the surge suppressors are extremely fast shunt elements, they have very soft current knees. Their clamp voltage must be chosen well above the normal signal levels, because they have excessive leakage currents as the knee is approached. This current can interfere with normal operation when signal levels are low or impedances are high. If the clamp voltage is too high, however, the input can be damaged.

Using a MAX366/MAX367 after the surge suppresser allows the surge-suppressor voltage to be set above the supply voltage (but within the overvoltage limits), dramatically reducing the effects of leakage (Figure 7). During a surge, the surge suppresser clamps the input voltage to roughly $\pm 10V$. This protects the MAX366/MAX367, but the MAX366/MAX367 still disconnect the signal from the op amp well within the $\pm 5V$ supply.

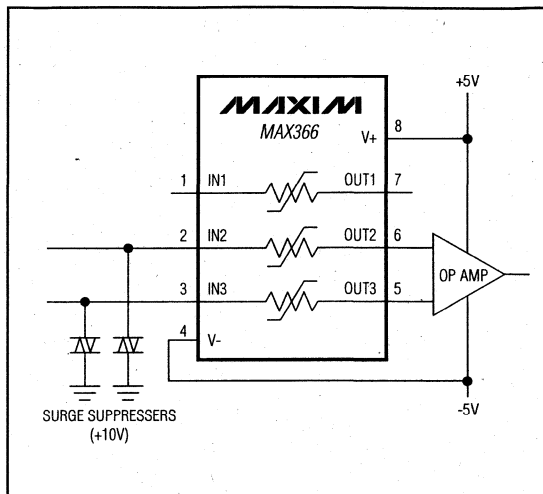
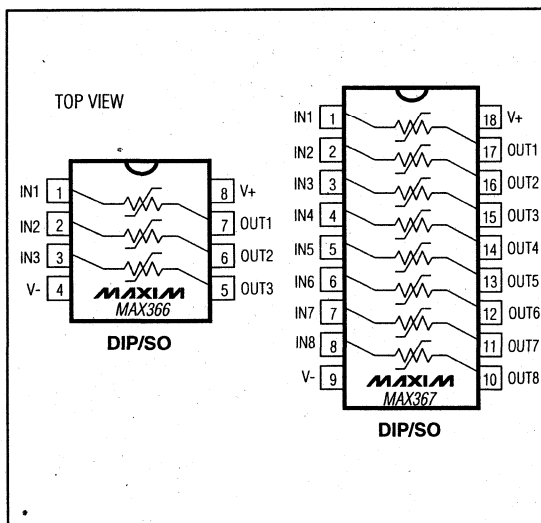
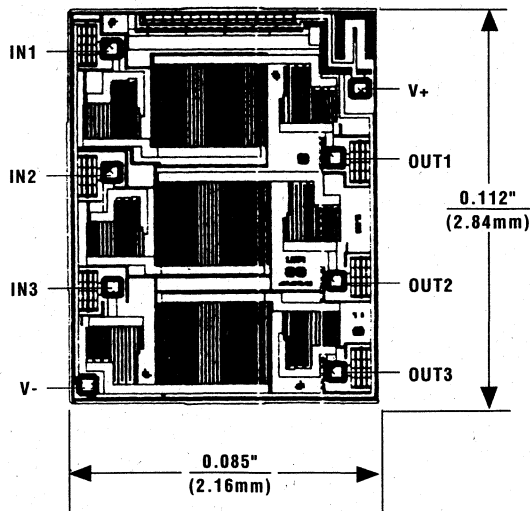


Figure 7. Surge-Suppression Circuit

Pin Configurations



Chip Topography



TRANSISTOR COUNT: 21

SUBSTRATE CONNECTED TO V+



Precision, Low-Voltage Analog Switches

General Description

The MAX381/MAX383/MAX385 are precision, low-voltage analog switches. The single-pole single-throw MAX381 and double-pole single-throw MAX385 dual switches are normally open. The single-pole double-throw MAX383 has two normally open and two normally closed poles. All three parts offer low on-resistance (less than 35Ω), guaranteed to match to within 2Ω between channels and to remain flat over the specified analog signal range (4Ω max). They also offer low leakage (less than 250pA at $+25^\circ\text{C}$ and less than 2.5nA at $+85^\circ\text{C}$) and fast switching (turn-on time less than 175ns and turn-off time less than 100ns).

The MAX381/MAX383/MAX385 are fabricated with Maxim's low-voltage silicon-gate process for high system accuracy. Design improvements guarantee extremely low charge injection ($<5\text{pC}$) and low power consumption ($<10\mu\text{W}$).

These monolithic switches operate with a single positive supply ($+3\text{V}$ to $+15\text{V}$) or with split supplies ($\pm 3\text{V}$ to $\pm 8\text{V}$) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits	Military Radios
Test Equipment	Communication Systems
Heads-Up Displays	Battery-Operated Systems
Audio Signal Routing	PBX, PABX
Guidance and Control Systems	

Features

- ◆ Single-Supply Operation ($+3\text{V}$ to $+15\text{V}$)
Bipolar-Supply Operation ($\pm 3\text{V}$ to $\pm 8\text{V}$)
- ◆ Pin-Compatible with DG401/DG403/DG405
- ◆ Low On-Resistance, 20Ω Typical (35Ω Max)
- ◆ Guaranteed Matched On-Resistance Between Channels, $<2\Omega$
- ◆ Guaranteed Flat On-Resistance over Specified Analog Signal Range, $<4\Omega$
- ◆ Guaranteed Charge Injection, $<5\text{pC}$
- ◆ Guaranteed Off-Channel Leakage, $<2.5\text{nA}$ at $+85^\circ\text{C}$
- ◆ TTL/CMOS-Logic Compatible with 3V , 5V , $\pm 3\text{V}$, and $\pm 5\text{V}$ Supplies
- ◆ Rail-to-Rail Analog Signal Handling Capability

Ordering Information

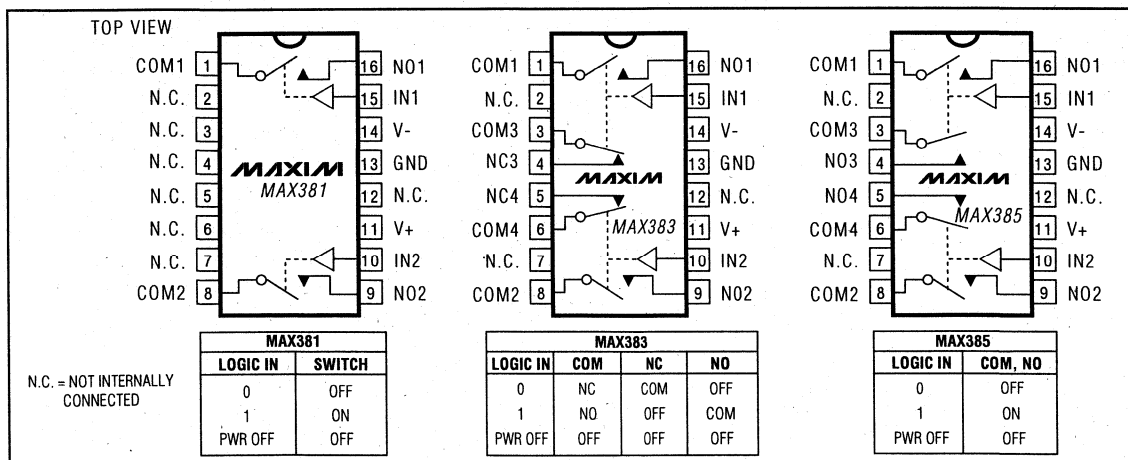
PART	TEMP. RANGE	PIN-PACKAGE
MAX381CPE	0°C to $+70^\circ\text{C}$	16 Plastic DIP
MAX381CSE	0°C to $+70^\circ\text{C}$	16 Narrow SO
MAX381C/D	0°C to $+70^\circ\text{C}$	Dice*
MAX381EPE	-40°C to $+85^\circ\text{C}$	16 Plastic DIP
MAX381ESE	-40°C to $+85^\circ\text{C}$	16 Narrow SO
MAX381EJE	-40°C to $+85^\circ\text{C}$	16 CERDIP**
MAX381MJE	-55°C to $+125^\circ\text{C}$	16 CERDIP**

Ordering Information continued on last page.

* Dice are tested at $T_A = +25^\circ\text{C}$ only.

** Contact factory for package availability.

Pin Configurations/Block Diagrams/Truth Tables



Precision, Low-Voltage Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND

V+	-0.3V to +17V
V-	+0.3V to -17V
V+ to V-	-0.3V to +17V
COM, NO, NC, IN	(V- - 2V) to (V+ + 2V) or 30mA, whichever occurs first

Continuous Current, any pin30mA

Peak Current, any pin
(pulsed at 1ms, 10% duty cycle max)100mA

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 10.53mW/°C above +70°C)842mW

Narrow SO (derate 8.70mW/°C above +70°C)696mW

CERDIP (derate 10.00mW/°C above +70°C)800mW

Operating Temperature Ranges

MAX38_C_E0°C to +70°C

MAX38_E_E-40°C to +85°C

MAX38_MJE-55°C to +125°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}	(Note 3)		V-		V+	V
On-Resistance	R _{ON}	V+ = 4.5V, V- = -4.5V, V _{NC} or V _{NO} = ±3.5V, I _{COM} = -10mA, V _{INH} = 2.4V, V _{INL} = 0.8V	T _A = +25°C	C, E	20	35	Ω
			T _A = T _{MIN} to T _{MAX}	M	20	30	
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V _{NC} or V _{NO} = ±3V, I _{COM} = -10mA, V+ = 5V, V- = -5V	T _A = +25°C	C, E, M	0.5	2	Ω
			T _A = T _{MIN} to T _{MAX}	C, E, M		4	
On-Resistance Flatness (Note 4)	R _{FLAT(ON)}	V _{NC} or V _{NO} = 3V, 0V, -3V; I _{COM} = -10mA, V+ = 5V; V- = -5V	T _A = +25°C	C, E, M		4	Ω
			T _A = T _{MIN} to T _{MAX}	C, E, M		6	
NC or NO Off Leakage Current (Note 5)	I _{NC(OFF)} or I _{NO(OFF)}	V _{COM} = ±4.5V, V _{NC} or V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	T _A = +25°C	C, E	-0.2	-0.01	nA
				M	-0.1	-0.01	
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5	2.5	
				M	-5.0	5.0	
COM Off Leakage Current (Note 5)	I _{COM(OFF)}	V _{COM} = ±4.5V, V _{NC} or V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	T _A = +25°C	C, E	-0.2	-0.01	nA
				M	-0.1	-0.01	
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5	2.5	
				M	-5.0	5.0	
COM On Leakage Current (Note 5)	I _{COM(ON)}	V _{COM} = ±4.5V, V _{NC} or V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	T _A = +25°C	C, E	-0.4	-0.04	nA
				M	-0.2	-0.04	
			T _A = T _{MIN} to T _{MAX}	C, E	-5.0	5.0	
				M	-20.0	20.0	

Precision, Low-Voltage Analog Switches

MAX381/MAX383/MAX385

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V		-1.0	0.005	1.0	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V		-1.0	0.005	1.0	μA
Logic High Input Voltage	V _{AH}		T _A = T _{MIN} to T _{MAX}	2.4			V
Logic Low Input Voltage	V _{AL}		T _A = T _{MIN} to T _{MAX}			0.8	V
DYNAMIC							
Turn-On Time	t _{ON}	V _{COM} = 3V, Figure 2	T _A = +25°C	100	175	ns	
			T _A = T _{MIN} to T _{MAX}		225		
Turn-Off Time	t _{OFF}	V _{COM} = 3V, Figure 2	T _A = +25°C	60	100	ns	
			T _A = T _{MIN} to T _{MAX}		150		
Break-Before-Make Time Delay (Note 3)	t _D	MAX383 only, Figure 3	T _A = +25°C	10	20	ns	
Charge Injection (Note 3)	V _{CTE}	C _L ≥ 1.0nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 4	T _A = +25°C		2	5	pC
Off Isolation (Note 6)	V _{ISO}	R _L = 100Ω, C _L = 5pF, f = 1MHz, Figure 5	T _A = +25°C		72		dB
Crosstalk (Note 7)	V _{CT}	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 6	T _A = +25°C		90		dB
Off Capacitance	C _{OFF}	f = 1MHz, Figure 7	T _A = +25°C		12		pF
COM Off Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 7	T _A = +25°C		12		pF
Channel On Capacitance	C _{COM(ON)}	f = 1MHz, Figure 8	T _A = +25°C		39		pF
SUPPLY							
Power-Supply Range				±3		±8	V
Positive Supply Current	I ₊	All channels on or off, V ₊ = 5.5V, V ₋ = -5.5V, V _{IN} = 0V or V ₊		-1.0	0.06	1.0	μA
Negative Supply Current	I ₋	All channels on or off, V ₊ = 5.5V, V ₋ = -5.5V, V _{IN} = 0V or V ₊		-1.0	-0.01	1.0	μA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON(max)} - \Delta R_{ON(min)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 5: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temperature.

Note 6: See Figure 4. Off isolation = $20 \log_{10} V_{COM}/V_{NC}$ or V_{NO} . VCOM = output, VNC or NO = input to off switch.

Note 7: Between any two switches. See Figure 5.

Note 8: Leakage testing at single supply is guaranteed by testing with dual supplies.

Precision, Low-Voltage Analog Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V- = 0V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP. RANGE	MIN TYP (Note 2) MAX			UNITS
SWITCH								
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}	(Note 3)			0V V+			V
On-Resistance	R _{ON}	V ₊ = 5.0V, V ₋ = 0V, V _{NC} or V _{NO} = 3.5V, I _{COM} = 1.0mA, V _{INH} = 2.4V, V _{INL} = 0.8V	T _A = +25°C	C, E	25	65	Ω	
				M		60		
			T _A = T _{MIN} to T _{MAX}	C, E, M		75		
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V _{NC} or V _{NO} = 3V, I _{COM} = 1.0mA, V ₊ = 5V	T _A = +25°C	C, E, M	0.5	2	Ω	
			T _A = T _{MIN} to T _{MAX}	C, E, M		4		
On-Resistance Flatness (Note 4)	R _{FLAT(ON)}	V _{NC} or V _{NO} = 3V, 2V, 1V; I _{COM} = 1.0mA; V ₊ = 5V; V ₋ = 0V	T _A = +25°C	C, E, M		6	Ω	
			T _A = T _{MIN} to T _{MAX}	C, E, M		8		
NC or NO Off Leakage Current (Note 8)	I _{NC(OFF)} or I _{NO(OFF)}	V _{COM} = 0V, V _{NC} or V _{NO} = 4.5V, V ₊ = 5.5V, V ₋ = 0V	T _A = +25°C	C, E	-0.2	-0.01	nA	
				M	-0.1	-0.01		0.1
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5			2.5
				M	-5.0			5.0
COM Off Leakage Current (Note 8)	I _{COM(OFF)}	V _{COM} = 4.5V, V _{NC} or V _{NO} = 0V, V ₊ = 5.5V, V ₋ = 0V	T _A = +25°C	C, E	-0.2	-0.01	nA	
				M	-0.1	-0.01		0.1
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5			2.5
				M	-5.0			5.0
COM On Leakage Current (Note 8)	I _{COM(ON)}	V _{COM} = 4.5V, V _{NC} or V _{NO} = 4.5V, V ₊ = 5.5V, V ₋ = 0V	T _A = +25°C	C, E	-0.4	-0.04	nA	
				M	-0.2	-0.04		0.2
			T _A = T _{MIN} to T _{MAX}	C, E	-5.0			5.0
				M	-20.0			20.0
DIGITAL LOGIC INPUT								
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V			-1.0	0.005	1.0	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V			-1.0	0.005	1.0	μA

Precision, Low-Voltage Analog Switches

MAX381/MAX383/MAX385

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC							
Turn-On Time	tON	VCOM = 3V, Figure 2	TA = +25°C	160	250	ns	
			TA = TMIN to TMAX	300			
Turn-Off Time	tOFF	VCOM = 3V, Figure 2	TA = +25°C	60	125	ns	
			TA = TMIN to TMAX	175			
Break-Before-Make Time Delay (Note 3)	tD	MAX383 only	TA = +25°C	10	20	ns	
Charge Injection (Note 3)	VCTE	CL = 1.0nF, VGEN = 0V, RGEN = 0Ω	TA = +25°C	2	5	pC	
SUPPLY							
Power-Supply Range	V+			2.7	16	V	
Positive Supply Current	I+	All channels on or off, VIN = 0V or V+, V+ = 5.5V, V- = 0V		-1.0	0.01	1.0	μA
Negative Supply Current	I-	All channels on or off, VIN = 0V or V+, V+ = 5.5V, V- = 0V		-1.0	-0.01	1.0	μA

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = 3.0V to 3.6V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	VCOM, VNO, VNC	(Note 3)		0V		V+	V
On-Resistance	RON	V+ = 3V, V- = 0V, VNC or VNO = 1.5V, ICOM = 1.0mA, VINH = 2.4V, VINL = 0.8V	TA = +25°C	C, E	75	185	Ω
				M		175	
			TA = TMIN to TMAX	C, E, M		250	
NC or NO Off Leakage Current (Note 8)	INC(OFF) or INO(OFF)	VCOM = 0V, VNC or VNO = 3V, V+ = 3.6V, V- = 0V	TA = +25°C	C, E	-0.2	-0.01	0.2
				M	-0.1	-0.01	0.1
			TA = TMIN to TMAX	C, E	-2.5		2.5
				M	-5.0		5.0
COM Off Leakage Current (Note 8)	ICOM(OFF)	VCOM = 3V, VNC or VNO = 0V, V+ = 3.6V, V- = 0V	TA = +25°C	C, E	-0.2	-0.01	0.2
				M	-0.1	-0.01	0.1
			TA = TMIN to TMAX	C, E	-2.5		2.5
				M	-5.0		5.0
COM On Leakage Current (Note 8)	ICOM(ON)	VCOM = 3V, VNC or VNO = 3V, V+ = 3.6V, V- = 0V	TA = +25°C	C, E	-0.4	-0.04	0.4
				M	-0.2	-0.04	0.2
			TA = TMIN to TMAX	C, E	-5.0		5.0
				M	-20.0		20.0

Precision, Low-Voltage Analog Switches

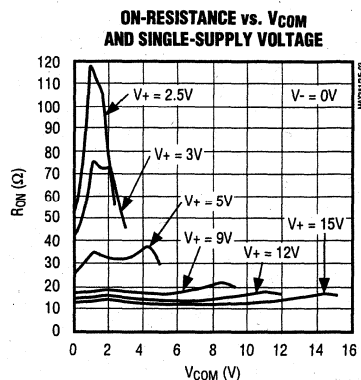
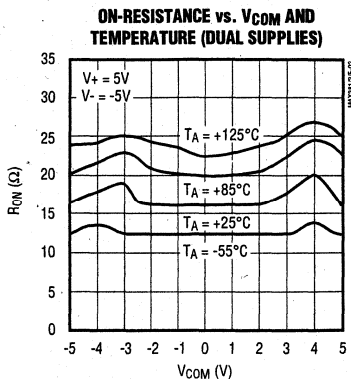
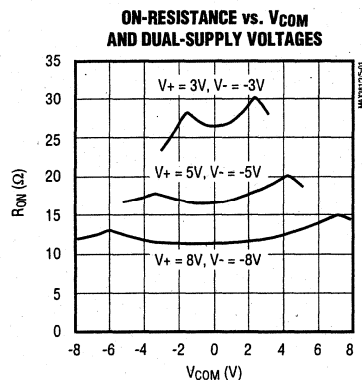
ELECTRICAL CHARACTERISTICS—Single +3.3V Supply (continued)

($V_+ = 3.0\text{V}$ to 3.6V , $GND = 0\text{V}$, $V_{INH} = 2.4\text{V}$, $V_{INL} = 0.8\text{V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT						
Input Current with Input Voltage High	I_{INH}	$V_{IN} = 2.4\text{V}$, all others = 0.8V	-1.0	0.005	1.0	μA
Input Current with Input Voltage Low	I_{INL}	$V_{IN} = 0.8\text{V}$, all others = 2.4V	-1.0	0.005	1.0	μA
DYNAMIC						
Turn-On Time (Note 3)	t_{ON}	$V_{COM} = 1.5\text{V}$, Figure 2 $T_A = +25^\circ\text{C}$			400	ns
Turn-Off Time (Note 3)	t_{OFF}	$V_{COM} = 1.5\text{V}$, Figure 2 $T_A = +25^\circ\text{C}$			150	ns
Break-Before-Make Time Delay (Note 3)	t_D	MAX383 only $T_A = +25^\circ\text{C}$	10	20		ns
Charge Injection (Note 3)	V_{CTE}	$C_L = 1.0\text{nF}$, $V_{GEN} = 0\text{V}$, $R_{GEN} = 0\Omega$ $T_A = +25^\circ\text{C}$		1	5	pC
SUPPLY						
Power-Supply Range	V_+		2.7		16	V
Positive Supply Current	I_+	All channels on or off, $V_{IN} = 0\text{V}$ or V_+ , $V_+ = 3.6\text{V}$, $V_- = 0\text{V}$	-1.0	0.01	1.0	μA
Negative Supply Current	I_-	All channels on or off, $V_{IN} = 0\text{V}$ or V_+ , $V_+ = 3.6\text{V}$, $V_- = 0\text{V}$	-1.0	-0.01	1.0	μA

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

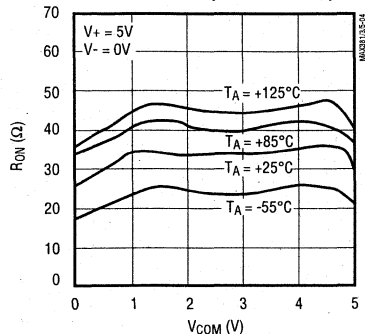


Precision, Low-Voltage Analog Switches

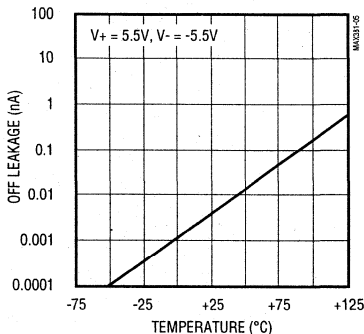
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

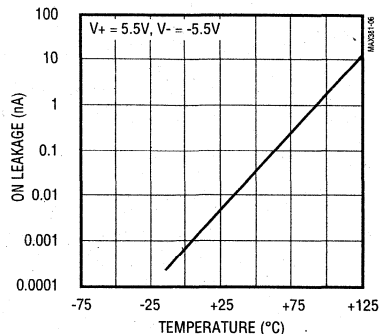
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



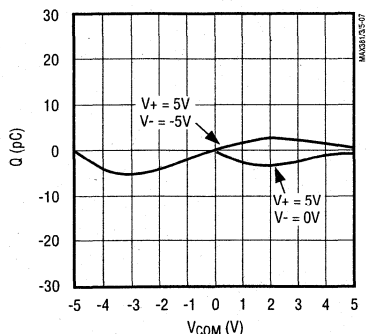
OFF LEAKAGE CURRENT vs. TEMPERATURE



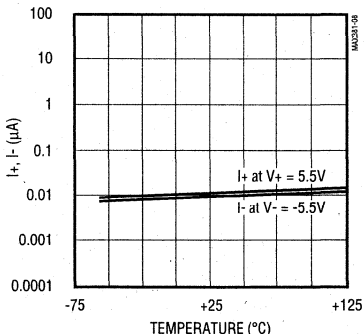
ON LEAKAGE CURRENT vs. TEMPERATURE



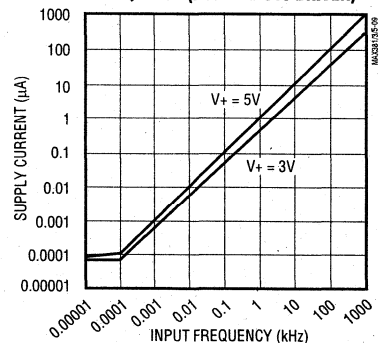
CHARGE INJECTION vs. V_{COM}



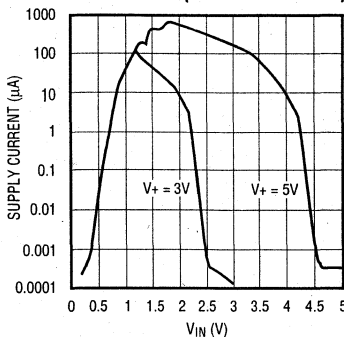
SUPPLY CURRENT vs. TEMPERATURE



MAX383 SUPPLY CURRENT vs. LOGIC INPUT FREQUENCY (BOTH INPUTS DRIVEN)



MAX383 SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE (BOTH INPUTS DRIVEN)



Precision, Low-Voltage Analog Switches

Pin Description

PIN			NAME	FUNCTION
MAX381	MAX383	MAX385		
1, 8	1, 3, 6, 8	1, 3, 6, 8	COM_	Analog Switch Common Terminal
2-7, 12	2, 7, 12	2, 7, 12	N.C.	Not Internally Connected
9, 16	9, 16	4, 5, 9, 16	NO_	Analog Switch Normally Open Terminal
—	4, 5	—	NC_	Analog Switch Normally Closed Terminal
10, 15	10, 15	10, 15	IN_*	Logic Level Input (Normally Low)
11	11	11	V+	Analog Signal and Logic Positive Supply Input
13	13	13	GND	Logic Negative Supply Input (Ground)
14	14	14	V-	Analog Signal Negative Supply Input

* IN1 controls COM1 and COM3; IN2 controls COM2 and COM4.

Applications Information

Operation with Supply Voltages Other than $\pm 5V$

The MAX381/MAX383/MAX385 switches operate with $\pm 3.0V$ to $\pm 8V$ bipolar supplies and a $+3V$ to $+15V$ single supply. In either case, analog signals ranging from $V+$ to $V-$ can be switched. The *Typical Operating Characteristics* graphs show the typical on-resistance variation with analog signal and supply voltage. The usual on-resistance temperature coefficient is $0.5\%/^{\circ}C$ (typ).

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence $V+$ on first, then $V-$, followed by the logic inputs, NO, or COM. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to one diode drop below $V+$ and one diode drop above $V-$, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between $V+$ and $V-$ should not exceed $17V$. These protection diodes are not recommended when using a single $3V$ supply.

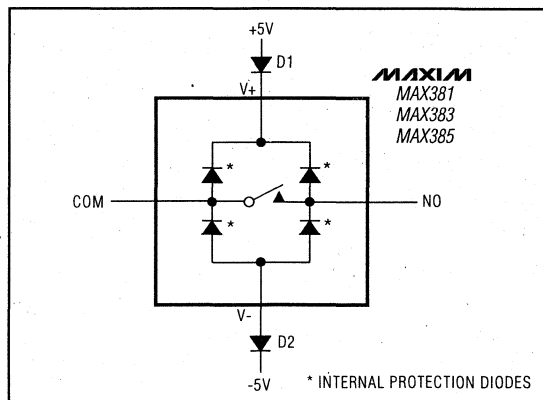


Figure 1. Overvoltage Protection Using Two External Blocking Diodes.

Precision, Low-Voltage Analog Switches

Test Circuits/Timing Diagrams

MAX381/MAX383/MAX385

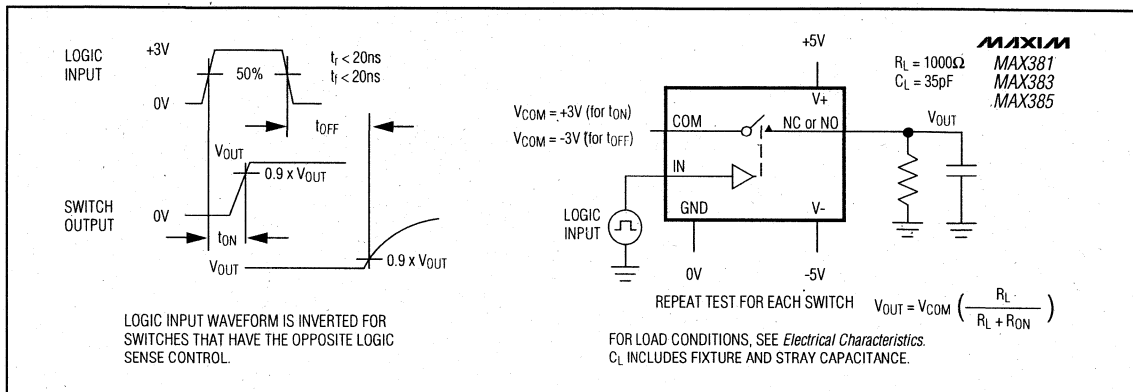


Figure 2. Switching-Time Test Circuit

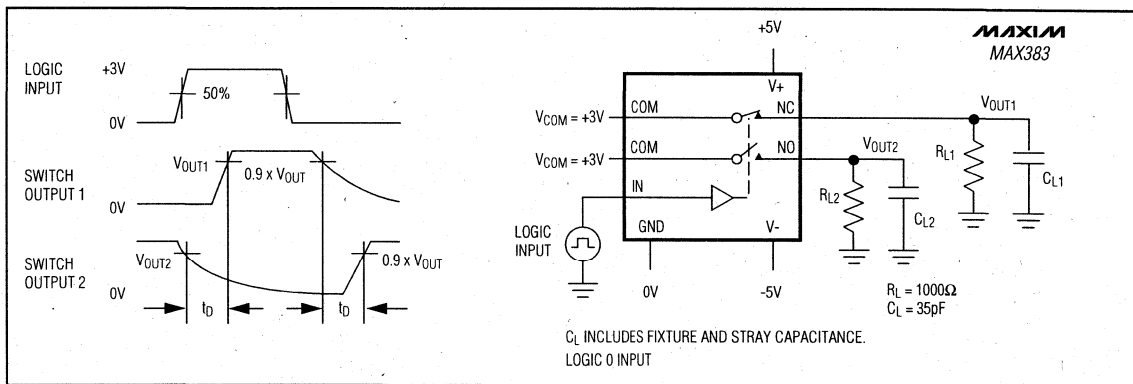


Figure 3. Break-Before-Make Test Circuit (MAX383 only)

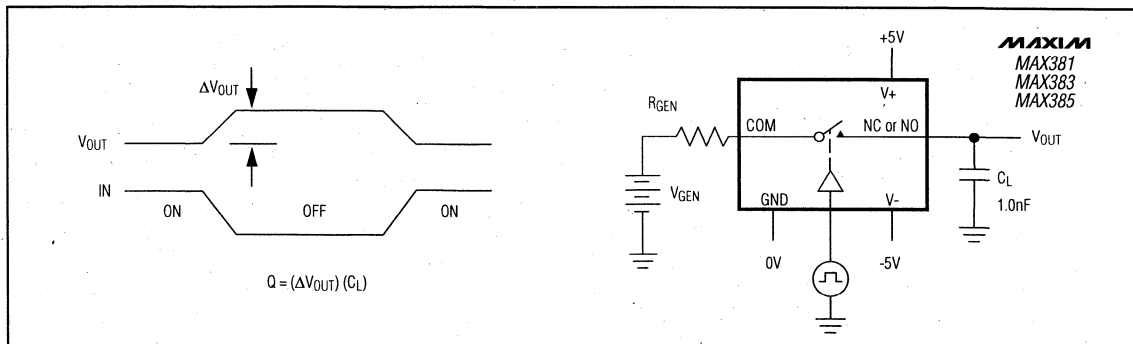


Figure 4. Charge-Injection Test Circuit

Precision, Low-Voltage Analog Switches

Test Circuits/Timing Diagrams (continued)

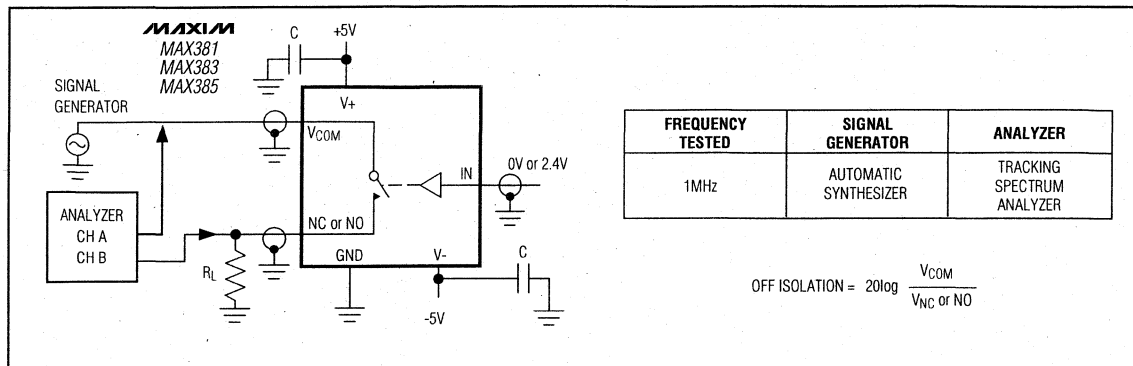


Figure 5. Off Isolation

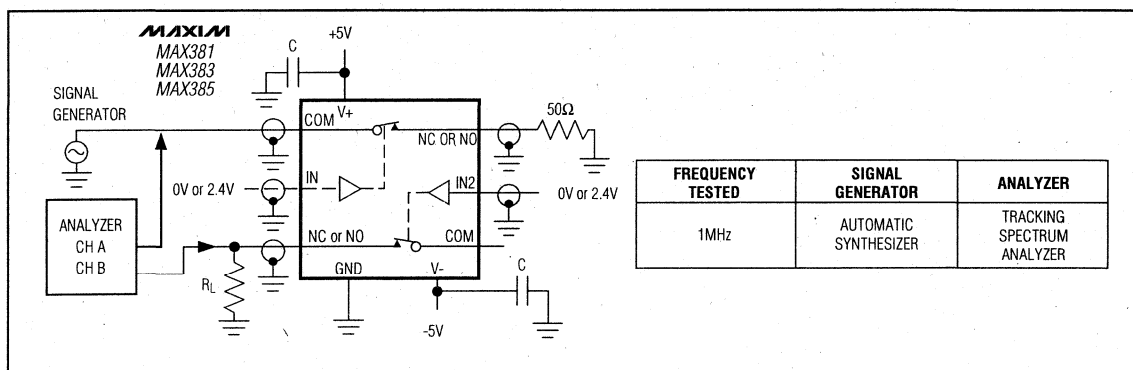


Figure 6. Crosstalk Test Circuit

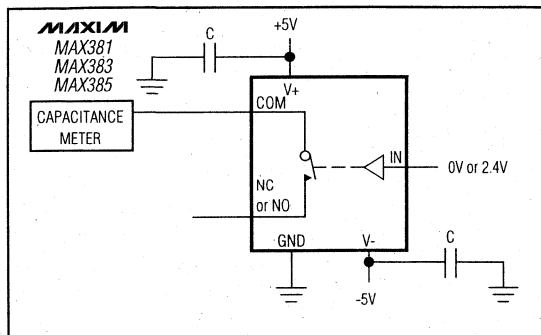


Figure 7. Channel-Off Capacitance

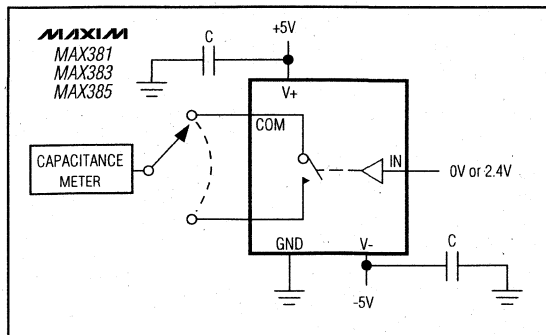


Figure 8. Channel-On Capacitance

Precision, Low-Voltage Analog Switches

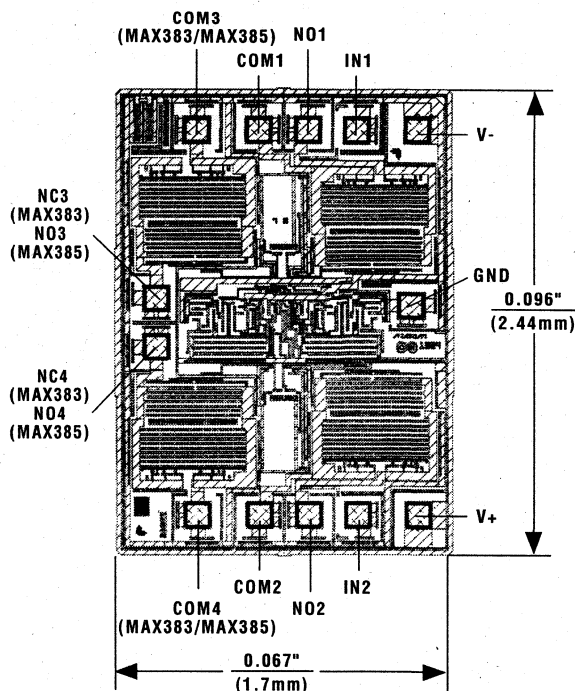
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX383 CPE	0°C to +70°C	16 Plastic DIP
MAX383CSE	0°C to +70°C	16 Narrow SO
MAX383C/D	0°C to +70°C	Dice*
MAX383EPE	-40°C to +85°C	16 Plastic DIP
MAX383ESE	-40°C to +85°C	16 Narrow SO
MAX383EJE	-40°C to +85°C	16 Cerdip**
MAX383MJE	-55°C to +125°C	16 Cerdip**
MAX385 CPE	0°C to +70°C	16 Plastic DIP
MAX385CSE	0°C to +70°C	16 Narrow SO
MAX385C/D	0°C to +70°C	Dice*
MAX385EPE	-40°C to +85°C	16 Plastic DIP
MAX385ESE	-40°C to +85°C	16 Narrow SO
MAX385EJE	-40°C to +85°C	16 Cerdip**
MAX385MJE	-55°C to +125°C	16 Cerdip**

* Dice are tested at $T_A = +25^\circ\text{C}$ only.

** Contact factory for package availability.

Chip Topography



TRANSISTOR COUNT: 57
SUBSTRATE CONNECTED TO V+

MAX3831/MAX383/MAX385



Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

General Description

The MAX382/MAX384 are low-voltage, CMOS, 1-of-8 and dual 4-channel muxes with latchable digital inputs. They feature low-voltage operation from a +2.7V to +16.5V single supply and from $\pm 3V$ to $\pm 8V$ dual supplies. Pin compatible with the DG428/DG429, these muxes offer low on-resistance (100Ω max) matched to within 4Ω max between channels. Additional features include off leakage less than $2.5nA$ at $+85^\circ C$ and guaranteed low charge injection ($10pC$ max). ESD protection is greater than 2000V per Method 3015.7.

Applications

Battery-Operated Systems
Audio Signal Routing
Low-Voltage Data-Acquisition Systems
Sample-and-Hold Circuits
Automatic Test Equipment

Features

- ♦ Pin-Compatible with Industry-Standard DG428/DG429, DG528/DG529, MAX368/MAX369
- ♦ Single-Supply Operation (+2.7V to +16.5V)
Bipolar Supply Operation ($\pm 3V$ to $\pm 8V$)
- ♦ Low Power Consumption ($<300\mu W$)
- ♦ Low On-Resistance, 100Ω max
- ♦ Guaranteed On-Resistance Match Between Channels, 4Ω max
- ♦ Low Leakage, $2.5nA$ at $+85^\circ C$
- ♦ TTL/CMOS-Logic Compatible

Ordering Information

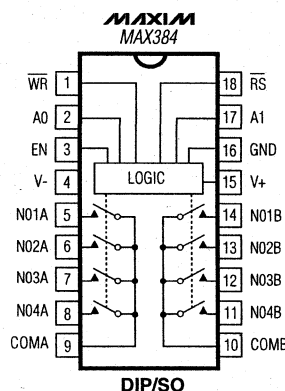
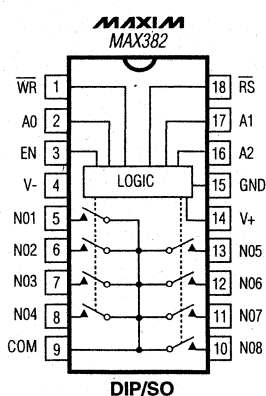
PART	TEMP. RANGE	PIN-PACKAGE
MAX382CPN	$0^\circ C$ to $+70^\circ C$	18 Plastic DIP
MAX382CWN	$0^\circ C$ to $+70^\circ C$	18 Wide SO
MAX382C/D	$0^\circ C$ to $+70^\circ C$	Dice*
MAX382EPN	$-40^\circ C$ to $+85^\circ C$	18 Plastic DIP
MAX382EWN	$-40^\circ C$ to $+85^\circ C$	18 Wide SO
MAX382EJN	$-40^\circ C$ to $+85^\circ C$	18 CERDIP**
MAX382MJN	$-55^\circ C$ to $+125^\circ C$	18 CERDIP**

Ordering Information continued on last page.

* Contact factory for dice specifications.

** Contact factory for package availability.

Pin Configurations



Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND

V+	-0.3V to +17V
V-	+0.3V to -17V
V+ to V-	-0.3V to +17V
Voltage into Any Terminal (Note 1)	(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)

Current into Any Terminal30mA

Peak Current, Any Terminal
(pulsed at 1ms, 10% duty cycle max)100mA

Continuous Power Dissipation (TA = +70°C)

Plastic DIP (derate 11.11mW/°C above +70°C)889mW

Wide SO (derate 9.52mW/°C above +70°C)762mW

CERDIP (derate 10.53mW/°C above +70°C)842mW

Operating Temperature Ranges

MAX38_C_N0°C to +70°C

MAX38_E_N-40°C to +85°C

MAX38_MJN-55°C to +125°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, VA_H = VENH = 2.4V, VA_L = VENL = 0.8V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS			
SWITCH												
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)				V-		V+	V			
Channel On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V		T _A = +25°C		60		100	Ω			
				T _A = T _{MIN} to T _{MAX}		125						
On-Resistance Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V, V ₊ = 5V, V ₋ = -5V		T _A = +25°C		4		Ω				
				T _A = T _{MIN} to T _{MAX}		6						
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	I _{NO} = 1mA, V _{COM} = ±3V, V ₊ = 5V, V ₋ = -5V		T _A = +25°C		10		Ω				
				T _A = T _{MIN} to T _{MAX}		13						
NO-Off Leakage Current (Note 6)	I _{NO(OFF)}	V _{NO} = ±4.5V, V _{COM} = ±4.5V, V ₊ = 5.5V, V ₋ = -5.5V		T _A = +25°C		-0.1		0.1	nA			
				T _A = T _{MIN} to T _{MAX}		C, E	-1.0			1.0		
						M	-10			10		
COM-Off Leakage Current (Note 6)	I _{COM(OFF)}	V _{COM} = ±4.5V, V _{NO} = ±4.5V, V ₊ = 5.5V, V ₋ = -5.5V		MAX382		T _A = +25°C		-0.2		0.2	nA	
						T _A = T _{MIN} to T _{MAX}		C, E	-2.5			2.5
				M	-20			20				
		MAX384		T _A = +25°C		-0.1		0.1				
				T _A = T _{MIN} to T _{MAX}		C, E	-1.5		1.5			
						M	-10		10			
COM-On Leakage Current (Note 6)	I _{COM(ON)}	V _{COM} = ±4.5V, V _{NO} = 4.5V,		MAX382		T _A = +25°C		-0.4		0.4	nA	
						T _A = T _{MIN} to T _{MAX}		C, E	-5			5
								M	-40			40
				MAX384		T _A = +25°C		-0.2		0.2		
						T _A = T _{MIN} to T _{MAX}		C, E	-2.5			2.5
								M	-20			20

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{A,H} = V_{ENH} = 2.4V, V_{A,L} = V_{ENL} = 0.8V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT						
Logic High Input Voltage	V _{A,H} , V _{ENH}	T _A = T _{MIN} to T _{MAX}	2.4			V
Logic Low Input Voltage	V _{A,L} , V _{ENL}	T _A = T _{MIN} to T _{MAX}			0.8	V
Input Current with Input Voltage High	I _{A,H} , I _{ENH}	V _{A,H} = 2.4V, V _{A,L} = 0.8V	-0.1		0.1	μA
Input Current with Input Voltage Low	I _{A,L} , I _{ENL}	V _{A,H} = 2.4V, V _{A,L} = 0.8V	-0.1		0.1	μA
SUPPLY						
Power-Supply Range	V+, V-		±2.4		±8	V
Positive Supply Current	I+	V _{EN} = V _A = 0V/V+, V+ = 5.5V, V- = -5.5V T _A = +25°C	-1		1	μA
Negative Supply Current	I-	V _{EN} = V _A = 0V/V+, V+ = 5.5V, V- = -5.5V T _A = T _{MIN} to T _{MAX}	-1		1	μA
AX, EN Data Hold Time	t _H	Figure 5 T _A = +25°C	100			ns
Reset Pulse Width	t _{RS}	Figure 6, V+ = 5V T _A = +25°C	100			ns
DYNAMIC						
Transition Time	t _{TRANS}	Figure 1		100	275	ns
Break-Before-Make Interval	t _{OPEN}	Figure 2 T _A = +25°C	0	20		ns
Enable Turn-On Time	t _{ON(EN)}	Figure 3 T _A = +25°C T _A = T _{MIN} to T _{MAX}		100	150 250	ns
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3 T _A = +25°C T _A = T _{MIN} to T _{MAX}		80	150 250	ns
Write Turn-On Time	t _{ON(WR)}	Figure 4 T _A = +25°C T _A = T _{MIN} to T _{MAX}			150 250	ns
Reset Turn-Off Time	t _{OFF(RS)}	Figure 6 T _A = +25°C T _A = T _{MIN} to T _{MAX}			150 250	ns
Charge Injection (Note 3)	V _{CTE}	C _L = 100pF, V _{NO} = 0V T _A = +25°C		2	5	pC
Off Isolation (Note 7)	V _{ISO}	V _{EN} = 0V, R _L = 1kΩ, f = 100kHz T _A = +25°C		-75		dB
Crosstalk Between Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{p-p} , R _L = 1kΩ T _A = +25°C		-92		dB
Logic Input Capacitance	C _{IN}	f = 1MHz T _A = +25°C		8		pF
NO-Off Capacitance	C _{NO(OFF)}	f = 1MHz, V _{EN} = V _{COM} = 0V T _A = +25°C		11		pF
COM-Off Capacitance	C _{COM(OFF)}	f = 1MHz, V _{EN} = V _{COM} = 0V MAX382 MAX384 T _A = +25°C		40 20		pF
COM-On Capacitance	C _{COM(ON)}	f = 1MHz, V _{EN} = V _{COM} = 0V MAX382 MAX384 T _A = +25°C		54 34		pF
MINIMUM INPUT TIMING REQUIREMENTS						
Write Pulse Width	t _w	Figure 5 T _A = +25°C	100			ns
AX, EN Data Setup Time	t _s	Figure 5 T _A = +25°C	100			ns

MAX382/MAX384

1

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
AX, EN Data Hold Time	t _H	Figure 5		T _A = +25°C	100			ns
Reset Pulse Width	t _{RS}	Figure 6, V+ = 5V		T _A = +25°C	100			ns
SWITCH								
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)			V-		V+	V
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V+ = 4.5V		T _A = +25°C	150		225	Ω
				T _A = T _{MIN} to T _{MAX}			280	
On-Resistance Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V+ = 4.5V		T _A = +25°C			10	Ω
				T _A = T _{MIN} to T _{MAX}			12	
On-Resistance Flatness	R _{FLAT}	I _{NO} = 1mA; V _{COM} = 3V, 2V, 1V; V+ = 5V		T _A = +25°C	10		16	Ω
				T _A = T _{MIN} to T _{MAX}	15		20	
NO-Off Leakage Current (Note 8)	I _{NO(OFF)}	V _{NO} = 4.5V, V _{COM} = 0V, V+ = 5.5V		T _A = +25°C	-0.1		0.1	nA
				T _A = T _{MIN} to T _{MAX}	C, E -1.0		1.0	
					M -10		10	
COM-Off Leakage Current (Note 8)	I _{COM(OFF)}	V _{COM} = 4.5V, V _{NO} = 0V, V+ = 5.5V	MAX382	T _A = +25°C	-0.2		0.2	nA
				T _A = T _{MIN} to T _{MAX}	C, E -2.5		2.5	
		V _{COM} = 4.5V, V _{NO} = 0V, V+ = 5.5V	MAX384	T _A = +25°C	-0.2		0.2	
				T _A = T _{MIN} to T _{MAX}	C, E -1.5		1.5	
					M -10		10	
COM-On Leakage Current (Note 8)	I _{COM(ON)}	V _{COM} = 4.5V, V _{NO} = 4.5V, V+ = 5.5V	MAX382	T _A = +25°C	-0.4		0.4	nA
				T _A = T _{MIN} to T _{MAX}	C, E -5		5	
			MAX384		M -40		40	
				T _A = +25°C	-0.2		0.2	
				T _A = T _{MIN} to T _{MAX}	C, E -2.5		2.5	
		M -20		20				
DIGITAL LOGIC INPUT								
Logic High Input Voltage	V _H , V _{ENH}			T _A = T _{MIN} to T _{MAX}	2.4			V
Logic Low Input Voltage	V _L , V _{ENL}			T _A = T _{MIN} to T _{MAX}			0.8	V
Input Current with Input Voltage High	I _H , I _{ENH}	V _H = 2.4V, V _L = 0.8V			-0.1		0.1	μA
Input Current with Input Voltage Low	I _L , I _{ENL}	V _H = 2.4V, V _L = 0.8V			-0.1		0.1	μA
SUPPLY								
Power-Supply Range					2.4		15	V
Positive Supply Current	I+	V _{EN} = V _A = 0V, V+ = 5.5V; V- = 0V			-1.0		1.0	μA
Negative Supply Current	I-	V _{EN} = V _A = 0V, V+ = 5.5V; V- = 0V			-1.0		1.0	μA
I _{GND} Supply Current	I _{GND}	V _{EN} = V+, 0V; V _A = 0V; V+ = 5.5V; V- = 0V		T _A = +25°C	-1.0		1.0	μA
				T _A = T _{MIN} to T _{MAX}	-1.0		1.0	

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

MAX382/MAX384

1

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{A_H} = V_{ENH} = 2.4V, V_{A_L} = V_{ENL} = 0.8V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC						
Transition Time	t _{TRANS}	Figure 1, V _{NO} = 3V		90	280	ns
Break-Before-Make Interval	t _{OPEN}	Figure 2 (Note 3)	5	40		ns
Enable Turn-On Time (Note 3)	t _{ON(EN)}	Figure 3	T _A = +25°C		130	200
			T _A = T _{MIN} to T _{MAX}		275	ns
Enable Turn-Off Time (Note 3)	t _{OFF(EN)}	Figure 3	T _A = +25°C		80	200
			T _A = T _{MIN} to T _{MAX}		275	ns
Write Turn-On Time (Note 3)	t _{ON(WR)}	Figure 4	T _A = +25°C		200	ns
			T _A = T _{MIN} to T _{MAX}		275	
Reset Turn-Off Time (Note 3)	t _{OFF(RS)}	Figure 4	T _A = +25°C		200	ns
			T _A = T _{MIN} to T _{MAX}		275	
Charge Injection (Note 3)	V _{CTE}	Figure 7, C _L = 100pF, V _{NO} = 0V	T _A = +25°C		1.5	5
						pC

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V ±10%, V- = 0V, GND = 0V, V_{A_H} = V_{ENH} = 2.4V, V_{A_L} = V_{ENL} = 0.8V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	VANALOG	(Note 3)		V-	V+	V	
On-Resistance	RON	INO = 1mA, VCOM = 1.5V, V+ = 3V	TA = +25°C	230	375	Ω	
			TA = TMIN to TMAX	425			
DYNAMIC							
Transition Time (Note 3)	tTRANS	Figure 1, VIN = 2.4V, VN01 = 1.5V, VN08 = 0V	TA = +25°C	230	575	ns	
Enable Turn-On Time (Note 3)	tON(EN)	Figure 3, VINH = 2.4V, VINL = 0V, VN01 = 1.5V	TA = +25°C	200	500	ns	
Enable Turn-Off Time (Note 3)	tOFF(EN)	Figure 3, VINH = 2.4V, VINL = 0V, VN01 = 1.5V	TA = +25°C	75	400	ns	
Write Turn-On Time (Note 3)	tON(WR)	Figure 4	TA = +25°C	200	500	ns	
Reset Turn-Off Time (Note 3)	tOFF(RS)	Figure 4	TA = +25°C	75	400	ns	
Charge Injection (Note 3)	VCTE	Figure 7, CL = 100pF, VNO = 0V	TA = +25°C	1	5	pC	

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges, i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 6: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.

Note 7: Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM}/V_{NO}. V_{COM} = output, V_{NO} = input to off switch.

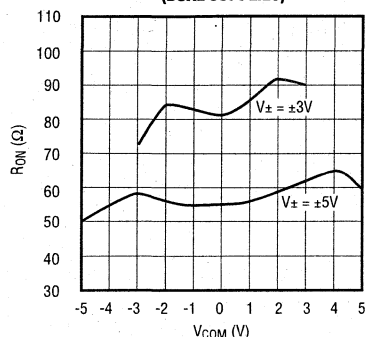
Note 8: Leakage testing at single supply is guaranteed by correlation testing with dual supplies.

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

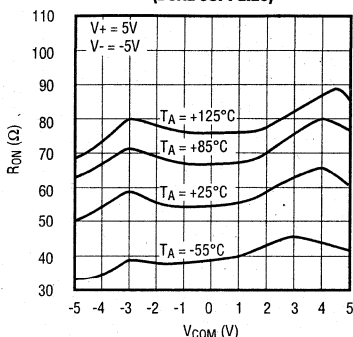
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

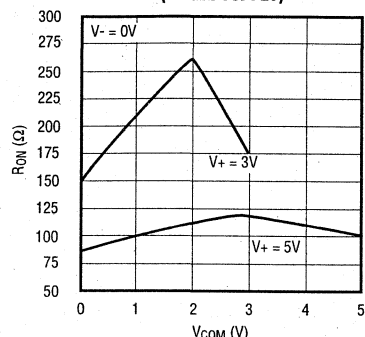
**ON-RESISTANCE vs. V_{COM}
(DUAL SUPPLIES)**



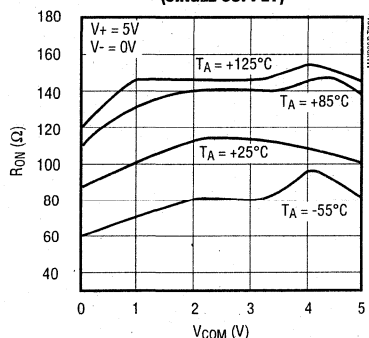
**ON-RESISTANCE vs. V_{COM}
AND TEMPERATURE
(DUAL SUPPLIES)**



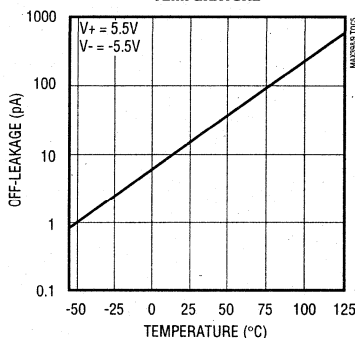
**ON-RESISTANCE vs. V_{COM}
(SINGLE SUPPLY)**



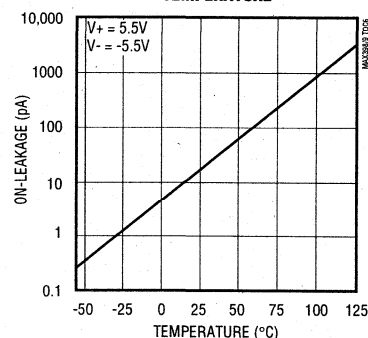
**ON-RESISTANCE vs. V_{COM}
AND TEMPERATURE
(SINGLE SUPPLY)**



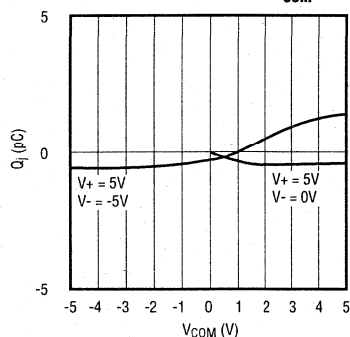
**OFF-LEAKAGE vs.
TEMPERATURE**



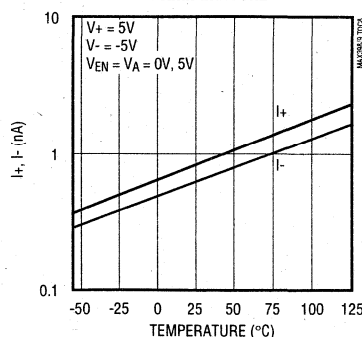
**ON-LEAKAGE vs.
TEMPERATURE**



CHARGE INJECTION vs. V_{COM}



**SUPPLY CURRENT vs.
TEMPERATURE**



Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

Pin Description

PIN		NAME*	FUNCTION
MAX382	MAX384		
1	1	WR	WRITE Logic Input
2, 16, 17	—	A0, A2, A1	Address Logic Inputs (see <i>Truth Tables</i> at end of data sheet)
—	2, 17	A0, A1	Address Logic Inputs (see <i>Truth Tables</i> at end of data sheet)
3	3	EN	Enable Logic Input (see <i>Truth Tables</i> at end of data sheet)
4	4	V-	Negative Supply Voltage Input. Connect to GND for single-supply operation.
5–8	—	NO1–NO4	Analog Signal Inputs—bidirectional
—	5–8	NO1A–NO4A	Analog Signal Inputs—bidirectional
9	—	COM	Analog Signal Output—bidirectional
—	9, 10	COMA, COMB	Analog Signal Outputs—bidirectional
10–13	—	NO8–NO5	Analog Signal Inputs—bidirectional
—	11–14	NO4B–NO1B	Analog Signal Inputs—bidirectional
14	15	V+	Positive Supply Voltage Input
15	16	GND	Ground
18	18	RS	RESET Logic Input

*Analog inputs and outputs are names of convenience only. Inputs and outputs are identical and interchangeable.

Applications Information

The internal structures of the MAX382/MAX384 include translators for the A2/A1/EN/WR/RS digital inputs, latches, and a decode section for channel selection (see *Truth Tables*). The analog-signal switches consist of parallel combinations of N and P MOSFETs.

WRITE (WR) and RESET (RS) strobes are provided for interfacing with μ P-bus lines, alleviating the need for the μ P to provide constant address inputs to the mux to hold a particular channel (Figures 2–7).

When the WR strobe is in the low state (less than 0.8V) and the RS strobe is in the high state (greater than 2.4V), the muxes are in the transparent mode—they act similar to nonlatching devices, such as the MAX398/MAX399.

When the WR goes high, the previous BCD address input is latched and held in that state indefinitely.

RS turns off all channels when it is low. All switches stay off until RS and EN are high and WR is low.

The MAX382/MAX384 work with both single and dual supplies and function over the +2.4V to +16V single-supply range. For example, with a single +5V power supply, analog signals in the 0V to +5V range can be switched normally. If negative signals around 0V are expected, a negative supply is needed.

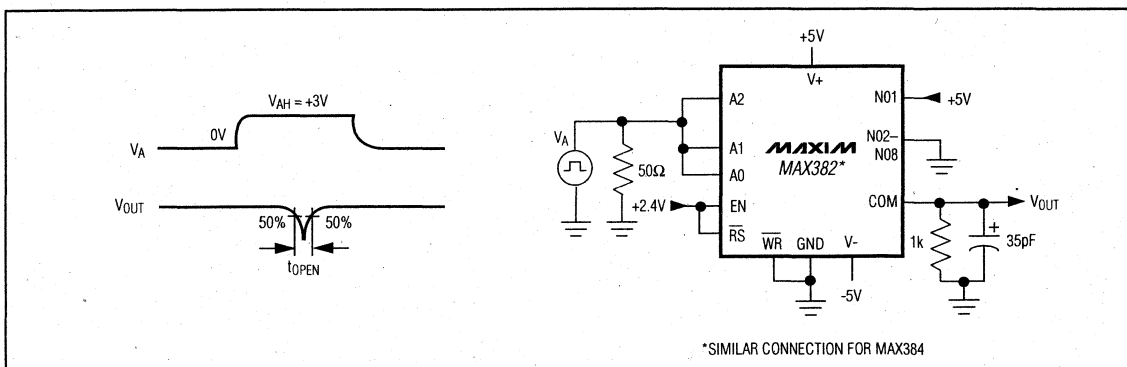
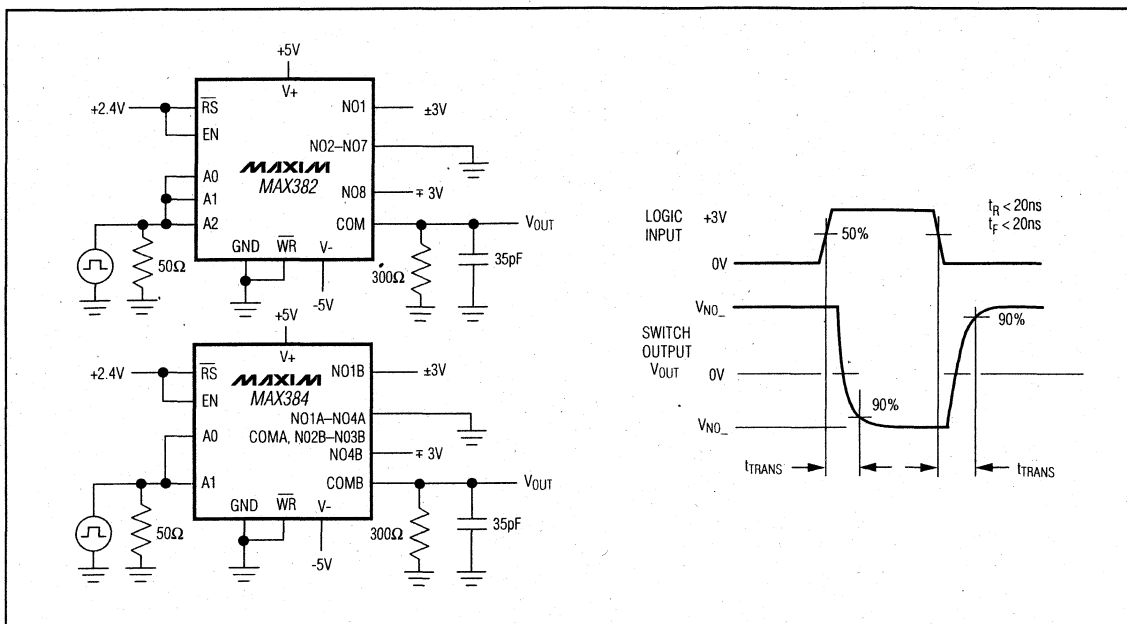
The EN latch allows all switches to be turned off under program control. This is useful when two or more are cascaded to build 16-line and larger analog-signal multiplexers.

MAX382/MAX384

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Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

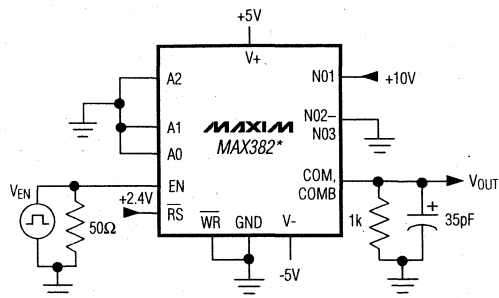
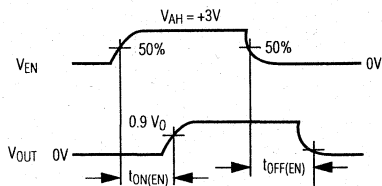
Test Circuits/Timing Diagrams



Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

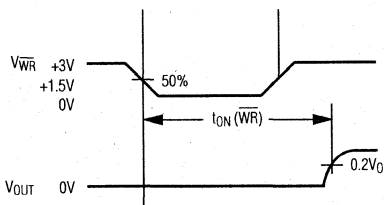
MAX382/MAX384

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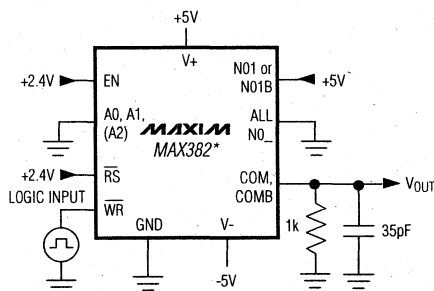


*SIMILAR CONNECTION FOR MAX384

Figure 3. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)



DEVICE MUST BE RESET PRIOR TO APPLYING $\overline{WR}$ PULSE



*SIMILAR CONNECTION FOR MAX384

Figure 4. Write Turn-On Time ($t_{ON(WR)}$)

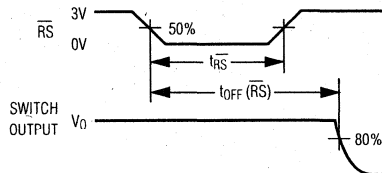
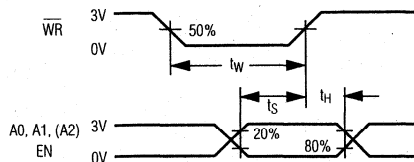


Figure 5. Write, Setup, and Hold Timing (t_W , t_S , t_H)

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

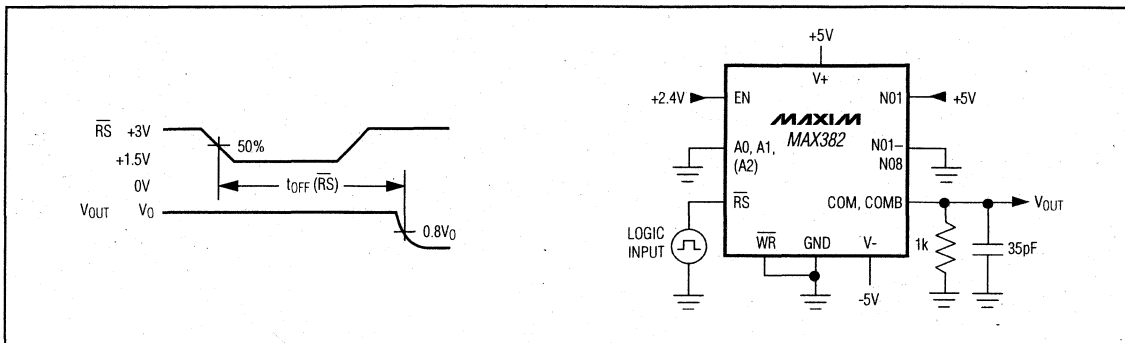


Figure 6. Reset Turn-Off Time ($t_{OFF}(\overline{RS})$)

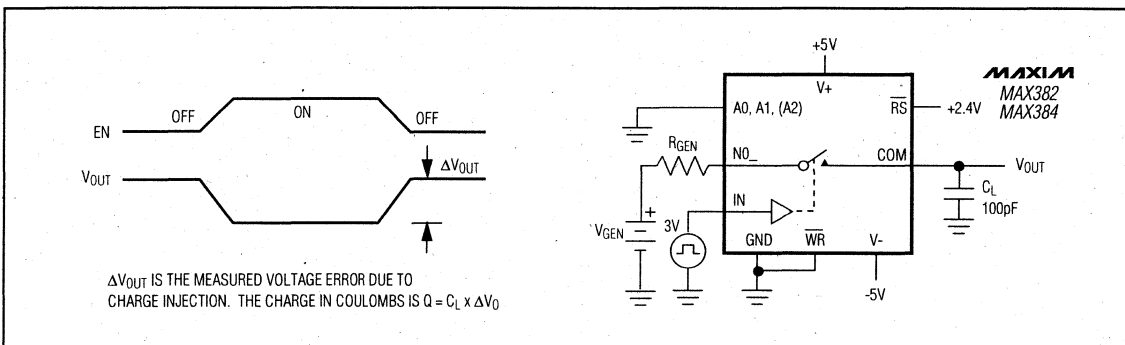


Figure 7. Charge Injection (V_{CTE})

Operation with Supply Voltages Other than $\pm 5V$

Using supply voltages less than $\pm 5V$ reduces the analog signal range. The MAX382/MAX384 muxes operate with $\pm 3V$ to $\pm 8V$ bipolar supplies or with a +2.7V to +16.5V single supply. Connect V_- to GND when operating with a single supply. Both devices can also operate with unbalanced supplies, such as +10V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with $\pm 3V$, $\pm 5V$, +3V and +5V supplies. (Switching times increase by a factor of two or more for operation at +5V or below.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, then V_- , followed by the logic inputs, NO, or COM. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with supply pins for overvoltage protection (Figure 8). Adding diodes reduces the analog signal range to one diode drop below V_+ and one diode drop above V_- , but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V_+ and V_- should not exceed 17V. These protection diodes are not recommended when using a single supply.

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

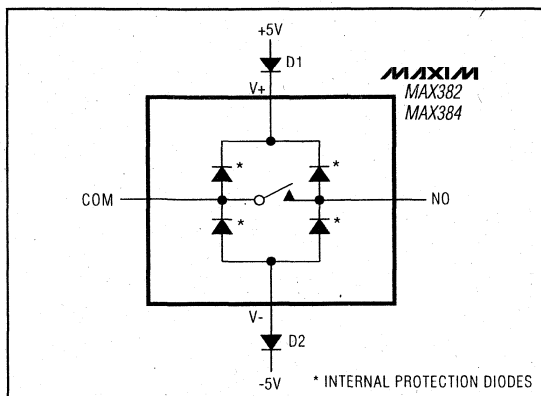
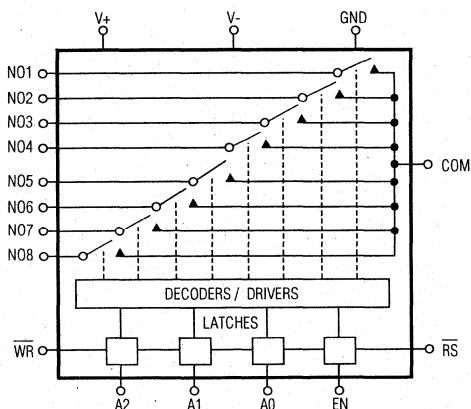


Figure 8. Overvoltage Protection Using External Blocking Diodes

Functional Diagrams/Truth Tables

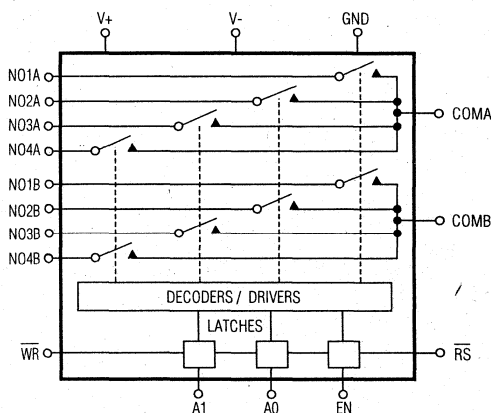
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MAX382 8-CHANNEL SINGLE-ENDED MULTIPLEXER



A2	A1	A0	EN	WR	RS	ON SWITCH
Latching						
X	X	X	X		1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

MAX384 DIFFERENTIAL 4-CHANNEL MULTIPLEXER



A1	A0	EN	WR	RS	ON SWITCH
Latching					
X	X	X		1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

LOGIC "0" = $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

Ordering Information (continued)

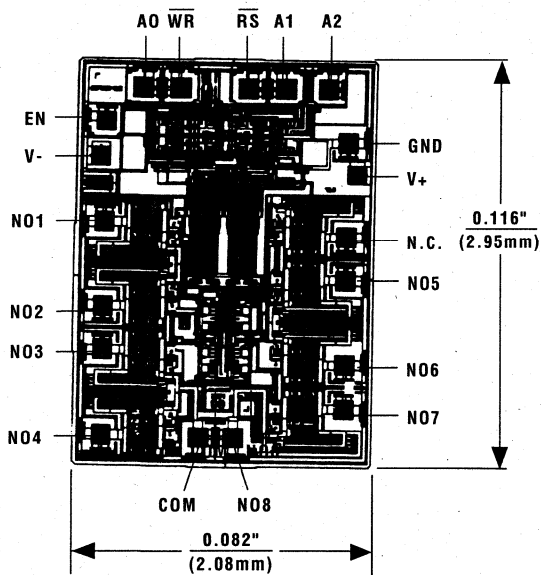
PART	TEMP. RANGE	PIN-PACKAGE
MAX384CPN	0°C to +70°C	18 Plastic DIP
MAX384CWN	0°C to +70°C	18 Wide SO
MAX384C/D	0°C to +70°C	Dice*
MAX384EPN	-40°C to +85°C	18 Plastic DIP
MAX384EWN	-40°C to +85°C	18 Wide SO
MAX384EJN	-40°C to +85°C	18 Cerdip**
MAX384MJN	-55°C to +125°C	18 Cerdip**

* Contact factory for dice specifications.

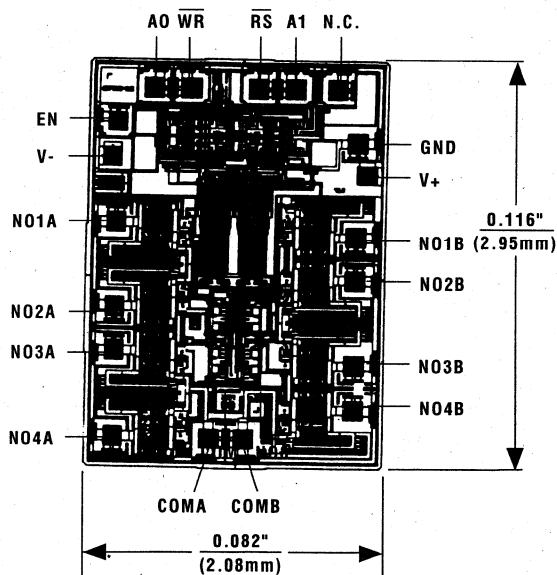
** Contact factory for package availability.

Chip Topographies

MAX382



MAX384



TRANSISTOR COUNT: 165
SUBSTRATE CONNECTED TO V+

MAXIM

Low-Voltage, Quad, SPDT, CMOS Analog Switch

General Description

The MAX394 is a precision, low-voltage, quad, single-pole/double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from $\pm 2.7\text{V}$ to $\pm 8\text{V}$, or with a single supply of $+2.7\text{V}$ to $+15\text{V}$. The MAX394 offers low on-resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range ($\Delta 4\Omega$ max). It also offers break-before-make switching (10ns typical), with turn-off times less than 75ns and turn-on times less than 130ns. The MAX394 is ideal for portable operation since quiescent current runs less than $1\mu\text{A}$ with all inputs high or low.

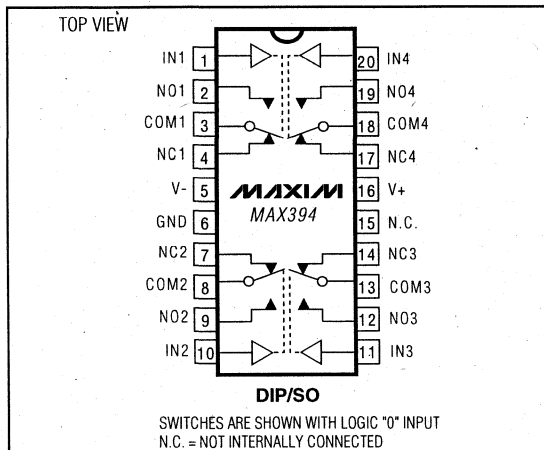
This monolithic, quad switch is fabricated with Maxim's low voltage silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption ($10\mu\text{W}$), and electrostatic discharge (ESD) greater than 2000V.

Logic inputs are TTL and CMOS compatible and guaranteed over a $+0.8\text{V}$ to $+2.4\text{V}$ range for supply voltages up to $+8\text{V}$. When supplies exceed $+8\text{V}$, the inputs are typically $+0.8\text{V}$ to $+4\text{V}$. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage.

Applications

Test Equipment	Portable Instruments
Communications Systems	Audio Signal Routing
PBX, PABX	Set-Top Boxes
Heads-Up Displays	

Pin Configuration



Features

- ◆ Low On-Resistance, $< 17\Omega$ Typical (35Ω max)
- ◆ Guaranteed Matched On-Resistance Between Channels, $< 2\Omega$
- ◆ Guaranteed Flat On-Resistance over Analog Signal Range, $\Delta 4\Omega$ Max
- ◆ Guaranteed Charge Injection $< 10\text{pC}$
- ◆ Guaranteed Off-Channel Leakage $< 2.5\text{nA}$ at $+85^\circ\text{C}$
- ◆ ESD Guaranteed $> 2000\text{V}$ per Method 3015.7
- ◆ Single-Supply Operation ($+2.7\text{V}$ to $+15\text{V}$)
Bipolar-Supply Operation ($\pm 2.7\text{V}$ to $\pm 8\text{V}$)
- ◆ TTL/CMOS-Logic Compatibility
- ◆ Rail-to-Rail Analog Signal Handling Capability
- ◆ Pin Compatible with MAX333, MAX333A

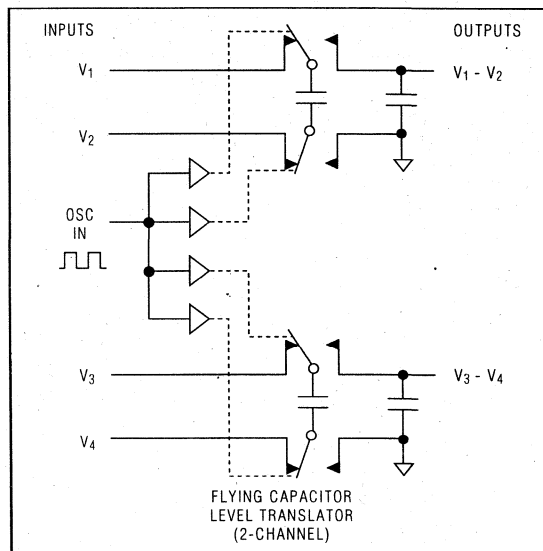
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX394CPP	0°C to $+70^\circ\text{C}$	20 Plastic DIP
MAX394CWP	0°C to $+70^\circ\text{C}$	20 Wide SO
MAX394C/D	0°C to $+70^\circ\text{C}$	Dice*
MAX394EPP	-40°C to $+85^\circ\text{C}$	20 Plastic DIP
MAX394EWP	-40°C to $+85^\circ\text{C}$	20 Wide SO
MAX394MJP	-55°C to $+125^\circ\text{C}$	20 CERDIP**

* Contact factory for dice specifications.

** Contact factory for availability.

Typical Operating Circuit



Low-Voltage, Quad, SPDT, CMOS Analog Switch

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND

V+	-0.3V to +17V
V-	+0.3V to -17V
V+ to V-	-0.3V to +17V
COM ₋ , NO ₋ , NC ₋ , IN ₋ (Note 1)	(V- - 2V) to (V+ + 2V) or 30mA, whichever occurs first

Continuous Current, Any Pin 30mA

Peak Current, Any Pin

(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 10.53mW/°C above +70°C) 842mW

Narrow SO (derate 8.70mW/°C above +70°C) 696mW

CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges

MAX394C_P 0°C to +70°C

MAX394E_P -40°C to +85°C

MAX394MJP -55°C to +125°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (soldering, 10sec) +300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 5V ±10%, V- = -5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}	(Note 3)		V-		V+	V
On-Resistance	R _{ON}	V+ = 4.5V, V- = -4.5V, V _{NC} or V _{NO} = ±3.5V, I _{COM} = 10mA, V _{INH} = 2.4V, V _{INL} = 0.8V	T _A = +25°C	C, E	20	35	Ω
			T _A = T _{MIN} to T _{MAX}	M	20	30	
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V _{NC} or V _{NO} = ±3V, I _{COM} = 10mA, V+ = 5V, V- = -5V	T _A = +25°C	C, E, M	0.5	2	Ω
			T _A = T _{MIN} to T _{MAX}	C, E, M		4	
On-Resistance Flatness (Note 4)	R _{FLAT(ON)}	V _{NC} or V _{NO} = 3V, 0V, -3V; I _{COM} = 10mA, V+ = 5V; V- = -5V	T _A = +25°C	C, E, M		4	Ω
			T _A = T _{MIN} to T _{MAX}	C, E, M		6	
NC or NO Off Leakage Current (Note 5)	I _{NC(OFF)} or I _{NO(OFF)}	V _{COM} = ±4.5V, V _{NC} or V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	T _A = +25°C	C, E	-0.2	-0.01	nA
				M	-0.1	-0.01	
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5	2.5	
				M	-20	20	
COM Leakage Current (Note 5)	I _{COM(ON)}	V _{COM} = ±4.5V, V _{NC} or V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	T _A = +25°C	C, E	-0.4	-0.04	nA
				M	-0.2	-0.04	
			T _A = T _{MIN} to T _{MAX}	C, E	-5.0	5.0	
				M	-20	20	

Low-Voltage, Quad, SPDT, CMOS Analog Switch

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ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 5V ±10%, V- = -5V ±10%, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V		-1.0	0.005	1.0	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V		-1.0	0.005	1.0	μA
Logic High Input Voltage	V _{A_H}		T _A = T _{MIN} to T _{MAX}	2.4			V
Logic Low Input Voltage	V _{A_L}		T _A = T _{MIN} to T _{MAX}			0.8	V
DYNAMIC							
Turn-On Time	t _{ON}	V _{COM} = 3V, Figure 2	T _A = +25°C		82	130	ns
			T _A = T _{MIN} to T _{MAX}			175	
Turn-Off Time	t _{OFF}	V _{COM} = 3V, Figure 2	T _A = +25°C		57	75	ns
			T _A = T _{MIN} to T _{MAX}			100	
Break-Before-Make Time Delay (Note 3)	t _D	Figure 5	T _A = +25°C	2	10		ns
Charge Injection (Note 3)	V _{CTE}	C _L = 1.0nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 6	T _A = +25°C		5	10	pC
Off Isolation (Note 6)	V _{ISO}	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 3	T _A = +25°C		66		dBm
Crosstalk (Note 7)	V _{CT}	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 8	T _A = +25°C		88		dBm
Off Capacitance	C _{OFF}	f = 1MHz, Figure 3	T _A = +25°C		12		pF
COM Off Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 3	T _A = +25°C		12		pF
Channel On Capacitance	C _{COM(ON)}	f = 1MHz, Figure 4	T _A = +25°C		39		pF
SUPPLY							
Power-Supply Range				±2.4		±8	V
Positive Supply Current	I ₊	All channels on or off, V ₊ = 5.5V, V ₋ = -5.5V, V _{IN} = 0V or V ₊		-1.0	0.06	1.0	μA
Negative Supply Current	I ₋	All channels on or off, V ₊ = 5.5V, V ₋ = -5.5V, V _{IN} = 0V or V ₊		-1.0	-0.01	1.0	μA

Low-Voltage, Quad, SPDT, CMOS Analog Switch

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = 5V ±10%, V- = 0V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP. RANGE	MIN TYP (Note 2) MAX			UNITS
SWITCH								
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}	(Note 3)			0V V+			V
On-Resistance	R _{ON}	V+ = 5.0V, V- = 0V, V _{NC} or V _{NO} = 3.5V, I _{COM} = 1.0mA, V _{INH} = 2.4V, V _{INL} = 0.8V	T _A = +25°C	C, E	25	65	Ω	
				M	60			
			T _A = T _{MIN} to T _{MAX}	C, E, M	75			
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V _{NC} or V _{NO} = 3V, I _{COM} = 1.0mA, V+ = 5V	T _A = +25°C	C, E, M	0.5	2	Ω	
			T _A = T _{MIN} to T _{MAX}	C, E, M	4			
On-Resistance Flatness (Note 4)	R _{FLAT(ON)}	V _{NC} or V _{NO} = 3V, 2V, 1V; I _{COM} = 1.0mA; V+ = 5V; V- = 0V	T _A = +25°C	C, E, M	6			Ω
			T _A = T _{MIN} to T _{MAX}	C, E, M	8			
NC or NO Off Leakage Current (Note 8)	I _{NC(OFF)} or I _{NO(OFF)}	V _{COM} = 0V, V _{NC} or V _{NO} = 4.5V, V+ = 5.5V, V- = 0V	T _A = +25°C	C, E	-0.2	-0.01	0.2	nA
				M	-0.1	-0.01	0.1	
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
				M	-20		20	
COM Leakage Current (Note 8)	I _{COM(ON)}	V _{COM} = 4.5V, V _{NC} or V _{NO} = 4.5V, V+ = 5.5V, V- = 0V	T _A = +25°C	C, E	-0.4	-0.04	0.4	nA
				M	-0.2	-0.04	0.2	
			T _A = T _{MIN} to T _{MAX}	C, E	-5.0		5.0	
				M	-20		20	
DIGITAL LOGIC INPUT								
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V			-1.0	0.005	1.0	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V			-1.0	0.005	1.0	μA

Low-Voltage, Quad, SPDT, CMOS Analog Switch

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ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC						
Turn-On Time (Note 3)	tON	VCOM = 3V, Figure 2	TA = +25°C	160	250	ns
			TA = TMIN to TMAX		300	
Turn-Off Time (Note 3)	tOFF	VCOM = 3V, Figure 2	TA = +25°C	60	125	ns
			TA = TMIN to TMAX		175	
Break-Before-Make Time Delay (Note 3)	tD		TA = +25°C	5	20	ns
Charge Injection (Note 3)	VCTE	CL = 1.0nF, VGEN = 0V, RGEN = 0Ω	TA = +25°C	3	5	pC
SUPPLY						
Power-Supply Range	V+		2.4		16	V
Positive Supply Current	I+	All channels on or off, VIN = 0V or V+, V+ = 5.5V, V- = 0V	-1.0	0.01	1.0	μA
Negative Supply Current	I-	All channels on or off, VIN = 0V or V+, V+ = 5.5V, V- = 0V	-1.0	-0.01	1.0	μA

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = 3.0V to 3.6V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	VCOM, VNO, VNC	(Note 3)		0		V+	V
On-Resistance	RON	V+ = 3V, V- = 0V, VNC or VNO = 1.5V, ICOM = 1.0mA, VINH = 2.4V, VINL = 0.8V	TA = +25°C	C, E	75	185	Ω
				M		175	
NC or NO Off Leakage Current (Note 8)	INC(OFF) or INO(OFF)	VCOM = 0V, VNC or VNO = 3V, V+ = 3.6V, V- = 0V	TA = +25°C	C, E	-0.2	-0.01	nA
				M	-0.1	-0.01	
			TA = TMIN to TMAX	C, E	-2.5		
				M	-5.0	5.0	
COM Leakage Current (Note 8)	ICOM(ON)	VCOM = 3V, VNC or VNO = 3V, V+ = 3.6V, V- = 0V	TA = +25°C	C, E	-0.4	-0.04	nA
				M	-0.2	-0.04	
			TA = TMIN to TMAX	C, E	-5.0		
				M	-20.0	20.0	

Low-Voltage, Quad, SPDT, CMOS Analog Switch

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply (continued)

($V_+ = 3.0V$ to $3.6V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT						
Input Current with Input Voltage High	I_{INH}	$V_{IN} = 2.4V$, all others = $0.8V$	-1.0	0.005	1.0	μA
Input Current with Input Voltage Low	I_{INL}	$V_{IN} = 0.8V$, all others = $2.4V$	-1.0	0.005	1.0	μA
DYNAMIC						
Turn-On Time (Note 3)	t_{ON}	$V_{COM} = 1.5V$, Figure 2 $T_A = +25^\circ C$			400	ns
Turn-Off Time (Note 3)	t_{OFF}	$V_{COM} = 1.5V$, Figure 2 $T_A = +25^\circ C$			150	ns
Break-Before-Make Delay (Note 3)	t_D	Figure 5 $T_A = +25^\circ C$	5	20		ns
Charge Injection (Note 3)	V_{CTE}	$C_L = 1.0nF$, $V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, Figure 6 $T_A = +25^\circ C$		1	5	pC
SUPPLY						
Power-Supply Range	V_+		2.7		16	V
Positive Supply Current	I_+	All channels on or off, $V_{IN} = 0V$ or V_+ , $V_+ = 3.6V$, $V_- = 0V$	-1.0	0.01	1.0	μA
Negative Supply Current	I_-	All channels on or off, $V_{IN} = 0V$ or V_+ , $V_+ = 3.6V$, $V_- = 0V$	-1.0	-0.01	1.0	μA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON(max)} - \Delta R_{ON(min)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 5: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temperature.

Note 6: See Figure 6. Off isolation = $20 \log_{10} V_{COM}/V_{NC}$ or V_{NO} , V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

Note 7: Between any two switches. See Figure 3.

Note 8: Leakage testing at single supply is guaranteed by testing with dual supplies.

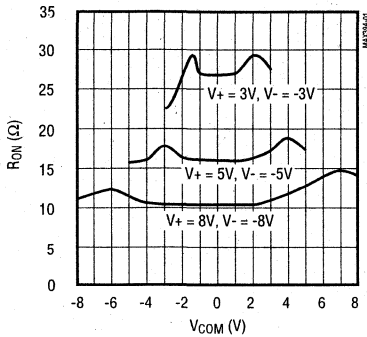
Low-Voltage, Quad, SPDT, CMOS Analog Switch

Typical Operating Characteristics

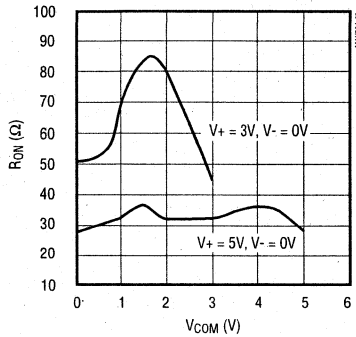
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

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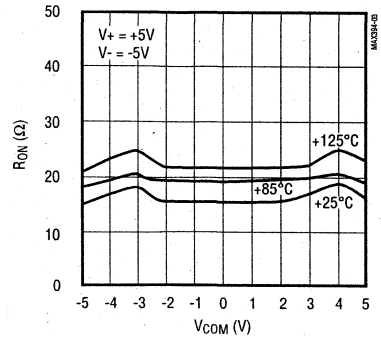
**ON-RESISTANCE vs. V_{COM}
(DUAL SUPPLIES)**



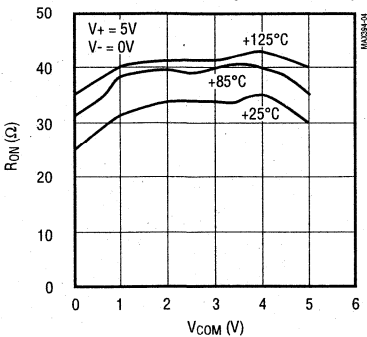
**ON-RESISTANCE vs. V_{COM}
(SINGLE SUPPLY)**



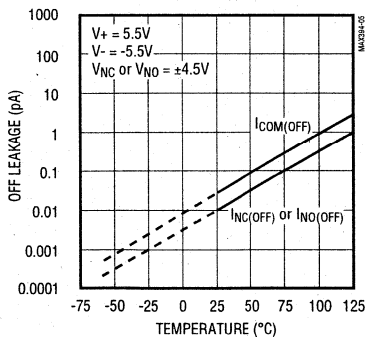
**ON-RESISTANCE vs. V_{COM}
OVER TEMPERATURE (DUAL SUPPLIES)**



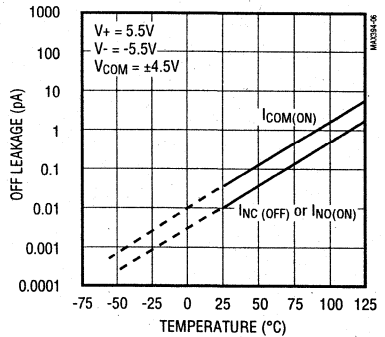
**ON-RESISTANCE vs. V_{COM}
OVER TEMPERATURE (SINGLE SUPPLY)**



**OFF LEAKAGE CURRENT
vs. TEMPERATURE**



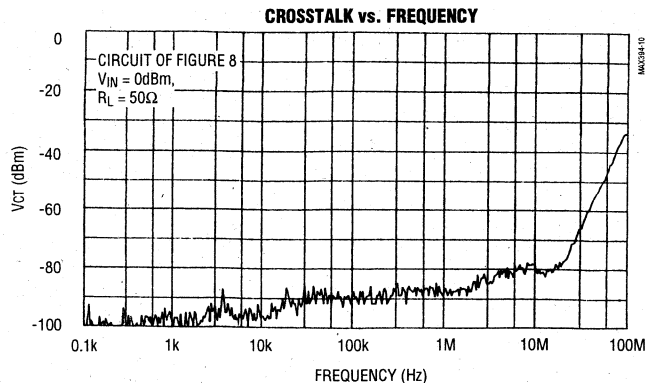
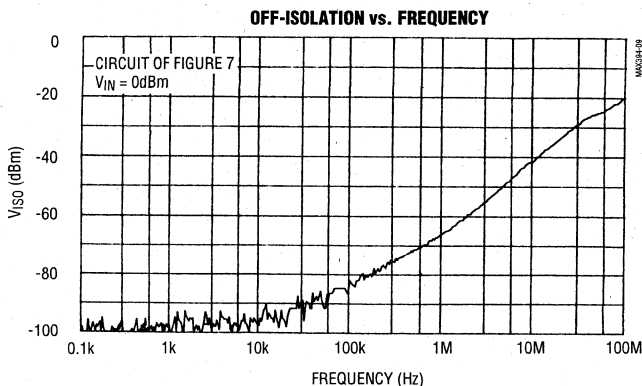
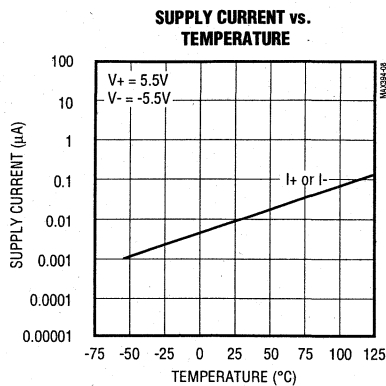
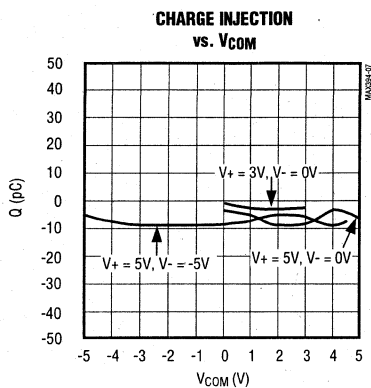
**ON LEAKAGE CURRENT
vs. TEMPERATURE**



Low-Voltage, Quad, SPDT, CMOS Analog Switch

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted).



Low-Voltage, Quad, SPDT, CMOS Analog Switch

Pin Description

PIN	NAME	FUNCTION
1, 10, 11, 20	IN1-IN4	Logic-Level Inputs
2, 9, 12, 19	NO1-NO4	Normally Open Switches
3, 8, 13, 18	COM1-COM4	Common Switch Poles
4, 7, 14, 17	NC1-NC4	Normally Closed Switches
5	V-	Negative Power Supply
6	GND	Ground
15	N.C.	Not Internally Connected
16	V+	Positive Power Supply

Applications Information

Operation with Supply Voltages Other than $\pm 5V$

The MAX394 switch operates with $\pm 2.7V$ to $\pm 8V$ bipolar supplies and a $+2.7V$ to $+15V$ single supply. In either case, analog signals ranging from $V+$ to $V-$ can be switched. The *Typical Operating Characteristics* graphs show the typical on-resistance variation with analog signal and supply voltage. The usual on-resistance temperature coefficient is $0.5\%/^{\circ}C$ (typ).

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the device. Proper power-supply sequencing is recommended for all CMOS devices. Always apply $V+$, followed by $V-$ (when using split supplies) before applying analog signals or logic inputs, especially if the analog or logic signals are not current-limited. If this sequencing is not possible and if the analog or logic inputs are not current-limited to less than

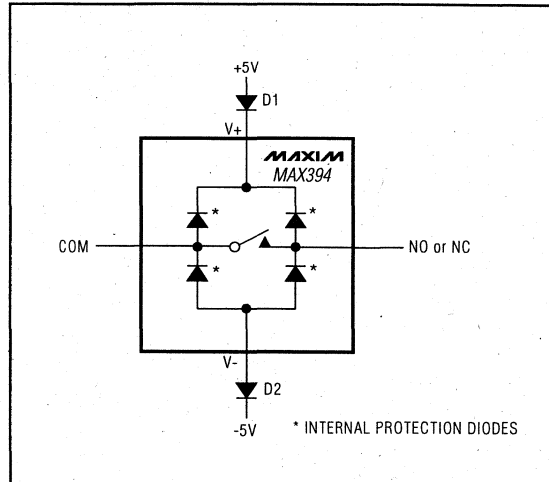


Figure 1. Overvoltage Protection Using Blocking Diodes

30mA, add a single diode (D1) for single-supply operation (Figure 1). If using dual supplies or if the analog signal can dip below ground in single-supply operation, add two small signal diodes (D1, D2), as shown in Figure 1. Adding protection diodes reduces the analog signal range to a diode drop above $V-$ for D2. Leakage is not affected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage ($V-$ to $V+$) must not exceed 17V.

Adding diodes D1 and D2 also protects against some overvoltage situations. With the circuit of Figure 1, if the supply voltage is below the absolute maximum rating and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result. For example, with $\pm 5V$ supplies, analog signals up to $\pm 8.5V$ will not damage the circuit of Figure 1. If only a single fault signal is present, the fault voltage can go to $+12V$ or $-12V$ without damage.

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Low-Voltage, Quad, SPDT, CMOS Analog Switch

Test Circuits/Timing Diagrams

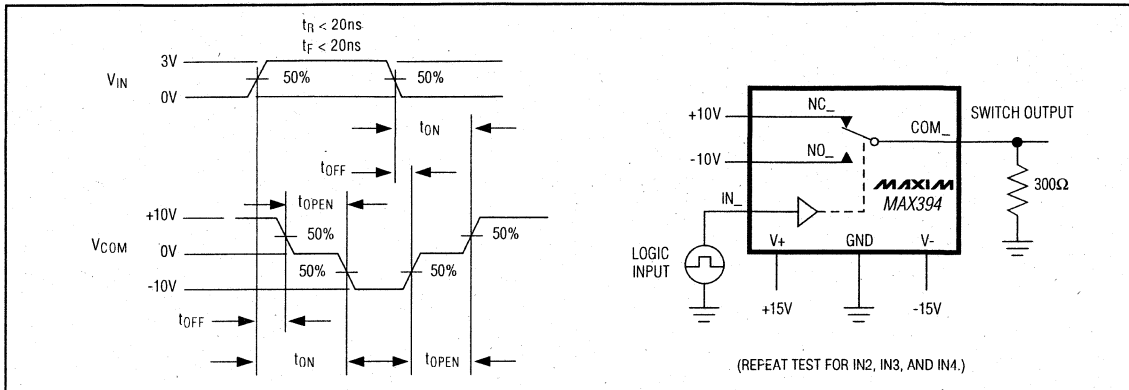


Figure 2. Switching-Time Test Circuit

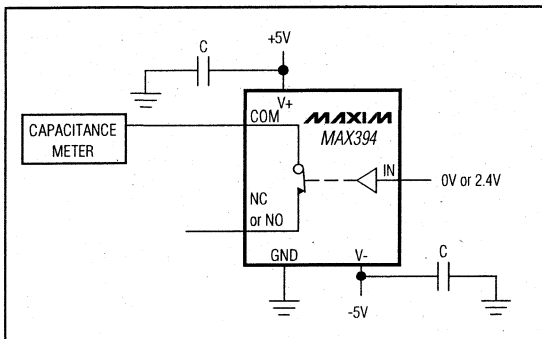


Figure 3. Channel Off Capacitance

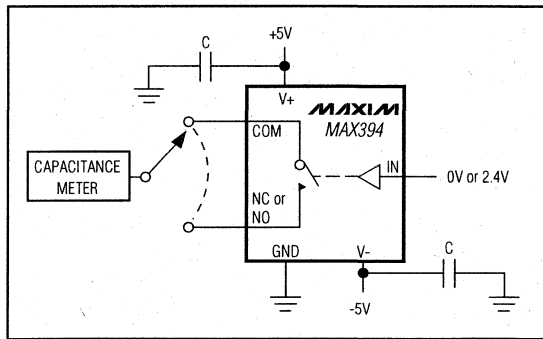


Figure 4. Channel On Capacitance

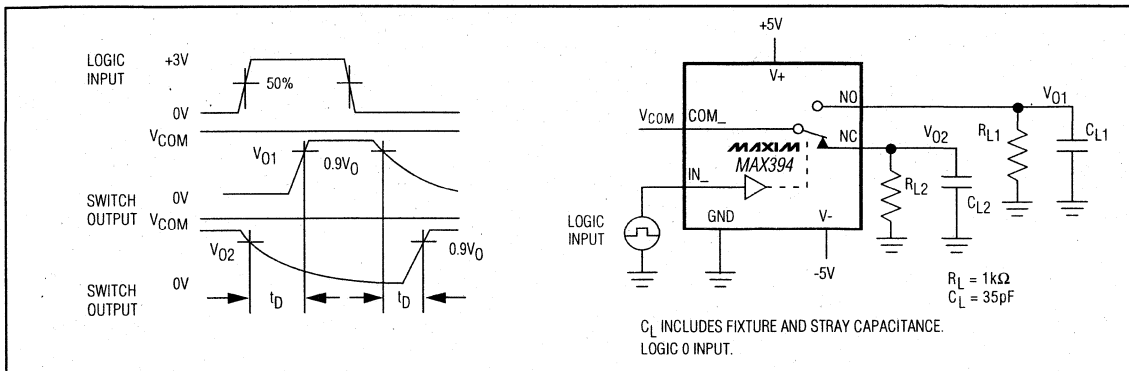


Figure 5. Break-Before-Make Delay

Low-Voltage, Quad, SPDT, CMOS Analog Switch

Test Circuits/Timing Diagrams (continued)

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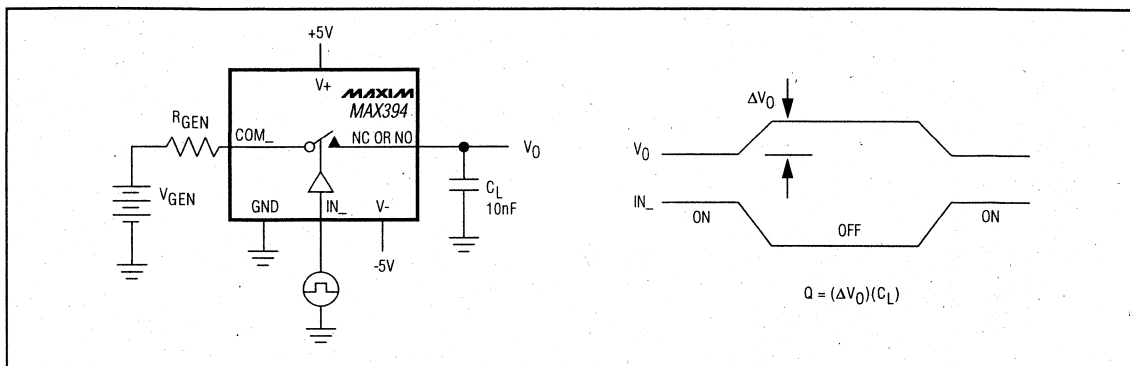


Figure 6. Charge Injection

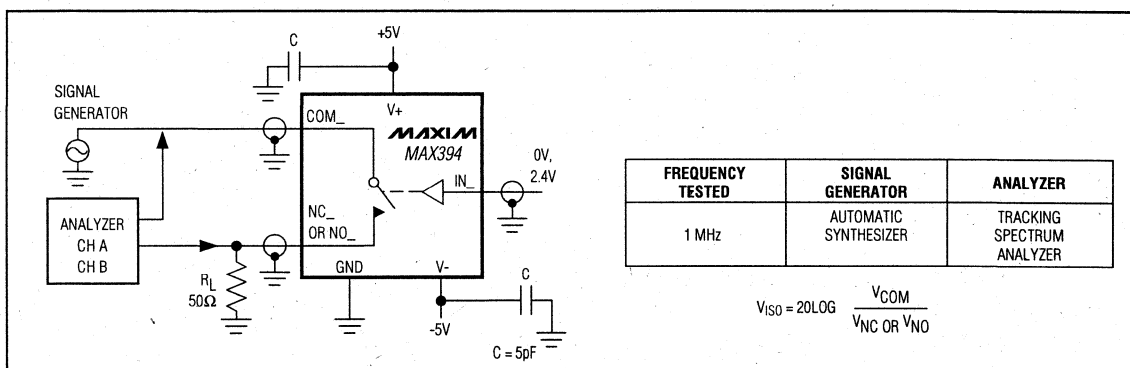


Figure 7. Off Isolation

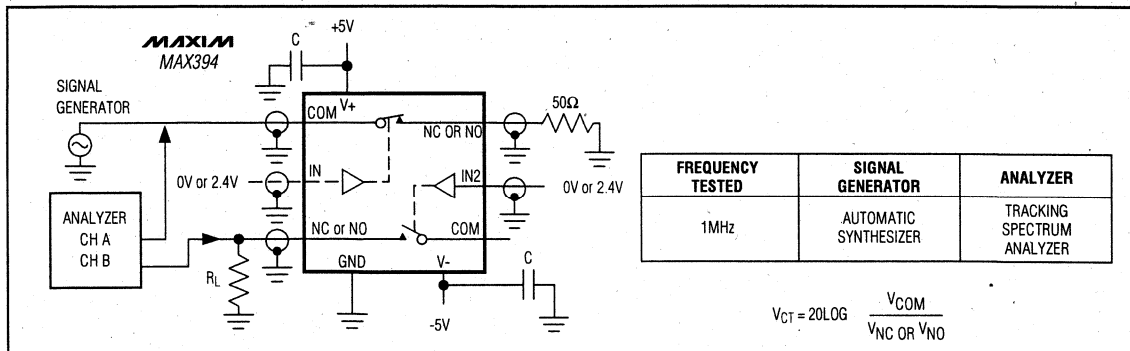
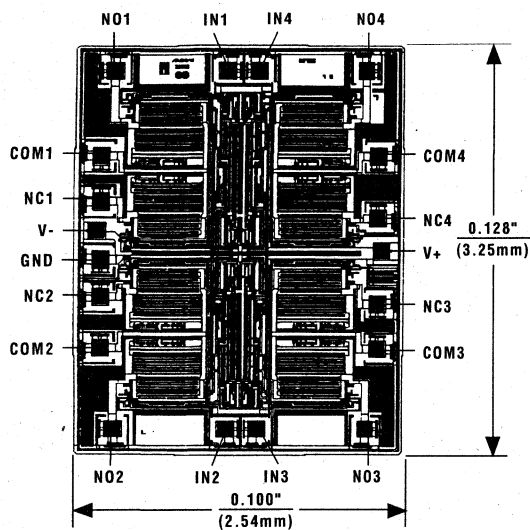


Figure 8. Crosstalk Test Circuit

Low-Voltage, Quad, SPDT, CMOS Analog Switch

Chip Topography



SUBSTRATE IS CONNECTED TO V+
TRANSISTOR COUNT: 137



Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

General Description

The MAX396/MAX397 low-voltage, CMOS analog multiplexers offer low on-resistance (100Ω max), which is matched to within 4Ω between switches and remains flat over the specified signal range (10Ω max). They also offer low leakage over temperature (input-off leakage current less than 1nA at $+85^\circ\text{C}$) and fast switching speeds (transition time less than 250ns). The MAX396 is a 16-channel device, and the MAX397 is a dual 8-channel device.

The MAX396/MAX397 are fabricated with Maxim's low-voltage silicon-gate process. Design improvements yield extremely low charge injection (5pC max) and guarantee electrostatic discharge (ESD) protection greater than 2000V per Method 3015.7

These muxes operate with a single $+2.7\text{V}$ to $+16\text{V}$ supply or with $\pm 2.7\text{V}$ to $\pm 8\text{V}$ dual supplies, while retaining CMOS-logic input compatibility and fast switching. The MAX396/MAX397 are pin compatible with the industry-standard MAX306/MAX307, DG406/DG407, and DG506A/DG507A.

Applications

Sample-and-Hold Circuits	Automatic Test Equipment
Avionics	Communications Systems
Battery-Operated Equipment	Audio Signal Routing
Low-Voltage Data Acquisition Systems	Industrial Process Control

Features

- ◆ Pin Compatible with MAX306/MAX307, DG406/DG407, DG506A/DG507A
- ◆ Single-Supply Operation ($+2.7\text{V}$ to $+16\text{V}$)
Dual-Supply Operation ($\pm 2.7\text{V}$ to $\pm 8\text{V}$)
- ◆ Low On-Resistance (100Ω max)
- ◆ Guaranteed R_{ON} Match Between Channels (4Ω max)
- ◆ Guaranteed R_{ON} Flatness over Specified Signal Range (10Ω max)
- ◆ Guaranteed Low Charge Injection (5pC max)
- ◆ Input-Off Leakage Current $< 1\text{nA}$ at $+85^\circ\text{C}$
- ◆ Output-Off Leakage Current $< 2.5\text{nA}$ at $+85^\circ\text{C}$
- ◆ Low Power Consumption $< 10\mu\text{W}$
- ◆ TTL/CMOS Compatible

Ordering Information

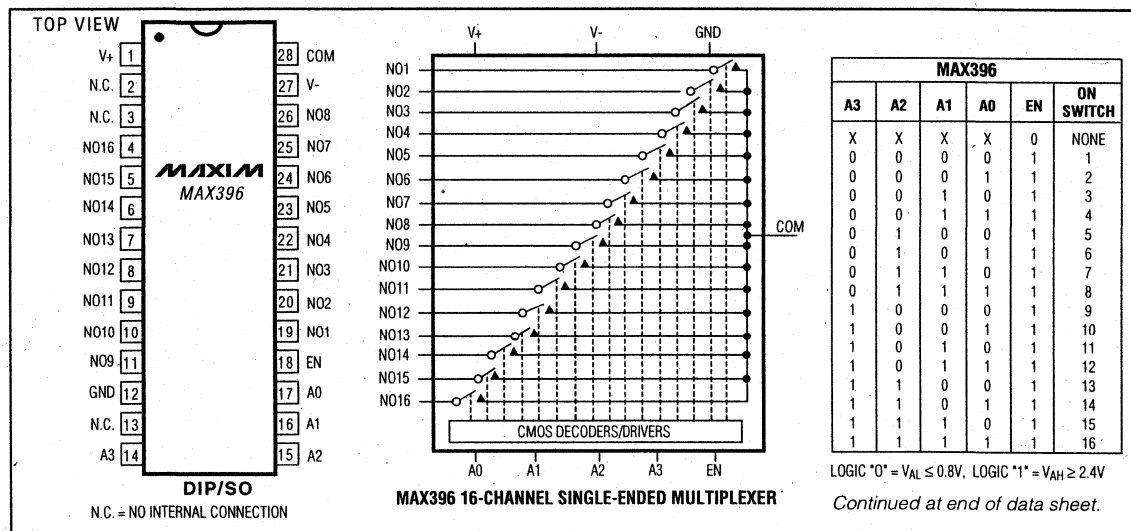
PART	TEMP. RANGE	PIN-PACKAGE
MAX396CPI	0°C to $+70^\circ\text{C}$	28 Plastic DIP
MAX396CWI	0°C to $+70^\circ\text{C}$	28 Wide SO
MAX396CAI	0°C to $+70^\circ\text{C}$	28 SSOP
MAX396CQI	0°C to $+70^\circ\text{C}$	28 PLCC**
MAX396C/D	0°C to $+70^\circ\text{C}$	Dice*

Ordering Information continued on last page.

* Contact factory for dice specifications.

** Contact factory for package availability.

Pin Configurations/Functional Diagrams/Truth Tables



Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

(Voltage referenced to GND, unless otherwise noted.)

V+	-0.3V to +17V
V-	+0.3V to -17V
V+ to V-	-0.3V to +17V
Voltage into Any Terminal (Note 1)	(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Current into Any Terminal	±30mA
Peak Current into Any Terminal	±50mA
Continuous Power Dissipation (T _A = +70°C)	
Plastic DIP (derate 14.29mW/°C above +70°C)	1143mW
Wide SO (derate 12.50mW/°C above +70°C)	1000mW

SSOP (derate 9.52mW/°C above +70°C)	762mW
PLCC (derate 10.53mW/°C above +70°C)	842mW
CERDIP (derate 16.67mW/°C above +70°C)	1333mW
Operating Temperature Ranges	
MAX39_C_I	0°C to +70°C
MAX39_E_I	-40°C to +85°C
MAX39_MJ1	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS	
SWITCH									
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)			V-		V+	V	
Channel On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V	T _A = +25°C		60		100	Ω	
			T _A = T _{MIN} to T _{MAX}				125		
On-Resistance Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V, V+ = 5V, V- = -5V	T _A = +25°C		1.8		4	Ω	
			T _A = T _{MIN} to T _{MAX}				6		
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	I _{NO} = 1mA, V _{COM} = ±3V, V+ = 5V, V- = -5V	T _A = +25°C		5		10	Ω	
			T _A = T _{MIN} to T _{MAX}				13		
NO-Off Leakage Current (Note 6)	I _{NO(OFF)}	V _{NO} = ±4.5V, V _{COM} = ±4.5V, V+ = 5.5V, V- = -5.5V	T _A = +25°C		-0.1	0.03	0.1	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-1.0		1.0		
				M	-10		10		
COM-Off Leakage Current (Note 6)	I _{COM(OFF)}	V _{COM} = ±4.5V, V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	MAX396	T _A = +25°C		-0.2	0.05	0.2	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
			M		-40		40		
		V _{COM} = ±4.5V, V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	MAX397	T _A = +25°C		-0.1	0.03	0.1	
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-20		20	
COM-On Leakage Current (Note 6)	I _{COM(ON)}	V _{COM} = ±4.5V, V _{NO} = 4.5V,	MAX396	T _A = +25°C		-0.4	0.09	0.4	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-5		5	
			M		-60		60		
		MAX397	T _A = +25°C		-0.2	0.05	0.2		
			T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5		
				M	-30		30		

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ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Logic High Input Voltage	V _{AH} , V _{ENH}			2.4			V
Logic Low Input Voltage	V _{AL} , V _{ENL}					0.8	V
Input Current with Input Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V		-0.1		0.1	μA
Input Current with Input Voltage Low	I _{AL} , I _{ENL}	V _A = V _{EN} = 0.8V		-0.1		0.1	μA
SUPPLY							
Power-Supply Range				±3		±8	V
Positive Supply Current	I ₊	V _{EN} = V _A = 0V/V ₊ , V ₊ = 5.5V, V ₋ = -5.5V	T _A = +25°C	-1		1	μA
Negative Supply Current	I ₋	V _{EN} = V _A = 0V/V ₊ , V ₊ = 5.5V, V ₋ = -5.5V		-1		1	μA
Ground Current	I _{GND}	V _{EN} = V _A = 0V/V ₊ , V ₊ = 5.5V, V ₋ = -5.5V	T _A = +25°C	-1		1	μA
			T _A = T _{MIN} to T _{MAX}	-1		1	
DYNAMIC							
Transition Time	t _{TRANS}	Figure 2	T _A = +25°C	95		150	ns
			T _A = T _{MIN} to T _{MAX}			250	
Break-Before-Make Interval	t _{OPEN}	Figure 4	T _A = +25°C	5		70	ns
Enable Turn-On Time	t _{ON(EN)}	Figure 3	T _A = +25°C	100		150	ns
			T _A = T _{MIN} to T _{MAX}			250	
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3	T _A = +25°C	55		150	ns
			T _A = T _{MIN} to T _{MAX}			200	
Charge Injection (Note 3)	V _{CTE}	C _L = 100pF, V _{NO} = 0V, Figure 5	T _A = +25°C	2		5	pC
Off Isolation (Note 7)	V _{ISO}	V _{EN} = 0V, R _L = 1kΩ, f = 100kHz	T _A = +25°C	-75			dB
Crosstalk Between Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{NO} = 1V _{p-p} , R _L = 1kΩ, Figure 7	T _A = +25°C	-92			dB
Logic Input Capacitance	C _{IN}	f = 1MHz	T _A = +25°C	8			pF
NO-Off Capacitance	C _{NO(OFF)}	f = 1MHz, V _{EN} = V _{COM} = 0V	T _A = +25°C	11			pF
COM-Off Capacitance	C _{COM(OFF)}	f = 1MHz, V _{EN} = V _{COM} = 0V	T _A = +25°C	80			pF
				40			
COM-On Capacitance	C _{COM(ON)}	f = 1MHz, V _{EN} = V _{COM} = 0V	T _A = +25°C	90			pF
				68			

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Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V- = 0V, GND = 0V, VAH = VENH = 2.4V, VAL = VENL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS	
SWITCH									
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)			V-		V+	V	
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V ₊ = 4.5V	T _A = +25°C		120		225	Ω	
			T _A = T _{MIN} to T _{MAX}				280		
On-Resistance Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V ₊ = 4.5V	T _A = +25°C		2		10	Ω	
			T _A = T _{MIN} to T _{MAX}				12		
On-Resistance Flatness	R _{FLAT}	I _{NO} = 1mA; V _{COM} = 3V, 2V, 1V; V ₊ = 5V	T _A = +25°C		5		16	Ω	
			T _A = T _{MIN} to T _{MAX}				20		
NO-Off Leakage Current (Note 8)	I _{NO} (OFF)	V _{NO} = 4.5V, V _{COM} = 0V, V ₊ = 5.5V	T _A = +25°C		-0.1	0.03	0.1	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-1.0		1.0		
				M	-10		10		
COM-Off Leakage Current (Note 8)	I _{COM} (OFF)	V _{COM} = 4.5V, V _{NO} = 0V, V ₊ = 5.5V	MAX396	T _A = +25°C		-0.2	0.05	0.2	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-40		40	
		V _{COM} = 4.5V, V _{NO} = 0V, V ₊ = 5.5V	MAX397	T _A = +25°C		-0.2	0.02	0.2	
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-20		20	
COM-On Leakage Current (Note 8)	I _{COM} (ON)	V _{COM} = 4.5V, V _{NO} = 4.5V, V ₊ = 5.5V	MAX396	T _A = +25°C		-0.4	0.09	0.4	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-5		5	
					M	-60		60	
			MAX397	T _A = +25°C		-0.2	0.04	0.2	
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-30		30	
DIGITAL LOGIC INPUT									
Logic High Input Voltage	V _{AH} , V _{ENH}				2.4			V	
Logic Low Input Voltage	V _{AL} , V _{ENL}						0.8	V	
Input Current with Input Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V			-0.1	0.001	0.1	μA	
Input Current with Input Voltage Low	I _{AL} , I _{ENL}	V _A = 0V, V _{EN} = 0.8V			-0.1	0.001	0.1	μA	
SUPPLY									
Power-Supply Range					2.7		15	V	
Positive Supply Current	I ₊	V _{EN} = V _A = 0V, V ₊ ; V ₊ = 5.5V; V ₋ = 0V			-1.0	0.06	1.0	μA	
Negative Supply Current	I ₋	V _{EN} = V _A = 0V, V ₊ ; V ₊ = 5.5V; V ₋ = 0V			-1.0	0.08	1.0	μA	
I _{IGND} Supply Current	I _{IGND}	V _{EN} = V ₊ , 0V; V _A = 0V; V ₊ = 5.5V; V ₋ = 0V	T _A = +25°C		-1.0	0.08	1.0	μA	
			T _A = T _{MIN} to T _{MAX}		-1.0		1.0		

Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

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ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC						
Transition Time (Note 3)	t _{TRANS}	V _{NO} = 3V, Figure 2	T _A = +25°C		105 245	ns
			T _A = T _{MIN} to T _{MAX}		350	
Break-Before-Make Interval	t _{OPEN}	(Note 3)	T _A = +25°C		10 65	ns
Enable Turn-On Time (Note 3)	t _{ON(EN)}		T _A = +25°C		125 200	ns
			T _A = T _{MIN} to T _{MAX}		275	
Enable Turn-Off Time (Note 3)	t _{OFF(EN)}		T _A = +25°C		100 125	ns
			T _A = T _{MIN} to T _{MAX}		200	
Charge Injection (Note 3)	V _{CTE}	C _L = 100pF, V _{NO} = 0V, Figure 5	T _A = +25°C		1.5 5	pC

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	VANALOG	(Note 3)		V-	V+		V
On-Resistance	RON	INO = 1mA, VCOM = 1.5V, V+ = 3V	TA = +25°C	315	550		Ω
			TA = TMIN to TMAX		650		
DYNAMIC							
Transition Time (Note 3)	tTRANS	Figure 2, VIN = 2.4V, VNO1 = 1.5V, VNO8 = 0V	TA = +25°C	230	575		ns
			TA = TMIN to TMAX		750		
Enable Turn-On Time (Note 3)	ton(EN)	Figure 3, VINH = 2.4V, VINL = 0V, VNO1 = 1.5V	TA = +25°C	260	500		ns
Enable Turn-Off Time (Note 3)	toff(EN)	Figure 3, VINH = 2.4V, VINL = 0V, VNO1 = 1.5V	TA = +25°C	135	400		ns
Charge Injection (Note 3)	VCTE	CL = 100pF, VNO = 0V, Figure 5	TA = +25°C	1	5		pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔR_{ON} = R_{ON}(MAX) - R_{ON}(MIN).

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges, i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 6: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.

Note 7: Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM}/V_{NO}. V_{COM} = output, V_{NO} = input to off switch.

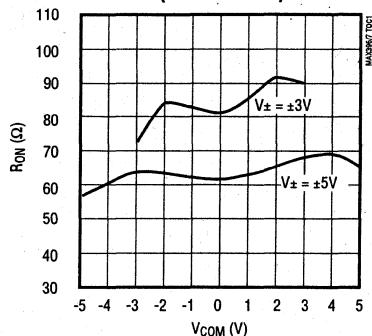
Note 8: Leakage testing at single supply is guaranteed by correlation testing with dual supplies.

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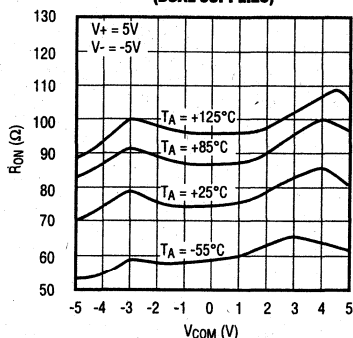
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

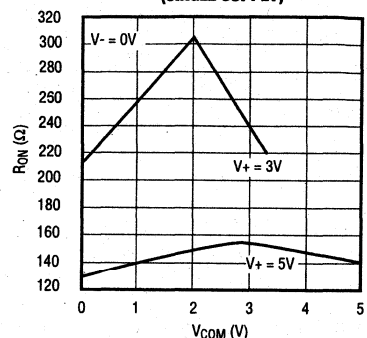
**ON-RESISTANCE vs. V_{COM}
(DUAL SUPPLIES)**



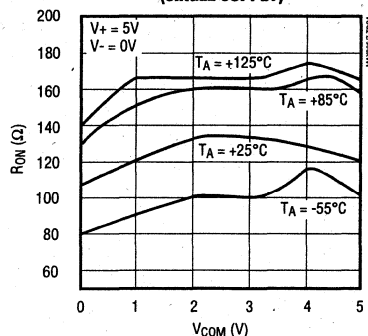
**ON-RESISTANCE vs. V_{COM}
AND TEMPERATURE
(DUAL SUPPLIES)**



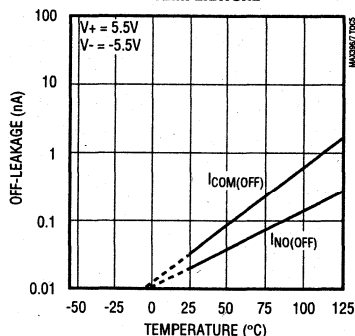
**ON-RESISTANCE vs. V_{COM}
(SINGLE SUPPLY)**



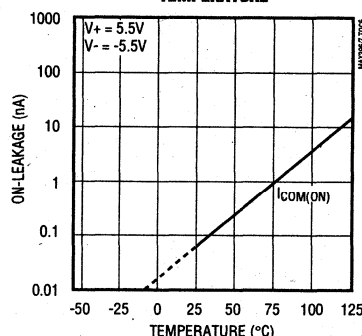
**ON-RESISTANCE vs. V_{COM}
AND TEMPERATURE
(SINGLE SUPPLY)**



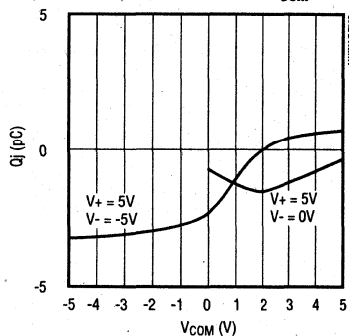
**OFF-LEAKAGE vs.
TEMPERATURE**



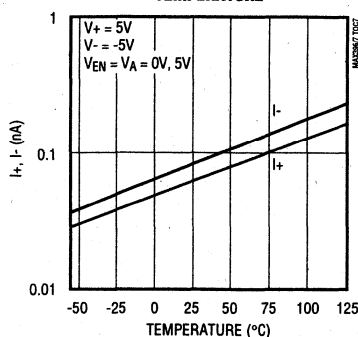
**ON-LEAKAGE vs.
TEMPERATURE**



CHARGE INJECTION vs. V_{COM}



**SUPPLY CURRENT vs.
TEMPERATURE**



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Pin Description

PIN		NAME	FUNCTION
MAX396	MAX397		
1	1	V+	Positive Supply-Voltage Input
2, 3, 13	—	N.C.	No Internal Connection
—	2	COMB	Analog Signal B Output* (bidirectional)
—	3, 13, 14	N.C.	No Internal Connection
4–11	—	NO16–NO9	Analog Signal Inputs* (bidirectional)
—	4–11	NO8B–NO1B	Analog Signal B Inputs* (bidirectional)
12	12	GND	Logic Ground
14–17	—	A3–A0	Logic Address Inputs
—	15, 16, 17	A2, A1, A0	Logic Address Inputs
18	18	EN	Logic Enable Input
19–26	—	NO1–NO8	Analog Signal Inputs* (bidirectional)
—	19–26	NO1A–NO8A	Analog Signal A Inputs* (bidirectional)
27	27	V-	Negative Supply-Voltage Input
28	—	COM	Analog Signal Output* (bidirectional)
—	28	COMA	Analog Signal A Output* (bidirectional)

*Analog signal inputs and outputs are names of convenience only; they are identical and interchangeable.

Applications Information

Operation with Supply Voltages Other than $\pm 5V$

Using supply voltages less than $\pm 5V$ reduces the analog signal range. The MAX396/MAX397 muxes operate with $\pm 3V$ to $\pm 8V$ bipolar supplies or with a +3V to +15V single supply. Connect V- to GND when operating with a single supply. Both devices can also operate with unbalanced supplies, such as +10V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with $\pm 3V$, $\pm 5V$, +3V, and +5V supplies. (Switching times increase by a factor of two or more for operation at 5V or below.)

These muxes operate with a single supply as low as 1V, although on-resistance and switching times become extremely high. Performance is not guaranteed below 2.7V. This is useful information only because it assures proper switch state while power supplies ramp up or down slowly.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs, NO, or COM. If power-supply sequencing

is not possible, add two small signal diodes (D1, D2) in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 17V. These protection diodes are not recommended when using a single supply.

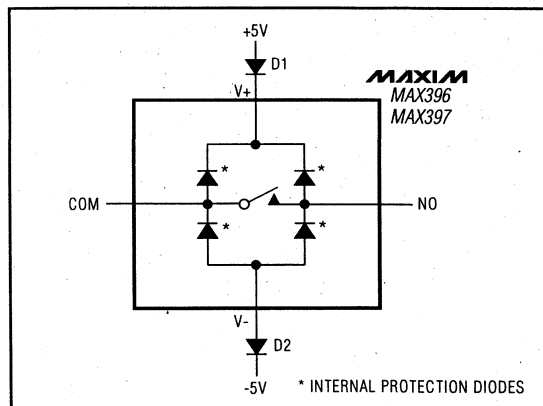


Figure 1. Overvoltage Protection Using External Blocking Diodes

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Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams

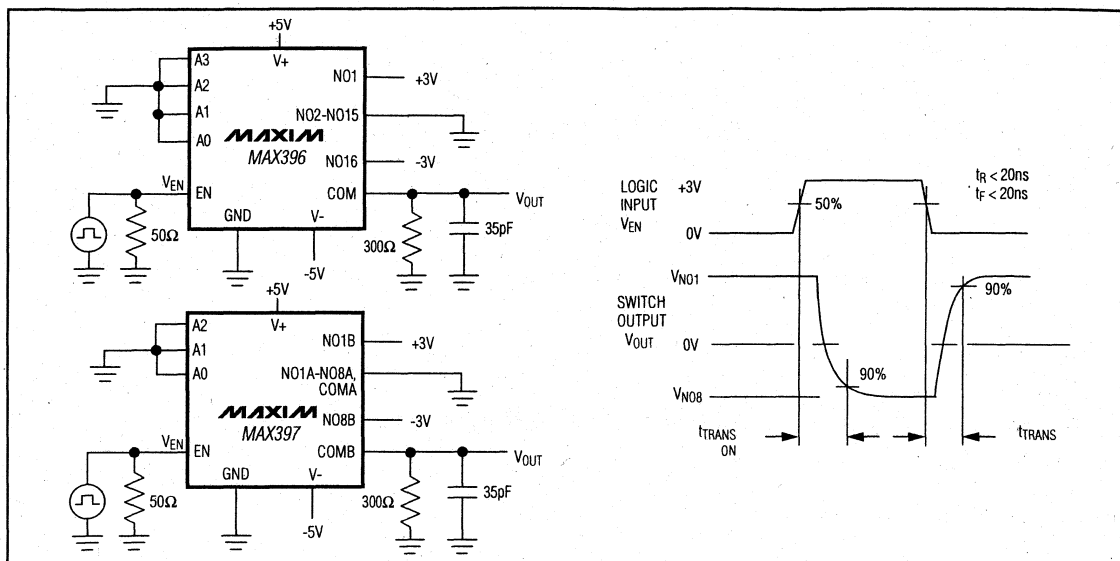


Figure 2. Transition Time

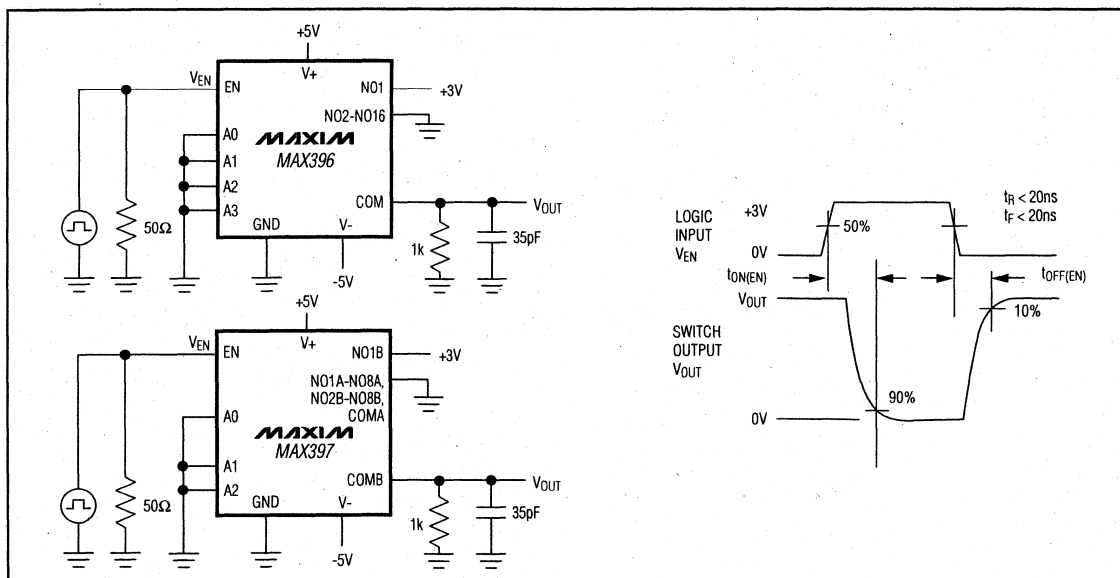


Figure 3. Enable Switching Time

Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

MAX396/MAX397

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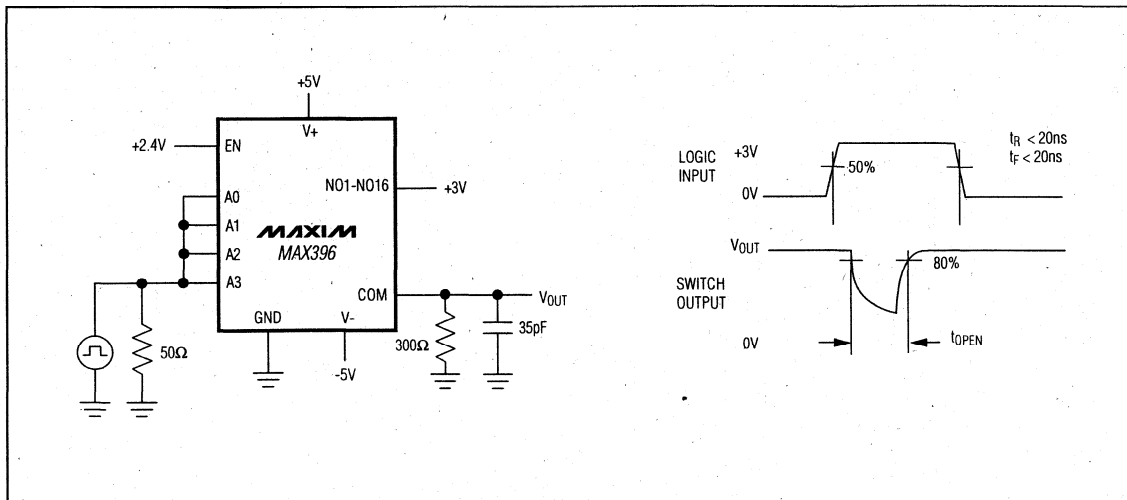


Figure 4. Break-Before-Make Interval

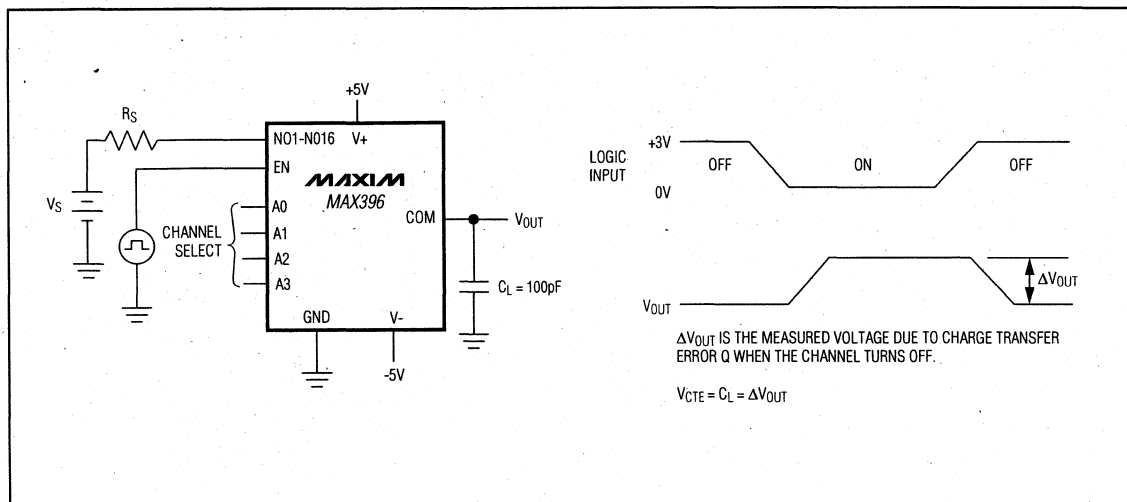


Figure 5. Charge Injection (VCTE)

Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

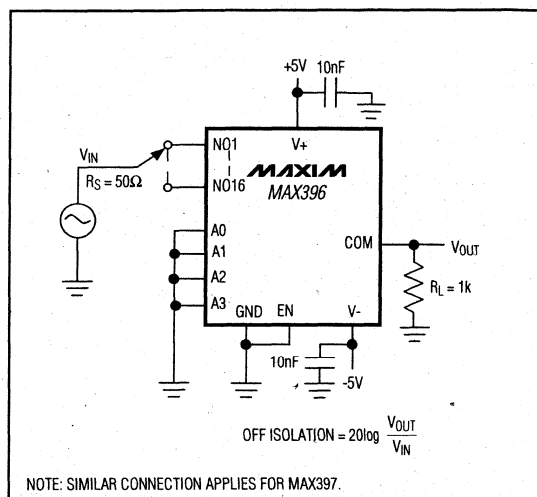


Figure 6. Off Isolation (V_{ISO})

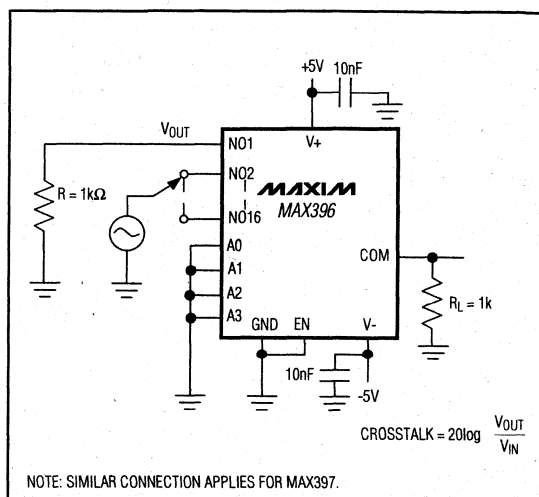


Figure 7. Crosstalk (V_{CT})

Pin Configurations (continued)

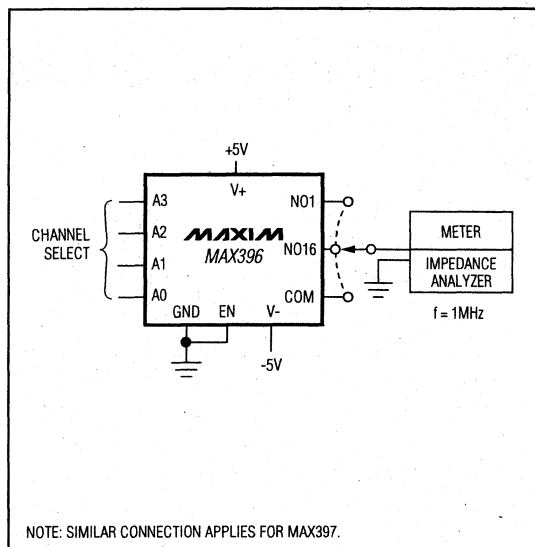
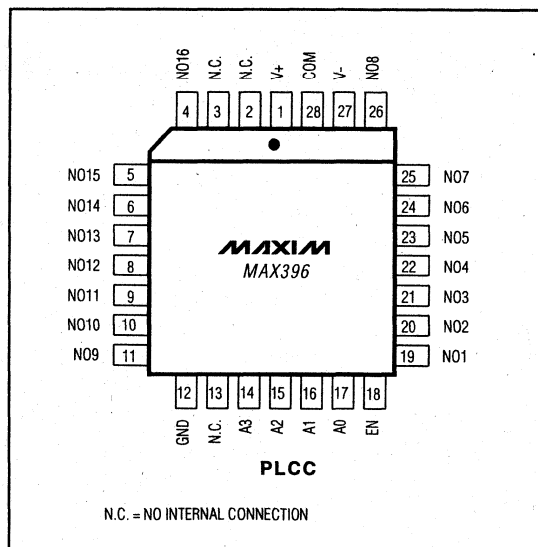


Figure 8. NO/COM Capacitance



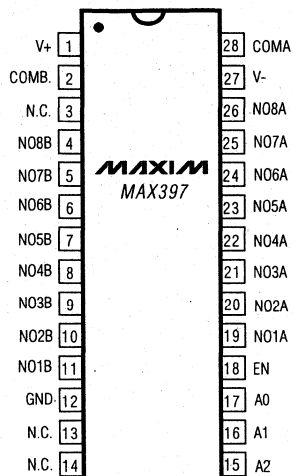
Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)

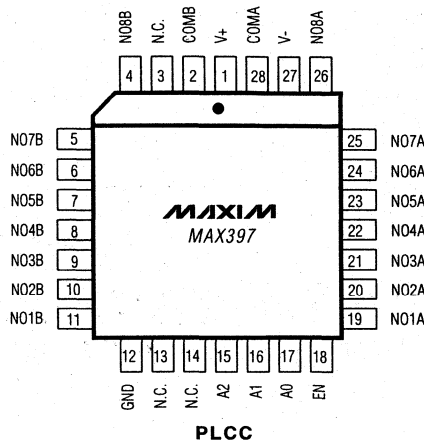
MAX396/MAX397

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TOP VIEW

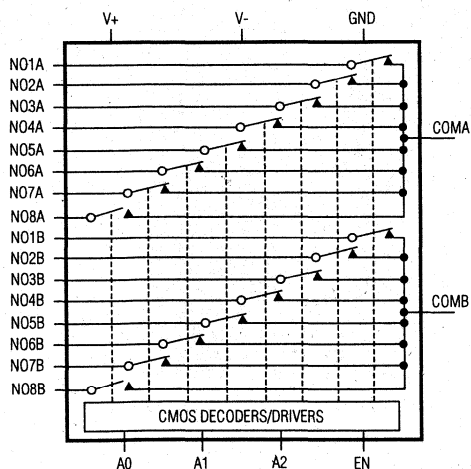


DIP/SO



PLCC

N.C. = NO INTERNAL CONNECTION



MAX397 8-CHANNEL DIFFERENTIAL MULTIPLEXER

MAX397				
A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "0" = $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

Precision, 16-Channel/Dual 8-Channel, Low-Voltage, CMOS Analog Multiplexers

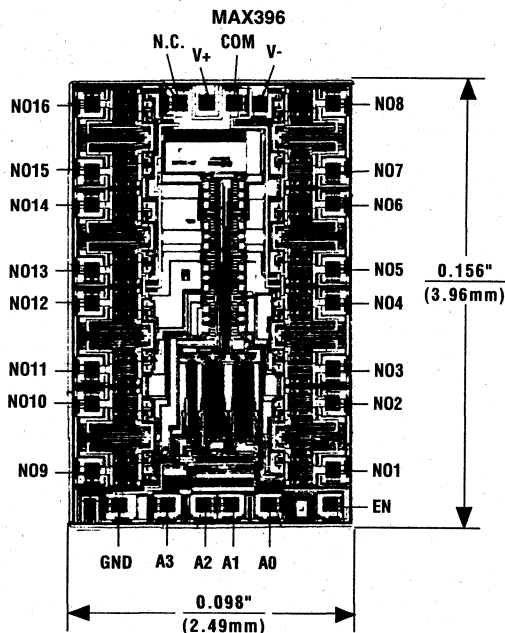
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX396EPI	-40°C to +85°C	28 Plastic DIP
MAX396EWI	-40°C to +85°C	28 Wide SO
MAX396EQI	-40°C to +85°C	28 PLCC**
MAX396MJI	-55°C to +125°C	28 CERDIP**
MAX397CPI	0°C to +70°C	28 Plastic DIP
MAX397CWI	0°C to +70°C	28 Wide SO
MAX397CAI	0°C to +70°C	28 SSOP
MAX397CQI	0°C to +70°C	28 PLCC**
MAX397C/D	0°C to +70°C	Dice*
MAX397EPI	-40°C to +85°C	28 Plastic DIP
MAX397EWI	-40°C to +85°C	28 Wide SO
MAX397EQI	-40°C to +85°C	28 PLCC**
MAX397MJI	-55°C to +125°C	28 CERDIP**

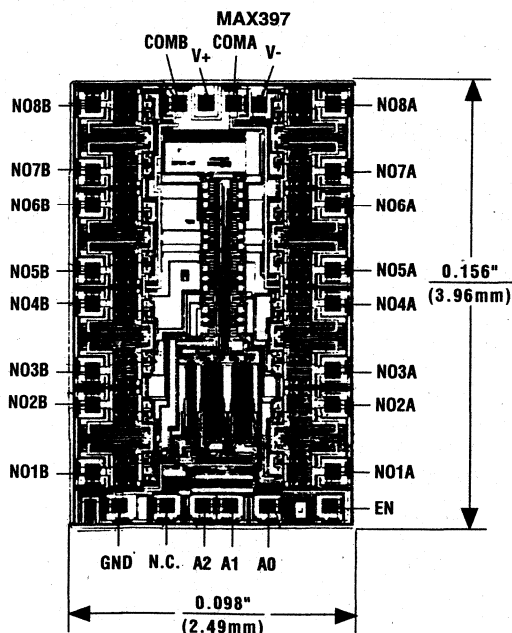
* Contact factory for dice specifications.

** Contact factory for package availability.

Chip Topographies



TRANSISTOR COUNT: 360
SUBSTRATE CONNECTED TO V+



TRANSISTOR COUNT: 360
SUBSTRATE CONNECTED TO V+



Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

General Description

The MAX398/MAX399 precision, monolithic, CMOS analog multiplexers (muxes) offer low on-resistance (less than 100 Ω), which is matched to within 4 Ω between channels and remains flat over the specified analog signal range (10 Ω max). They also offer low leakage over temperature (NO-off leakage current less than 2.5nA at +85°C) and fast switching speeds (transition time less than 250ns). The MAX398 is an 8-channel device, and the MAX399 is a dual 4-channel device.

The MAX398/MAX399 are fabricated with Maxim's low-voltage silicon-gate process. Design improvements yield extremely low charge injection (less than 5pC) and guarantee electrostatic discharge protection greater than 2000V.

These muxes operate with a single +3V to +15V supply or bipolar $\pm$ 3V to $\pm$ 8V supplies, while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. The MAX398/MAX399 are pin compatible with the industry-standard DG408, DG409, DG508A, and DG509A.

Applications

Sample-and-Hold Circuits
Automatic Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX
Audio Signal Routing
Low-Voltage Data Acquisition Systems

Features

- ◆ Pin Compatible with Industry-Standard DG408/DG409/DG508A/DG509A
- ◆ Guaranteed On-Resistance Match Between Channels (<4 Ω)
- ◆ Low On-Resistance (<100 Ω)
- ◆ Guaranteed Flat On-Resistance over Signal Range (<10 Ω)
- ◆ Guaranteed Low Charge Injection (<5pC)
- ◆ NO-Off Leakage Current <1nA at +85°C
- ◆ COM-Off Leakage Current <2.5nA at +85°C
- ◆ Electrostatic Discharge Protection >2000V
- ◆ Single-Supply Operation (+3V to +15V)
Bipolar-Supply Operation ($\pm$ 3V to $\pm$ 8V)
- ◆ Low Power Consumption (<300 μ W)
- ◆ Rail-to-Rail Signal Handling
- ◆ TTL/CMOS-Logic Compatible

Ordering Information

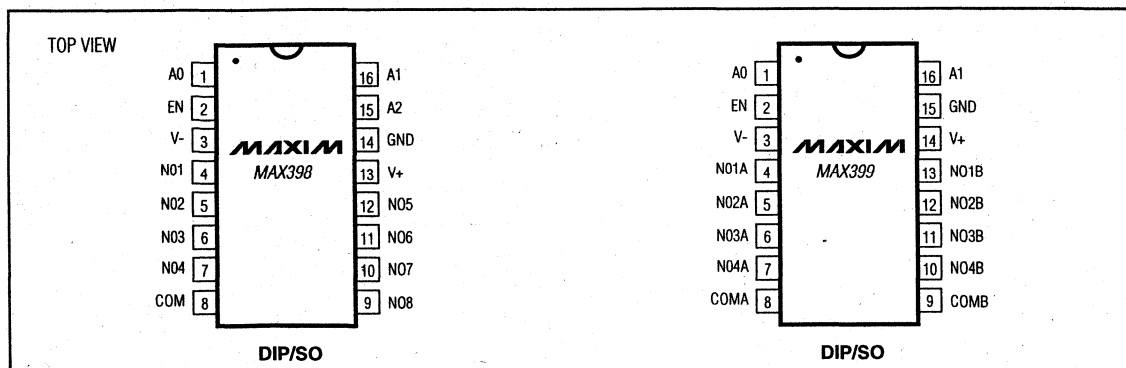
PART	TEMP. RANGE	PIN-PACKAGE
MAX398CPE	0°C to +70°C	16 Plastic DIP
MAX398CSE	0°C to +70°C	16 Narrow SO
MAX398C/D	0°C to +70°C	Dice*
MAX398EPE	-40°C to +85°C	16 Plastic DIP
MAX398ESE	-40°C to +85°C	16 Narrow SO
MAX398EJE	-40°C to +85°C	16 Cerdip**
MAX398MJE	-55°C to +125°C	16 Cerdip**

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

** Contact factory for package availability.

Pin Configurations



MAXIM

Maxim Integrated Products 1-99

Call toll free 1-800-998-8800 for free samples or literature.

MAX398/MAX399

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Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND

V+-0.3V to +17V

V-+0.3V to -17V

V+ to V--0.3V to +17V

Voltage into Any Terminal (Note 1).....(V- - 2V) to (V+ + 2V) or
30mA (whichever occurs first)

Current into Any Terminal30mA

Peak Current, Any Terminal
(pulsed at 1ms, 10% duty cycle max)40mA

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 7.5mW/°C above +70°C)470mW

Narrow SO (derate 8.7mW/°C above +70°C)696mW

CERDIP (derate 10.0mW/°C above +70°C)900mW

Operating Temperature Ranges

MAX39_C_0°C to +70°C

MAX39_E_-40°C to +85°C

MAX39_MJE-55°C to +125°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS	
SWITCH									
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)			V-		V+	V	
Channel On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V	T _A = +25°C		60		100	Ω	
			T _A = T _{MIN} to T _{MAX}				125		
R _{ON} Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = ±3.5V, V+ = 5V, V- = -5V	T _A = +25°C				4	Ω	
			T _A = T _{MIN} to T _{MAX}				6		
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	I _{NO} = 1mA, V _{COM} = ±3V, V+ = 5V, V- = -5V	T _A = +25°C				10	Ω	
			T _A = T _{MIN} to T _{MAX}				13		
NO-Off Leakage Current (Note 6)	I _{NO(OFF)}	V _{NO} = ±4.5V, V _{COM} = ±4.5V, V+ = 5.5V, V- = -5.5V	T _A = +25°C		-0.1		0.1	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-1.0		1.0		
				M	-10		10		
COM-Off Leakage Current (Note 6)	I _{COM(OFF)}	V _{COM} = ±4.5V, V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	MAX398	T _A = +25°C		-0.2		0.2	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-20		20	
		V _{COM} = ±4.5V, V _{NO} = ±4.5V, V+ = 5.5V, V- = -5.5V	MAX399	T _A = +25°C		-0.1		0.1	
				T _A = T _{MIN} to T _{MAX}	C, E	-1.5		1.5	
					M	-10		10	
COM-On Leakage Current (Note 6)	I _{COM(ON)}	V _{COM} = ±4.5V, V _{NO} = 4.5V,	MAX398	T _A = +25°C		-0.4		0.4	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-5		5	
					M	-40		40	
			MAX399	T _A = +25°C		-0.2		0.2	
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-20		20	

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, VAH = VENH = +2.4V, VAL = VENL = +0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
DIGITAL LOGIC INPUT								
Logic High Input Voltage	V _{AH} , V _{ENH}			T _A = T _{MIN} to T _{MAX}	2.4		V	
Logic Low Input Voltage	V _{AL} , V _{ENL}			T _A = T _{MIN} to T _{MAX}		0.8	V	
Input Current with Input Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V			-0.1	0.1	μA	
Input Current with Input Voltage Low	I _{AL} , I _{ENL}	V _A = V _{EN} = 0.8V			-0.1	0.1	μA	
SUPPLY								
Power-Supply Range					±3	±8	V	
Positive Supply Current	I ⁺	V _{EN} = V _A = 0V/V ⁺ , V ⁺ = 5.5V, V ⁻ = -5.5V		T _A = +25°C	-1	1	μA	
Negative Supply Current	I ⁻	V _{EN} = V _A = 0V/V ⁺ , V ⁺ = 5.5V, V ⁻ = -5.5V		T _A = T _{MIN} to T _{MAX}	-1	1	μA	
Ground Current	I _{GND}	V _{EN} = V _A = 0V/V ⁺ , V ⁺ = 5.5V, V ⁻ = -5.5V		T _A = +25°C	-1	1	μA	
				T _A = T _{MIN} to T _{MAX}	-1	1		
DYNAMIC								
Transition Time	t _{TRANS}	Figure 1				150	ns	
Break-Before-Make Interval	t _{OPEN}	Figure 2		T _A = +25°C	0	40	ns	
Enable Turn-On Time	t _{ON(EN)}	Figure 3		T _A = +25°C		60	150	
				T _A = T _{MIN} to T _{MAX}		250		
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3		T _A = +25°C		40	150	
				T _A = T _{MIN} to T _{MAX}		200		
Charge Injection (Note 3)	Q	C _L = 10nF, V _S = 0V, R _S = 0Ω		T _A = +25°C		2	5	pC
Off Isolation (Note 7)		V _{EN} = 0V, R _L = 1kΩ, f = 100kHz		T _A = +25°C		-75		dB
Crosstalk Between Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{p-p} , R _L = 1kΩ		T _A = +25°C		-92		dB
Logic Input Capacitance	C _{IN}	f = 1MHz		T _A = +25°C		8		pF
NO-Off Capacitance	C _{NO(OFF)}	f = 1MHz, V _{EN} = V _D = 0V		T _A = +25°C		11		pF
COM-Off Capacitance	C _{COM(OFF)}	f = 1MHz, V _{EN} = V _D = 0V	MAX398	T _A = +25°C		40		pF
			MAX399			20		
COM-On Capacitance	C _{COM(ON)}	f = 1MHz, V _{EN} = V _D = 0V	MAX398	T _A = +25°C		54		pF
			MAX399			34		

MAX398/MAX399

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Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single 5V

($V_+ = 5V \pm 10\%$, $V_- = 0V$, $GND = 0V$, $V_{AH} = V_{ENH} = +2.4V$, $V_{AL} = V_{ENL} = +0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V _{COM} , V _{NO}	(Note 3)				V ₋		V ₊	V
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V ₊ = 4.5V	T _A = +25°C		150		225	Ω	
			T _A = T _{MIN} to T _{MAX}				280		
R _{ON} Matching Between Channels (Note 4)	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V ₊ = 4.5V	T _A = +25°C				10	Ω	
			T _A = T _{MIN} to T _{MAX}				12		
On-Resistance Flatness	R _{FLAT}	I _{NO} = 1mA; V _{COM} = 3V, 2V, 1V; V ₊ = 5V	T _A = +25°C				10	Ω	
			T _A = T _{MIN} to T _{MAX}				15		
NO-Off Leakage Current (Note 8)	I _{NO(OFF)}	V _{NO} = 4.5V, V _{COM} = 0V, V ₊ = 5.5V	T _A = +25°C		-0.1		0.1	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-1.0		1.0		
				M	-10		10		
COM-Off Leakage Current (Note 8)	I _{COM(OFF)}	V _{COM} = 4.5V, V _{NO} = 0V, V ₊ = 5.5V	MAX398	T _A = +25°C		-0.2		0.2	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-20		20	
		V _{COM} = 4.5V, V _{NO} = 0V, V ₊ = 5.5V	MAX399	T _A = +25°C		-0.2		0.2	
				T _A = T _{MIN} to T _{MAX}	C, E	-1.5		1.5	
					M	-10		10	
COM-On Leakage Current (Note 8)	I _{COM(ON)}	V _{COM} = 4.5V, V _{NO} = 4.5V, V ₊ = 5.5V	MAX398	T _A = +25°C		-0.4		0.4	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-5		5	
					M	-40		40	
			MAX399	T _A = +25°C		-0.2		0.2	
				T _A = T _{MIN} to T _{MAX}	C, E	-2.5		2.5	
					M	-20		20	
DIGITAL LOGIC INPUT									
Logic High Input Voltage	V _{AH} , V _{ENH}				T _A = T _{MIN} to T _{MAX}	2.4			V
Logic Low Input Voltage	V _{AL} , V _{ENL}				T _A = T _{MIN} to T _{MAX}			0.8	V
Input Current with Input Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V				-0.1		0.1	μA
Input Current with Input Voltage Low	I _{AL} , I _{ENL}	V _A = 0V V _{EN} = 0.8V				-0.1		0.1	μA
SUPPLY									
Power-Supply Range						3		15	V
Positive Supply Current	I ₊	V _{EN} = V _A = 0V, V ₊ ; V ₊ = 5.5V; V ₋ = 0V				-1.0		1.0	μA
Negative Supply Current	I ₋	V _{EN} = V _A = 0V, V ₊ ; V ₊ = 5.5V; V ₋ = 0V				-1.0		1.0	μA
I _{GND} Supply Current	I _{GND}	V _{EN} = V ₊ , 0V; V _A = 0V; V ₊ = 5.5V; V ₋ = 0V		T _A = +25°C		-1.0		1.0	μA
				T _A = T _{MIN} to T _{MAX}		-1.0		1.0	

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

MAX398/MAX399

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ELECTRICAL CHARACTERISTICS—Single 5V (continued)

(V+ = 5V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC						
Transition Time	t _{TRANS}	V _{NO} = 3V		90	245	ns
Break-Before-Make Interval	t _{OPEN}	T _A = +25°C	10	40		ns
Enable Turn-On Time	t _{ON(EN)}	T _A = +25°C		90	200	ns
		T _A = T _{MIN} to T _{MAX}			275	
Enable Turn-Off Time	t _{OFF(EN)}	T _A = +25°C		50	125	ns
		T _A = T _{MIN} to T _{MAX}			200	
Charge Injection (Note 3)	Q	C _L = 10nF, V _S = 0V, R _S = 0Ω		1.5	5	pC

ELECTRICAL CHARACTERISTICS—Single 3V

(V+ = 3V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = +2.4V, V_{AL} = V_{ENL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V _{ANALOG}	(Note 3)		V-		V+	V
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 1.5V, V+ = 3V	T _A = +25°C	230	375	Ω	
			T _A = T _{MIN} to T _{MAX}		425		
DYNAMIC							
Transition Time (Note 3)	t _{TRANS}	Figure 1, V _{IN} = 2.4V, V _{NO1} = 1.5V, V _{NO8} = 0V	T _A = +25°C	230	575	ns	
Enable Turn-On Time (Note 3)	t _{ON(EN)}	Figure 3, V _{INH} = 2.4V, V _{INL} = 0V, V _{NO1} = 1.5V	T _A = +25°C	200	500	ns	
Enable Turn-Off Time (Note 3)	t _{OFF(EN)}	Figure 3, V _{INH} = 2.4V, V _{INL} = 0V, V _{NO1} = 1.5V	T _A = +25°C	75	400	ns	
Charge Injection (Note 3)	Q	C _L = 10nF, V _S = 0V, R _S = 0Ω	T _A = +25°C	1	5	pC	

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔR_{ON} = R_{ONMAX} - R_{ONMIN}.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges, i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 6: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.

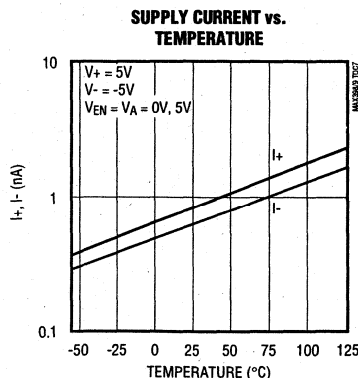
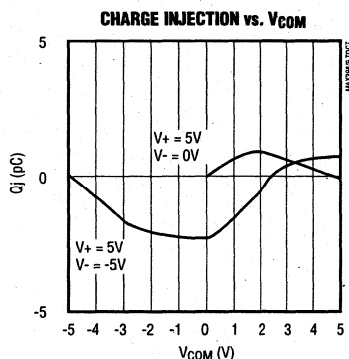
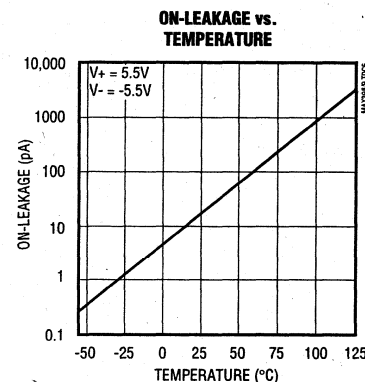
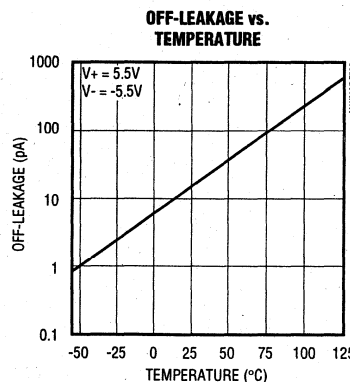
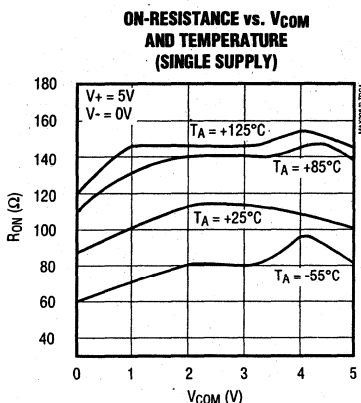
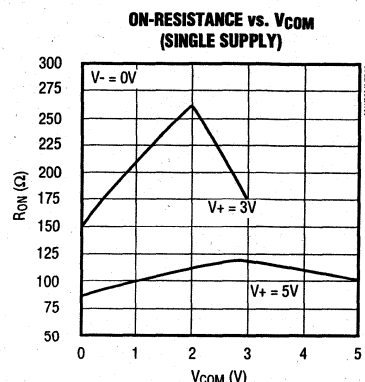
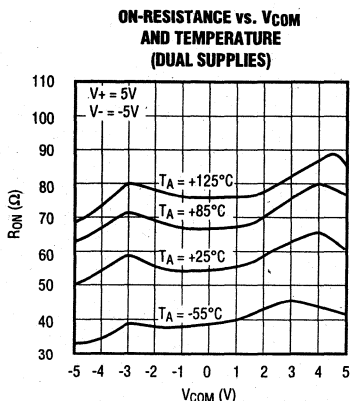
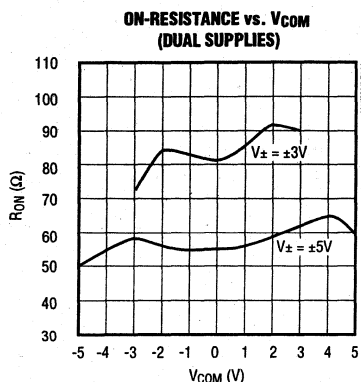
Note 7: Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM}/V_{NO}. V_{COM} = output, V_{NO} = input to off switch.

Note 8: Leakage testing at single supply is guaranteed by correlation testing with dual supplies.

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Pin Description

PIN		NAME	FUNCTION
MAX398	MAX399		
1, 15, 16	—	A0, A2, A1	Address Inputs
—	1, 16	A0, A1	Address Inputs
2	2	EN	Enable Input, connect to V+ if not used
3	3	V-	Negative Supply Voltage Input
4-7	—	NO1-NO4	Analog Inputs—bidirectional
—	4-7	NO1A-NO4A	Analog Inputs—bidirectional
8	—	COM	Analog Output—bidirectional
—	8, 9	COMA, COMB	Analog Outputs—bidirectional
9-12	—	NO8-NO5	Analog Inputs—bidirectional
—	10-13	NO4B-NO1B	Analog Inputs—bidirectional
13	14	V+	Positive Supply Voltage Input
14	15	GND	Ground

MAX398/MAX399

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Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Applications Information

Operation with Supply Voltages Other than $\pm 5V$

Using supply voltages less than $\pm 5V$ reduces the analog signal range. The MAX398/MAX399 muxes operate with $\pm 3V$ to $\pm 8V$ bipolar supplies or with a $+3V$ to $+15V$ single supply. Connect V_- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies, such as $+10V$ and $-5V$. The *Typical Operating Characteristics* graphs show typical on-resistance with $\pm 3V$, $\pm 5V$, $+3V$ and $+5V$ supplies. (Switching times increase by a factor of two or more for operation at $5V$.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, then V_- , followed by the logic inputs, NO, or COM. If power-supply sequencing is not possible, add two small signal diodes ($D1$, $D2$) in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to one diode drop below V_+ and one diode drop

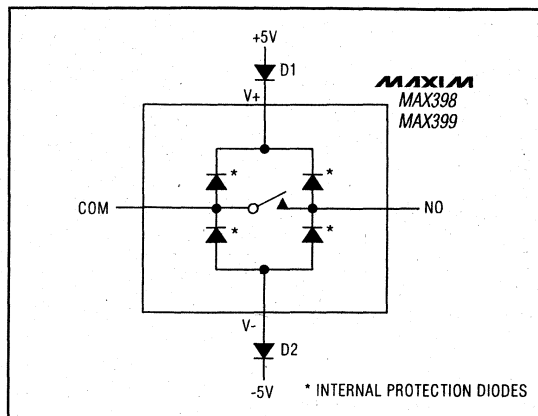


Figure 1. Overvoltage Protection Using External Blocking Diodes

above V_- , but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V_+ and V_- should not exceed $17V$. These protection diodes are not recommended when using a single supply.

Test Circuits/Timing Diagrams

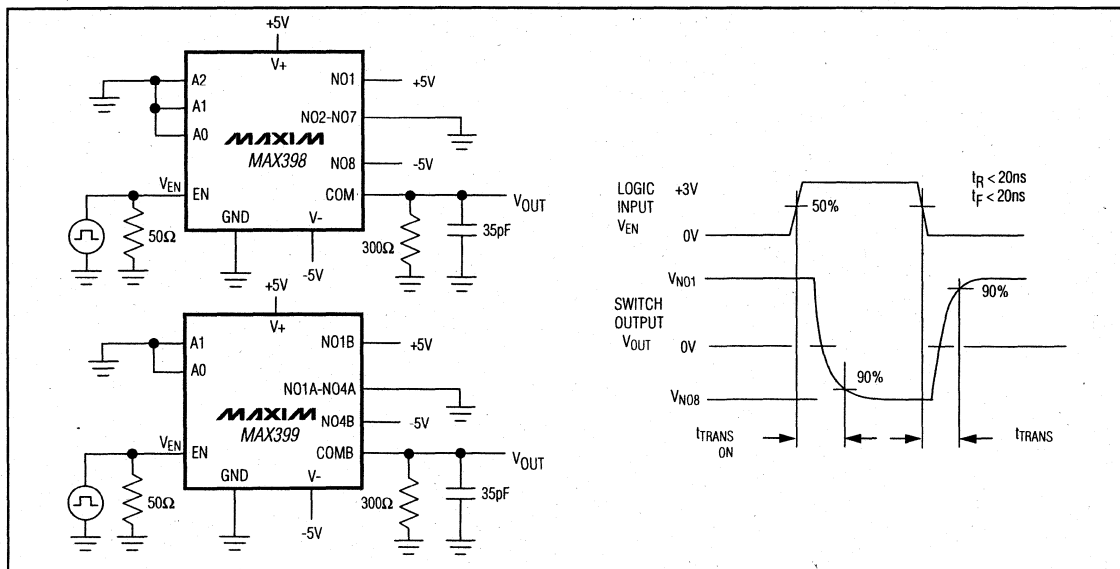


Figure 2. Transition Time

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

MAX398/MAX399

1

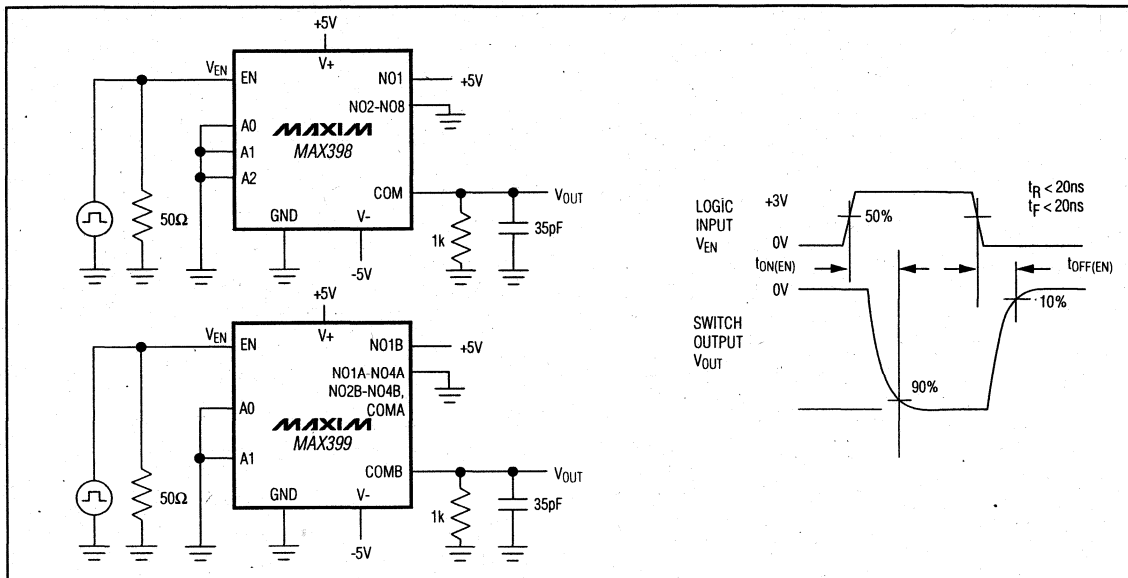


Figure 3. Enable Switching Time

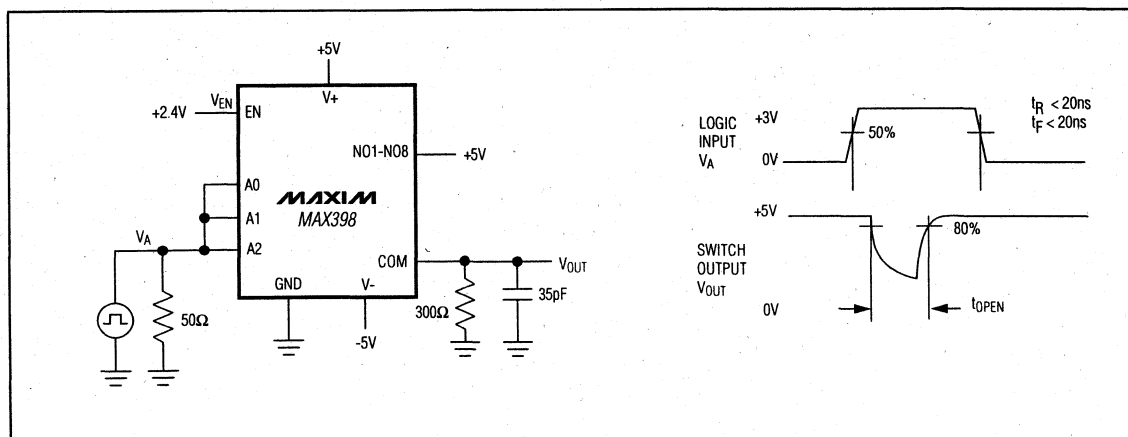


Figure 4. Break-Before-Make Interval

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

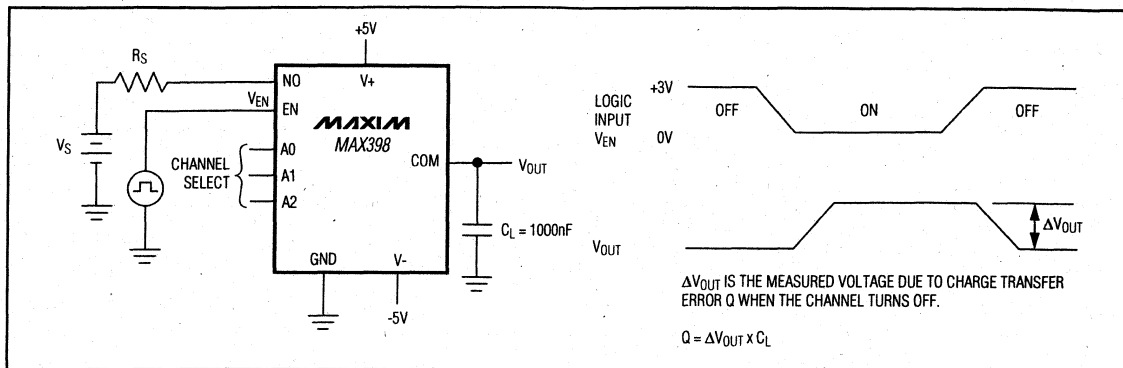


Figure 5. Charge Injection

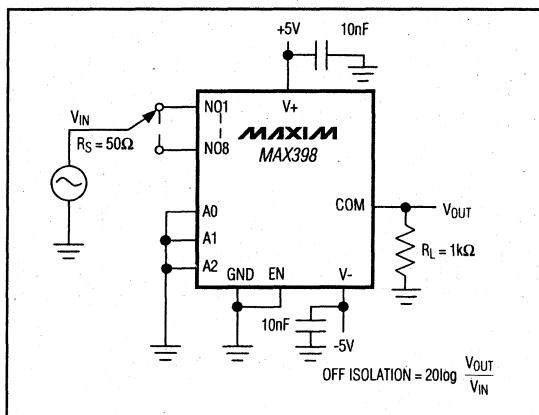


Figure 6. Off Isolation

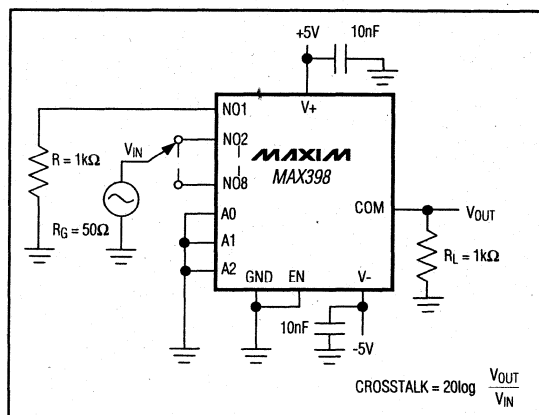


Figure 7. Crosstalk

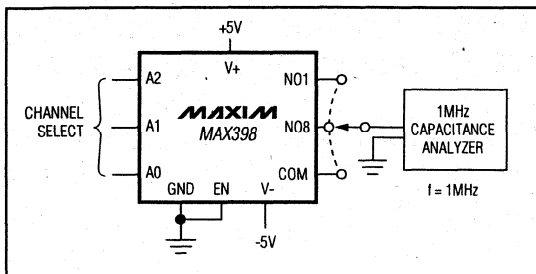


Figure 8. NO/COM Capacitance

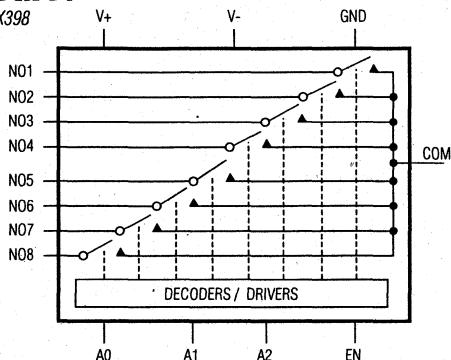
Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Functional Diagrams/Truth Tables

MAX398/MAX399

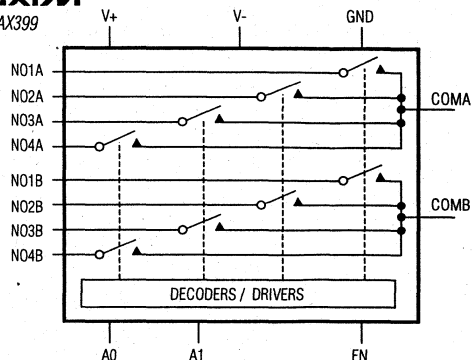
1

MAXIM
MAX398



MAX398				
A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

MAXIM
MAX399



MAX399			
A1	A0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

LOGIC "0" $V_{AL} \leq +0.8$ V, LOGIC "1" $V_{AH} \geq +2.4$ V

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Ordering Information (continued)

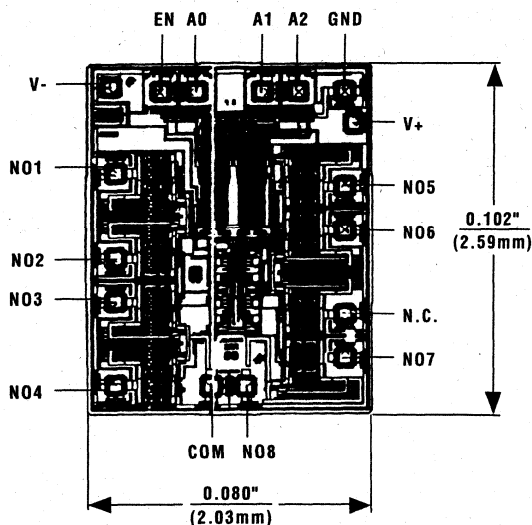
PART	TEMP. RANGE	PIN-PACKAGE
MAX399CPE	0°C to +70°C	16 Plastic DIP
MAX399CSE	0°C to +70°C	16 Narrow SO
MAX399C/D	0°C to +70°C	Dice*
MAX399EPE	-40°C to +85°C	16 Plastic DIP
MAX399ESE	-40°C to +85°C	16 Narrow SO
MAX399EJE	-40°C to +85°C	16 CERDIP**
MAX399MJE	-55°C to +125°C	16 CERDIP**

* Contact factory for dice specifications.

** Contact factory for package availability.

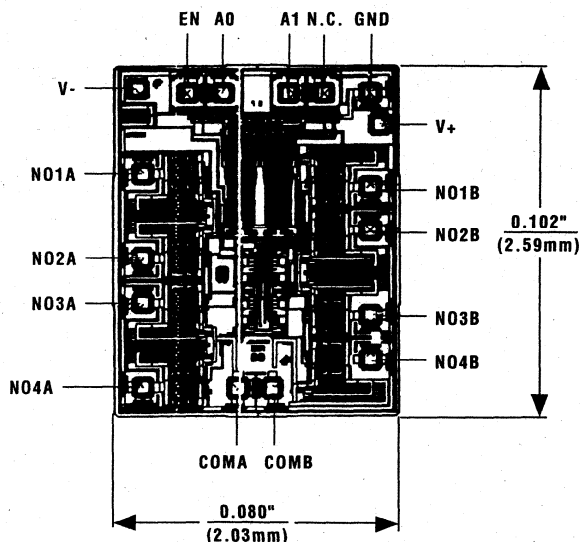
Chip Topographies

MAX398



TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+

MAX399



TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+



Interface Products

Interface Products, Product Tables and Trees	2-2
MAX1482 20 μ A, 1/8-Unit-Load, Slew-Rate-Limited, Full-Duplex RS-485 Transceiver	2-7
MAX1483 20 μ A, 1/8-Unit-Load, Slew-Rate-Limited, Half-Duplex RS-485 Transceiver	2-7
MAX1487E 2.5Mbps, $\pm$ 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**	2-19
MAX1488E $\pm$ 15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver*	2-31
MAX1489E $\pm$ 15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver*	2-33
MAX203E $\pm$ 15kV ESD-Protected, Complete, 5V, Dual RS-232 Transceiver*	2-35
MAX3212 1 μ A, 2.7V to 3.6V, 3-Driver/5-Receiver, True RS-232 Transceiver	2-37
MAX3218 1 μ A, 1.8V to 4.25V RS-232 Transceiver w/ AutoShutdown™	2-49
MAX3222 300 μ A, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1 μ F Capacitors	2-61
MAX3223 1 μ A, 3V to 5.5V, True RS-232 Transceiver w/ AutoShutdown™	2-73
MAX3232 300 μ A, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1 μ F Capacitors	2-61
MAX3241 300 μ A, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1 μ F Capacitors	2-61
MAX3243 1 μ A, 3V to 5.5V, True RS-232 Transceiver w/ AutoShutdown™	2-73
MAX3483 3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver	2-87
MAX3485 3.3V, 10Mbps, True RS-485/RS-422 Transceiver	2-87
MAX3486 3.3V, 2.5Mbps, True RS-485/RS-422 Transceiver	2-87
MAX3488 3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver	2-87
MAX3490 3.3V, 10Mbps, True RS-485/RS-422 Transceiver	2-87
MAX3491 3.3V, 10Mbps, True RS-485/RS-422 Transceiver	2-87
MAX481E 2.5Mbps, $\pm$ 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**	2-19
MAX483E 250kbps, $\pm$ 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver w/ Shutdown**	2-19
MAX485E 2.5Mbps, $\pm$ 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**	2-19
MAX487E 250kbps, $\pm$ 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver w/ 1/4-Unit Load**	2-19
MAX488E 250kbps, $\pm$ 15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver**	2-19
MAX489E 250kbps, $\pm$ 15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver**	2-19
MAX490E 2.5Mbps, $\pm$ 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver**	2-19
MAX491E 2.5Mbps, $\pm$ 15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver	2-19

*Advance Information—first page of data sheet in preparation.

**Future Product.

LINE DRIVERS/RECEIVERS

AppleTalk™

MAX216 (1 single-ended driver/2 single-ended receivers,
1 differential driver/1 differential receiver)

RS-232

see next page for
RS-485/RS-422

+3V POWERED

4 DRIVERS, 5 RCVRs

MAX560
(2 receivers active in shutdown)
MAX561 (shutdown)

3 DRIVERS, 5 RCVRs

★ MAX212
(true RS-232, 3mA ICC max)
★ MAX241
(true RS-232, 0.1µF caps,
1mA ICC max)
MAX562
(2.7V to 5.25V operation)

2 DRIVERS, 2 RCVRs

MAX218
(1.8V to 4.25V VCC in,
true RS-232 out)
★ MAX222
(true RS-232, 0.1µF caps,
2 receivers active
in shutdown)
★ MAX232
(true RS-232, 0.1µF caps)

MAX563
(120kbps data rate,
2 receivers active
in shutdown)

1µA SUPPLY CURRENT

★ MAX3212
(3Tx, 5Rx, 2.7V to 3.6V operation)
★ MAX3218
(2Tx, 2Rx, 1.8V to 4.25V operation)
★ MAX3223
(2Tx, 2Rx, 3.0V to 5.5V operation,
0.1µF caps)
★ MAX3243
(3Tx, 5Rx, 3.0V to 5.5V operation,
0.1µF caps)

+5V, 4 EXT. CAPS

2 DRIVERS, 2 RCVRs

MAX202 (0.1µF caps, low cost)
MAX220 (ultra-low power)
MAX222 (I_Q = 10µA in shutdown)
MAX232 (industry standard)
MAX232A (116kbps/sec data rate, 0.1µF caps)
MAX242 (receivers active in shutdown)
MAX243 (simplified cabling)

COMPLETE PC SERIAL PORTS

MAX211 (pin compatible with MAX241, 0.1µF caps)
MAX213 (2 receivers active in shutdown, 0.1µF caps)
MAX214 (programmable DTE/DCE port)
MAX223 (2 receivers active in shutdown)
MAX241 (industry standard)

HIGH DRIVER/RCVR COUNT

MAX200 (5 drivers, 0 receivers, 0.1µF caps)
MAX204 (4 drivers, 0 receivers, 0.1µF caps)
MAX206 (4 drivers, 3 receivers, 0.1µF caps)
MAX207 (5 drivers, 3 receivers, 0.1µF caps)
MAX208 (4 drivers, 4 receivers, 0.1µF caps)
MAX230 (5 drivers, 0 receivers)
MAX234 (4 drivers, 0 receivers)
MAX236 (4 drivers, 3 receivers)
MAX237 (5 drivers, 3 receivers)
MAX238 (4 drivers, 4 receivers)
MAX240 (5 drivers, 5 receivers)
MAX244 (8 drivers, 10 receivers)
MAX248 (8 drivers, 8 receivers)
MAX249 (8 drivers, 10 receivers)

+5V, INTERNAL CAPS

2 DRIVERS, 2 RCVRs

MAX203 (available in SO)
MAX233
MAX233A (116kbps/sec)

HIGH DRIVER/RCVR COUNT

MAX205 (5 drivers, 5 receivers)
MAX225 (5 drivers, 5 receivers, SO package)
MAX235 (5 drivers, 5 receivers)
MAX245 (8 drivers, 10 receivers)
MAX246 (8 drivers, 10 receivers)
MAX247 (8 drivers, 9 receivers)

+5V/+12V OR BATTERY POWER, 2 EXT. CAPS

2 DRIVERS, 2 RCVRs

MAX201 (0.1µF caps)
MAX231

±15kV ESD PROTECTION

★ MAX1488E (±15kV ESD per human body model & IEC 801-2)
★ MAX1489E (±15kV ESD per human body model & IEC 801-2)

+5V

MAX202E (2Tx/2Rx, ±15kV ESD per human body model & IEC 801-2)
★ MAX203E (2Tx/2Rx, ±15kV ESD per human body model & IEC 801-2, no external caps)
MAX211E (4Tx/5Rx, ±15kV ESD per human body model & IEC 801-2)
MAX213E (4Tx/5Rx, ±15kV ESD per human body model & IEC 801-2)
MAX232E (2Tx/2Rx, ±15kV ESD per human body model & IEC 801-2)
MAX241E (4Tx/5Rx, ±15kV ESD per human body model & IEC 801-2)

ISOLATION PRODUCTS

2-CHIP SET

MAX250
MAX251

COMPLETE MODULE

MAX252A (UL recognized)
MAX252B (500V isolation)

COMPLETE PC SERIAL PORTS

MAX209
(3 drivers, 5 receivers, 0.1µF caps)
MAX239
(3 drivers, 5 receivers)

★ New product

† Future Product

☆ Evaluation kit available

AppleTalk is a trademark of Apple Computer, Inc.

LINE DRIVERS/RECEIVERS

see previous page for
RS-232/AppleTalk™

RS-485/RS-422

+5V-POWERED

+3V-POWERED

ESD PROTECTION

1 DRIVER, 1 RCVR
FULL DUPLEX

1 DRIVER, 1 RCVR
1/2 DUPLEX

ISOLATION
PRODUCTS

1 DRIVER, 1 RCVR
FULL DUPLEX

1 DRIVER, 1 RCVR
1/2 DUPLEX

† MAX1487E
(MAX485E plus 1/4-unit load)

† MAX481E
(1µA shutdown, half duplex)

† MAX483E
(250kbps, reduces EMI by 100x)

† MAX485E
(industry standard with ±15kV ESD)

† MAX487E
(MAX483E plus 1/4-unit load)

† MAX488E
(250kbps, reduces EMI by 100x)

† MAX489E
(MAX488E plus driver/receiver enable)

† MAX490E
(2.5Mbps)

★ MAX491E
(MAX490E plus driver/receiver enable)

★ MAX1482
(250kbps, 256 transceivers on the bus)

MAX488
(250kbps, reduces EMI by 100x)

MAX489
(MAX488 plus driver/receiver enables)

MAX490
(direct LTC490 replacement)

MAX491
(direct LTC491 replacement)

★ MAX1483
(250kbps, 256 transceivers on the bus)

MAX1487
(2.5Mbps, 128 transceivers on the bus)

MAX481
(MAX485 plus 1µA shutdown)

MAX483
(250kbps, reduces EMI by 100x)

MAX485
(direct LTC485 replacement)

MAX487
(MAX483 plus 1/4-unit load)

MAX1480A
(complete 2.5Mbps isolated RS-485 in one package)

MAX1480B
(complete 250kbps isolated RS-485 in one package)

MAX4253
(isolated power for MAX488x family)

★ MAX3488
(250kbps, reduces EMI by 100x)

★ MAX3490
(10Mbps, 8-pin package)

★ MAX3491
(10Mbps, driver/receiver enables)

★ MAX3483
(250kbps, reduces EMI by 100x)

★ MAX3485
(10Mbps guaranteed data rate)

★ MAX3486
(2.5Mbps guaranteed data rate)

★ New product
† Future product

Interface Products

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
+3V RS-232 PRODUCTS										
MAX212	+3 to +3.6	3/5	1.5	2	0.33/0.68	Yes	✓	Yes	250	5 receivers active in shutdown, I _{CC} = 1.5mA, chip inductor
MAX218	+1.8 to +4.25	2/2	1.9	2	0.33/0.68	Yes	✓	Yes	250	True RS-232 performance from 1.8V to 4.25V input
MAX3212	+2.7 to +3.6	3/5	1µA	2	0.33/0.68	Yes	✓	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3218	+1.8 to +4.25	2/2	1µA	2	0.33/0.68	Yes	✓	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3222	+3 to +5.5	2/2	300µA	4	0.1	Yes	✓	Yes	230	2 receivers active in shutdown, 0.5mA I _{CC} , true RS-232
MAX3223	+3 to +5.5	2/2	1µA	4	0.1	Yes	✓	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3232	+3 to +5.5	2/2	300µA	4	0.1	No	✓	Yes	230	Industry-standard MAX232 pinout, true RS-232
MAX3241	+3 to +5.5	3/5	300µA	4	0.1	Yes	✓	Yes	230	Mouse driveability, 2 spare receivers active in shutdown, true RS-232
MAX3243	+3 to +5.5	3/5	1µA	4	0.1	Yes	✓	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX560	+3 to +3.6	4/5	5	4	1	Yes	✓	No	120	+3V, MAX561 with receivers active in shutdown
MAX561	+3 to +3.6	4/5	5	4	1	Yes	✓	No	120	+3V, complete IBM PC serial port
MAX562	+2.7 to +5.25	3/5	20	5	0.33/0.68	Yes	✓	No	250	+2.7V to +5.25V operation, 230kbps guaranteed data rate
MAX563	+3 to +3.6	2/2	4	4	0.1	Yes	✓	No	200	2 receivers active in shutdown
+5V RS-232 PRODUCTS										
MAX214	+5	3/5	9	4	1	Yes		Yes	120	Programmable DTE/DCE port
MAX220	+5	2/2	500µA	4	4.7/10	No		Yes	22	Ultra-low power, industry-standard pinout
MAX222	+5	2/2	4	4	0.1	Yes		Yes	200	+5V IBM PC serial port with receivers active in shutdown
MAX223(MAX213)	+5	4/5	7	4	1(0.1)	Yes	✓	Yes	120	MAX241 + receivers active in shutdown
MAX225	+5	5/5	11	0	-	Yes		Yes	120	Available in 28-pin SO package
MAX230(MAX200)	+5	5/0	7	4	1(0.1)	Yes		Yes	120	5 drivers with shutdown
MAX231(MAX201)	+5 and +7.5 to +13.2	2/2	400µA	2	1(0.1)	No		Yes	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232(MAX202)	+5	2/2	5	4	1(0.1)	No		Yes	120(64)	Industry standard
MAX232A	+5	2/2	4	4	0.1	No		Yes	200	High slow rate, small caps, guaranteed 120kbps data rate
MAX233(MAX203)	+5	2/2	5	0	-	No		Yes	120	No external caps, MAX203 available in SOIC
MAX233A	+5	2/2	4	0	-	No		Yes	200	No external caps, high slow rate
MAX234(MAX204)	+5	4/0	7	4	1(0.1)	No		Yes	120	Replaces 1488
MAX235(MAX205)	+5	5/5	7	0	-	Yes		Yes	120	No external caps
MAX236(MAX206)	+5	4/3	7	4	1(0.1)	Yes		Yes	120	Shutdown, three-state
MAX237(MAX207)	+5	5/3	7	4	1(0.1)	No		Yes	120	Complements IBM PC serial port
MAX238(MAX208)	+5	4/4	7	4	1(0.1)	No		Yes	120	Replaces 1488 and 1489
MAX239(MAX209)	+5 and +7.5 to +13.2	3/5	7	2	1(0.1)	No		Yes	120	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX240	+5	5/5	7	4	1	Yes		Yes	120	DIP or flatpack package
MAX241(MAX211)	+5	4/5	7	4	1(0.1)	Yes		Yes	120	Complete IBM PC serial port, industry standard
MAX242	+5	2/2	4	4	0.1	Yes	✓	Yes	200	Separate shutdown and enable
MAX243	+5	2/2	4	4	0.1	No		Yes	200	Open-line detection simplifies cabling
MAX244	+5	8/10	11	4	1	No		Yes	120	High slow rate
MAX245	+5	8/10	11	0	-	Yes	✓	Yes	120	High slow rate, int. caps, two shutdown modes
MAX246	+5	8/10	11	0	-	Yes	✓	Yes	120	High slow rate, int. caps, three shutdown modes
MAX247	+5	8/9	11	0	-	Yes	✓	Yes	120	High slow rate, int. caps, nine operating modes
MAX248	+5	8/8	11	4	1	Yes	✓	Yes	120	High slow rate, selective half-chip enables
MAX249	+5	6/10	11	4	1	Yes	✓	Yes	120	Available in quad flatpack package

Interface Products (continued)

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
RS-232 ISOLATION PRODUCTS										
MAX230	+5	2/2	100µA	—	—	Yes	—	Yes	120	Isolated RS-232 chip set
MAX251	+5	2/2	100µA	—	—	Yes	—	Yes	120	Isolated RS-232 chip set
MAX252A	+5	2/2	130	0	—	Yes	—	Yes	20	UL recognized, 1500V isolation
MAX252B	+5	2/2	130	0	—	Yes	—	Yes	20	Economical 500V isolation

Part Number	Data Rate (Mbps)	No. of RS-485 Drivers/Receivers	Supply Current (µA)	Shutdown Supply Current (µA)	Duplex	No. of Rx/Tx On Bus	Features
+5V RS-485/RS-422 PRODUCTS							
MAX1482	0.25	1/1	20	0.1	Full	256	250kbps, 256 transceivers on bus
MAX1483	0.25	1/1	20	0.1	Half	256	250kbps, 256 transceivers on bus
MAX1487	2.5	1/1	250	300	Half	128	2.5Mbps, 128 transceivers on bus
MAX481	2.5	1/1	500	1	Half	32	MAX485 + 1µA shutdown mode
MAX483	0.25	1/1	350	1	Half	32	Slow-rate limiting reduces EMI and reflections
MAX485	2.5	1/1	500	300	Half	32	Direct LTC485 replacement
MAX487	0.25	1/1	250	1	Half	128	MAX483 plus 1/4-unit load
MAX488	0.25	1/1	350	—	Full	32	Slow-rate limiting reduces EMI and reflections
MAX489	0.25	1/1	350	1	Full	32	MAX488 plus driver/receiver enable
MAX490	2.5	1/1	500	—	Full	32	Direct LTC490 replacement
MAX491	2.5	1/1	500	300	Full	32	Direct LTC491 replacement

Part Number	Data Rate (Mbps)	No. of RS-485 Drivers/Receivers	Supply Current (µA)	Shutdown Supply Current (µA)	Duplex	No. of Rx/Tx On Bus	Features
+3V (+3.0V to +3.6V) RS-485/RS-422 PRODUCTS							
MAX3483	0.25	1/1	1mA	1	Half	32	Slow-rate limiting reduces EMI and reflections
MAX3485	10	1/1	1mA	1	Half	32	Guaranteed 10Mbps data rate
MAX3486	2.5	1/1	1mA	1	Half	32	Guaranteed 2.5Mbps data rate
MAX3488	0.25	1/1	1mA	—	Full	32	Slow-rate limiting reduces EMI and reflections
MAX3490	10	1/1	1mA	—	Full	32	Guaranteed 10Mbps data rate
MAX3491	10	1/1	1mA	1	Full	32	MAX3490 plus driver/receiver enable

Part Number	Data Rate (Mbps)	No. of RS-485 Drivers/Receivers	ESD Voltage (kV)	Supply Current (µA)	Shutdown Supply Current (µA)	Duplex	No. of Rx/Tx On Bus	Features
HIGH ESD RS-485 PRODUCTS								
MAX1487E†	2.5	1/1	±15	250	300	Half	128	2.5Mbps, 128 transceivers on bus
MAX481E†	2.5	1/1	±15	500	1	Half	32	MAX485 + 1µA shutdown mode
MAX483E†	0.25	1/1	±15	350	1	Half	32	Slow-rate limiting reduces EMI and reflections
MAX485E†	2.5	1/1	±15	500	300	Half	32	Direct LTC485 replacement
MAX487E†	0.25	1/1	±15	250	—	Half	128	MAX483 plus 1/4-unit load
MAX488E†	0.25	1/1	±15	350	—	Full	32	Slow-rate limiting reduces EMI and reflections
MAX489E†	0.25	1/1	±15	350	1	Full	32	MAX488 plus driver/receiver enable
MAX490E†	2.5	1/1	±15	500	—	Full	32	Direct LTC490 replacement
MAX491E	2.5	1/1	±15	500	300	Full	32	Direct LTC491 replacement

† Future product—contact factory for pricing and availability. Specifications are preliminary.

Interface Products (continued)

Part Number	Power Supply (V)	Data Rate (Mbps)	No. of RS-485 Drivers/Receivers	Supply Current (mA)	Isolated Power (mW)	Isolation Voltage (V)	Shutdown Supply Current (μA)	Full Duplex	Features
RS-485 ISOLATION PRODUCTS									
MAX1480A	+5	2.5	1/1	10	-	1500	1	No	Complete isolated RS-485 in one package
MAX1480B	+5	0.25	1/1	10	-	1500	1	No	Complete isolated RS-485 in one package
MAX253	+5	-	-	5	750	-	1	-	Isolated power driver for RS-485

Part Number	Power Supply (V)	No. of Single-Ended Drivers/Receivers	No. of Differential Drivers/Receivers	Shutdown	Single-Ended Data Rate (kbps)	Differential Data Rate (Mbps)	Description
APPLETALK™ TRANSCIVER							
MAX216	±5	1/2	1/1	Yes	120	1	Complete AppleTalk™ interface

Part Number	Power Supply (V)	No. of RS-232 Drivers/Receivers	ESD Voltage (kV)	Ext. Caps	Shutdown & Three-State	Rx Active In Shutdown	Data Rate (kbps)	Features
HIGH ESD RS-232 PRODUCTS								
MAX1488E	+5, ±12	4/0	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX1489E	+5	0/4	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX202E	+5	2/2	±15	4 x 0.1μF			120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX203E	+5	2/2	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX211E	+5	4/5	±15	4 x 0.1μF	Yes		120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX213E	+5	4/5	±15	4 x 0.1μF	Yes	✓	120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX232E	+5	2/2	±15	4 x 1.0μF	Yes		120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX241E	+5	4/5	±15	4 x 1.0μF	Yes		120	±15kV ESD per human body model and ±15kV per IEC 801-2

MAXIM

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

General Description

The MAX1482 and MAX1483 are low-power transceivers for RS-485 and RS-422 communication. Both feature slew-rate-limited drivers that minimize EMI and reduce reflections caused by improperly terminated cables. Data rates are guaranteed up to 250kbps.

The MAX1482/MAX1483 draw only 20 μ A of supply current. Additionally, they have a low-current shutdown mode that consumes only 0.1 μ A. Both parts operate from a single +5V supply.

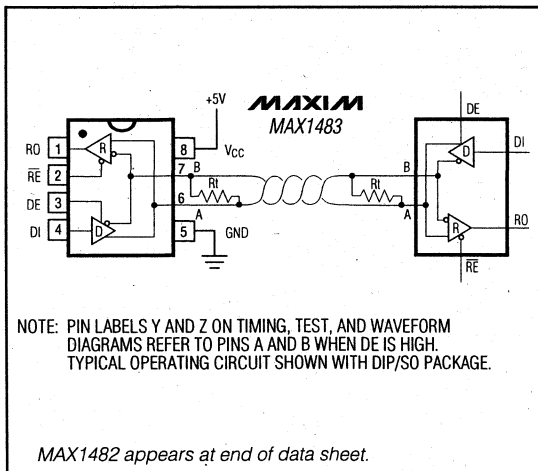
Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX1482 is full duplex and the MAX1483 is half duplex. Both parts have a 1/8-unit-load input impedance that guarantees up to 256 transceivers on the bus.

Applications

Low-Power RS-485/RS-422 Networks
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks
Large 256-Node LANs

Typical Operating Circuits



Features

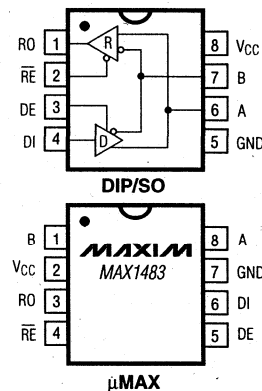
- ♦ Low 20 μ A Operating Current
- ♦ Slew-Rate Limited for Reduced EMI and Reduced Reflections
- ♦ 0.1 μ A Low-Current Shutdown Mode
- ♦ Designed for RS-485 and RS-422 Applications
- ♦ Operate from a Single +5V Supply
- ♦ -7V to +12V Common-Mode Input Voltage Range
- ♦ Allows up to 256 Transceivers on the Bus—Guaranteed (1/8-unit load)
- ♦ Current Limiting and Thermal Shutdown for Driver Overload Protection

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1482CPD	0°C to +70°C	14 Plastic DIP
MAX1482CSD	0°C to +70°C	14 SO
MAX1482EPD	-40°C to +85°C	14 Plastic DIP
MAX1482ESD	-40°C to +85°C	14 SO
MAX1483CPA	0°C to +70°C	8 Plastic DIP
MAX1483CSA	0°C to +70°C	8 SO
MAX1483CUA	0°C to +70°C	8 μ MAX
MAX1483EPA	-40°C to +85°C	8 Plastic DIP
MAX1483ESA	-40°C to +85°C	8 SO

Pin Configurations

TOP VIEW



MAX1482 appears at end of data sheet.

MAXIM

Maxim Integrated Products 2-7

Call toll free 1-800-998-8800 for free samples or literature.

MAX1482/MAX1483

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20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC})	7V	8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
Control Input Voltages ($\overline{RE}$, DE)	-0.5V to (V _{CC} + 0.5V)	14-Pin SO (derate 8.33mW/°C above +70°C)	667mW
Driver Input Voltage (DI)	-0.5V to (V _{CC} + 0.5V)	8-Pin μ MAX (derate 4.10mW/°C above +70°C)	330mW
Driver Output Voltages	-7.5V to 12.5V	Operating Temperature Ranges	
Receiver Input Voltages (A, B)	-7.5V to 12.5V	MAX148_C_	0°C to +70°C
Receiver Output Voltage (RO)	-0.5V to (V _{CC} + 0.5V)	MAX148_E_	-40°C to +85°C
Continuous Power Dissipation (T _A = +70°C)		Storage Temperature Range	-65°C to +160°C
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	727mW	Lead Temperature (soldering, 10sec)	+300°C
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)	800mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V $\pm$ 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V _{OD1}				5	V
Differential Driver Output (with load)	V _{OD2}	R = 50 Ω (RS-422), Figure 1	2		5	V
		R = 27 Ω (RS-485), Figure 1	1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	Δ V _{OD}	R = 27 Ω or 50 Ω , Figure 1			0.2	V
Driver Common-Mode Output Voltage	V _{OC}	R = 27 Ω or 50 Ω , Figure 1			3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	Δ V _{OC}	R = 27 Ω or 50 Ω , Figure 1			0.2	V
Three-State (high impedance) Output Current at Driver	I _{OZD}	MAX1482 only, -7V < V _Y and V _Z < 12V			$\pm$ 50	μ A
Logic Input High Voltage	V _{IH}	DE, DI, $\overline{RE}$	2.0			V
Logic Input Low Voltage	V _{IL}	DE, DI, $\overline{RE}$			0.8	V
Logic Input Current	I _{IN1}	DE, DI, $\overline{RE}$			$\pm$ 2	μ A
Input Current (A, B)	I _{IN2}	MAX1482, DE = 0V, V _{CC} = 0V or 5.25V	V _{IN} = 12V		150	μ A
			V _{IN} = -7V		-100	
		MAX1483, DE = 0V, V _{CC} = 0V or 5.25V	V _{IN} = 12V		200	
			V _{IN} = -7V		-150	
Receiver Differential Threshold Voltage	V _{TH}	-7V $\leq$ V _{CM} $\leq$ 12V	-0.2		0.2	V
Receiver Input Hysteresis	Δ V _{TH}	V _{CM} = 0V		75		mV
Receiver Output High Voltage	V _{OH}	I _O = -4mA, V _{ID} = 200mV	3.5			V
Receiver Output Low Voltage	V _{OL}	I _O = 4mA, V _{ID} = -200mV			0.4	V
Three-State (high impedance) Output Current at Receiver	I _{OZR}	0.4V $\leq$ V _O $\leq$ 2.4V			$\pm$ 1	μ A
Receiver Input Resistance	R _{IN}	-7V $\leq$ V _{CM} $\leq$ 12V	96			k Ω

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

MAX1482/MAX1483

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V $\pm$ 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
No-Load Supply Current	I _{CC}	MAX1482, RE = 0V or V _{CC}	DE = V _{CC}	25	45	μ A
			DE = 0V	20	35	
		MAX1483, RE = 0V or V _{CC}	DE = V _{CC}	55	85	
			DE = 0V	20	35	
Supply Current in Shutdown	I _{SHDN}	DE = 0V, RE = V _{CC}		0.1	10	μ A
Driver Short-Circuit Current	I _{OSD}	DI = high or low, -7V $\leq$ V _O $\leq$ 12V (Note 2)	35		250	mA
Receiver Short-Circuit Current	I _{OSR}	0V $\leq$ V _O $\leq$ V _{CC}	$\pm$ 7		$\pm$ 95	mA

SWITCHING CHARACTERISTICS

(V_{CC} = 5V $\pm$ 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t _{PLH}	Figures 3 and 5, R _{DIFF} = 54 Ω , C _{L1} = C _{L2} = 100pF			2	μ s
	t _{PHL}				2	
Driver Output Skew to Output	t _{SKEW}	Figures 3 and 5, R _{DIFF} = 54 Ω , C _{L1} = C _{L2} = 100pF			800	ns
Driver Rise or Fall Time	t _R , t _F	Figures 3 and 5, R _{DIFF} = 54 Ω , C _{L1} = C _{L2} = 100pF	0.25		2	μ s
Driver Enable to Output High	t _{ZH}	Figures 4 and 6, C _L = 100pF, S2 closed	0.2		2	μ s
Driver Enable to Output Low	t _{ZL}	Figures 4 and 6, C _L = 100pF, S1 closed	0.1		2	μ s
Driver Disable Time from Low	t _{LZ}	Figures 4 and 6, C _L = 15pF, S1 closed	0.3		3.0	μ s
Driver Disable Time from High	t _{HZ}	Figures 4 and 6, C _L = 15pF, S2 closed	0.3		3.0	μ s
Receiver Input to Output	t _{PLH} , t _{PHL}	Figures 3 and 7, R _{DIFF} = 54 Ω , C _{L1} = C _{L2} = 100pF	0.25		2.25	μ s
t _{PLH} - t _{PHL} Differential Receiver Skew	t _{SKD}	Figures 3 and 7, R _{DIFF} = 54 Ω , C _{L1} = C _{L2} = 100pF		160		ns
Receiver Enable to Output Low	t _{ZL}	Figures 2 and 8, C _R L = 15pF, S1 closed			90	ns
Receiver Enable to Output High	t _{ZH}	Figures 2 and 8, C _R L = 15pF, S2 closed			90	ns
Receiver Disable Time from Low	t _{LZ}	Figures 2 and 8, C _R L = 15pF, S1 closed			90	ns
Receiver Disable Time from High	t _{HZ}	Figures 2 and 8, C _R L = 15pF, S2 closed			90	ns
Maximum Data Rate	f _{MAX}		250			kbps
Time to Shutdown	t _{SHDN}	(Note 3)	50	200	600	ns
Driver Enable from Shutdown to Output High	t _{ZH} (SHDN)	Figures 4 and 6, C _L = 100pF, S2 closed			2	μ s
Driver Enable from Shutdown to Output Low	t _{ZL} (SHDN)	Figures 4 and 6, C _L = 100pF, S1 closed			2	μ s
Receiver Enable from Shutdown to Output High	t _{ZH} (SHDN)	Figures 2 and 8, C _L = 15pF, S2 closed, A - B = 2V			3	μ s
Receiver Enable from Shutdown to Output Low	t _{ZL} (SHDN)	Figures 2 and 8, C _L = 15pF, S1 closed, B - A = 2V			3	μ s

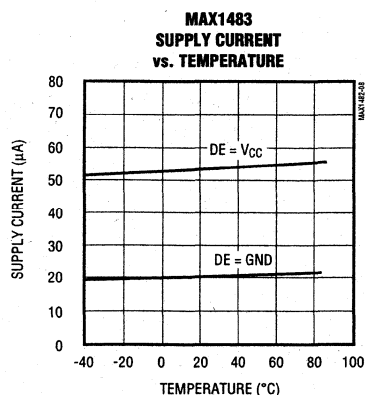
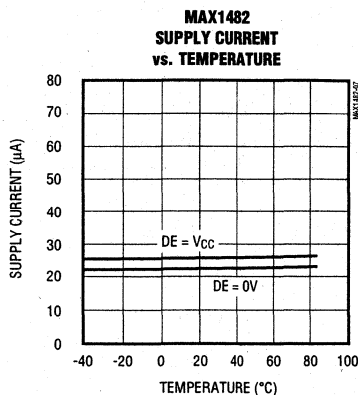
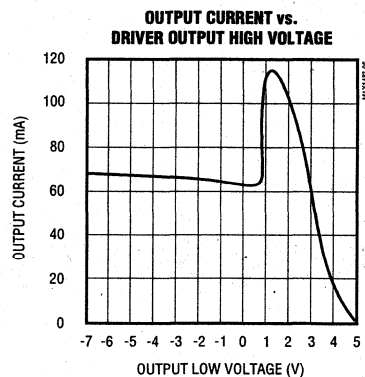
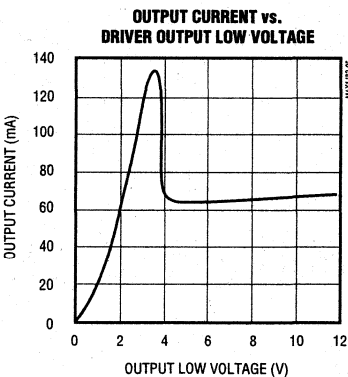
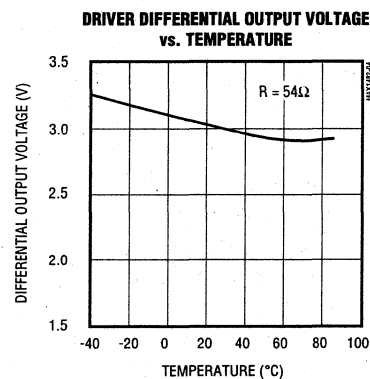
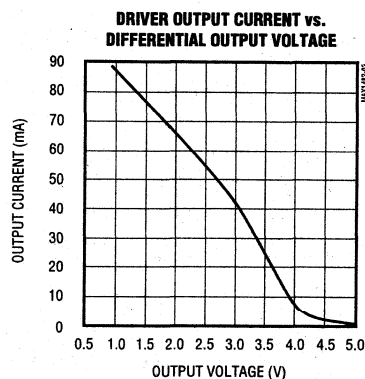
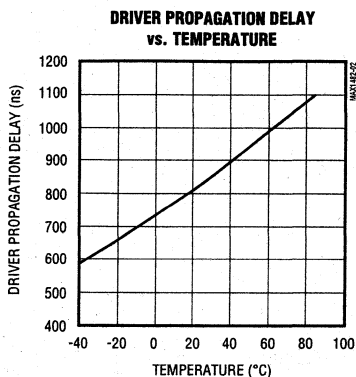
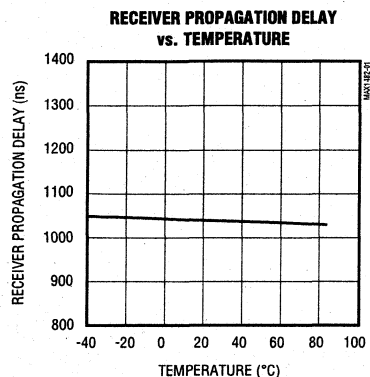
Note 2: Applies to peak current. See *Typical Operating Characteristics*.

Note 3: The MAX1482/MAX1483 are put into shutdown by bringing RE high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

Pin Description

PIN			NAME	FUNCTION
MAX1482	MAX1483			
DIP/SO	DIP/SO	μMAX		
2	1	3	RO	Receiver Output. With the receiver output enabled ($\overline{RE}$ low), RO is high if $A > B$ by 200mV or when A and B are not connected, and RO is low if $A < B$ by 200mV.
3	2	4	$\overline{RE}$	Receiver Output Enable. When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is high, RO is high impedance. If $\overline{RE}$ is high and DE is low, the MAX1482/MAX1483 enter a low-power (0.1μA) shutdown state.
4	3	5	DE	Driver Output Enable. The driver outputs, A and B, (Y and Z for the MAX1482) are enabled by bringing DE high. When DE is low, the driver outputs are high impedance, and the devices can function as line receivers if $\overline{RE}$ is low. If $\overline{RE}$ is high and DE is low, the parts will enter a low-power (0.1μA) shutdown state. If the driver outputs are enabled, the devices function as line drivers.
5	4	6	DI	Driver Input. With DE high, a low on DI forces output Y low and output Z high, and a high on DI forces output Y high and output Z low.
6, 7	5	7	GND	Ground
9	—	—	Y	Noninverting Driver Output
10	—	—	Z	Inverting Driver Output
—	6	8	A	Noninverting Receiver Input and Noninverting Driver Output
12	—	—	A	Noninverting Receiver Input
—	7	1	B	Inverting Receiver Input and Inverting Driver Output
11	—	—	B	Inverting Receiver Input
14	8	2	VCC	Positive Supply: 4.75V to 5.25V
1, 8, 13	—	—	N.C.	No Connect—not internally connected

MAX1482/MAX1483

2

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

Test Circuits

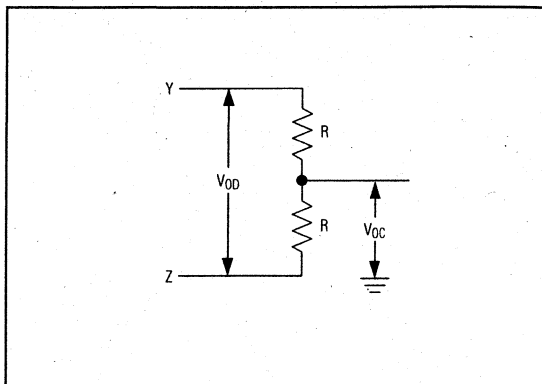


Figure 1. Driver DC Test Load

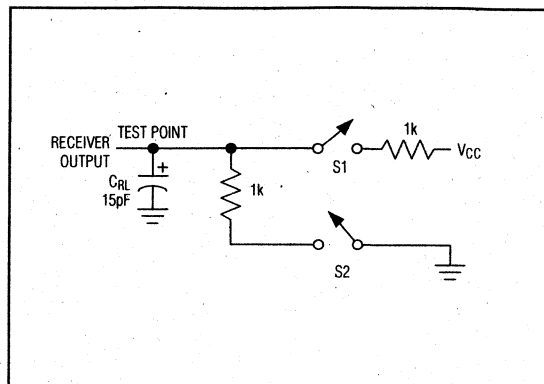


Figure 2. Receiver Timing Test Load

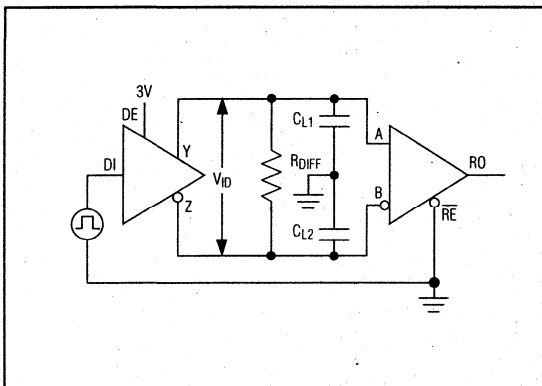


Figure 3. Driver/Receiver Timing Test Circuit

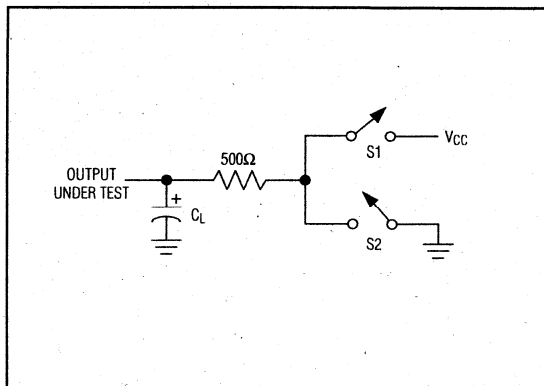


Figure 4. Driver Timing Test Load

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

Switching Waveforms

MAX1482/MAX1483

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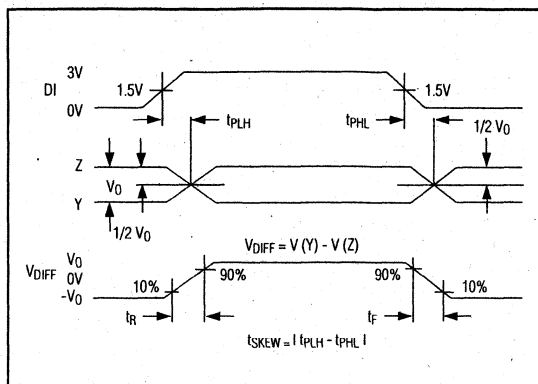


Figure 5. Driver Propagation Delays

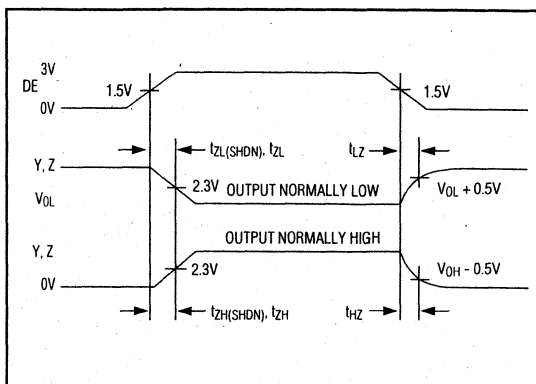


Figure 6. Driver Enable and Disable Times

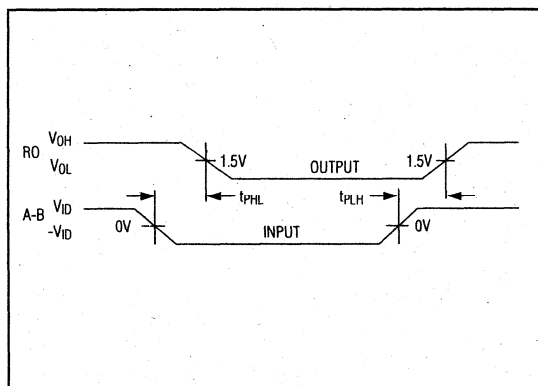


Figure 7. Receiver Propagation Delays

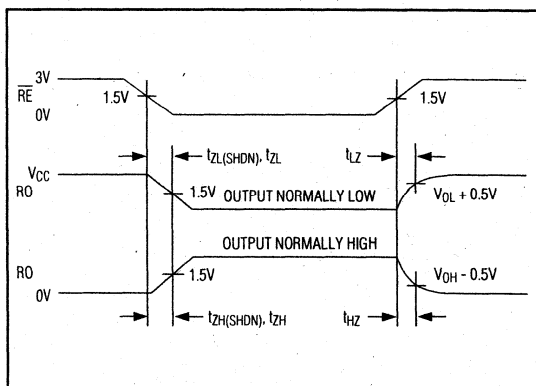


Figure 8. Receiver Enable and Disable Times

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

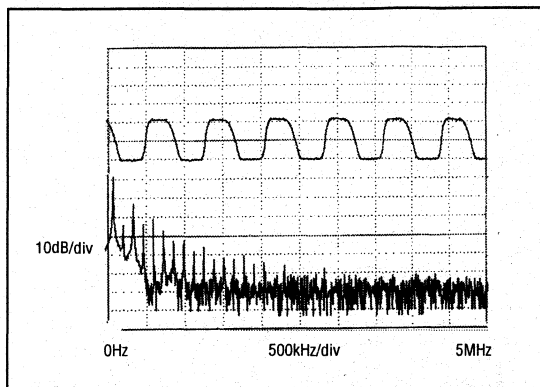


Figure 9. Driver Output Waveform and FFT, Transmitting 250kbps (125kHz) Signal

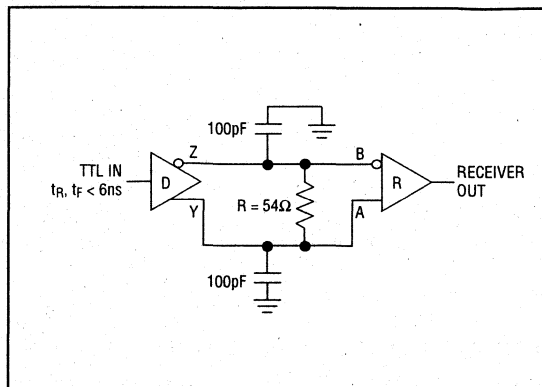


Figure 10. Receiver Propagation-Delay Test Circuit

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
X	0	X	High-Z	High-Z

X = Don't Care

High-Z = High Impedance

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE*	A-B	RO
0	0	$\geq +0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs open	1
1	0	X	High-Z

X = Don't Care

High-Z = High Impedance

* DE = 0 for MAX1483 and is a Don't Care for MAX1482.

Applications Information

The MAX1482/MAX1483 are low-power transceivers for RS-485 and RS-422 communications. The MAX1482 and MAX1483 are specified for data rates of at least 250kbps. The MAX1482 is a full-duplex transceiver while the MAX1483 is half duplex. When disabled, the driver and receiver outputs are high impedance.

The 96k Ω , 1/8-unit-load receiver input impedance of the MAX1482/MAX1483 allows up to 256 transceivers on a bus, compared to the 1-unit load (12k Ω input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX1482/MAX1483 and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus.

Reduced EMI and Reflections

The MAX1482/MAX1483 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 9 shows both the driver output waveform of a MAX1482/MAX1483 transmitting a 125kHz signal and the Fourier analysis of that signal.

High-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

MAX1482/MAX1483

2

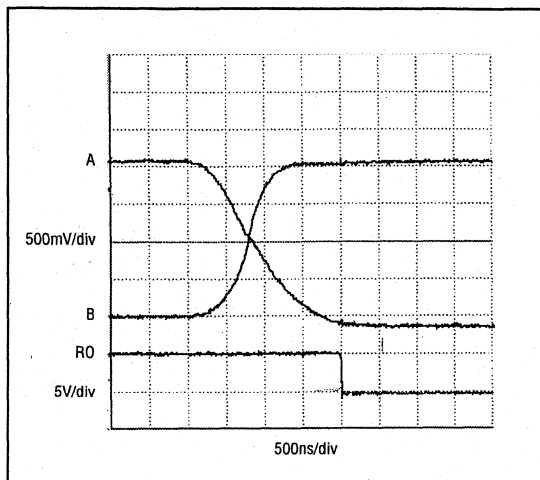


Figure 11. Receiver t_{PHL}

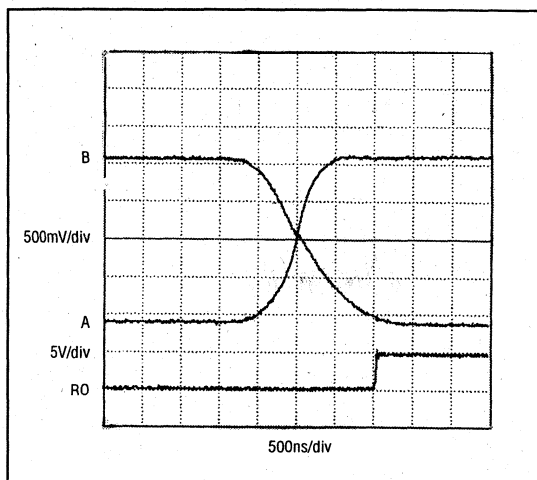


Figure 12. Receiver t_{PLH}

Low-Power Shutdown Mode

A low-power shutdown mode is initiated by bringing $\overline{RE}$ high and DE low. The devices will not shut down unless **both** the driver and receiver are disabled. In shutdown, the devices typically draw only 0.1 μ A of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the receiver, the t_{ZH} and t_{ZL} enable times assume the part was not in the low-power shutdown state. The $t_{ZH}(SHDN)$ and $t_{ZL}(SHDN)$ enable times assume the parts were shut down (see *Electrical Characteristics*).

It takes the receivers longer to become enabled from the low-power shutdown state ($t_{ZH}(SHDN)$, $t_{ZL}(SHDN)$) than from the operating mode (t_{ZH} , t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0, 1 or 1, 1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Digital encoding schemes depend on the driver and receiver skew. Skew is defined as the difference between the rising and falling propagation delay times. Typical propagation delays are shown in Figures 11 and 12 using Figure 10's test circuit.

The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is typically under 160ns.

The driver skew times are typically 160ns (800ns max).

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

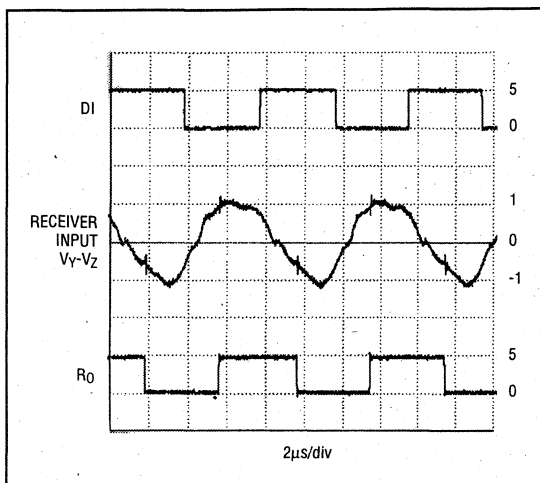


Figure 13. System Differential Voltage at 250kbps (125kHz) Driving 4000 Feet of Cable

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 16.

Figure 13 shows the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 120 Ω loads. Even after 4000 feet of cable, the MAX1482/MAX1483 output shows virtually no distortion.

Typical Applications

The MAX1482/MAX1483 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 14 and 15 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 16.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible (although the slew-rate-limited MAX1482 and MAX1483 are more tolerant of imperfect termination than standard RS-485 ICs).

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

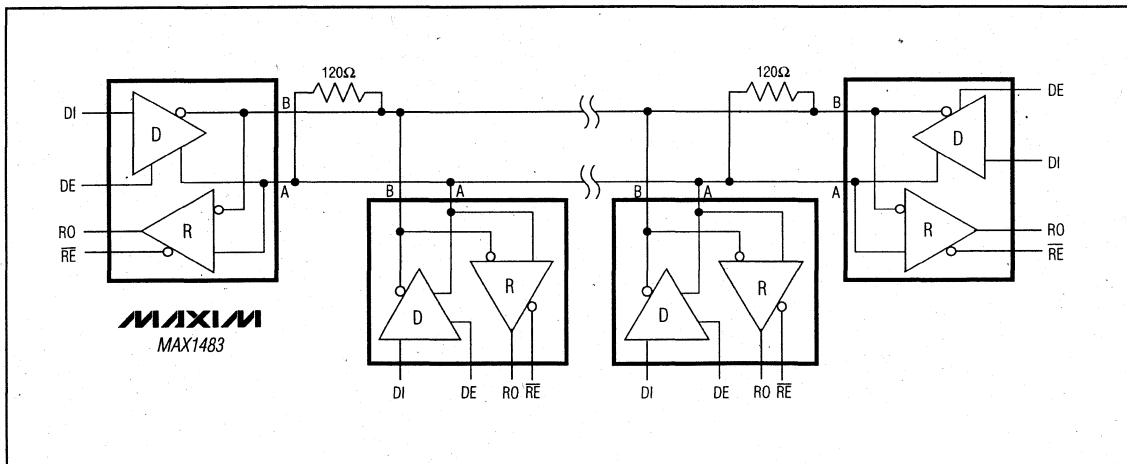
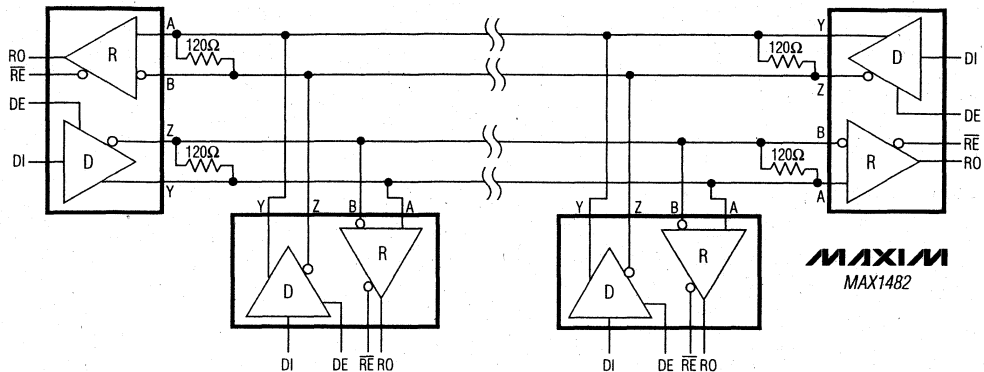


Figure 14. MAX1483 Typical Half-Duplex RS-485 Network

20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

MAX1482/MAX1483

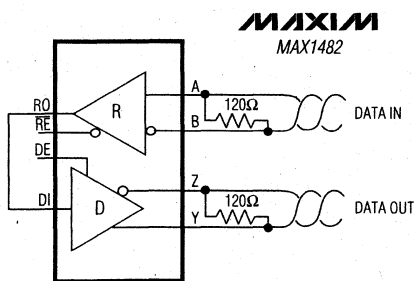
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NOTE: $\overline{RE}$ AND DE ON.

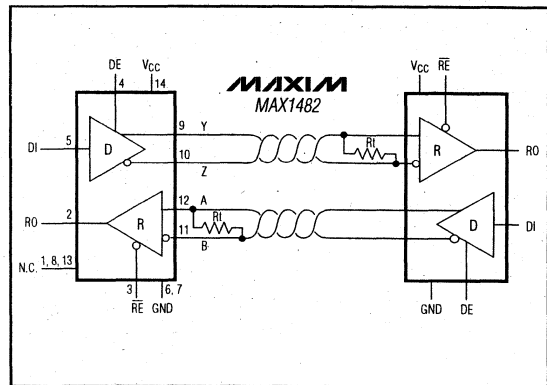
Figure 15. MAX1482 Full-Duplex RS-485 Network

Typical Operating Circuits (continued)



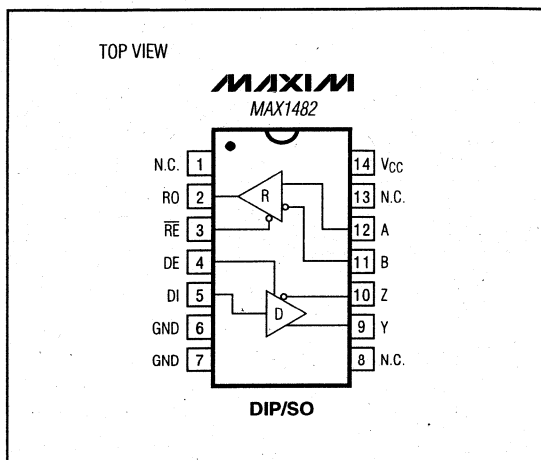
NOTE: $\overline{RE}$ AND DE ON.

Figure 16. Line Repeater for MAX1482



20 μ A, 1/8-Unit-Load, Slew-Rate-Limited RS-485 Transceivers

Pin Configurations (continued)





±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

General Description

The MAX481E, MAX483E, MAX485E, MAX487E-MAX491E, and MAX1487E are low-power transceivers for RS-485 and RS-422 communications in harsh environments. Each driver output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. These parts contain one driver and one receiver. The MAX483E, MAX487E, MAX488E, and MAX489E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw as little as 120µA supply current when unloaded or when fully loaded with disabled drivers (see *Selection Table*). Additionally, the MAX481E, MAX483E, and MAX487E have a low-current shutdown mode in which they consume only 0.1µA. All parts operate from a single +5V supply.

Drivers are short-circuit current limited, and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487E and MAX1487E feature quarter-unit-load receiver input impedance, allowing up to 128 transceivers on the bus. The MAX488E-MAX491E are designed for full-duplex communications, while the MAX481E, MAX483E, MAX485E, MAX487E, and MAX1487E are designed for half-duplex applications. For applications in a less demanding environment, see the pin- and function-compatible MAX481, MAX483, MAX485, MAX487-MAX491, and MAX1487.

Applications

Low-Power RS-485 Transceivers
Low-Power RS-422 Transceivers
Level Translators
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks

Features

- ◆ ESD Protection: ±15kV—Human Body Model
- ◆ Available in µMAX Package (the smallest 8-pin SO)
- ◆ Slew-Rate Limited for Error-Free Data Transmission (MAX483E/487E/488E/489E)
- ◆ Low Quiescent Current:
 - 120µA (MAX483E/487E/488E/489E)
 - 230µA (MAX1487E)
 - 300µA (MAX481E/485E/490E/491E)
- ◆ -7V to +12V Common-Mode Input Voltage Range
- ◆ Three-State Outputs
- ◆ 30ns Propagation Delays, 5ns Skew (MAX481E/485E/490E/491E/1487E)
- ◆ Full-Duplex and Half-Duplex Versions Available
- ◆ Allows up to 128 Transceivers on the Bus (MAX487E/MAX1487E)
- ◆ Current Limiting and Thermal Shutdown for Driver Overload Protection

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481ECPA	0°C to +70°C	8 Plastic DIP
MAX481ECSA	0°C to +70°C	8 SO
MAX481ECUA	0°C to +70°C	8 µMAX
MAX481EEPA	-40°C to +85°C	8 Plastic DIP
MAX481EESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481E	Half	2.5	No	Yes	Yes	300	32	8
MAX483E	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485E	Half	2.5	No	No	Yes	300	32	8
MAX487E	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488E	Full	0.25	Yes	No	No	120	32	8
MAX489E	Full	0.25	Yes	No	Yes	120	32	14
MAX490E	Full	2.5	No	No	No	300	32	8
MAX491E	Full	2.5	No	No	Yes	300	32	14
MAX1487E	Half	2.5	No	No	Yes	230	128	8



±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC})	12V
Control Input Voltage ($\overline{RE}$, $\overline{DE}$)	-0.5V to (V _{CC} + 0.5V)
Driver Input Voltage (DI)	-0.5V to (V _{CC} + 0.5V)
Driver Output Voltage (A, B)	-8V to +12.5V
Receiver Input Voltage (A, B)	-8V to +12.5V
Receiver Output Voltage (RO)	-0.5V to (V _{CC} + 0.5V)
Continuous Power Dissipation (T _A = +70°C)	
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)	800mW

8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
14-Pin SO (derate 8.33mW/°C above +70°C)	667mW
8-Pin μ MAX (derate 4.1mW/°C above +70°C)	830mW
Operating Temperature Ranges	
MAX4_ _C_ _/MAX1487EC_ _A	0°C to +70°C
MAX4_ _E_ _/MAX1487EE_ _A	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V $\pm$ 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V _{OD1}				5	V
Differential Driver Output (with load)	V _{OD2}	R = 50 Ω (RS-422)	2			V
		R = 27 Ω (RS-485), Figure 8	1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	Δ V _{OD}	R = 27 Ω or 50 Ω , Figure 8			0.2	V
Driver Common-Mode Output Voltage	V _{OC}	R = 27 Ω or 50 Ω , Figure 8			3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	Δ V _{OD}	R = 27 Ω or 50 Ω , Figure 8			0.2	V
Input High Voltage	V _{IH}	DE, DI, $\overline{RE}$	2.0			V
Input Low Voltage	V _{IL}	DE, DI, $\overline{RE}$			0.8	V
Input Current	I _{IN1}	DE, DI, $\overline{RE}$			$\pm$ 2	μ A
Input Current (A, B)	I _{IN2}	DE = 0V; V _{CC} = 0V or 5.25V, all devices except MAX487E/MAX1487E	V _{IN} = 12V		1.0	mA
			V _{IN} = -7V		-0.8	
		MAX487E/MAX1487E, DE = 0V, V _{CC} = 0V or 5.25V	V _{IN} = 12V		0.25	mA
			V _{IN} = -7V		-0.2	
Receiver Differential Threshold Voltage	V _{TH}	-7V $\leq$ V _{CM} $\leq$ 12V	-0.2		0.2	V
Receiver Input Hysteresis	Δ V _{TH}	V _{CM} = 0V		70		mV
Receiver Output High Voltage	V _{OH}	I _O = -4mA, V _{ID} = 200mV	3.5			V
Receiver Output Low Voltage	V _{OL}	I _O = 4mA, V _{ID} = -200mV			0.4	V
Three-State (high impedance) Output Current at Receiver	I _{OZR}	0.4V $\leq$ V _O $\leq$ 2.4V			$\pm$ 1	μ A
Receiver Input Resistance	R _{IN}	-7V $\leq$ V _{CM} $\leq$ 12V, all devices except MAX487E/MAX1487E	12			k Ω
		-7V $\leq$ V _{CM} $\leq$ 12V, MAX487E/MAX1487E	48			k Ω

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I _{CC}	MAX488E/MAX489E, DE, DI, $\overline{RE}$ = 0V or V _{CC}		120	250	μA
		MAX490E/MAX491E, DE, DI, $\overline{RE}$ = 0V or V _{CC}		300	500	
		MAX481E/MAX485E, RE = 0V or V _{CC}		500	900	
		DE = V _{CC}		300	500	
		DE = 0V		300	500	
		MAX1487E, RE = 0V or V _{CC}		300	500	
		DE = V _{CC}		230	400	
		DE = 0V		230	400	
		MAX483E/MAX487E, RE = 0V or V _{CC}		350	650	
		DE = V _{CC}		250	400	
		DE = 0V		120	250	
Supply Current in Shutdown	I _{SHDN}	MAX481E/483E/487E, DE = 0V, $\overline{RE}$ = V _{CC}		0.1	10	μA
Driver Short-Circuit Current, V _O = High	I _{OSD1}	-7V ≤ V _O ≤ 12V (Note 4)	35		250	mA
Driver Short-Circuit Current, V _O = Low	I _{OSD2}	-7V ≤ V _O ≤ 12V (Note 4)	35		250	mA
Receiver Short-Circuit Current	I _{OSR}	0V ≤ V _O ≤ V _{CC}	7		95	mA
ESD Protection		A, B, Y and Z pins, tested using Human Body Model		±15		kV

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t _{PLH}	Figures 10 and 12, R _{DIFF} = 54Ω, C _{L1} = C _{L2} = 100pF	10		60	ns
	t _{PHL}		10		60	
Driver Output Skew to Output	t _{SKEW}	Figures 10 and 12, R _{DIFF} = 54Ω, C _{L1} = C _{L2} = 100pF			10	ns
Driver Rise or Fall Time	t _r , t _f	Figures 10 and 12, R _{DIFF} = 54Ω, C _{L1} = C _{L2} = 100pF	3		40	ns
		MAX481E, MAX485E, MAX1487E MAX490EC/E, MAX491EC/E	5		25	
Driver Enable to Output High	t _{ZH}	Figures 11 and 13, C _L = 100pF, S2 closed			70	ns
Driver Enable to Output Low	t _{ZL}	Figures 11 and 13, C _L = 100pF, S1 closed			70	ns
Driver Disable Time from Low	t _{LZ}	Figures 11 and 13, C _L = 15pF, S1 closed			70	ns
Driver Disable Time from High	t _{HZ}	Figures 11 and 13, C _L = 15pF, S2 closed			70	ns
Receiver Input to Output	t _{PLH} , t _{PHL}	Figures 10 and 14, R _{DIFF} = 54Ω, C _{L1} = C _{L2} = 100pF	20	60	200	ns
		MAX481E, MAX485E, MAX1487E MAX490EC/E, MAX491EC/E	20	60	150	
t _{PLH} - t _{PHL} Differential Receiver Skew	t _{SKD}	Figures 10 and 14, R _{DIFF} = 54Ω, C _{L1} = C _{L2} = 100pF		5		ns
Receiver Enable to Output Low	t _{ZL}	Figures 9 and 15, C _R L = 15pF, S1 closed		20	50	ns
Receiver Enable to Output High	t _{ZH}	Figures 9 and 15, C _R L = 15pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t _{LZ}	Figures 9 and 15, C _R L = 15pF, S1 closed		20	50	ns
Receiver Disable Time from High	t _{HZ}	Figures 9 and 15, C _R L = 15pF, S2 closed		20	50	ns
Maximum Data Rate	f _{MAX}		2.5			Mbps
Time to Shutdown	t _{SHDN}	MAX481 (Note 5)	50	200	600	ns

MAX481E/MAX483E/MAX485E/MAX487E-MAX491E/MAX1487E

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E (continued)

(VCC = 5V ±5%, TA = TMIN to TMAX, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481E)	tZH(SHDN)	Figures 11 and 13, CL = 100pF, S2 closed			100	ns
Driver Enable from Shutdown to Output Low (MAX481E)	tZL(SHDN)	Figures 11 and 13, CL = 100pF, S1 closed			100	ns
Receiver Enable from Shutdown to Output High (MAX481E)	tZH(SHDN)	Figures 9 and 15, CL = 15pF, S2 closed, A - B = 2V			1000	ns
Receiver Enable from Shutdown to Output Low (MAX481E)	tZL(SHDN)	Figures 9 and 15, CL = 15pF, S1 closed, B - A = 2V			1000	ns

SWITCHING CHARACTERISTICS—MAX483E, MAX487E/MAX488E/MAX489E

(VCC = 5V ±5%, TA = TMIN to TMAX, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	tPLH	Figures 10 and 12, RDIFF = 54Ω, CL1 = CL2 = 100pF	250		2000	ns
	tPHL		250		2000	
Driver Output Skew to Output	tsKEW	Figures 10 and 12, RDIFF = 54Ω, CL1 = CL2 = 100pF			800	ns
Driver Rise or Fall Time	tr, tf	Figures 10 and 12, RDIFF = 54Ω, CL1 = CL2 = 100pF	250		2000	ns
Driver Enable to Output High	tZH	Figures 11 and 13, CL = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	tZL	Figures 11 and 13, CL = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	tLZ	Figures 11 and 13, CL = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	tHZ	Figures 11 and 13, CL = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	tPLH	Figures 10 and 14, RDIFF = 54Ω, CL1 = CL2 = 100pF	250		2000	ns
	tPHL		250		2000	
tPLH - tPHL Differential Receiver Skew	tsKD	Figures 10 and 14, RDIFF = 54Ω, CL1 = CL2 = 100pF		100		ns
Receiver Enable to Output Low	tZL	Figures 9 and 15, CRL = 15pF, S1 closed			50	ns
Receiver Enable to Output High	tZH	Figures 9 and 15, CRL = 15pF, S2 closed			50	ns
Receiver Disable Time from Low	tLZ	Figures 9 and 15, CRL = 15pF, S1 closed			50	ns
Receiver Disable Time from High	tHZ	Figures 9 and 15, CRL = 15pF, S2 closed			50	ns
Maximum Data Rate	fMAX	tPLH, tPHL < 50% of data period	250			kbps
Time to Shutdown	tSHDN	MAX483E/MAX487E (Note 5)	50		600	ns
Driver Enable from Shutdown to Output High	tZH(SHDN)	MAX483E/MAX487E, Figures 11 and 13, CL = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	tZL(SHDN)	MAX483E/MAX487E, Figures 11 and 13, CL = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	tZH(SHDN)	MAX483E/MAX487E, Figures 9 and 15, CL = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	tZL(SHDN)	MAX483E/MAX487E, Figures 9 and 15, CL = 15pF, S1 closed			2500	ns

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 2: All typical specifications are given for $V_{CC} = 5V$ and $T_A = +25^{\circ}C$.

Note 3: Supply current specification is valid for loaded transmitters when $DE = 0V$.

Note 4: Applies to peak current. See *Typical Operating Characteristics*.

Note 5: The MAX481E/MAX483E/MAX487E are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

Pin Description

PIN					NAME	FUNCTION
MAX481E/MAX483E MAX485E/MAX487E MAX1487E		MAX488E MAX490E		MAX489E MAX491E		
DIP/SO	μMAX	DIP/SO	μMAX	DIP/SO		
1	3	2	4	2	RO	Receiver Output: If $A > B$ by 200mV, RO will be high; If $A < B$ by 200mV, RO will be low.
2	4	—	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	5	—	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	6	3	5	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	7	4	6	6, 7	GND	Ground
—	—	5	7	9	Y	Noninverting Driver Output
—	—	6	8	10	Z	Inverting Driver Output
6	8	—	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	—	8	2	12	A	Noninverting Receiver Input
7	1	—	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	—	7	1	11	B	Inverting Receiver Input
8	2	1	3	14	V _{CC}	Positive Supply: $4.75V \leq V_{CC} \leq 5.25V$
—	—	—	—	1, 8, 13	N.C.	No Connect—not internally connected

MAX481E/MAX483E/MAX485E/MAX487E-MAX491E/MAX1487E

$\pm 15\text{kV}$ ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

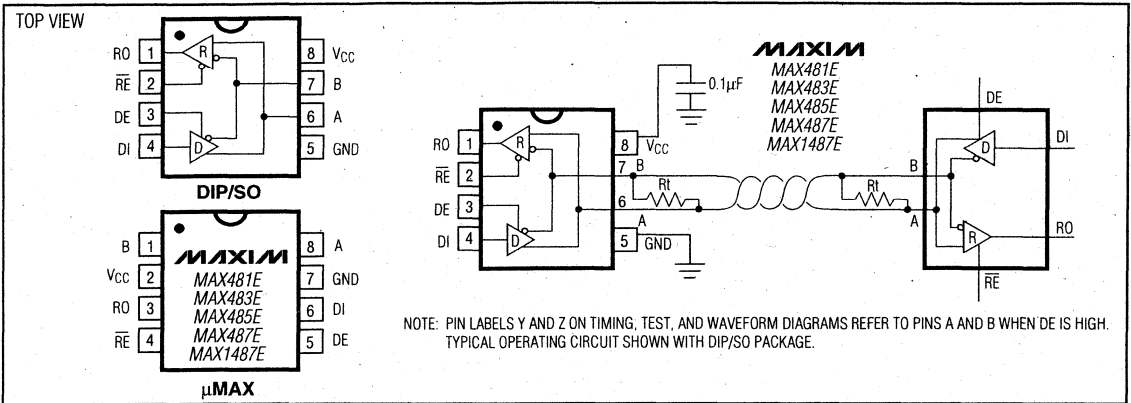


Figure 1. MAX481E/MAX483E/MAX485E/MAX1487E Pin Configuration and Typical Operating Circuit

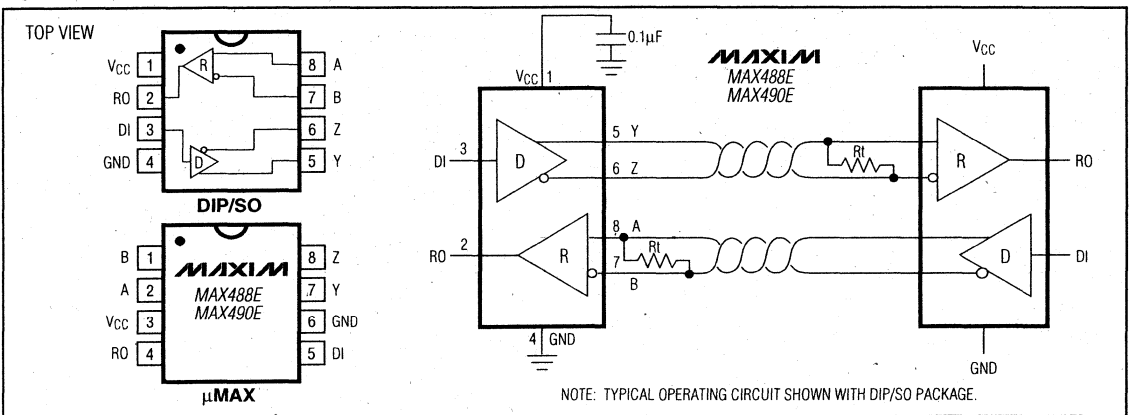


Figure 2. MAX488E/MAX490E Pin Configuration and Typical Operating Circuit

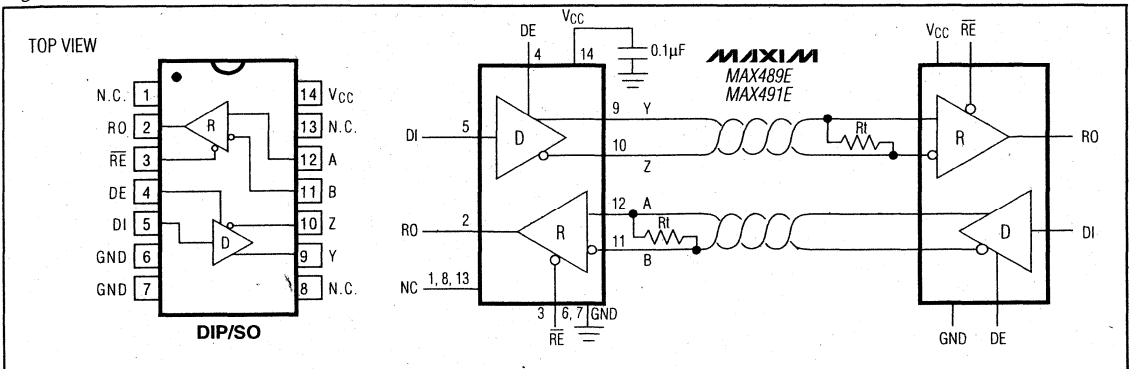


Figure 3. MAX489E/MAX491E Pin Configuration and Typical Operating Circuit

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

Function Tables (MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{\text{RE}}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care

High-Z = High impedance

* Shutdown mode for MAX481E/MAX483E/MAX487E

Table 2. Receiving

INPUTS			OUTPUT
$\overline{\text{RE}}$	DE	A-B	RO
0	0	$\geq +0.2\text{V}$	1
0	0	$\leq -0.2\text{V}$	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care

High-Z = High impedance

* Shutdown mode for MAX481E/MAX483E/MAX487E

Applications Information

The MAX481E/MAX483E/MAX485E/MAX487E-MAX491E and MAX1487E are low-power transceivers for RS-485 and RS-422 communications. These "E" versions of the MAX481, MAX483, MAX485, MAX487-MAX491, and MAX1487 provide extra protection against ESD. The rugged MAX481E, MAX483E, MAX485E, MAX497E-MAX491E, and MAX1487E are intended for harsh environments where high-speed communication is important. These devices eliminate the need for transient suppressor diodes and the associated high capacitance loading. The standard (non-"E") MAX481, MAX483, MAX485, MAX487-MAX491, and MAX1487 are recommended for applications where cost is critical.

The MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E can transmit and receive at data rates up to 2.5Mbps, while the MAX483E, MAX487E, MAX488E, and MAX489E are specified for data rates up to 250kbps. The MAX488E-MAX491E are full-duplex transceivers, while the MAX481E, MAX483E, MAX487E, and MAX1487E are half-duplex. In addition, driver enable (DE) and receiver enable (RE) pins are included on the MAX481E, MAX483E, MAX485E, MAX487E, MAX489E, MAX491E, and MAX1487E. When disabled, the driver and receiver outputs are high impedance.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engi-

neers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX481E, MAX483E, MAX485E, MAX487E-MAX491E, and MAX1487E keep working without latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to ±15kV using the Human Body Model.

Other ESD test methodologies include IEC10004-2 contact discharge and IEC1000-4-2 air-gap discharge (formerly IEC801-2).

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits (Figure 6).

MAX481E/MAX483E/MAX485E/MAX487E-MAX491E/MAX1487E

$\pm 15\text{kV}$ ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

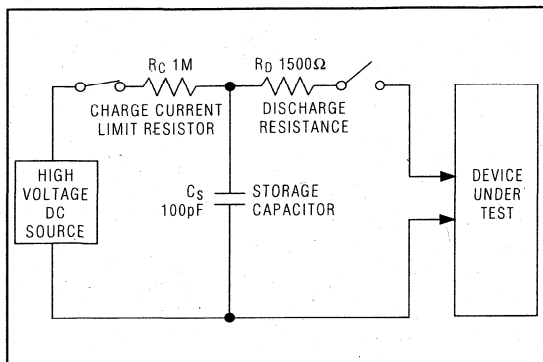


Figure 4. Human Body ESD Test Model

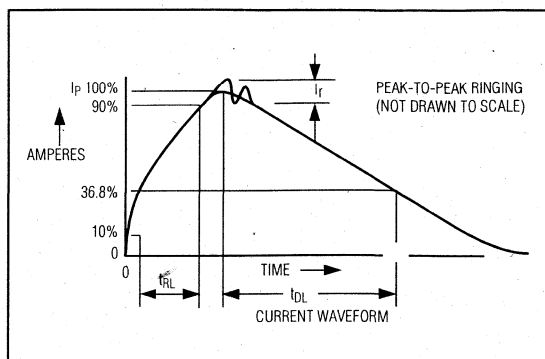


Figure 5. Human Body Model Current Waveform

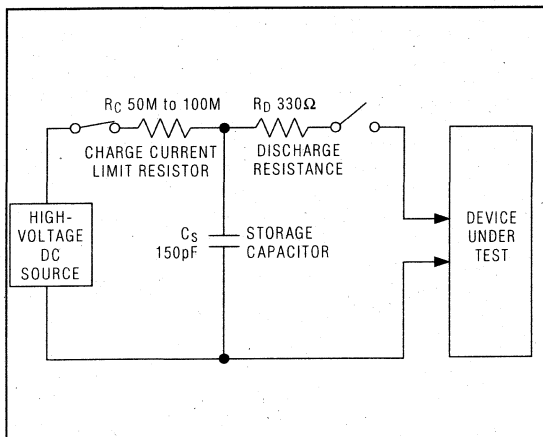


Figure 6. IEC1000-4-2 ESD Test Model

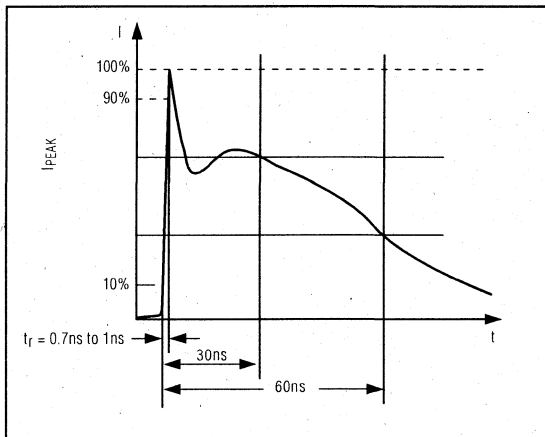


Figure 7. IEC1000-4-2 ESD Generator Current Waveform

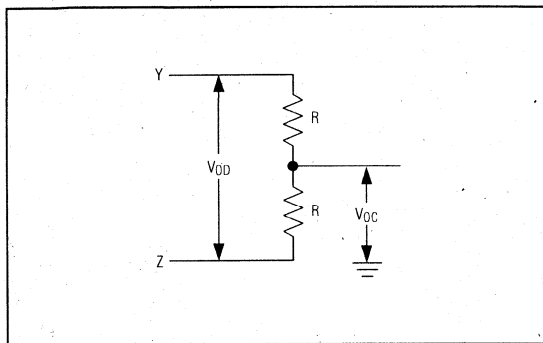


Figure 8. Driver DC Test Load

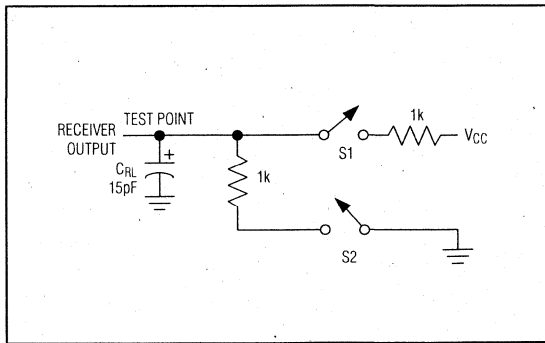


Figure 9. Receiver Timing Test Load

$\pm 15\text{kV}$ ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

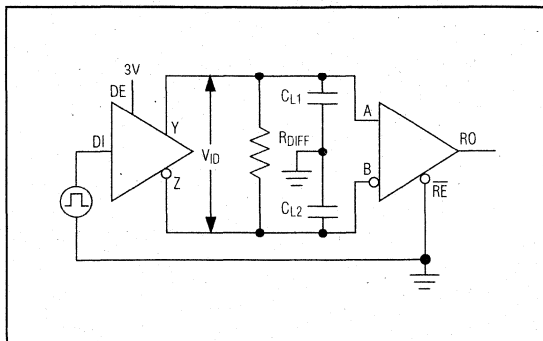


Figure 10. Driver/Receiver Timing Test Circuit

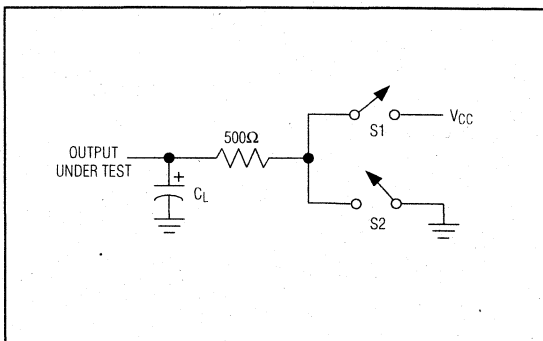


Figure 11. Driver Timing Test Load

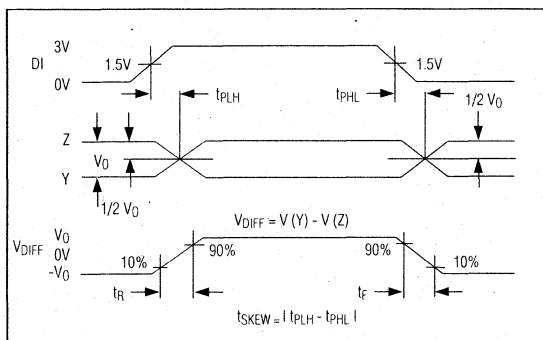


Figure 12. Driver Propagation Delays

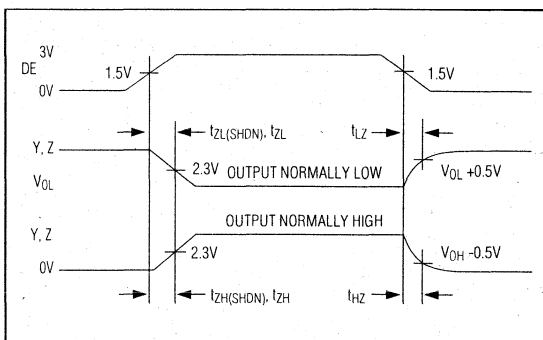


Figure 13. Driver Enable and Disable Times (except MAX488E and MAX490E)

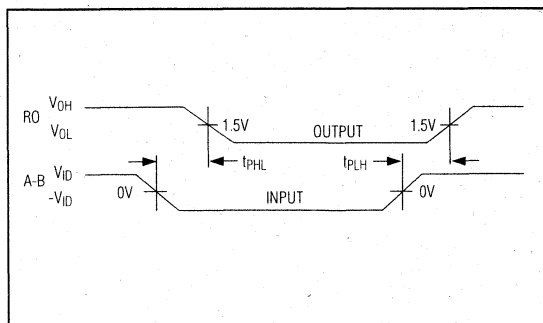


Figure 14. Receiver Propagation Delays

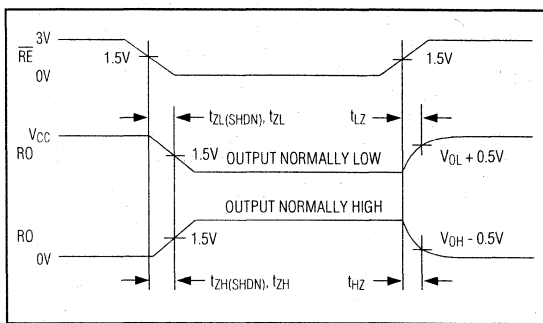


Figure 15. Receiver Enable and Disable Times (except MAX488E and MAX490E)

MAX481E/MAX483E/MAX485E/MAX487E-MAX491E/MAX1487E

$\pm 15\text{kV}$ ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7 shows the current waveform for the 8kV IEC1000-4-2 ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

MAX487E/MAX1487E: 128 Transceivers on the Bus

The 48k Ω , 1/4-unit-load receiver input impedance of the MAX487E and MAX1487E allows up to 128 transceivers on a bus, compared to the 1-unit load (12k Ω input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487E/MAX1487E and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481E, MAX483E, MAX485E, and MAX488E-MAX491E have standard 12k Ω receiver input impedance.

MAX483E/MAX487E/MAX488E/MAX489E: Reduced EMI and Reflections

The MAX483E and MAX487E-MAX489E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables.

Low-Power Shutdown Mode (MAX481E/MAX483E/MAX487E)

A low-power shutdown mode is initiated by bringing both RE high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.1 μA of supply current.

RE and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if RE is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481E, MAX483E, and MAX487E, the tZH and tZL enable times assume the part was not in the low-power shutdown state (the MAX485E, MAX488E-MAX491E, and MAX1487E can not be shut down). The tZH(SHDN) and tZL(SHDN) enable times assume the parts were shut down (see *Electrical Characteristics*).

It takes the drivers and receivers longer to become enabled from the low-power shutdown state (tZH(SHDN), tZL(SHDN)) than from the operating mode (tZH, tZL). (The parts are in operating mode if the RE, DE inputs equal a logical 0, 1 or 1, 1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Typical Applications

The MAX481E, MAX483E, MAX485E, MAX487E-MAX491E, and MAX1487E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 16 and 17 show typical network application circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483E and MAX487E-MAX489E are more tolerant of imperfect termination. Bypass the VCC pin with 0.1 μF .

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

$\pm 15\text{kV}$ ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

MAX481E/MAX483E/MAX485E/MAX487E-MAX491E/MAX1487E

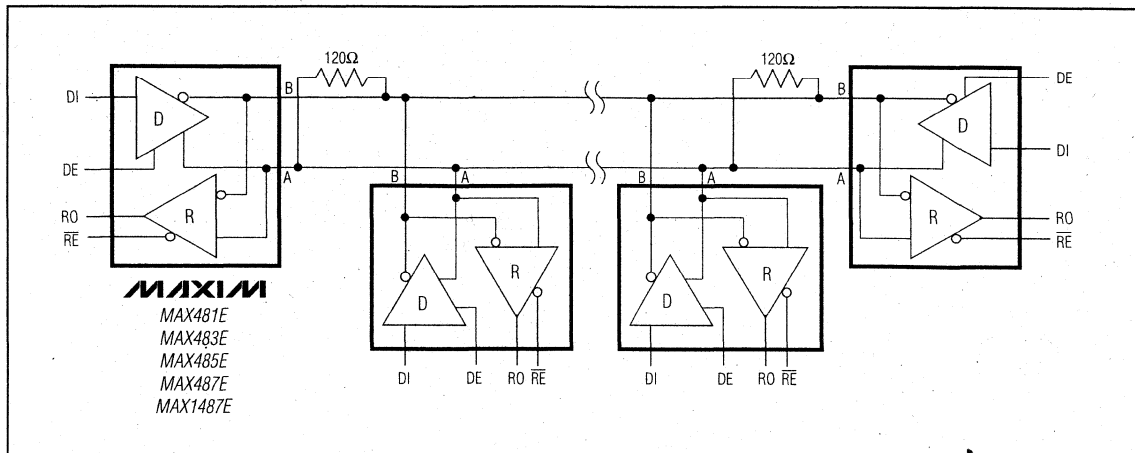


Figure 16. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Typical Half-Duplex RS-485 Network

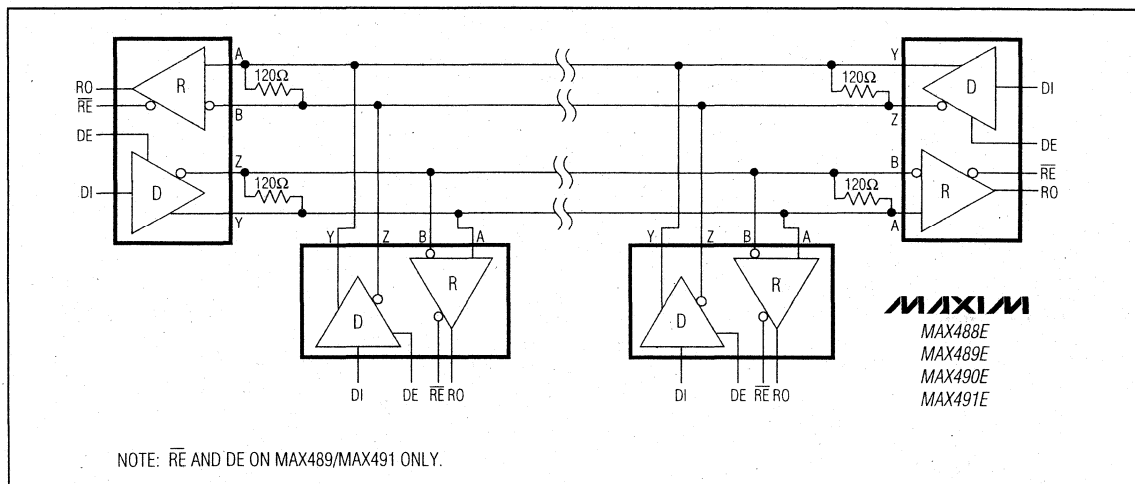


Figure 17. MAX488E-MAX491E Full-Duplex RS-485 Network

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

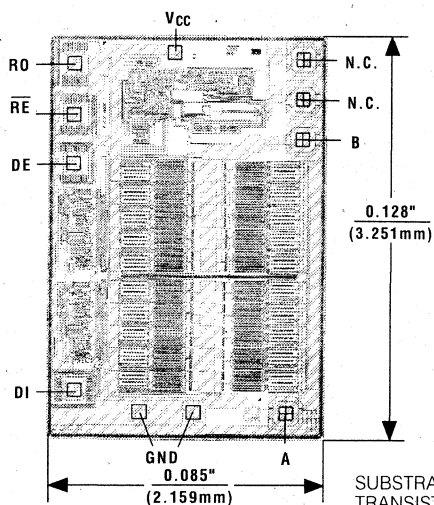
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX483ECPA	0°C to +70°C	8 Plastic DIP
MAX483ECSA	0°C to +70°C	8 SO
MAX483ECUA	0°C to +70°C	8 μ MAX
MAX483EEPA	-40°C to +85°C	8 Plastic DIP
MAX483EESA	-40°C to +85°C	8 SO
MAX485ECPA	0°C to +70°C	8 Plastic DIP
MAX485ECSA	0°C to +70°C	8 SO
MAX485ECUA	0°C to +70°C	8 μ MAX
MAX485EEPA	-40°C to +85°C	8 Plastic DIP
MAX485EESA	-40°C to +85°C	8 SO
MAX487ECPA	0°C to +70°C	8 Plastic DIP
MAX487ECSA	0°C to +70°C	8 SO
MAX487ECUA	0°C to +70°C	8 μ MAX
MAX487EEPA	-40°C to +85°C	8 Plastic DIP
MAX487EESA	-40°C to +85°C	8 SO
MAX488ECPA	0°C to +70°C	8 Plastic DIP
MAX488ECSA	0°C to +70°C	8 SO
MAX488ECUA	0°C to +70°C	8 μ MAX
MAX488EEPA	-40°C to +85°C	8 Plastic DIP
MAX488EESA	-40°C to +85°C	8 SO

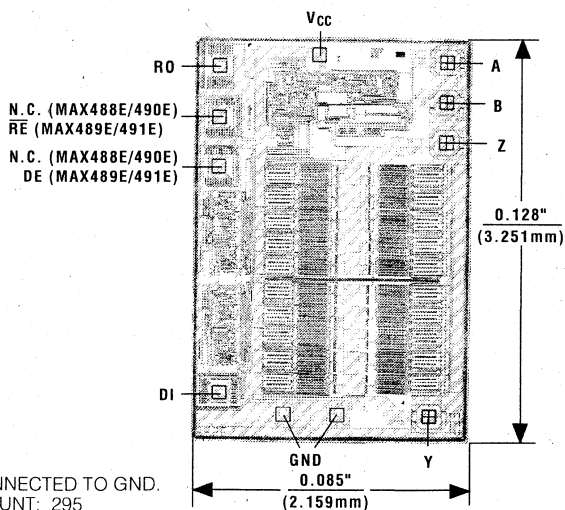
PART	TEMP. RANGE	PIN-PACKAGE
MAX489ECPD	0°C to +70°C	14 Plastic DIP
MAX489ECSA	0°C to +70°C	14 SO
MAX489ECPD	-40°C to +85°C	14 Plastic DIP
MAX489EESA	-40°C to +85°C	14 SO
MAX490ECPA	0°C to +70°C	8 Plastic DIP
MAX490ECSA	0°C to +70°C	8 SO
MAX490ECUA	0°C to +70°C	8 μ MAX
MAX490EEPA	-40°C to +85°C	8 Plastic DIP
MAX490EESA	-40°C to +85°C	8 SO
MAX491ECPD	0°C to +70°C	14 Plastic DIP
MAX491ECSA	0°C to +70°C	14 SO
MAX491ECPD	-40°C to +85°C	14 Plastic DIP
MAX491EESA	-40°C to +85°C	14 SO
MAX1487ECPA	0°C to +70°C	8 Plastic DIP
MAX1487ECSA	0°C to +70°C	8 SO
MAX1487ECUA	-40°C to +85°C	8 μ MAX
MAX1487EEPA	-40°C to +85°C	8 Plastic DIP
MAX1487EESA	-55°C to +125°C	8 SO

Chip Topographies

MAX481E/483E/485E/487E/1487E



MAX488E/489E/490E/491E



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/95

MAXIM

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver

General Description

The MAX1488E quad, low-power line driver is designed for EIA/TIA-232, EIA/TIA-562, and CCITT V.28 communications in harsh environments. Each transmitter output is protected against ±15kV electrostatic discharge (ESD) shocks. The inputs are TTL and CMOS compatible with minimal loading. The outputs feature internally controlled slew-rate limiting and current limiting. This device has a guaranteed 120kbps data rate. Power-supply current is less than 180µA over a ±4.5V to ±13.2V supply voltage range.

The MAX1488E is pin compatible with the MC1488, MC14C88, SN75188, SN75C188, DS1488, and DS14C88. It is available in 14-pin plastic DIP and SO packages.

Applications

PC Motherboards

Modems

Interface Data Terminal Equipment (DTE) with Data Circuit-Terminating Equipment (DCE)

Equipment Meeting IEC1000-4-2 (formerly IEC801-2) or ±15kV ESD Protection

Features

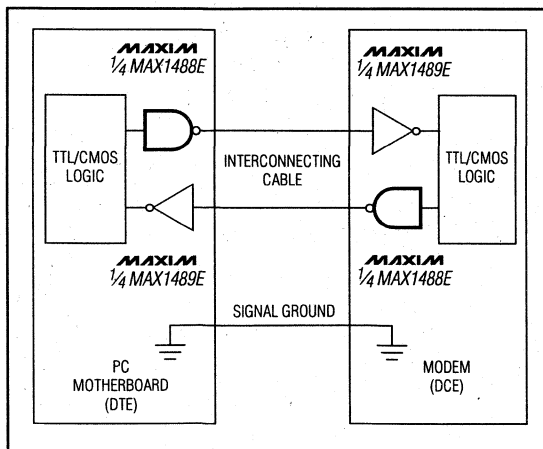
- ◆ ESD Protection:
 - ±15kV—Human Body Model
 - ±8kV—IEC801-2, Contact Discharge
 - ±15kV—IEC801-2, Air-Gap Discharge
- ◆ Latchup Free, Even During an ESD Event
- ◆ Low 85µA Supply Current from IEE or ICC
- ◆ Guaranteed 120kbps Data Rate
- ◆ No External Capacitors Required for Slew-Rate Limiting
- ◆ Pin Compatible with MC1488, MC14C88, SN75188, SN75C188, DS1488, and DS14C88

Ordering Information

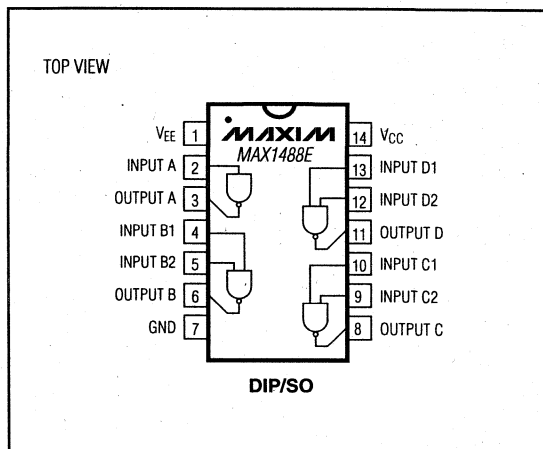
PART	TEMP. RANGE	PIN-PACKAGE
MAX1488ECPD	0°C to +70°C	14 Plastic DIP
MAX1488ECSO	0°C to +70°C	14 SO
MAX1488EC/D	0°C to +70°C	Dice*
MAX1488ECPD	-40°C to +85°C	14 Plastic DIP
MAX1488EESD	-40°C to +85°C	14 SO

* Dice are specified at $T_A = +25^\circ\text{C}$.

Typical Operating Circuit



Pin Configuration



MAX1488E

2

MAXIM

Maxim Integrated Products 2-31

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/95

MAXIM

±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver

General Description

The MAX1489E quad, low-power line receiver is designed for EIA/TIA-232, EIA/TIA-562, and CCITT V.28 communications in harsh environments. Each receiver input is protected against ±15kV electrostatic discharge (ESD) shocks. These inputs have a ±25V range and feature hysteresis and time-domain filtering. The outputs are TTL and CMOS compatible. The MAX1489E has a 120kbps guaranteed data rate. Supply current is typically 350µA.

The MAX1489E is pin compatible with the MC1489, MC14C89, SN75189, SN75C189, DS1489, and DS14C89. It is available in 14-pin plastic DIP and SO packages.

Applications

PC Motherboards

Modems

Interfacing Data Terminal Equipment (DTE) with Data Circuit-Terminating Equipment (DCE)

Equipment Meeting IEC1000-4-2 (formerly IEC801-2) or ±15kV ESD Protection

Features

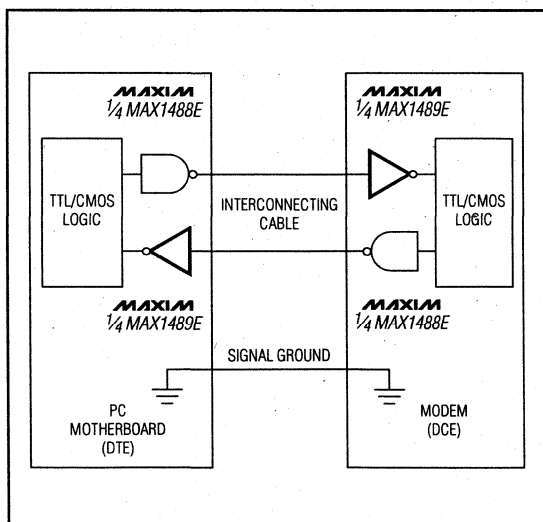
- ♦ Enhanced ESD Protection:
 - ±15kV—Human Body Model
 - ±8kV—IEC1000-4-2, Contact Discharge
 - ±15kV—IEC1000-4-2, Air-Gap Discharge
- ♦ Latchup Free During an ESD Event
- ♦ Low 350µA Supply Current
- ♦ Input Hysteresis and Time-Domain Filtering Eliminate the Need for External Filtering
- ♦ Stable Input Thresholds
- ♦ Pin Compatible with MC1489, MC14C89, SN75189, SN75C189, DS1489, and DS14C89

Ordering Information

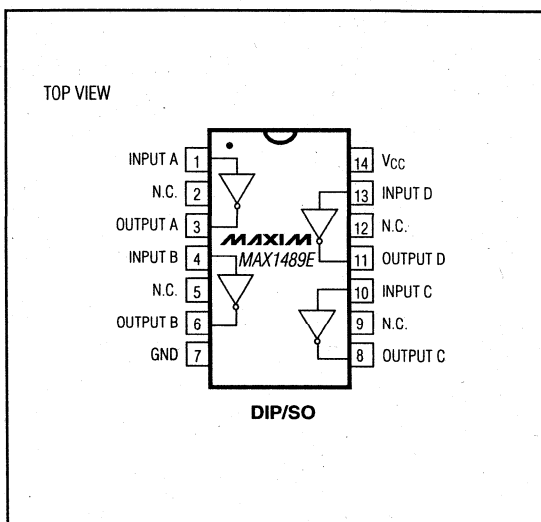
PART	TEMP. RANGE	PIN-PACKAGE
MAX1489ECPD	0°C to +70°C	14 Plastic DIP
MAX1489ECSO	0°C to +70°C	14 SO
MAX1489EC/D	0°C to +70°C	Dice*
MAX1489ECPD	-40°C to +85°C	14 Plastic DIP
MAX1489EESO	-40°C to +85°C	14 SO

* Dice are specified at T_A = +25°C.

Typical Operating Circuit



Pin Configuration



MAX1489E

2

MAXIM

Maxim Integrated Products 2-33

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/95

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceiver

General Description

The MAX203E transceiver is designed for RS-232 and V.28 communications in harsh environments. Each driver output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The MAX203E has two drivers and two receivers. The drivers and receivers meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps when loaded in accordance with the EIA/TIA-232E specification.

The MAX203E comes in 20-pin DIP and wide SO packages, and requires no external charge-pump capacitors.

Applications

Notebook, Subnotebook, and Palmtop Computers

Battery-Powered Equipment

Hand-Held Equipment

Features

Better than Bipolar!

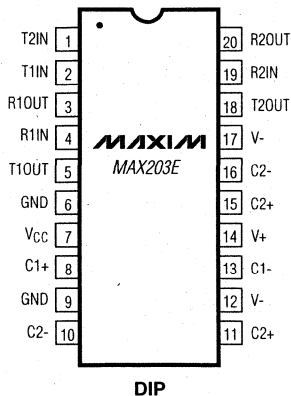
- ♦ ESD Protection for RS-232 I/O Pins:
 - ±15kV—Human Body Model
 - ±8kV—IEC801-2, Contact Discharge
 - ±15kV—IEC801-2, Air-Gap Discharge
- ♦ Latchup Free (unlike bipolar equivalents)
- ♦ 2 Drivers, 2 Receivers
- ♦ Guaranteed 120kbps Data Rate—LapLink™ Compatible
- ♦ Guaranteed 3V/μs Min Slew Rate
- ♦ Operate from Single +5V Power Supply

MAX203E

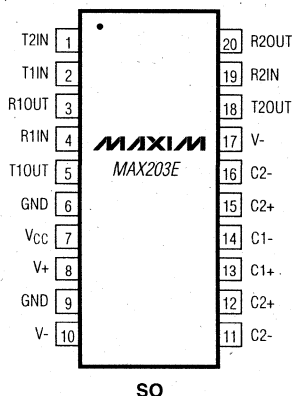
2

Pin Configurations

TOP VIEW



DIP



SO

LapLink is a registered trademark of Traveling Software, Inc.

MAXIM

Maxim Integrated Products 2-35

Call toll free 1-800-998-8800 for free samples or literature.

MAXIM

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

General Description

The MAX3212 uses Maxim's new proprietary Auto-Shutdown mode to reduce supply current to 1 μ A. The MAX3212, with 3 RS-232 drivers and 5 RS-232 receivers, is intended for 2.7V to 3.6V-powered EIA/TIA-232E and V.28/V.24 serial interface. True RS-232 levels are maintained across the operating range. A guaranteed data rate of 235kbps provides compatibility with popular software for communicating with personal computers.

Supply current is reduced to 1 μ A with Maxim's new AutoShutdown feature. When the MAX3212 does not sense a valid signal level on the receiver inputs, the on-board power supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing software.

A second power-management feature is incorporated to permit automatic shutdown when the RS-232 connection is valid but inactive. In this case, a transition detector facilitates shutdown when the receivers are presented with stationary RS-232 levels for long periods.

Three-state drivers are provided on receiver outputs so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART. The MAX3212 is available in 28-pin SO and SSOP packages.

Applications

Notebook and Palmtop Computers
Peripherals
Instruments
Battery-Powered Equipment

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3212CWI	0°C to +70°C	28 Wide SO
MAX3212CAI	0°C to +70°C	28 SSOP
MAX3212EWI	-40°C to +85°C	28 Wide SO
MAX3212EAI	-40°C to +85°C	28 SSOP

Pin Configuration appears at end of data sheet.

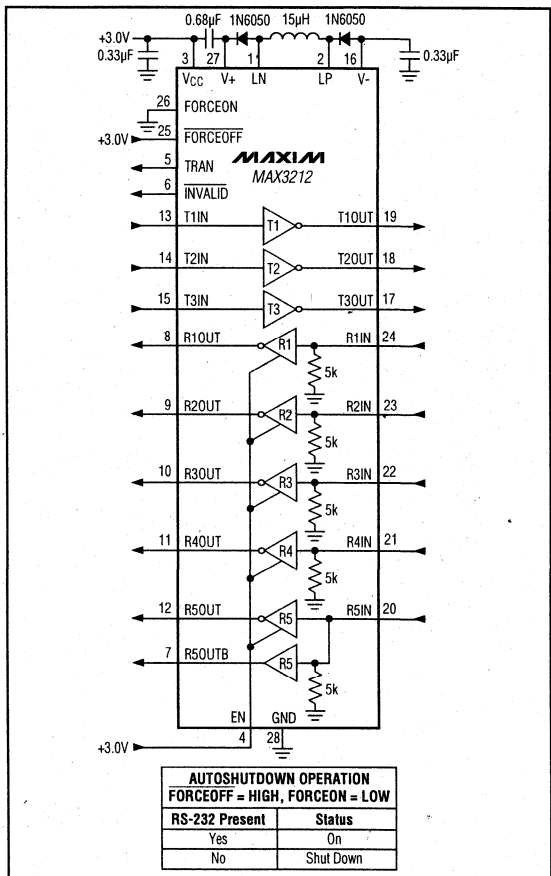
* Patent pending

Features

BETTER THAN BIPOLAR!

- ◆ 1 μ A Supply Current Using AutoShutdown
- ◆ Operates from Single +2.7V to +3.6V Supply
- ◆ 28-Pin SSOP or Wide SO Packages
- ◆ Meets All EIA/TIA-232E & EIA/TIA-562 Specifications
- ◆ Mouse Driveability—Guaranteed
- ◆ Low-Cost, Surface-Mount External Components
- ◆ 235kbps Guaranteed Data Rate—LapLink™ Compatible
- ◆ +5V Logic Compatible
- ◆ Complementary Receiver Output Always Active
- ◆ Flow-Through Pinout

Typical Operating Circuit



MAX3212*

2

MAXIM

Maxim Integrated Products 2-37

Call toll free 1-800-998-8800 for free samples or literature.

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltages

V _{CC}	-0.3V to +4.6V
V ₊	(V _{CC} - 0.3V) to +7.4V
V ₋	-7.4V to +2.0V
LN	-0.3V to (V ₊ + 1.0V)
LP	(V ₋ - 1.0V) to (V ₊ + 0.3V)

Input Voltages

T _{IN} , EN, FORCEON, FORCEOFF	-0.3V to +7.0V
R _{IN}	±25V

Output Voltages

T _{OUT}	±15V
R _{OUT} , R5OUTB, INVALID, TRAN	-0.3V to (V ₊ + 0.3V)

Short-Circuit Duration, T_{OUT}.....Continuous

Continuous Power Dissipation (T_A = +70°C)

Wide SO (derate 11.76mW/°C above +70°C).....941mW

SSOP (derate 8.00mW/°C above +70°C)640mW

Operating Temperature Ranges

MAX3212C_I

MAX3212E_I

Storage Temperature Range

Lead Temperature (soldering, 10sec)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Operating Voltage Range	Meets or exceeds EIA/TIA-232E specifications	2.7		3.6	V
V _{CC} Supply Current	All R _{IN} unconnected, FORCEON = GND		1	10	μA
	FORCEOFF = GND		1	10	μA
	FORCEON = FORCEOFF = V _{CC} , no load		1.5	3.0	mA
LOGIC INPUT AND RECEIVER OUTPUTS					
Input Logic Threshold Low	T _{IN} , EN, FORCEON, FORCEOFF			0.3V _{CC} - 0.1	V
Input Logic Threshold High	T _{IN} , EN, FORCEON, FORCEOFF	0.67V _{CC} + 0.1			V
Input Current High	T _{IN} , EN, FORCEON, FORCEOFF			1	μA
Input Current Low	T _{IN} , EN, FORCEON, FORCEOFF			1	μA
Hysteresis	T _{IN} , V _{CC} = 3.3V		0.3		V
Logic Output Voltage Low	I _{OUT} = 1.0mA			0.4	V
Logic Output Voltage High	I _{OUT} = -1.0mA	V _{CC} - 0.5			V
Logic Output Leakage Current	EN = GND, 0V < R _{OUT} < V _{CC}			±10	μA
AUTOSHUTDOWN (FORCEON = GND, FORCEOFF = V_{CC})					
Receiver Input Thresholds, Transmitters Enabled	Figure 4	Positive threshold		3.0	V
		Negative threshold	-3.0		
Receiver Input Thresholds, Transmitters Disabled	1μA supply current, Figure 4	-0.3		0.3	V
INVALID Output Voltage Low	I _{OUT} = 1.0mA			0.4	V
INVALID Output Voltage High	I _{OUT} = -1.0mA	V _{CC} - 0.6			V
Receiver Threshold to Transmitters Enabled, t _{WU}	Figure 4b		250		μs
Receiver Positive or Negative Threshold to Invalid High, t _{INVH}	Figure 4		1		μs
Receiver Positive or Negative Threshold to Invalid Low, t _{INVL}	Figure 4		30		μs

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVERS					
Input Voltage Operating Range		-25		+25	V
Input Voltage Threshold Low		0.4			V
Input Voltage Threshold High				3.0	V
Input Hysteresis			0.7		V
Input Resistance	-15V < V _{IN} < 15V	3	5	7	k Ω
EIA/TIA-232E TRANSMITTERS					
Output Voltage Swing (V _{HIGH} , V _{LOW})	All transmitters loaded with 3k Ω to GND	± 5.0	± 5.5		V
Output Resistance	V _{CC} = V- = V+ = 0V, -2V < T _{OUT} < 2V	300			Ω
EIA/TIA-232E Short-Circuit Current			28	60	mA
MOUSE DRIVEABILITY					
Transmitter Output Voltage	T _{1N} = T _{2IN} = GND, T _{3IN} = V _{CC} , T _{3OUT} loaded with 3k Ω to GND, T _{1OUT} and T _{2OUT} loaded with 5mA	± 5			V

TIMING CHARACTERISTICS

(V_{CC} = 2.7V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data Rate		R _L = 3kΩ, C _L = 1000pF, one transmitter switching, 150pF load on each receiver		235	250		kbps
Receiver Output Enable Time	t _{ER}				70	200	ns
Receiver Output Disable Time	t _{DR}				420	700	ns
Transmitter Output Enable Time	t _{ET}	Includes power-supply start-up			250		μs
Transmitter Output Disable Time	t _{DT}				600		ns
Receiver Propagation Delay	t _{PHLR}	150pF load			630	2000	ns
	t _{PLHR}				630	2000	
Receiver Skew		t _{PHL} - t _{PLH}			40		ns
Transmitter Propagation Delay	t _{PHLT}	2500pF 3kΩ load			800	2000	ns
	t _{PLHT}				800	2000	
Transmitter Skew		t _{PHL} - t _{PLH}			52		ns
Transition-Region Slew Rate		R _L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V	C _L = 50pF to 2500pF	4.0	10	30	V/μs
			C _L = 50pF to 1000pF	6	13	30	
EN High to TRAN Reset Delay						5	μs
EN High Pulse Width						1	μs

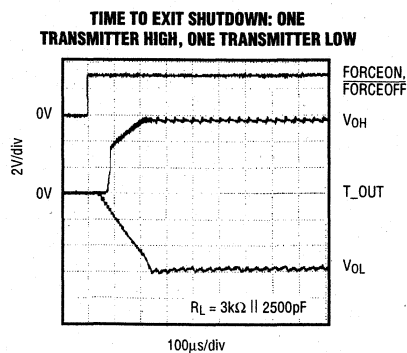
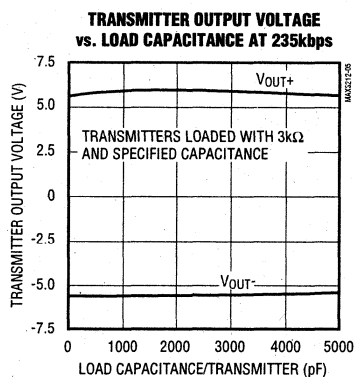
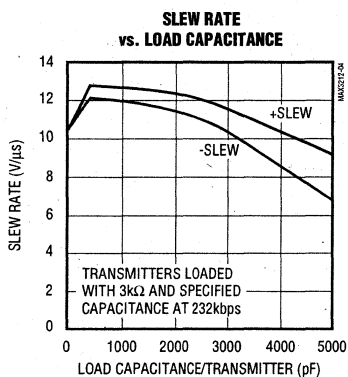
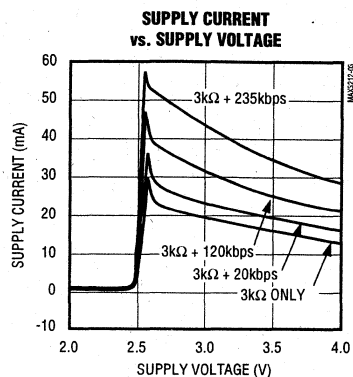
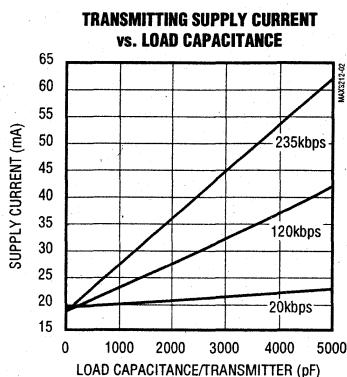
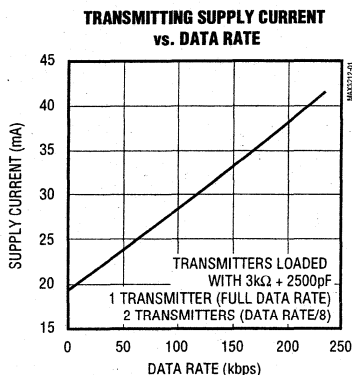
MAX3212

2

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)



+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

Pin Description

PIN	NAME	FUNCTION
1	LN	Inductor/Diode Connection Point
2	LP	Inductor/Diode Connection Point
3	VCC	Supply Voltage Input, 2.7V to 3.6V
4	EN	Receiver Enable Control. Drive EN low to force receiver outputs into a high-Z state. Drive EN high for normal operation. Cycle EN high then low to reset TRAN. TRAN is always low when EN is high.
5	TRAN	Transition Detection Output. TRAN latches high when a transition occurs on any receiver input while EN is low. Reset by cycling the EN pin high then low.
6	INVALID	Output of Invalid Signal Detector. Low if invalid RS-232 levels are present on all receiver inputs, otherwise high.
7	R5OUTB	Complementary Output of R5OUT—always active
8–12	R1OUT–R5OUT	Receiver Outputs. Swing from GND to VCC. High-impedance when EN is low.
13, 14, 15	T1IN, T2IN, T3IN	Transmitter Inputs
16	V-	Negative Supply generated on-board
17, 18, 19	T3OUT, T2OUT, T1OUT	Transmitter Outputs
20–24	R5IN–R1IN	Receiver Inputs
25	FORCEOFF	Drive low to shut down transmitters and on-board power supply, overriding all automatic circuitry and FORCEON (see Figure 3).
26	FORCEON	Drive high to override automatic circuitry, keeping transmitters on (see Figure 3). FORCEOFF = high.
27	V+	Positive Supply generated on-board
28	GND	Ground

Detailed Description

The MAX3212 line driver/receiver is intended for 3V-powered EIA/TIA-232E and V.28/V.24 communications interfaces where 3 drivers and 5 receivers are required. The operating voltage range extends from 3.6V down to 2.7V while still maintaining true RS-232 and EIA/TIA-562 transmitter output voltage levels.

The circuit comprises three sections: power supply, transmitters, and receivers. The power-supply section converts the supplied 3V to about $\pm 6.5V$, to provide the voltages necessary for the drivers to meet true RS-232 levels. External components are small and inexpensive.

The transmitters and receivers are guaranteed to operate at data rates of 235kbps.

The MAX3212 is equipped with Maxim's new proprietary AutoShutdown circuitry. This achieves a supply current of 1 μ A by shutting down the device when the RS-232 cable is disconnected or when the connected peripheral transmitters are turned off. While shut down, all receivers can remain active or can be disabled

under logic control. A complementary receiver remains active in all cases, enabling a system incorporating the MAX3212 to remain shut down and still monitor incoming RS-232 activity.

Three-state drivers on all receiver outputs are provided so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART.

Switch-Mode Power Supply

The switch-mode power supply uses a single inductor with two inexpensive diodes and two capacitors to generate $\pm 6.5V$ from the 2.7V to 3.6V input. The *Typical Operating Circuit* shows the complete circuit for the power supply.

Use a 15 μ H inductor with a saturation current rating of at least 350mA and under 1 Ω resistance. Use 1N6050 diodes or equivalent. Surface-mount equivalents for the 1N6050 include the Motorola MMBD6050LT1, Philips PMBD6050, and Allegro (formerly Sprague) TMPD6050LT.

For C1 and C2, use ceramic capacitors with values no less than indicated in the *Typical Operating Circuit*. These capacitors determine the ripple on V+ and V-, but

MAX3212

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+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

not the absolute voltages. Increasing the size of C1 and C2 increases the time V₊ and V₋ take to reach their final value. Bypass V_{CC} to GND with at least 0.33 μ F close to the MAX3212. Increase this to 4.7 μ F if there are no other V_{CC} supply bypass components less than 6 inches (15cm) away from the MAX3212.

Component suppliers are listed in Table 1.

RS-232 Drivers

All three drivers are identical and deliver EIA/TIA-232E and EIA/TIA-562 output voltage levels when V_{CC} is between 2.7V and 3.6V. When FORCEOFF is driven low or when the AutoShutdown circuitry senses invalid voltage levels at all receiver inputs, the drivers are disabled and the outputs are forced into a high-impedance state.

RS-232 Receivers

The MAX3212 receivers convert RS-232 signals to CMOS-logic output levels. All receivers have one inverting three-state output. Receiver 5 also has a complementary (noninverting) output. In shutdown, all five

inverting receivers can be either active or inactive under logic control.

The complementary output (R5OUTB) is always active, regardless of the state of EN or the part's shutdown status. R5OUTB can monitor RS-232 activity while the other receivers are high impedance. This allows Ring Indicator to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where the UART's V_{CC} is set to 0V in shutdown. (See Figure 2.)

Enable Control

The EN input has two functions: It allows enabling/disabling of the receivers, and it is used to reset the transition detector.

Driving EN low places five inverting receiver outputs (R_{OUT}) into a high-impedance state. R5OUTB is always active, regardless of the state of EN or the part's shutdown status (Table 2). EN has no effect on T_{OUT}.

EN also resets the transition detector. Drive EN high and then low to reset the TRAN output low. TRAN goes high when a transition occurs on any receiver input.

Table 1. Suggested Component Suppliers

MANUFACTURER	PART NUMBER	PHONE	FAX
Diodes			
Allegro	TMPD6050LT	USA (508) 853-5000	USA (508) 853-5049
Motorola	MMBD6050LT1	USA (408) 749-0510	USA (408) 991-7420
Philips	PMBD6050	USA (401) 762-3800	USA (401) 767-4493
Inductors			
Murata-Erie	LQH4N150K-TA	USA (404) 436-1300 Japan (075) 951-9111	USA (404) 684-1541 Japan (075) 955-6526
Sumida	CD43150	USA (708) 956-0666 Japan (03) 3607-5111	USA (708) 956-0702 Japan (03) 3607-5428
TDK	NLC453232T-150K	USA (708) 803-6100 Japan (03) 3278-5111	USA (708) 803-6296 Japan (03) 3278-5358

Table 2. AutoShutdown Logic

RS-232 SIGNAL PRESENT AT RECEIVER INPUT	FORCEOFF INPUT	FORCEON INPUT	INVALID OUTPUT	TRANSCIEVER STATUS
Yes	H	X	H	Normal Operation
No	H	H	L	Normal Operation (Forced On)
No	H	L	L	Shutdown (AutoShutdown)
Yes	L	X	H	Shutdown (Forced Off)
No	L	X	L	Shutdown (Forced Off)

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

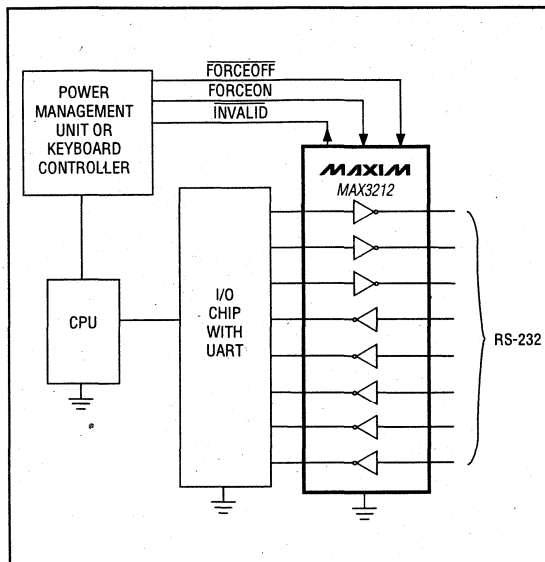


Figure 1. Interface Under Control of PMU

AutoShutdown

A 1 μ A supply current is achieved with Maxim's new AutoShutdown feature, which operates when **FORCEON** is low and **FORCEOFF** is high. When the MAX3212 senses no valid signal level on any receiver input for typically 30 μ s, the on-board power supply and drivers shut down. Internal 5k Ω resistors pull the receiver inputs to ground, disabling the transmitters and reducing supply current to 1 μ A when the device is in AutoShutdown mode. This occurs if the RS-232 cable is disconnected or if the connected peripheral transmitters are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system. When using the AutoShutdown feature, **INVALID** is high when the device is on and low when the device is shut down. The **INVALID** output indicates the condition of the receiver inputs; **INVALID** can be used in any mode.

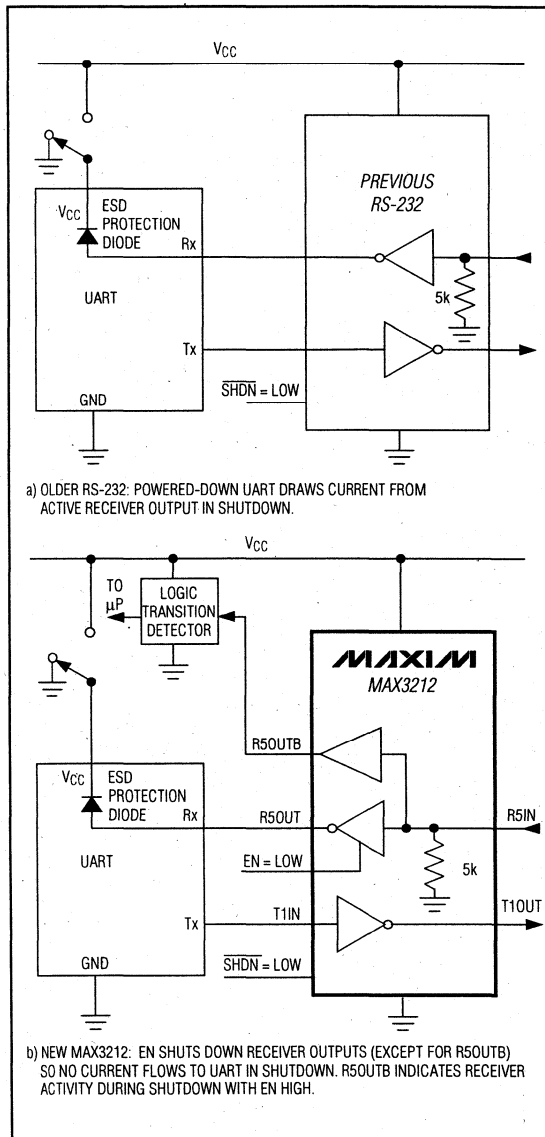


Figure 2. Detection of RS-232 Activity when the UART and Interface Are Shut Down: MAX3212 (b) vs. Previous Transceivers (a)

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

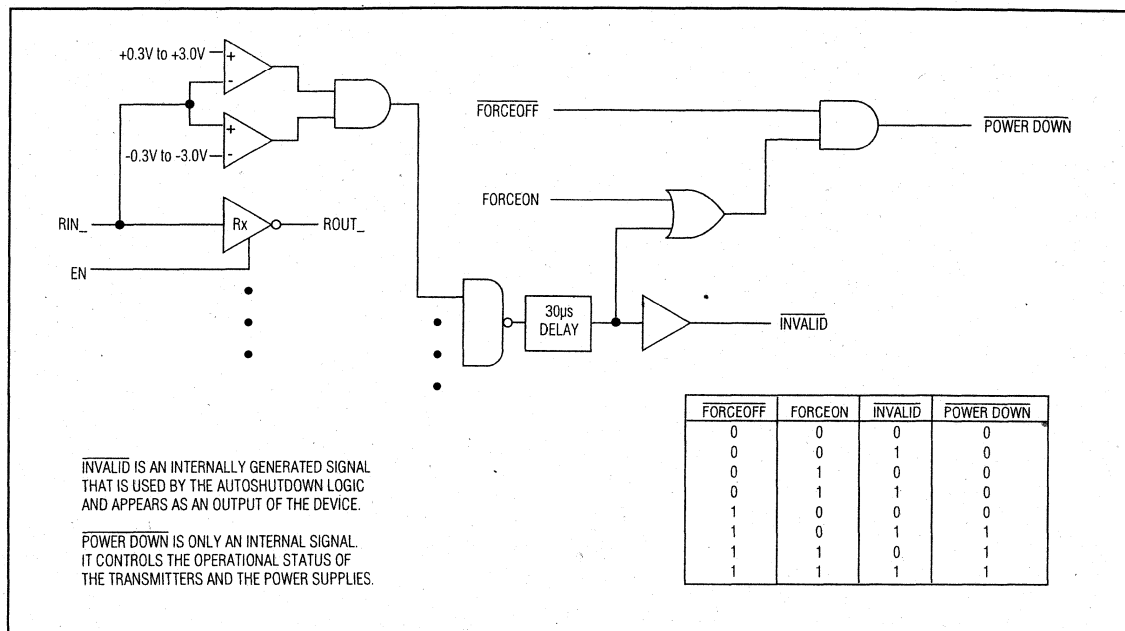


Figure 3. AutoShutdown Logic

Table 2 summarizes the MAX3212 operating modes. FORCEON and FORCEOFF override the automatic circuitry and force the transceiver into its normal operating state or into its low-power standby state. When neither control is asserted, the IC selects between these states automatically based on receiver input levels. Figure 4 depicts valid and invalid RS-232 receiver levels. The MAX3212 shuts down after sensing invalid RS-232 levels for greater than 30 μ s, ensuring the AutoShutdown mode is not enabled for slow-moving signals (1V/ μ s).

A mouse or another system with AutoShutdown may need a period of time to wake up. Figure 5 shows a circuit that forces the transmitters on for 100ms after start-up, allowing enough time for the other system to realize that the MAX3212 system is awake. If the other system outputs valid RS-232 signals within that time, the RS-232 ports on both systems remain enabled.

Transition Detector

The MAX3212 also has an on-board transition detector that monitors activity on the receiver inputs. In systems with a sleep mode, the transition detector output (TRAN) can be used to wake up the system when activity at the receiver inputs is detected. Before putting the system to sleep, set TRAN low by cycling EN high and then low. TRAN remains low as long as no activity is detected on the receiver inputs. When any receiver is toggled, TRAN latches high. Connect TRAN to a microprocessor interrupt, or if the system wakes up periodically TRAN can be polled. Transition detection is useful when valid RS-232 levels are present at the receiver inputs but no data is being sent. For example, if a printer is attached to the serial port but is not in use, the microprocessor senses this and forces the MAX3212 off.

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

MAX3212

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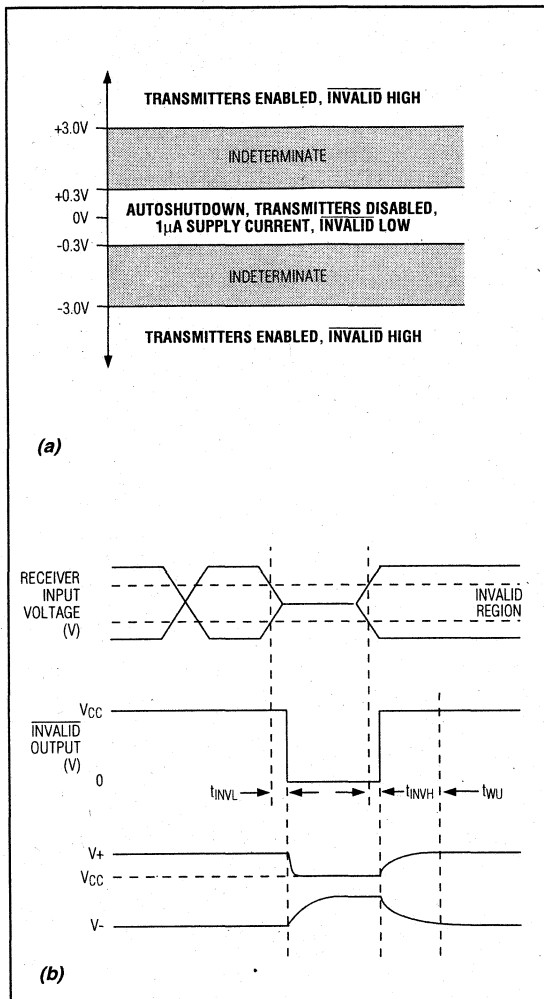


Figure 4. AutoShutdown Trip Levels

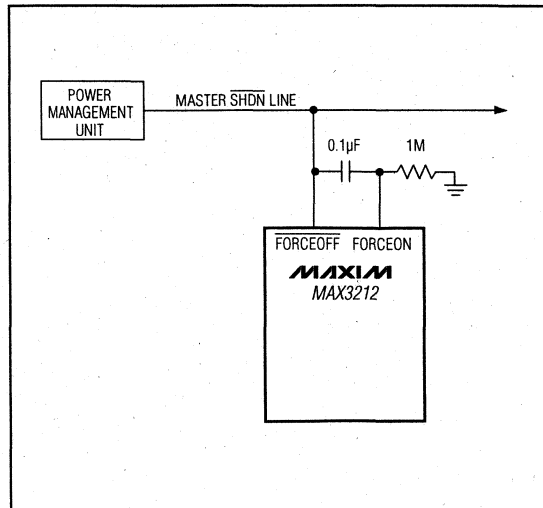


Figure 5. AutoShutdown with Initial Turn-On to Wake Up a Mouse or Another System

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

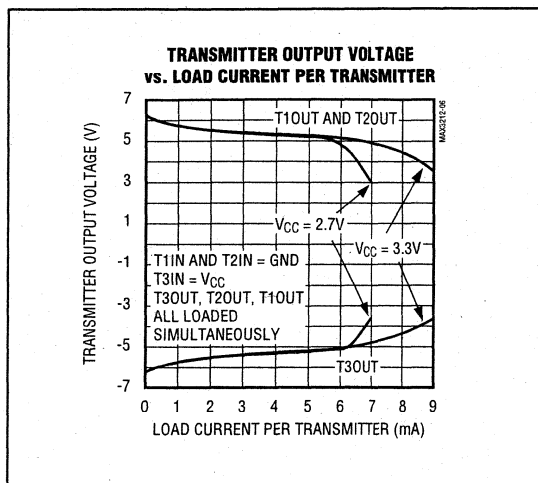


Figure 6. Mouse Emulation Circuit Current

Driving the MAX3212 from 5V Logic

The MAX3212 can directly interface with various 5V logic families, including ACT and HCT CMOS.

Mouse Driveability

The MAX3212 has been specifically designed to power serial mice while operating from low-voltage power supplies. It has been tested with samples of ten major mouse models from six manufacturers, including the leading three, Logitech (5 models), Mouse Systems, and Microsoft. The MAX3212 successfully drove all serial mice and met their respective current and voltage requirements.

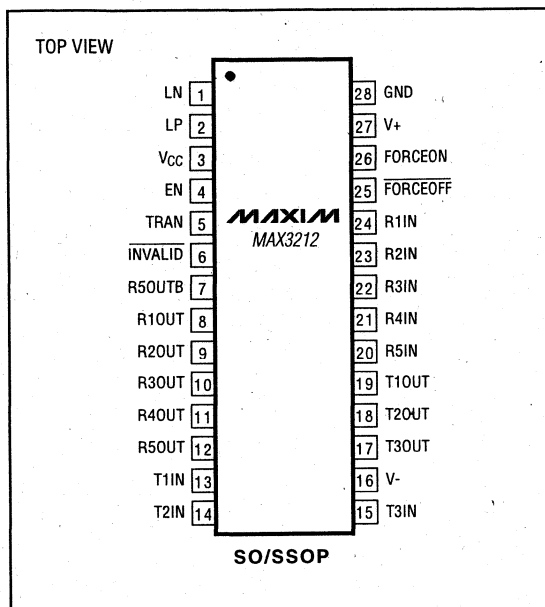
Figure 6 shows the transmitter output voltages under increasing load current. The MAX3212's switching regulator ensures the transmitters will supply at least $\pm 5V$ during worst-case load conditions.

+3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

PART	POWER-SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	GUAR-ANTEED DATA RATE (kbps)	EIA/TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	120	232	Drives mice
MAX218	1.8 to 4.25	2/2	2	120	232	Operates directly from batteries without a voltage regulator
MAX562	2.7 to 5.25	3/5	5	230	562	Wide supply range
MAX563	3.0 to 3.6	2/2	2	230	562	0.1 μ F capacitors
MAX3212	2.7 to 3.6	3/5	5	235	232	AutoShutdown, complementary receiver, drives mice, transient detection
MAX3222	3.0 to 5.5	2/2	2	120	232	0.1 μ F capacitors
MAX3223	3.0 to 5.5	2/2	2	120	232	0.1 μ F capacitors, AutoShutdown
MAX3232	3.0 to 5.5	2/2	N/A	120	232	0.1 μ F capacitors
MAX3241	3.0 to 5.5	3/5	5	120	232	0.1 μ F capacitors, 2 complementary receivers, drives mice
MAX3243	3.0 to 5.5	3/5	1	120	232	0.1 μ F capacitors, AutoShutdown, complementary receiver, drives mice

+2.7V to +3.6V-Powered, 1 μ A Supply Current, 3-Driver/5-Receiver, True RS-232 Transceiver

Pin Configuration



MAX3212

2

MAXIM

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

General Description

The MAX3218 RS-232 transceiver is intended for battery-powered EIA/TIA-232E and V.28/V.24 communications interfaces that need two drivers and two receivers with minimum power consumption from a single low-voltage supply. It provides a wide +1.8V to +4.25V operating voltage range while maintaining true RS-232 and EIA/TIA-562 voltage levels. The MAX3218 runs from two alkaline, NiCd, or NiMH cells without any form of voltage regulator. A guaranteed 120kbps data rate provides compatibility with popular software for communicating with personal computers.

Supply current is reduced to 1 μ A with Maxim's new AutoShutdown™ feature. When the MAX3218 does not sense a valid signal level on the receiver inputs, the on-board power-supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to either RS-232 receiver input. As a result, the system saves power without changes to the existing software. Additionally, the MAX3218 can be forced into or out of shutdown, under logic control.

While shut down, all receivers can remain active or can be disabled under logic control, permitting a system incorporating the CMOS MAX3218 to monitor external devices while in low-power shutdown. Three-state drivers are provided on both receiver outputs so that multiple receivers, generally of different interface standards, can be on the same bus. The MAX3218 is available in 20-pin DIP and SSOP packages.

Applications

Battery-Powered Equipment
Subnotebook Computers
PDAs
Hand-Held Equipment
Peripherals
Cellular Phones

* Patent Pending

™ AutoShutdown is a trademark of Maxim Integrated Products.

Features

BETTER THAN BIPOLAR!

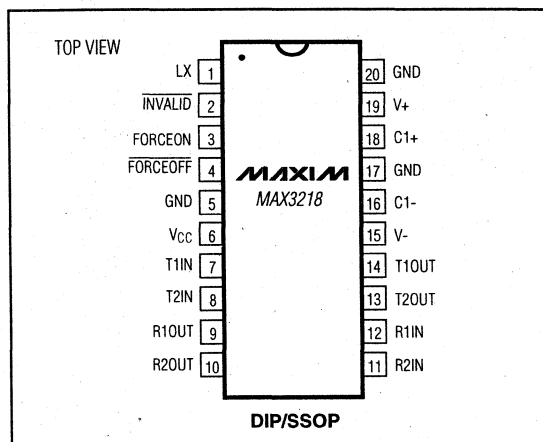
- ♦ 1 μ A Supply Current Using AutoShutdown™
- ♦ Operates Directly from Two Alkaline, NiCd or NiMH Cells
- ♦ +1.8V to +4.25V Single-Supply Voltage Range
- ♦ 120kbps Data Rate Guaranteed
- ♦ Low-Cost Surface-Mount Components
- ♦ Meets EIA/TIA-232E Specifications
- ♦ Three-State Receiver Outputs
- ♦ Flow-Through Pinout
- ♦ On-Board DC-DC Converters
- ♦ 20-Pin SSOP and DIP Packages

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3218CPP	0°C to +70°C	20 Plastic DIP
MAX3218CAP	0°C to +70°C	20 SSOP
MAX3218C/D	0°C to +70°C	Dice†
MAX3218EPP	-40°C to +85°C	20 Plastic DIP
MAX3218EAP	-40°C to +85°C	20 SSOP

† Contact factory for dice specifications.

Pin Configuration


MAX3218*
2
MAXIM

Maxim Integrated Products 2-49

Call toll free 1-800-998-8800 for free samples or literature.

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

ABSOLUTE MAXIMUM RATINGS

Supply Voltages

V _{CC}	-0.3V to +4.6V
V ₊	(V _{CC} - 0.3V) to +7.5V
V ₋	+0.3V to -7.4V
V _{CC} to V ₋	+12V
LX.....	-0.3V to (1V + V ₊)

Input Voltages

T _{IN} , FORCEON, FORCEOFF.....	-0.3V to +7V
R _{IN}	±25V

Output Voltages

T _{OUT}	±15V
R _{OUT}	-0.3V to (V _{CC} + 0.3V)

Short-Circuit Duration, R_{OUT}, T_{OUT} to GND Continuous

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 11.11mW/°C above +70°C)889mW

SSOP (derate 8.00mW/°C above +70°C)640mW

Operating Temperature Ranges

MAX3218C_P..... 0°C to +70°C

MAX3218E_P..... -40°C to +85°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (soldering, 10sec) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{CC} = 1.8V to 4.25V, C1 = 0.47 μ F, C2 = C3 = C4 = 1 μ F, L1 = 15 μ H, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.0V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Operating Voltage Range		1.8		4.25	V
Supply Current, AutoShutdown™	V _{CC} = 3.0V, T _A = +25°C, all R _{IN} open, FORCEON = GND, FORCEOFF = V _{CC}		1.0	10	μ A
Supply Current, Shutdown	FORCEOFF = GND, T _A = +25°C, V _{CC} = 3.0V		1.0	10	μ A
Supply Current, AutoShutdown™ Disabled	FORCEON = FORCEOFF = V _{CC} = 3.0V, no load		2.0	3.0	mA
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold Low	T _{IN} , FORCEON, FORCEOFF			0.33 x V _{CC}	V
Input Logic Threshold High	T _{IN} , FORCEON, FORCEOFF	0.67 x V _{CC}			V
Input Leakage Current	T _{IN} , FORCEON = FORCEOFF = 0V or V _{CC}		0.001	±1	μ A
Output Voltage Low	R _{OUT} , I _{OUT} = 1.0mA			0.4	V
Output Voltage High	R _{OUT} , I _{OUT} = -0.4mA	V _{CC} - 0.25	V _{CC} - 0.08		V
Output Leakage Current	R _{OUT} , 0V ≤ R _{OUT} ≤ V _{CC} , FORCEON = FORCEOFF = 0V		0.05	±10	μ A
AUTOSHUTDOWN (FORCEON = GND, FORCEOFF = V_{CC})					
Receiver Input Thresholds, Transmitters Enabled	Figure 4a	Positive threshold		2.8	V
		Negative threshold	-2.8		
Receiver Input Thresholds Transmitters Disabled	1 μ A supply current, Figure 4a	-0.3		0.3	V
INVALID Output Low Voltage	I _{OUT} = 1.0mA, -0.3V < R _{IN} < 0.3V			0.4	V
INVALID Output High Voltage	I _{OUT} = -0.4mA, R _{IN} > 2.8V	V _{CC} - 0.25			V

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

MAX3218

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = 1.8V to 4.25V, C_1 = 0.47 μ F, C_2 = C_3 = C_4 = 1 μ F, L_1 = 15 μ H, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at V_{CC} = 3.0V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS					
Input Voltage Range		-25		+25	V
Input Threshold Low	V_{CC} = 2.0V to 4.25V	0.4			V
	V_{CC} = 1.8V to 4.25V	0.3			
Input Threshold High	V_{CC} = 1.8V to 4.25V			3.0	V
	V_{CC} = 1.8V to 3.6V			2.8	
Input Hysteresis			0.7		V
Input Resistance	-15V < R_{IN} < 15V	3	5	7	k Ω
EIA/TIA-232E TRANSMITTER OUTPUTS					
Output Voltage Swing	All transmitter outputs loaded with 3k Ω to ground	± 5	± 6		V
Output Resistance	V_{CC} = 0V, -2V < T_{OUT} < 2V	300			Ω
Output Short-Circuit Current			± 24	± 100	mA

TIMING CHARACTERISTICS

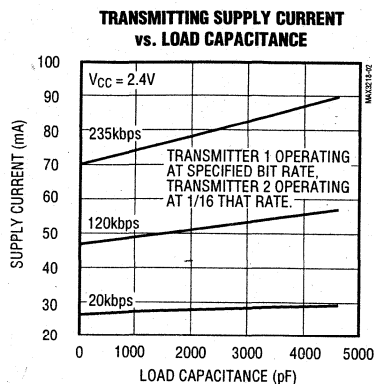
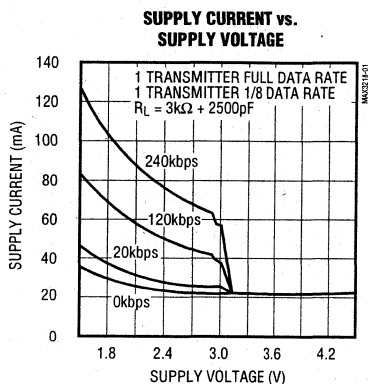
(Circuit of Figure 1, V_{CC} = 1.8V to 4.25V, C_1 = 0.47 μ F, C_2 = C_3 = C_4 = 1 μ F, L_1 = 15 μ H, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at V_{CC} = 3.0V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate		2500pF 3k Ω load each transmitter, one transmitter switching, 150pF load each receiver	120	235		kbps
Receiver Output Enable Time	t_{ER}			90	300	ns
Receiver Output Disable Time	t_{DR}			200	500	ns
Transmitter Output Enable Time	t_{ET}			250	450	μ s
Transmitter Output Disable Time	t_{DT}			500		ns
Receiver Propagation Delay	t_{PHLR}	150pF load		290	1000	ns
	t_{PLHR}	150pF load		260	1000	
Transmitter Propagation Delay	t_{PHLT}	2500pF 3k Ω load		1.9	2.7	μ s
	t_{PLHT}	2500pF 3k Ω load		1.8	2.7	
Transition Region Slew Rate		T_A = +25°C, V_{CC} = 3.0V, R_L = 3k Ω to 7k Ω , C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V	3.0		30	V/ μ s
AUTOSHUTDOWN TIMING						
Receiver Threshold to Transmitters Enabled	t_{WU}	Figure 4b		250		μ s
Receiver Positive or Negative Threshold to INVALID High	t_{INVH}	Figure 4b		1		μ s
Receiver Positive or Negative Threshold to INVALID Low	t_{INVL}	Figure 4b		30		μ s

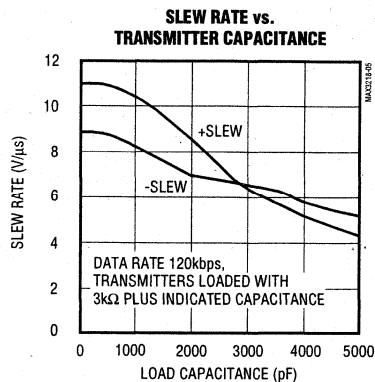
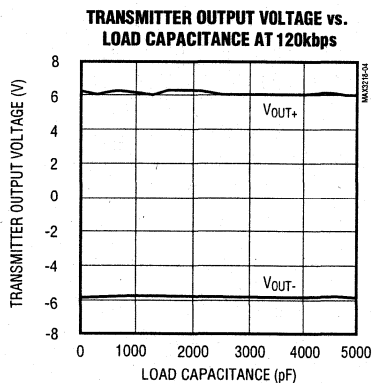
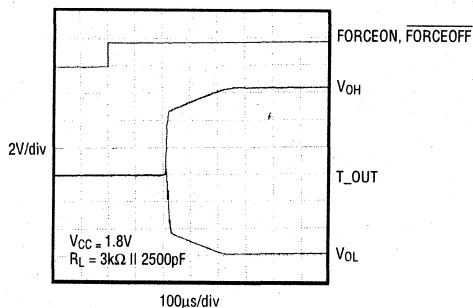
1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

Typical Operating Characteristics

(Circuit of Figure 1, $V_{CC} = 1.8V$, all transmitter outputs loaded with $3k\Omega$, $T_A = +25^\circ C$, unless otherwise noted.)



TIME TO EXIT SHUTDOWN (ONE TRANSMITTER HIGH, ONE TRANSMITTER LOW)



1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

Pin Description

MAX3218

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PIN	NAME	FUNCTION
1	LX	Inductor/Diode Connection Point
2	INVALID	Output of Invalid Signal Detector. Low if invalid RS-232 levels are present on all receiver inputs, otherwise high.
3	FORCEON	Drive high when FORCEOFF = high to override automatic circuitry, keeping transmitters on.
4	FORCEOFF	Drive low to shut down transmitters and on-board power supply, overriding all automatic circuitry and FORCEON.
5, 17, 20	GND	Ground
6	VCC	Supply Voltage Input, 1.8V to 4.25V. Bypass to GND with at least 1 μ F.
7, 8	T1IN, T2IN	Transmitter Inputs
9, 10	R1OUT, R2OUT	Receiver Outputs
11, 12	R2IN, R1IN	Receiver Inputs
13, 14	T2OUT, T1OUT	Transmitter Outputs, swing between V+ and V-
15	V-	Negative Supply generated on-board
16, 18	C1-, C1+	Terminal for Charge-Pump Capacitor
19	V+	Positive Supply generated on-board

Detailed Description

The MAX3218 line driver/receiver is intended for battery-powered EIA/TIA-232 and V.28/V.24 communications interfaces that require two drivers and two receivers. The operating voltage extends from 1.8V to 4.25V, yet the device maintains true RS-232 and EIA/TIA-562 transmitter output voltage levels. This wide supply voltage range permits direct operation from a variety of batteries without the need for a voltage regulator. For example, the MAX3218 can be run directly from a single lithium cell or a pair of alkaline cells. It can also be run directly from two NiCd or NiMH cells from full-charge voltage down to the normal 0.9V/cell end-of-life point. The 4.25V maximum supply voltage allows the two rechargeable cells to be trickle- or fast-charged while driving the MAX3218.

The circuit comprises three sections: power supply, transmitters, and receivers. The power-supply section converts the supplied input voltage to 6.5V, providing the voltages necessary for the drivers to meet true RS-232 levels. External components are small and inexpensive.

The transmitters and receivers are guaranteed to operate at 120kbps data rates, providing compatibility with LapLink™ and other high-speed communications software.

The MAX3218 is equipped with Maxim's new proprietary AutoShutdown™ circuitry. This achieves a 1 μ A supply current by shutting down the device when the RS-232 cable is disconnected or when the connected peripheral transmitters are turned off. While shut down, both receivers can remain active or can be disabled under logic control. With this feature, the MAX3218 can be in low-power shutdown mode and still monitor activity on external devices. Three-state drivers are provided on both receiver outputs.

Three-state drivers on both receiver outputs are provided so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART.

Switch-Mode Power Supply

The switch-mode power supply uses a single inductor with one diode and three small capacitors to generate ± 6.5 V from an input voltage in the 1.8V to 4.25V range.

Inductor Selection

Use a 15 μ H inductor with a saturation current rating of at least 350mA and less than 1 Ω resistance. Table 1 lists suppliers of inductors that meet the 15 μ H/350mA/1 Ω specifications.

™ LapLink is a trademark of Traveling Software, Inc.
AutoShutdown is a trademark of Maxim Integrated Products.

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

Table 1. Suggested Component Suppliers

MANUFACTURER	PART NUMBER	PHONE	FAX
Inductors			
Murata-Erie	LQH4N150K-TA	USA (814) 237-1431	USA (814) 238-0490
Sumida	CD43150	USA (708) 956-0666 Japan (03) 3607-5111	USA (708) 956-0702 Japan (03) 3607-5428
TDK	NLC453232T-150K	USA (708) 803-6100 Japan (03) 3278-5111	USA (708) 803-6296 Japan (03) 3278-5358
Diodes—Surface-Mount			
Allegro	TMPD6050LT	USA (508) 853-5000	USA (508) 853-7556
Central Semiconductor	CMPSH-3 (Schottky)	USA (516) 435-1110	USA (516) 435-1824
Motorola	MMBD6050LT1 (silicon)	USA (408) 749-0510	USA (408) 991-7420
Philips	PMBD6050 (silicon)	USA (401) 762-3800	USA (401) 767-4493
Diodes—Through-Hole			
Motorola	1N6050 (silicon), 1N5817 (Schottky)	USA (408) 749-0510	USA (408) 991-7420

Diode Selection

Key diode specifications are fast recovery time (<10ns), average current rating (>100mA), and peak current rating (>350mA). Inexpensive fast silicon diodes, such as the 1N6050, are generally recommended. More expensive Schottky diodes improve efficiency and give slightly better performance at very low V_{CC} voltages. Table 1 lists suppliers of both surface-mount and through-hole diodes. 1N914s are usually satisfactory, but specifications and performance vary widely with different manufacturers.

Capacitor Selection

Use capacitors with values at least as indicated in Figure 1. Capacitor C2 determines the ripple on V_+ , but not the absolute voltage. Capacitors C1 and C3 determine both the ripple and the absolute voltage of V_- . Bypass V_{CC} to GND with at least 1 μ F (C4) placed close to pins 5 and 6. If the V_{CC} line is not bypassed elsewhere (e.g., at the power supply), increase C4 to 4.7 μ F.

You may use ceramic or polarized capacitors in all locations. If you use polarized capacitors, tantalum types are preferred because of the high operating frequency of the power supplies (about 250kHz). If aluminum electrolytics are used, higher capacitance values may be required.

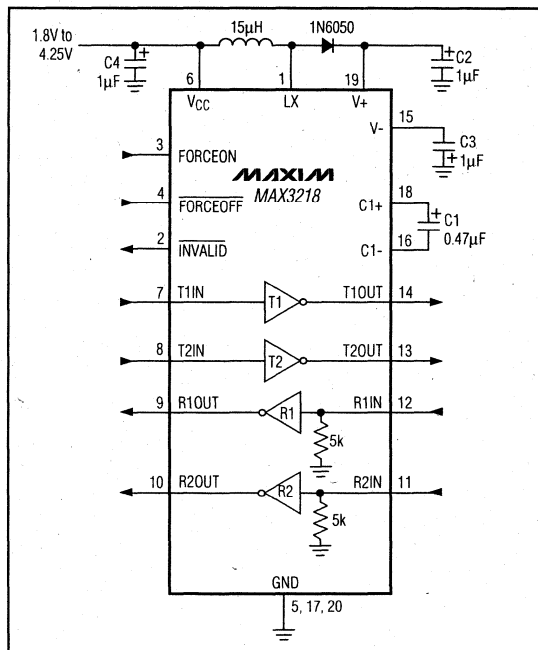


Figure 1. Typical Operating Circuit

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

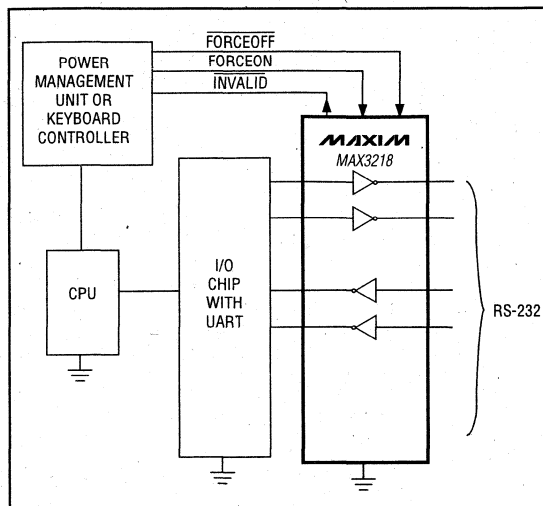


Figure 2. Interface Under Control of PMU

RS-232 Drivers

The two drivers are identical, and deliver EIA/TIA-232E and EIA/TIA-562 output voltage levels when V_{CC} is between 1.8V and 4.25V. One transmitter can drive up to 3k Ω in parallel with 2500pF at up to 120kbps. Connect unused drivers to either GND or V_{CC} . When **FORCEOFF** is driven low, or when AutoShutdown circuitry senses invalid voltage levels at **all** receiver inputs, the drivers are disabled and their outputs are forced into a high-impedance state. Driver inputs do not have internal pull-up resistors.

RS-232 Receivers

The two receivers are identical, and accept both EIA/TIA-232E and EIA/TIA-562 input signals. The CMOS receiver outputs are inverting and swing rail-to-rail. Receivers are disabled only when **FORCEON** and **FORCEOFF** inputs are low. (See Table 2.)

Table 3. AutoShutdown Logic

RS-232 SIGNAL PRESENT AT RECEIVER INPUT	FORCEOFF INPUT	FORCEON INPUT	INVALID OUTPUT	TRANSCIEVER STATUS
Yes	H	X	H	Normal Operation
No	H	H	L	Normal Operation (Forced On)
No	H	L	L	Shutdown (AutoShutdown)
Yes	L	X	H	Shutdown (Forced Off)
No	L	X	L	Shutdown (Forced Off)

Table 2. Receiver Status

FORCEON	FORCEOFF	RECEIVER STATUS
X	H	Receiver Enabled
H	X	
L	L	Receiver Disabled

Shutdown

When **FORCEOFF** is low, power supplies are disabled and the transmitters are placed in a high-impedance state. Receiver operation is not affected by taking **FORCEOFF** low. Power consumption is dramatically reduced in shutdown mode. Supply current is minimized when the receiver inputs are static in any one of three states: floating (ground), GND, or V_{CC} .

AutoShutdown™

A 1 μ A supply current is achieved with Maxim's new AutoShutdown feature, which operates when **FORCEON** is low and **FORCEOFF** is high. When the MAX3218 senses no valid signal level on either receiver input for typically 30 μ s, the on-board power supply and drivers shut down, reducing supply current to 1 μ A. Internal 5k Ω resistors pull undriven receiver inputs to ground. This occurs if the RS-232 cable is disconnected or if the connected peripheral transmitters are turned off. The system turns on again when a valid level is applied to either RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system. When using the AutoShutdown feature, **INVALID** is high when the device is on and low when the device is shut down. The **INVALID** output indicates the condition of the receiver inputs.

Table 3 summarizes the MAX3218 operating modes. **FORCEON** and **FORCEOFF** override the automatic circuitry and force the transceiver into its normal operating state or into its low-power standby state. When neither control is asserted, the IC selects between these states automatically based on receiver input levels. Figure 4 depicts valid and invalid RS-232 receiver levels. The

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

MAX3218 shuts down after sensing invalid RS-232 levels for greater than 30 μ s, ensuring that the AutoShutdown mode is not enabled for slow-moving signals (>1V/ μ s).

Another system with AutoShutdown may need a period of time to wake up. Figure 5 shows a circuit that forces the transmitters on for 100ms after start-up, allowing enough time for the other system to realize that the MAX3218 system is awake. If the other system outputs valid RS-232 signals within that time, the RS-232 ports on both systems remain enabled.

Applications Information

Operation from Regulated/Unregulated Dual System Power Supplies

The MAX3218 is intended for use with three different power-supply sources: it can be powered directly from a battery, from a 3.0V or 3.3V power supply, or simultaneously from both. Figure 1 shows the single-supply configuration. Figure 6 shows the circuit for operation from both a 3V supply and a raw battery supply—an ideal configuration where a regulated 3V supply is being derived from two cells. In this application, the MAX3218's logic levels remain appropriate for interface with 3V logic, yet most of the power for the MAX3218 is

drawn directly from the battery, without suffering the efficiency losses of the DC-DC converter. This prolongs battery life.

Bypass the input supplies with 0.1 μ F at V_{CC} (C4) and at least 1 μ F at the inductor (C5). Increase C5 to 4.7 μ F if the power supply has no other bypass capacitor connected to it.

Low-Power Operation

The following suggestions will help you get maximum life out of your batteries.

Transmit at the highest practical data rate. Although this raises the supply current while transmission is in progress, the transmission will be over sooner. If the MAX3218 is shut down (using **FORCEOFF**) as soon as each transmission ends, this practice will save energy.

Operate your whole system from the raw battery voltage rather than suffer the losses of a regulator or DC-DC converter. If this is not possible, but your system is powered from two cells and employs a 3V DC-DC converter to generate the main logic supply, use the circuit of Figure 6. This circuit draws most of the MAX3218's power straight from the battery, but still provides logic-level compatibility with the 3V logic.

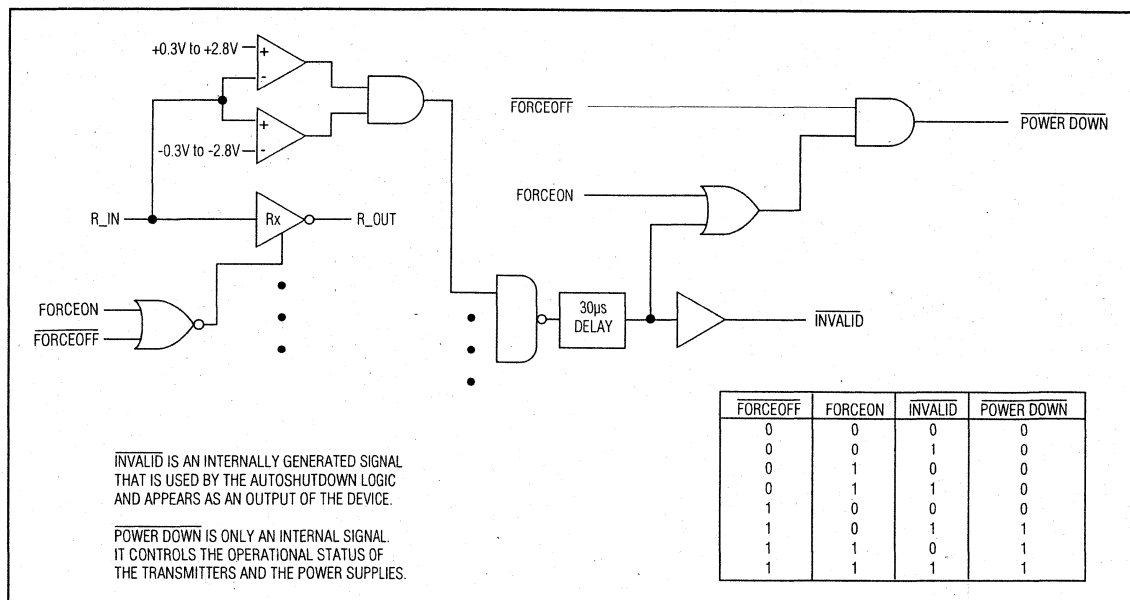


Figure 3. AutoShutdown Logic

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

MAX3218

2

Keep communications cables short to minimize capacitive loading. Lowering the capacitive loading on the transmitter outputs reduces the MAX3218's power consumption. Using short, low-capacitance cable also helps transmission at the highest data rates.

EIA/TIA-232E and EIA/TIA-562 Standards

RS-232 circuits consume much of their power because the EIA/TIA-232E standard demands that the transmitters deliver at least 5V to receivers with impedances that can be as low as 3k Ω . For applications where power consumption is critical, the EIA/TIA-562 standard provides an alternative.

EIA/TIA-562 transmitter output voltage levels need only reach ± 3.7 V, and because they have to drive the same 3k Ω receiver loads, the total power consumption is considerably reduced. Since the EIA/TIA-232E and EIA/TIA-562 receiver input voltage thresholds are the same, interoperability between EIA/TIA-232E and EIA/TIA-562 devices is guaranteed. Maxim's MAX560 and MAX561 are EIA/TIA-562 transceivers that operate on a single supply from 3.0V to 3.6V, and the MAX562 transceiver operates from 2.7V to 5.25V while producing EIA/TIA-562 levels.

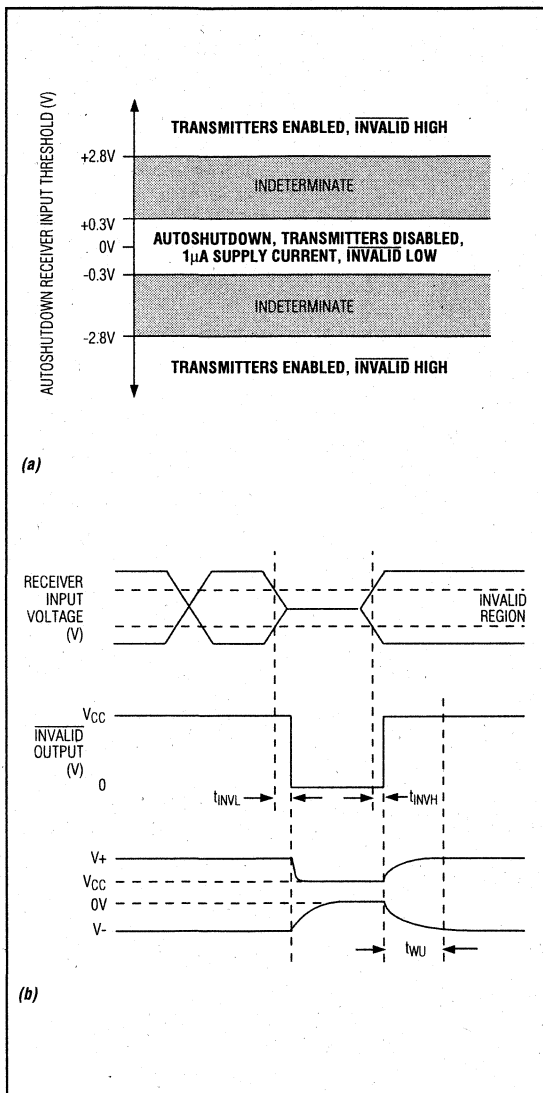


Figure 4. AutoShutdown Trip Levels

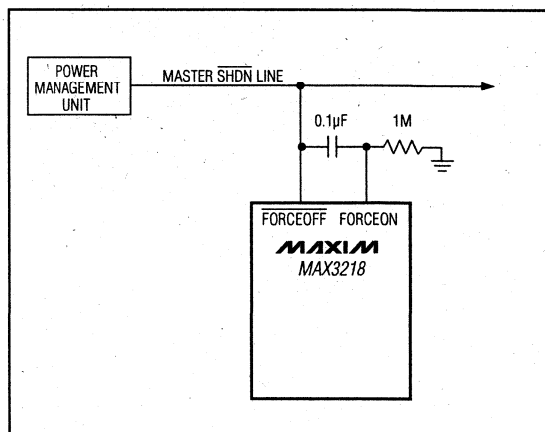
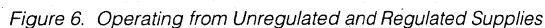


Figure 5. AutoShutdown with Initial Turn-On to Wake Up a System

MAX3218



1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

+3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

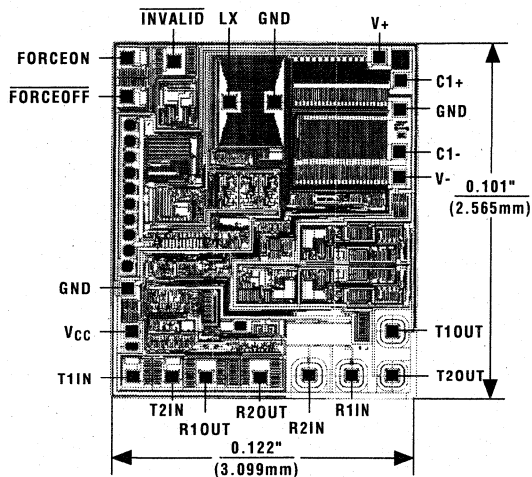
MAX3218

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PART	SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	GUARANTEED DATA RATE (kbps)	EIA/TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	120	232	Drives mice
MAX3212	2.7 to 3.6	3/5	5	120	232	AutoShutdown, complementary receiver, drives mice, transient detection
MAX218	1.8 to 4.25	2/2	2	120	232	Operates directly from a battery without a voltage regulator
MAX3218	1.8 to 4.25	2/2	2	120	232	Same as MAX218 but with AutoShutdown
MAX560	3.0 to 3.6	4/5	2	120	562	Pin-compatible with MAX213
MAX561	3.0 to 3.6	4/5	0	120	562	Pin-compatible with MAX214
MAX562	2.7 to 5.25	3/5	5	230	562	Wide supply range
MAX563	3.0 to 3.6	2/2	2	120	562	0.1 μ F capacitors
MAX3222	3.0 to 5.5	2/2	2	120	232	0.1 μ F capacitors
MAX3223	3.0 to 5.5	2/2	2	120	232	AutoShutdown, 0.1 μ F capacitors
MAX3232	3.0 to 5.5	2/2	2	120	232	Pin-compatible with MAX232
MAX3241	3.0 to 5.5	3/5	5	120	232	0.1 μ F capacitors, 2 complementary receivers, drives mice
MAX3243	3.0 to 5.5	3/5	1	120	232	0.1 μ F capacitors, AutoShutdown, complementary receiver, drives mice

1 μ A Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown™

Chip Topography



TRANSISTOR COUNT: 571
SUBSTRATE CONNECTED TO GND



3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

General Description

The MAX3222/MAX3232/MAX3241 have a proprietary low-dropout transmitter output stage enabling true RS-232 performance from 3.0V to 5.5V supplies with a dual charge pump. The devices require only four small 0.1 μ F external capacitors and are guaranteed to run at data rates of 120kbps while maintaining RS-232 output levels.

These devices are ideal for 3.3V-only systems, mixed 3.3V and 5V systems, or 5V-only systems that require true RS-232 performance.

The MAX3222/MAX3232 have two receivers and two drivers. The MAX3222 has a 1 μ A shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1 μ A supply current. The MAX3222 is pin, package, and functionally compatible with the industry-standard MAX242, and the MAX3232 with the industry-standard MAX232.

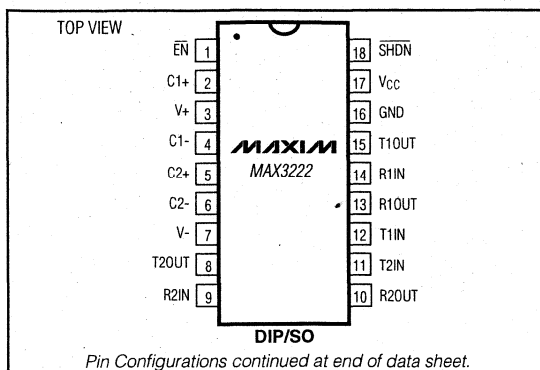
The MAX3241 is a complete serial port (3 drivers/5 receivers) designed for notebook and subnotebook computers. In shutdown, all 5 receivers can remain active while using only 1 μ A supply current. Receivers R1 and R2 have two extra outputs in addition to their standard outputs. These extra outputs are always active, allowing external devices such as a modem to be monitored without forward biasing the protection diodes in circuitry that may have V_{CC} completely removed.

The MAX3222 and MAX3241 are available in space-saving SSOP packages.

Applications

Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment
Peripherals
Printers

Pin Configurations



Features

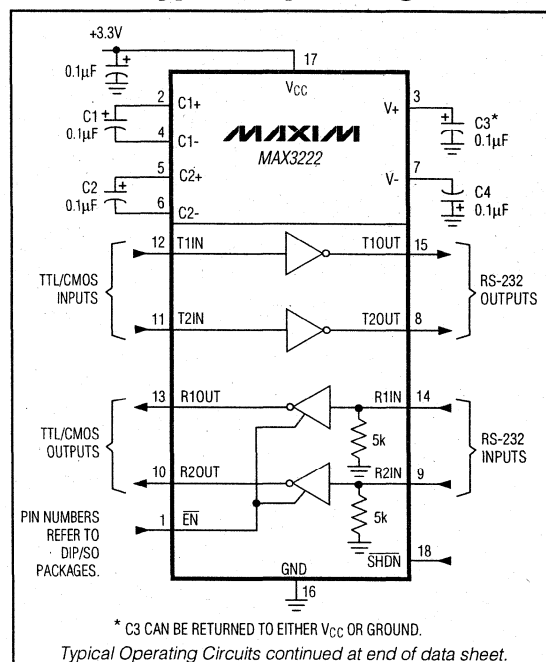
- ◆ Low 300 μ A Supply Current
- ◆ Guaranteed 120kbps Data Rate
- ◆ 1 μ A Low-Power Shutdown with Receivers Active (MAX3222/MAX3241)
- ◆ Flow-Through Pinout (MAX3241)
- ◆ Meets EIA/TIA-232 Specifications Down to 3.0V
- ◆ Guaranteed Mouse Driveability (MAX3241)
- ◆ Pin Compatible with Industry-Standard MAX232 (MAX3232)
Pin Compatible with Industry-Standard MAX242 (MAX3222)
- ◆ 6V/ μ s Guaranteed Slew Rate

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3222CPN	0°C to +70°C	18 Plastic DIP
MAX3222CWN	0°C to +70°C	18 Wide SO
MAX3222CAP	0°C to +70°C	20 SSOP

Ordering Information continued at end of data sheet.

Typical Operating Circuits



*Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.

MAXIM

Maxim Integrated Products 2-61

Call toll free 1-800-998-8800 for free samples or literature.

MAX3222/MAX3232/MAX3241*

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

ABSOLUTE MAXIMUM RATINGS

V _{CC}	-0.3V to +6V
V ₊ (Note 1).....	-0.3V to +7V
V ₋ (Note 1).....	+0.3V to -7V
(V ₊ + V ₋) (Note 1).....	+13V
Input Voltages	
T _{IN} , SHDN, EN.....	-0.3V to +6V
R _{IN}	±25V
Output Voltages	
T _{OUT}	±13.2V
R _{OUT}	-0.3V to (V _{CC} + 0.3V)
Short-Circuit Duration	
T _{OUT}	Continuous

Continuous Power Dissipation (T_A = +70°C)

16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)...	842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)	696mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C)	889mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C)	762mW
20-Pin SSOP (derate 8.00mW/°C above +70°C)	640mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) ...	1000mW
28-Pin SSOP (derate 9.52mW/°C above +70°C)	762mW

Operating Temperature Ranges

MAX32_ _C_	0°C to +70°C
MAX32_ _E_	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: V₊ and V₋ can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V, C₁–C₄ = 0.1 μ F (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
V _{CC} Power-Supply Current	No load, V _{CC} = 3.3V or 5.0V, T _A = +25°C		0.3	1.0	mA
Shutdown Supply Current	T _A = +25°C		1	10	μ A
LOGIC					
Input Logic Threshold Low	T _{IN} ; EN, SHDN (MAX3222/MAX3241 only)			0.8	V
Input Logic Threshold High	T _{IN} ; EN, SHDN (MAX3222/MAX3241 only)	V _{CC} = 3.3V	2.0		V
		V _{CC} = 5.0V	2.4		
Input Leakage Current	T _{IN} ; EN, SHDN = 0V or V _{CC} (MAX3222/MAX3241 only)		±0.01	±1.0	μ A
Output Leakage Current	EN = V _{CC} (MAX3222/MAX3241)		±0.05	±10	μ A
Output Voltage Low	I _{OUT} = 1.6mA			0.4	V
Output Voltage High	I _{OUT} = -1.0mA	V _{CC} - 0.6	V _{CC} - 0.1		V
RECEIVER INPUTS					
Input Voltage Range		-25		+25	V
Input Threshold Low	T _A = +25°C	V _{CC} = 3.3V	0.6	1.2	V
		V _{CC} = 5.0V	0.8	1.5	
Input Threshold High	T _A = +25°C	V _{CC} = 3.3V	1.5	2.4	V
		V _{CC} = 5.0V	1.8	2.4	
Input Hysteresis			0.3		V
Input Resistance	T _A = +25°C	3	5	7	k Ω
TRANSMITTER OUTPUTS					
Output Voltage Swing	All transmitter outputs loaded with 3k Ω to ground, V _{CC} = 3.15V to 5.5V	±5.0	±5.4		V
Output Resistance	V _{CC} = V ₊ = V ₋ = 0V, V _{OUT} = ±2V	300	10M		Ω
Output Short-Circuit Current		±35	±60		mA
Output Leakage Current	V _{OUT} = ±12V, V _{CC} = 0V or 3.0V to 5.5V, transmitters disabled, SHDN = 0V (MAX3222, MAX3241)		±25		μ A

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

ELECTRICAL CHARACTERISTICS (continued)

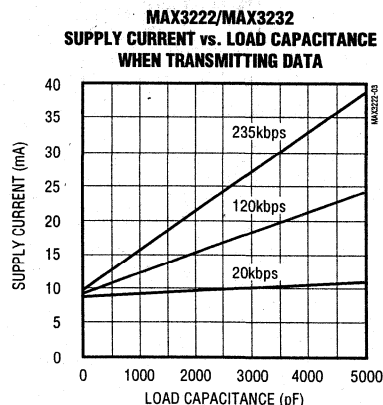
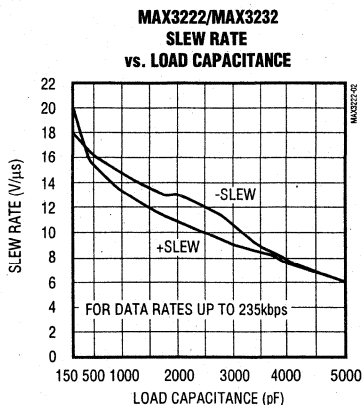
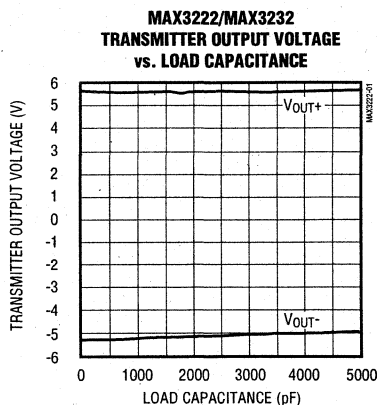
(V_{CC} = 3.0V to 5.5V, C_1 – C_4 = 0.1 μ F (Note 2), T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MOUSE DRIVEABILITY (MAX3241)					
Transmitter Output Voltage	$T1IN = T2IN = GND$, $T3IN = V_{CC}$, $T3OUT$ loaded with 3k Ω to GND, $T1OUT$ and $T2OUT$ loaded with 2.5mA each	± 5			V
TIMING CHARACTERISTICS					
Maximum Data Rate	$V_{CC} = 3.15V$ to 5.5V, $R_L = 3k\Omega$, $C_L = 1000pF$, one transmitter switching	120	235		kbps
Receiver Propagation Delay	R_{IN} to R_{OUT} , $C_L = 150pF$	t_{PHL}	0.3		μs
		t_{PLH}	0.3		
Receiver Output Enable Time	Normal operation (MAX3222/MAX3241)		200		ns
Receiver Output Disable Time	Normal operation (MAX3222/MAX3241)		200		ns
Transmitter Skew	$ t_{PHL} - t_{PLH} $		300		ns
Receiver Skew	$ t_{PHL} - t_{PLH} $		300		ns
Transition-Region Slew Rate	$V_{CC} = 3.3V$, $R_L = 3k\Omega$ to 7k Ω , $T_A = +25^\circ C$, $C_L = 150pF$ to 2500pF, measured from +3V to -3V or -3V to +3V, Figure 1	6	8.0	30	V/ μs

Note 2: C_1 – C_4 = 0.1 μ F, tested at 3.3V $\pm$ 10%. C_1 = 0.047 μ F, C_2 – C_4 = 0.33 μ F, tested at 5.0V $\pm$ 10%.

Typical Operating Characteristics

(V_{CC} = 3.3V, 235kbps data rate, 0.1 μ F capacitors, all transmitters loaded with 3k Ω , T_A = +25°C, unless otherwise noted.)

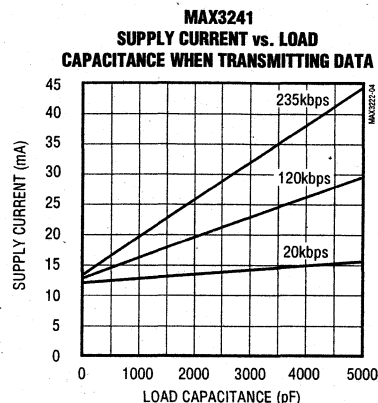
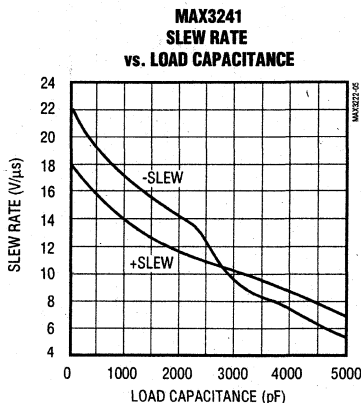
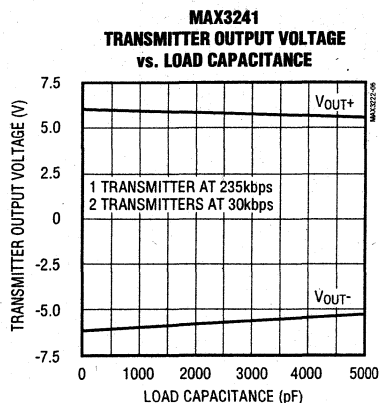


MAX3222/MAX3232/MAX3241

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, 235kbps data rate, 0.1 μ F capacitors, all transmitters loaded with 3k Ω , T_A = +25°C, unless otherwise noted.)



Pin Description

PIN				NAME	FUNCTION
MAX3222		MAX3232	MAX3241		
DIP/SO	SSOP				
5	5	4	1	C2+	Positive terminal of inverting charge-pump capacitor
6	6	5	2	C2-	Negative terminal of inverting charge-pump capacitor
7	7	6	3	V-	-5.5V generated by the charge pump
9, 14	9, 16	8, 13	4–8	R_IN	RS-232 Receiver Inputs
8, 15	8, 17	7, 14	9, 10, 11	T_OUT	RS-232 Transmitter Outputs
11, 12	12, 13	10, 11	12, 13, 14	T_IN	TTL/CMOS Transmitter Inputs
10, 13	10, 15	9, 12	15–19	R_OUT	TTL/CMOS Receiver Outputs
—	—	—	20, 21	R_OUTB	Noninverting Complementary Receiver Outputs—always active
18	20	—	22	SHDN	Shutdown Control—active low
1	1	—	23	EN	Receiver Enable—active low
4	4	3	24	C1-	Negative terminal of the voltage doubler charge-pump capacitor
16	18	15	25	GND	Ground
17	19	16	26	Vcc	+3.0V to +5.5V Supply Voltage
3	3	2	27	V+	+5.5V generated by the charge pump
2	2	1	28	C1+	Positive terminal of the voltage doubler charge-pump capacitor
—	11, 14	—	—	N.C.	No Connection

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3222/MAX3232/MAX3241's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), regardless of the input voltage (V_{CC}) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode; if the output voltages are less than 5.5V, the charge pumps are enabled, and if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the $V+$ and $V-$ supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels.

The transmitters guarantee a 120kbps data rate with worst-case loads of 3k Ω in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Typically, these three devices can

operate at data rates of 235kbps. Transmitters can be paralleled to drive multiple receivers or mice.

The MAX3222/MAX3241's output stage is turned off (high impedance) when the device is in shutdown mode. When the power is off, the MAX3222/MAX3232/MAX3241 permit the outputs to be driven up to $\pm 12V$.

The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC} .

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. The MAX3222/MAX3241 receivers have inverting three-state outputs. In shutdown, the receivers can be active or inactive (see Table 1).

The MAX3241's two complementary outputs (R1OUTB, R2OUTB) are always active, regardless of the state of $\overline{EN}$ or $\overline{SHDN}$ allowing Ring Indicator to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 2).

™ LapLink is a trademark of Traveling Software.

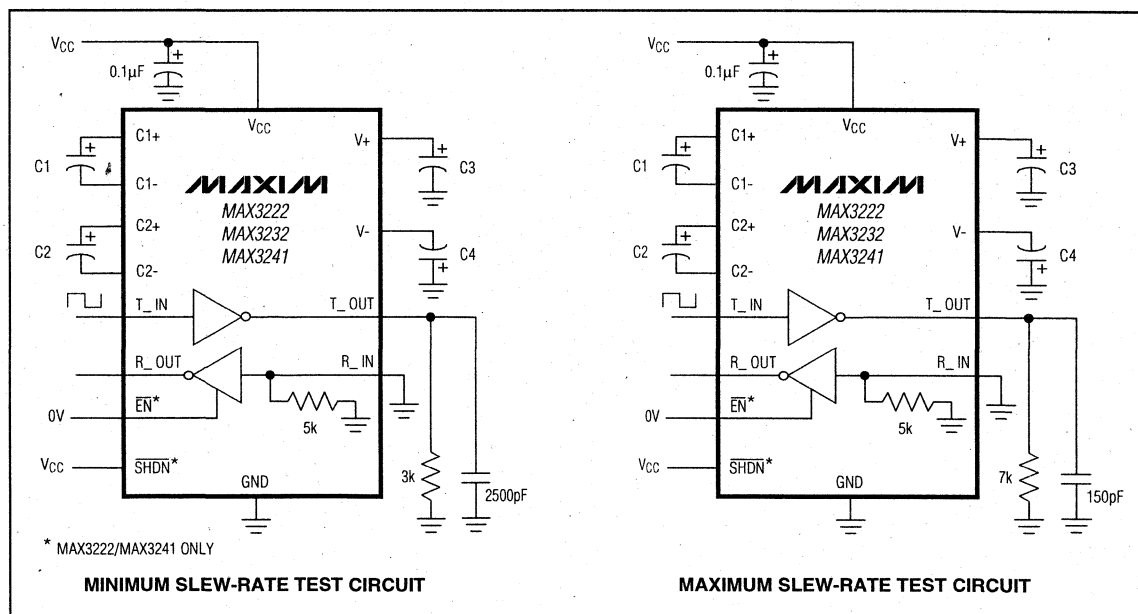


Figure 1. Slew-Rate Test Circuits

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

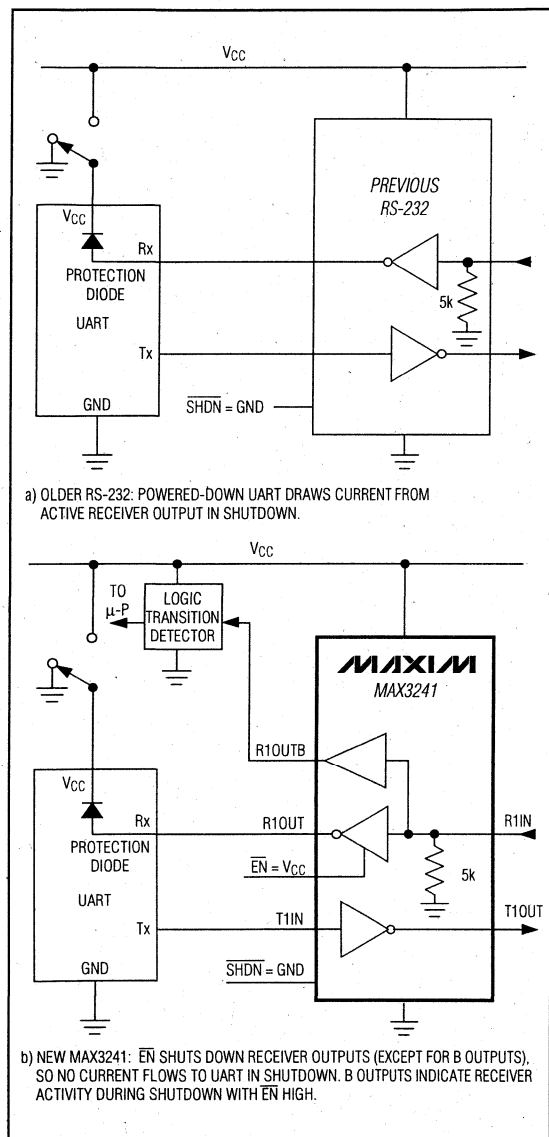


Figure 2. Detection of RS-232 Activity when the UART and Interface are Shut Down; Comparison of MAX3241 (b) with Previous Transceivers (a).

MAX3222/MAX3241 Shutdown Mode

Supply current reduces to less than 1 μ A in shutdown mode (SHDN = low). When shut down, the device's charge pumps are turned off, V₊ is pulled down to V_{CC}, V₋ is pulled to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 100 μ s, as shown in Figure 3. Connect SHDN to V_{CC} if the shutdown mode is not used. SHDN has no effect on R_OUT or R_OUTB.

MAX3222/MAX3241 Enable Control

The inverting receiver outputs (R_OUT) are put into a high-impedance state when $\overline{\text{EN}}$ is high. The complementary outputs R1OUTB and R2OUTB are always active, regardless of the state of $\overline{\text{EN}}$ and SHDN (Table 1). $\overline{\text{EN}}$ has no effect on T_OUT.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; polarized or non-polarized capacitors can be used. The charge pump requires 0.1 μ F capacitors for 3.3V operation. For other supply voltages, refer to Table 2 for required capacitor values. Do not use values smaller than those listed in Table 2. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. However, do not increase C1 without also increasing the values of C2, C3, and C4, to maintain the proper ratios (C1 to the other capacitors).

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V₊ and V₋.

Power-Supply Decoupling

In most circumstances a 0.1 μ F bypass capacitor is adequate. In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C1. Connect bypass capacitors as close to the IC as possible.

Operation Down to 2.7V

Transmitter outputs will meet EIA/TIA-562 levels of ± 3.7 V with supply voltages as low as 2.7V.

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

Table 1. MAX3222/MAX3241 Shutdown and Enable Control Truth Table

$\overline{\text{SHDN}}$	$\overline{\text{EN}}$	T_OUT	R_OUT	R_OUTB (MAX3241)
0	0	High-Z	Active	Active
0	1	High-Z	High-Z	Active
1	0	Active	Active	Active
1	1	Active	High-Z	Active

Table 2. Required Minimum Capacitor Values

V _{CC} (V)	C1 (μ F)	C2, C3, C4 (μ F)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

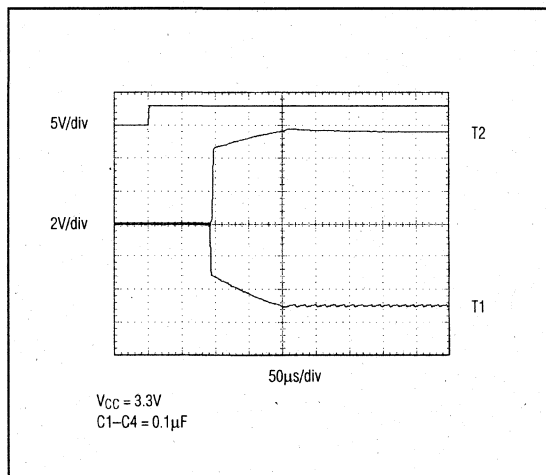


Figure 3. Transmitter Outputs when Exiting Shutdown or Powering Up

Transmitter Outputs when Exiting Shutdown

Figure 3 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3k Ω in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V₋ exceeds approximately 3V.

Mouse Driveability

The MAX3241 has been specifically designed to power serial mice while operating from low-voltage power supplies. It has been tested with leading mouse brands from manufacturers such as Microsoft and Logitech. The MAX3241 successfully drove all serial mice tested and met their respective current and voltage requirements. Figure 4a shows the transmitter output voltages under increasing load current at 3.0V. Figure 4b shows a typical mouse connection using the MAX3241.

MAX3222/MAX3232/MAX3241

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

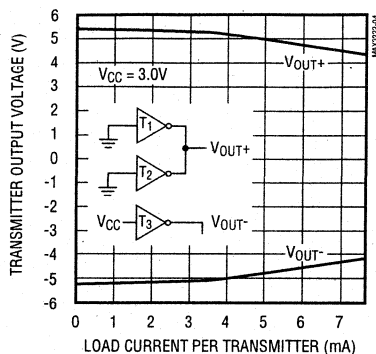


Figure 4a. MAX3241 Transmitter Output Voltage vs. Load Current per Transmitter

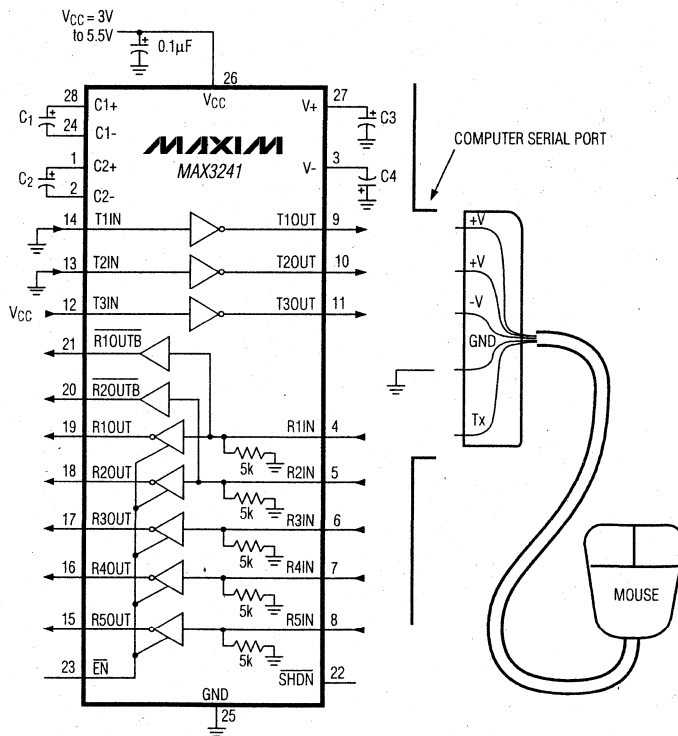


Figure 4b. Mouse Driver Test Circuit

3.0V to 5.5V, 300µA Supply Current, True RS-232 Transceivers using Four 0.1µF External Capacitors

Table 3. Logic Family Compatibility with Various Supply Voltages

SYSTEM POWER-SUPPLY VOLTAGE (V)	MAX32__ V _{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS-logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. Incompatible with AC, HC, or CD4000 CMOS.

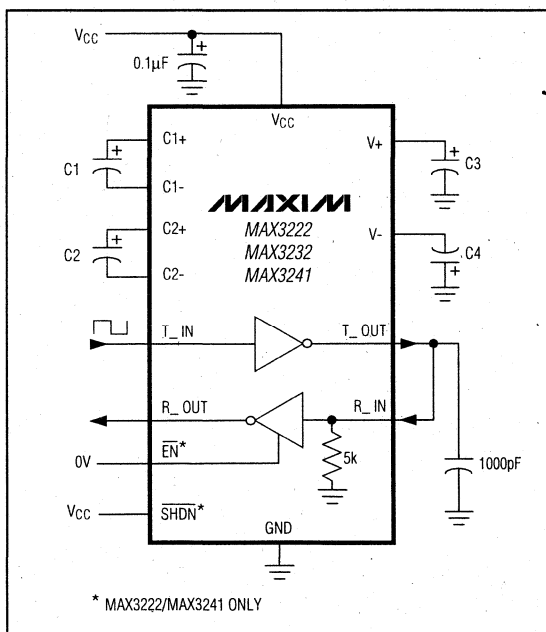


Figure 5. Loopback Test Circuit

High Data Rates

The MAX3222/MAX3232/MAX3241 maintain the RS-232 $\pm 5.0V$ minimum transmitter output voltage even at high data rates. Figure 5 shows a transmitter loopback test circuit. Figure 6 shows a loopback test result at 120kbps, and Figure 7 shows the same test at 235kbps. For Figure 6, all transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 7, a single transmitter was driven at 235kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

Interconnection with 3V and 5V Logic

The MAX3222/MAX3232/MAX3241 can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 3 for more information on possible combinations of interconnections.

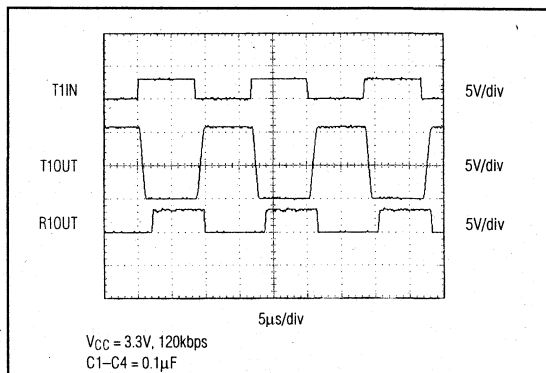


Figure 6. Loopback Test Result at 120kbps

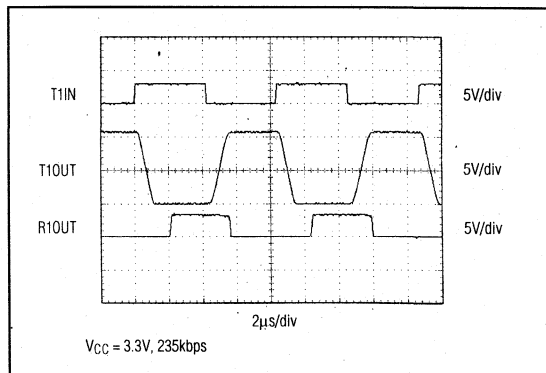


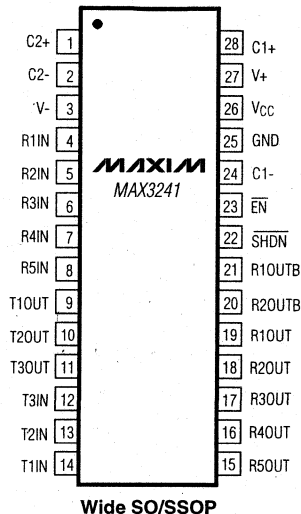
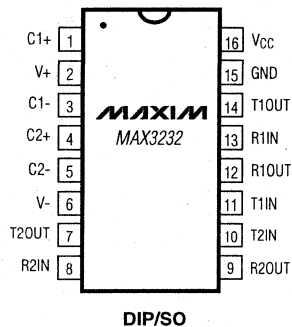
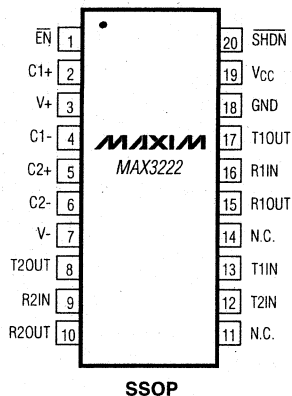
Figure 7. Loopback Test Result at 235kbps

MAX3222/MAX3232/MAX3241

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

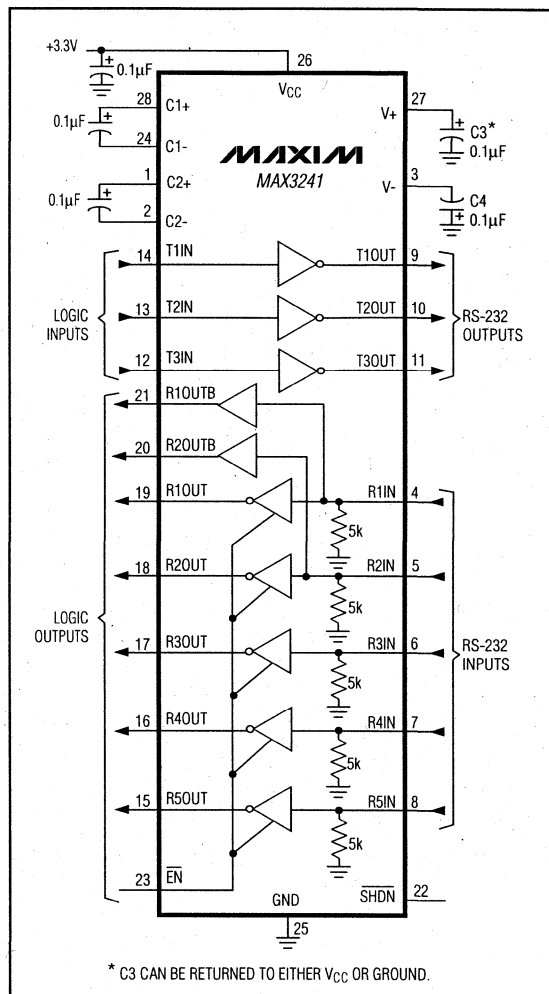
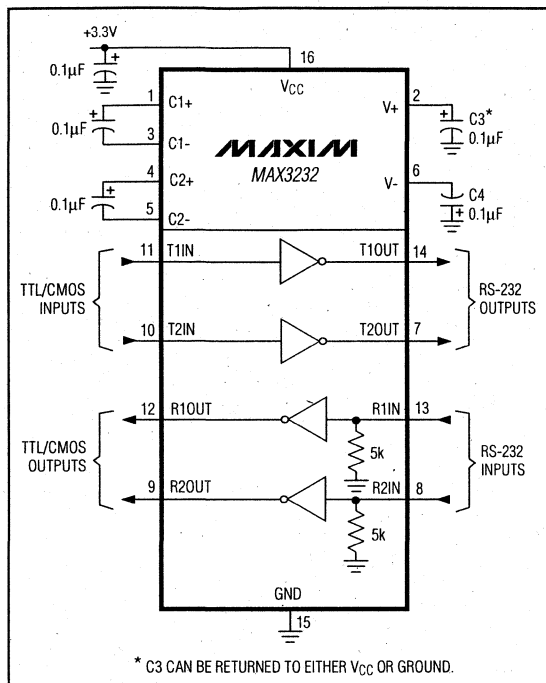
Pin Configurations (continued)

TOP VIEW



3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

Typical Operating Circuits (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX3222C/D	0°C to +70°C	Dice*
MAX3222EPN	-40°C to +85°C	18 Plastic DIP
MAX3222EWN	-40°C to +85°C	18 Wide SO
MAX3222EAP	-40°C to +85°C	20 SSOP
MAX3232CPE	0°C to +70°C	16 Plastic DIP
MAX3232CSE	0°C to +70°C	16 Narrow SO
MAX3232CWE	0°C to +70°C	16 Wide SO
MAX3232EPE	-40°C to +85°C	16 Plastic DIP
MAX3232ESE	-40°C to +85°C	16 Narrow SO
MAX3232EWE	-40°C to +85°C	16 Wide SO
MAX3241CWI	0°C to +70°C	28 Wide SO
MAX3241CAI	0°C to +70°C	28 SSOP
MAX3241EWI	-40°C to +85°C	28 Wide SO
MAX3241EAI	-40°C to +85°C	28 SSOP

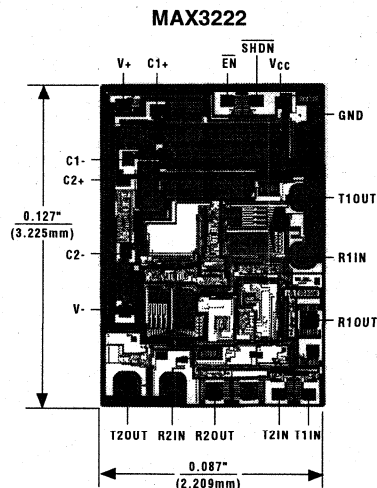
* Dice are tested at $T_A = +25^\circ\text{C}$, DC parameters only.

3.0V to 5.5V, 300 μ A Supply Current, True RS-232 Transceivers using Four 0.1 μ F External Capacitors

3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

PART	POWER-SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	GUARANTEED DATA RATE (kbps)	EIA/TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	120	232	Drives mice
MAX218	1.8 to 4.25	2/2	2	120	232	Operates directly from batteries without a voltage regulator
MAX562	2.7 to 5.25	3/5	5	230	562	Wide supply range
MAX563	3.0 to 3.6	2/2	2	230	562	0.1 μ F capacitors
MAX3212	2.7 to 3.6	3/5	5	235	232	AutoShutdown, complementary receiver, drives mice, transient detection
MAX3222	3.0 to 5.5	2/2	2	120	232	0.1 μ F capacitors
MAX3223	3.0 to 5.5	2/2	2	120	232	0.1 μ F capacitors, AutoShutdown
MAX3232	3.0 to 5.5	2/2	N/A	120	232	0.1 μ F capacitors
MAX3241	3.0 to 5.5	3/5	5	120	232	0.1 μ F capacitors, 2 complementary receivers, drives mice
MAX3243	3.0 to 5.5	3/5	1	120	232	0.1 μ F capacitors, AutoShutdown, complementary receiver, drives mice

Chip Topography



TRANSISTOR COUNT: 339
SUBSTRATE CONNECTED TO GND

MAXIM

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

General Description

The MAX3223/MAX3243 achieve 1 μ A supply current with Maxim's revolutionary AutoShutdown™ feature. When the MAX3223/MAX3243 do not sense a valid signal level on their receiver inputs, the on-board power supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system.

The MAX3223/MAX3243 transceivers are 3V-powered EIA/TIA-232 and V.28/V.24 communications interfaces intended for notebook computer applications. A (proprietary) high efficiency dual charge pump power supply and a low dropout transmitter combine to deliver true RS-232 performance from 3.0V to 5.5V supplies. A guaranteed data rate of 120kbps provides compatibility with popular software for communicating with personal computers.

The MAX3223/MAX3243 require only 0.1 μ F capacitors in 3.3V operation, and can operate from input voltages ranging from 3.0V to 5.5V. They are ideal for 3.3V-only systems, mixed 3.3V and 5.0V systems, or 5.0V-only systems that require true RS-232 performance.

The MAX3243 3-driver/5-receiver, complete serial port is ideal for notebook or subnotebook computers. Besides having all receivers active in shutdown, one receiver has a second, complementary output that is always active. This receiver can monitor an external device (such as a modem) in shutdown, without forward biasing the protection diodes in a UART that may have VCC completely removed.

Applications

Notebook, Subnotebook, and Palmtop Computers
 Battery-Powered Equipment
 Hand-Held Equipment
 Peripherals
 Printers

Typical Operating Circuits appear at end of data sheet.

™ AutoShutdown is a trademark of Maxim Integrated Products.

* Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.

MAXIM

Maxim Integrated Products 2-73

Call toll free 1-800-998-8800 for free samples or literature.

Features

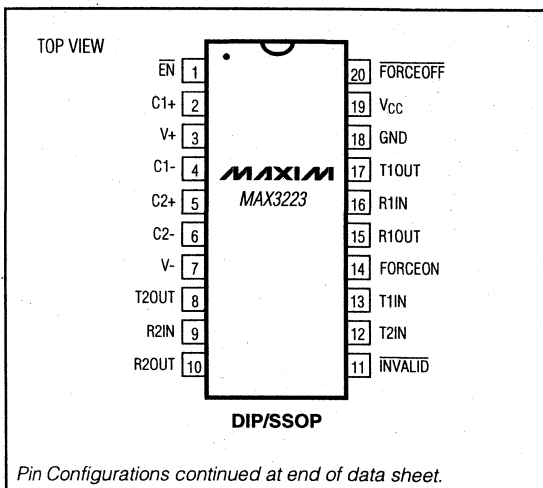
- ♦ 1 μ A Supply Current Achieved with AutoShutdown™
- ♦ Small 0.1 μ F Capacitors
- ♦ True RS-232 Operation from VCC = 3.0V to 5.5V
- ♦ Meets EIA/TIA-562 Specifications Down to 2.7V
- ♦ Guaranteed 120kbps Data Rate
- ♦ 6V/ μ s Min Guaranteed Slew Rate
- ♦ Guaranteed Mouse Driveability (MAX3243)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3223CPP	0°C to +70°C	20 Plastic DIP
MAX3223CAP	0°C to +70°C	20 SSOP
MAX3223C/D	0°C to +70°C	Dice*
MAX3223EPP	-40°C to +85°C	20 Plastic DIP
MAX3223EAP	-40°C to +85°C	20 SSOP
MAX3243CWI	0°C to +70°C	28 Wide SO
MAX3243CAI	0°C to +70°C	28 SSOP
MAX3243EWI	-40°C to +85°C	28 Wide SO
MAX3243EAI	-40°C to +85°C	28 SSOP

*Dice are tested at T_A = +25°C only.

Pin Configurations



MAX3223/MAX3243*

2

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

ABSOLUTE MAXIMUM RATINGS

V _{CC}	-0.3V to +6V
V ₊ (Note 1)	-0.3V to +7V
V ₋ (Note 1)	+0.3V to -7V
V ₊ + V ₋ (Note 1)	+13V
Input Voltages	
T _{IN} , FORCEOFF, FORCEON, $\overline{\text{EN}}$ (MAX3223)	-0.3V to +6V
R _{IN}	±25V
Output Voltages	
T _{OUT}	±13.2V
R _{OUT} , INVALID	-0.3V to (V _{CC} + 0.3V)
Short-Circuit Duration	
T _{OUT}	Continuous

Continuous Power Dissipation (T _A = +70°C)	
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C)	640mW
20-Pin SSOP (derate 8.00mW/°C above +70°C)	640mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C)	1000mW
28-Pin SSOP (derate 9.52mW/°C above +70°C)	762mW
Operating Temperature Range	
MAX32_ _C_	0°C to +70°C
MAX32_ _E_	-40°C to +85°C
Storage Temperature Range	
Lead Temperature (soldering, 10sec)	+300°C

Note 1: V₊ and V₋ can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V; C₁–C₄ = 0.1 μ F (Note 2); T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Current, AutoShutdown™	V _{CC} = 3.3V or 5.0V, T _A = +25°C	All R _{IN} open, FORCEON = GND, FORCEOFF = V _{CC}		1.0	10	μA
Supply Current, Shutdown		FORCEOFF = GND		1.0	10	μA
Supply Current, AutoShutdown™ Disabled		FORCEON = FORCEOFF = V _{CC} , no load		0.3	1.0	mA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T _{IN} , FORCEON, FORCEOFF, EN (MAX3223)				0.8	V
Input Logic Threshold High	T _{IN} , EN, FORCEON, FORCEOFF	V _{CC} = 3.3V	2.0			V
		V _{CC} = 5.0V	2.4			
Input Leakage Current	T _{IN} , EN, FORCEON, FORCEOFF			±0.01	±1.0	μA
Output Leakage Current	Receivers disabled			±0.05	±10	μA
Output Voltage Low	I _{OUT} = 1.6mA				0.4	V
Output Voltage High	I _{OUT} = -1.0mA		V _{CC} - 0.6	V _{CC} - 0.1		V
AUTOSHUTDOWN (FORCEON = GND, FORCEOFF = V _{CC})						
Receiver Input Thresholds to Transmitters Enable	Figure 5	Positive threshold			2.7	V
		Negative threshold	-2.7			
Receiver Input Thresholds to Transmitters Disable	1μA supply current, Figure 5		-0.3		0.3	V
INVALID Output Voltage Low	I _{OUT} = 1.6mA				0.4	V
INVALID Output Voltage High	I _{OUT} = -1.0mA		V _{CC} - 0.6			V
Receiver Threshold to Transmitters Enabled, t _{WU}	Figure 5			250		μs
Receiver Positive or Negative Threshold to INVALID High, t _{INVH}	Figure 5			1		μs
Receiver Positive or Negative Threshold to INVALID Low, t _{INVL}	Figure 5			30		μs

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 5.5V; C₁–C₄ = 0.1 μ F (Note 2); T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	
RECEIVER INPUTS							
Input Voltage Range			-25		25	V	
Input Threshold Low	T _A = +25°C	V _{CC} = 3.3V	0.6	1.2		V	
		V _{CC} = 5.0V	0.8	1.5			
Input Threshold High	T _A = +25°C	V _{CC} = 3.3V		1.5	2.4	V	
		V _{CC} = 5.0V		1.8	2.4		
Input Hysteresis				0.3		V	
Input Resistance	T _A = +25°C		3	5	7	kΩ	
TRANSMITTER OUTPUTS							
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±5.4		V	
Output Resistance	V _{CC} = V ₊ = V ₋ = 0V, T _{OUT} = ±2V		300	10M		Ω	
Output Short-Circuit Current				±35	±60	mA	
Output Leakage Current	V _{OUT} = ±12V, V _{CC} = 0V or 3.0V to 5.5V, Transmitters disabled				±25	μA	
MOUSE DRIVEABILITY (MAX3243)							
Transmitter Output Voltage	T ₁ IN = T ₂ IN = GND, T ₃ IN = V _{CC} , T ₃ OUT loaded with 3kΩ to GND, T ₁ OUT and T ₂ OUT loaded with 2.5mA each		±5			V	
TIMING CHARACTERISTICS							
Maximum Data Rate	R _L = 3kΩ, C _L = 1000pF, one transmitter switching		120	235		kbps	
Receiver Propagation Delay	Receiver IN to Receiver OUT, C _L = 150pF	t _{PHL}	0.3			μs	
		t _{PLH}	0.3				
Receiver Output Enable Time	Normal operation		200			ns	
Receiver Output Disable Time	Normal operation		200			ns	
Transmitter Skew	t _{PHL} - t _{PLH}		100			500	ns
Receiver Skew	t _{PHL} - t _{PLH}		200			1000	ns
Transition-Region Slew Rate	V _{CC} = 3.3V, R _L = 3kΩ to 7kΩ, T _A = +25°C, measured from +3V to -3V or -3V to +3V	C _L = 150pF to 2500pF	4	8.0	30	V/μs	
		C _L = 150pF to 1000pF	6		30		

Note 2: C₁–C₄ = 0.1 μ F, tested at 3.3V ±10%. C₁ = 0.047 μ F, C₂–C₄ = 0.33 μ F, tested at 5.0V ±10%.

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Pin Description

PIN		NAME	FUNCTION
MAX3223	MAX3243		
1	—	$\overline{\text{EN}}$	Receiver Enable Control. Drive low for normal operation. Drive high to force the receiver outputs into a high-Z state.
5	1	C2+	Positive terminal of inverting charge-pump capacitor
6	2	C2-	Negative terminal of inverting charge-pump capacitor
7	3	V-	-5.5V generated by the charge pump
16, 9	4-8	R_IN	RS-232 Receiver Inputs
17, 8	9, 10, 11	T_OUT	RS-232 Transmitter Outputs
13, 12	12, 13, 14	T_IN	TTL/CMOS Transmitter Inputs
15, 10	15-19	R_OUT	TTL/CMOS Receiver Outputs
—	20	R2OUTB	Noninverting Receiver Output—active in shutdown
11	21	$\overline{\text{INVALID}}$	Output of the valid signal detector. Indicates if a valid RS-232 level is present on receiver inputs when logic "1".
20	22	$\overline{\text{FORCEOFF}}$	Drive low to shut down transmitters and on-board power supply. This overrides all automatic circuitry and FORCEON. See Table 1.
14	23	FORCEON	Drive high to override automatic circuitry keeping transmitters on ($\overline{\text{FORCEOFF}}$ must be high). See Table 1.
4	24	C1-	Negative terminal of the voltage doubler charge-pump capacitor
18	25	GND	Ground
19	26	VCC	+3.0V to +5.5V Supply Voltage
3	27	V+	+5.5V generated by the charge pump
2	28	C1+	Positive terminal of the voltage doubler charge-pump capacitor

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3223/MAX3243 internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), regardless of the input voltage (VCC) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode; if the output voltages are less than 5.5V, the charge pumps are enabled, and if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels.

The transmitters guarantee a 120kbps data rate with worst-case loads of 3k Ω in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Typically, the MAX3223/MAX3243 can operate at data rates of 235kbps. Transmitters can be paralleled to drive multiple receivers or mice (MAX3243). Figure 1 shows a complete system connection.

When $\overline{\text{FORCEOFF}}$ is driven to ground, or the Auto-Shutdown™ circuitry senses invalid voltage levels at all receiver inputs, the transmitters are disabled and the outputs are forced into a high-impedance state.

™ LapLink is a trademark of Traveling Software

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

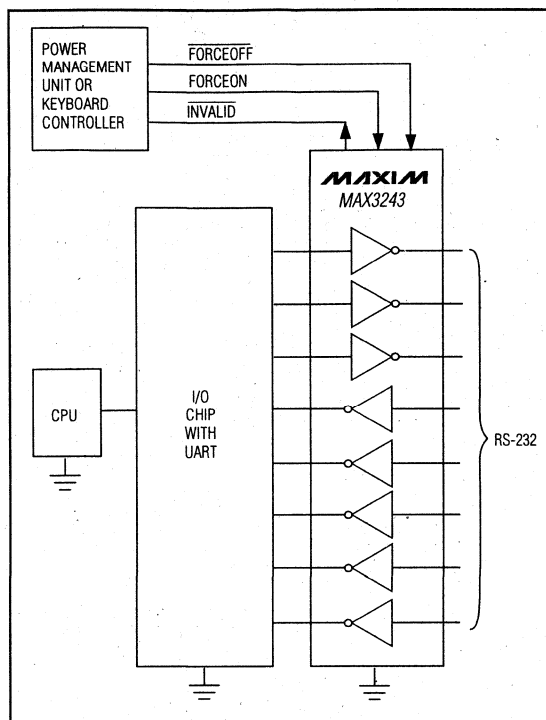


Figure 1. Interface Under Control of PMU

RS-232 Receivers

The MAX3223/MAX3243's receivers convert RS-232 signals to CMOS-logic output levels. All receivers have one inverting three-state output. In shutdown ($\text{FORCEOFF} = \text{low}$) or in AutoShutdown™, the MAX3223 receivers are active. Driving EN high places the two receivers in a high-impedance state. The MAX3243 receivers are high impedance when the part is shut down. See Table 1.

The MAX3243 has an always active complementary output (R2OUTB). R2OUTB is an extra output that monitors receiver activity while the other receivers are high impedance. This allows Ring Indicator to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 2).

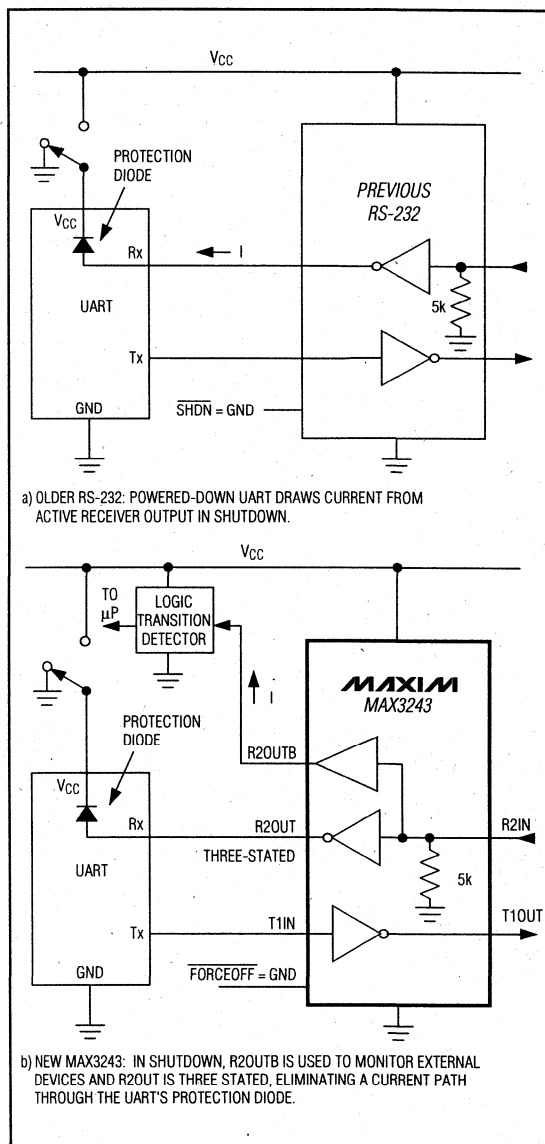


Figure 2. The MAX3243 detects RS-232 activity when the UART and interface are shut down.

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Table 1a. MAX3223 FORCEOFF and Enable Control Truth Table

FORCEOFF	EN	T_OUT	R_OUT
0	0	High-Z	Active
0	1	High-Z	High-Z
1	0	Active*	Active
1	1	Active*	High-Z

Table 1b. MAX3243 FORCEOFF Control Truth Table

FORCEOFF	T_OUT	R_OUT	R2OUTB
0	High-Z	High-Z	Active
1	Active*	Active*	Active

***Note:** If the part is in AutoShutdown™ mode ($\overline{\text{FORCEOFF}} = V_{CC}$, $\text{FORCEON} = \text{GND}$), it is shut down if no valid RS-232 levels are present on all receiver inputs.

AutoShutdown™

A 1µA supply current is achieved with Maxim's new AutoShutdown™ feature, which operates when FORCEON is low and FORCEOFF is high. When the MAX3223/MAX3243 sense no valid signal levels on all receiver inputs for 30µs, the on-board power supply and drivers are shut off, reducing supply current to 1µA. This occurs if the RS-232 cable is disconnected or the connected peripheral transmitters are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system. When using AutoShutdown™, the INVALID output is high when the device is on and low when the device is shut down. Because INVALID indicates the receiver inputs' condition, it can be used in any mode (Figure 3).

Table 2 and Figure 3c summarize the MAX3223/MAX3243 operating modes. FORCEON and FORCEOFF override the automatic circuitry and force the transceiver into its normal operating state or into its low-power standby state. When neither control is asserted, the IC selects between these states automatically based on receiver input levels. Figures 3a, 3b, and 5a depict valid and invalid RS-232 receiver levels.

A mouse or other system with AutoShutdown™ may need time to wake up. Figure 4 shows a circuit that

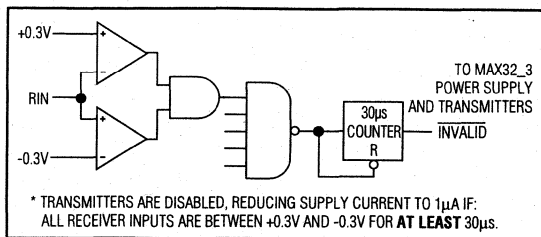


Figure 3a. MAX32_3 Entering 1µA Supply Mode via AutoShutdown™

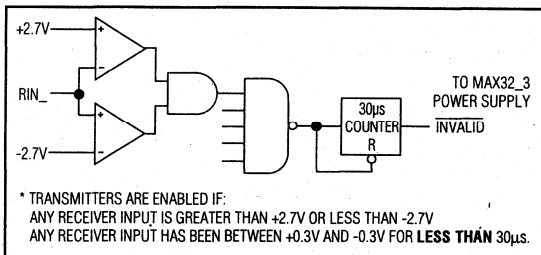


Figure 3b. MAX32_3 with Transmitters Enabled Using AutoShutdown™

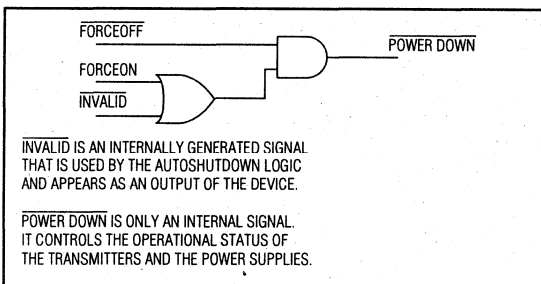


Figure 3c. AutoShutdown™ Logic

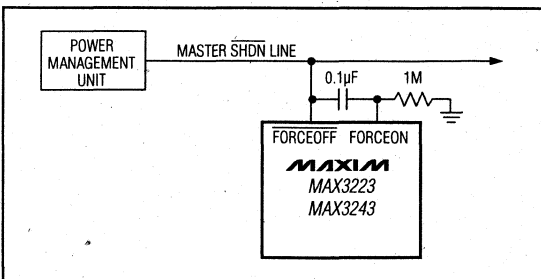


Figure 4. AutoShutdown™ with Initial Turn-On to Wake Up a Mouse or Another System

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

MAX3223/MAX3243

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Table 2. AutoShutdown Logic

RS-232 SIGNAL PRESENT AT RECEIVER INPUT	FORCEOFF INPUT	FORCEON INPUT	INVALID OUTPUT	TRANSCIVER STATUS
Yes	H	X	H	Normal Operation
No	H	H	L	Normal Operation (Forced On)
No	H	L	L	Shutdown (AutoShutdown)
Yes	L	X	H	Shutdown (Forced Off)
No	L	X	L	Shutdown (Forced Off)

forces the transmitters on for 100ms, allowing enough time for the other system to realize that the MAX3223/MAX3243 is awake. If the other system outputs valid RS-232 signals within that time, the RS-232 ports on both systems remain enabled.

When shut down, the device's charge pumps are turned off, $V+$ decays to V_{CC} , $V-$ decays to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 100 μ s (Figure 5b).

Software-Controlled Shutdown

If direct software control is desired, **INVALID** can be used to indicate DTR or Ring Indicator signal. Tie **FORCEOFF** and **FORCEON** together to bypass AutoShutdown so the line acts like a **SHDN** input.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; either polarized or nonpolarized capacitors may be used. The charge pump requires 0.1 μ F capacitors for 3.3V operation. For other supply voltages, refer to Table 3 for required capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. However, do not increase C1 without also increasing the values of C2, C3, and C4 to maintain the proper ratios (C1 to the other capacitors).

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and influences the amount of ripple on $V+$ and $V-$.

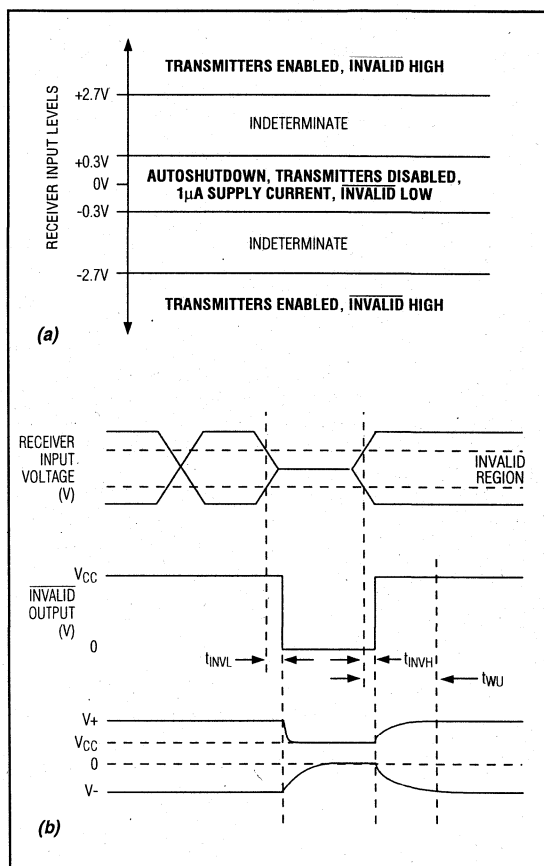


Figure 5. AutoShutdown Trip Levels

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

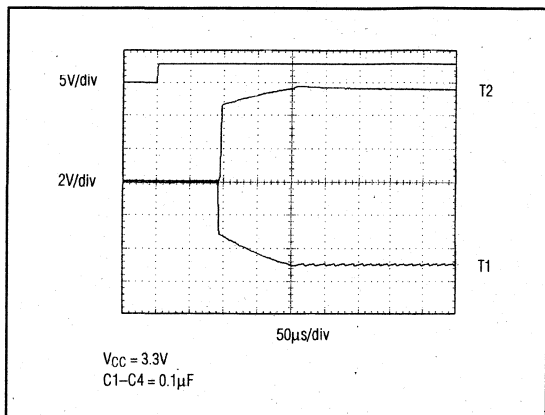


Figure 6. Transmitter Outputs when Exiting Shutdown or Powering Up

Power-Supply Decoupling

In most circumstances a 0.1 μ F bypass capacitor is adequate. In applications that are sensitive to power-supply noise, decouple VCC to ground with a capacitor of the same value as the charge-pump capacitor C1. Connect bypass capacitors as close to the IC as possible.

Transmitter Outputs when Exiting Shutdown

Figure 6 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels. Each transmitter is loaded with 3k Ω in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V_{ex} exceeds approximately 3V. Figure 7a shows the MAX3243's transmitter output voltage vs. current per transmitter. Figure 7b is a mouse driver test circuit.

Mouse Driveability (MAX3243)

The MAX3243 has been specifically designed to power serial mice while operating from low-voltage power supplies. It has been tested with samples of ten major mouse models from six manufacturers including the leading three: Logitech (5 models), Mouse Systems and

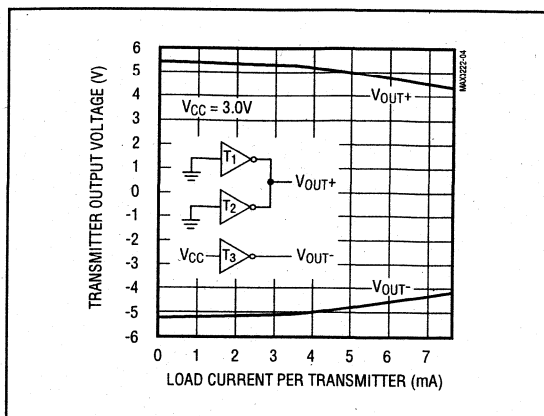


Figure 7a. MAX3243 Transmitter Output Voltage vs. Load Current Per Transmitter

Microsoft. The MAX3243 successfully drove all serial mice and met their respective current and voltage requirements. Figure 7a shows the transmitter outputs under increasing load current. The MAX3243's switching regulator ensures the transmitters will supply at least ± 5 V during worst-case conditions. The AutoShutdown™ feature does not work with a mouse, so $\overline{\text{FORCEOFF}}$ and FORCEON should be connected to VCC.

High Data Rates

The MAX3223/MAX3243 maintain the RS-232 ± 5.0 V minimum transmitter output voltage even at high data rates. Figure 8 shows a transmitter loopback test circuit. Figure 9 shows a loopback test result at 120kbps, and Figure 10 shows the same test at 240kbps. For Figure 9, all three transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 10, a single transmitter was driven at 235kbps, but all three transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

Interconnection with 3V and 5V Logic

The MAX3223/MAX3243 can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 4 for more information on possible combinations of interconnections.

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

MAX3223/MAX3243

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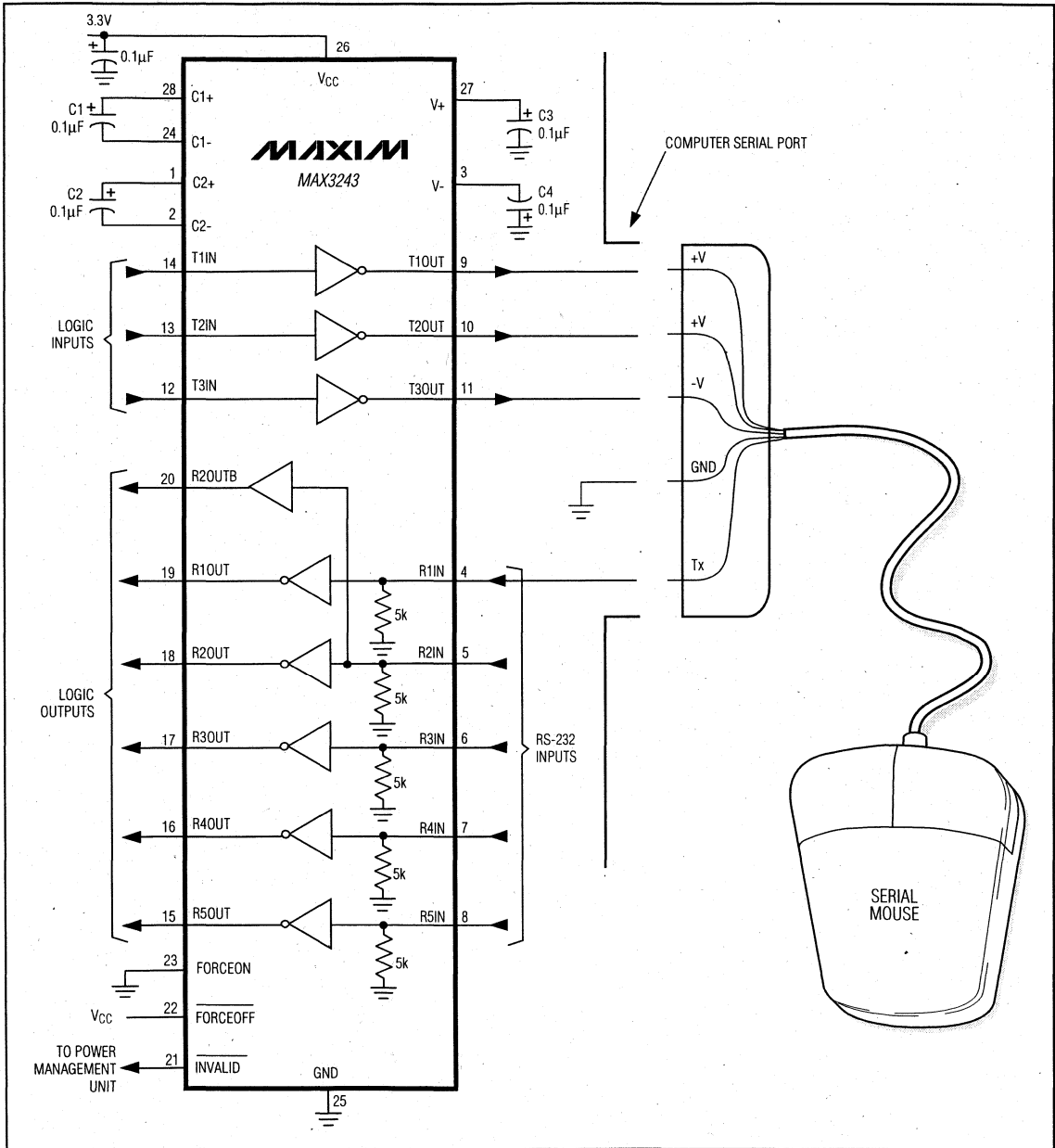


Figure 7b. Mouse Driver Test Circuit

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

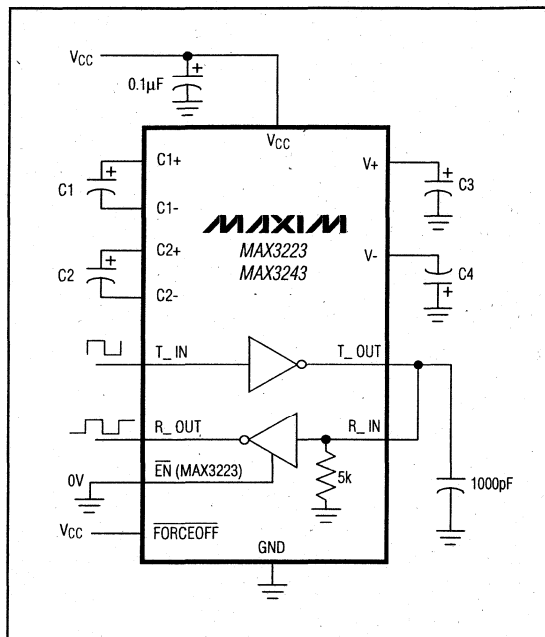


Figure 8. Loopback Test Circuit

Table 3. Required Capacitor Values

V _{CC} (V)	C1 (μ F)	C2, C3, C4 (μ F)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

Table 4. Logic Family Compatibility with Various Supply Voltages

SYSTEM POWER-SUPPLY VOLTAGE (V)	V _{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS-logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. Incompatible with AC, HC, or CD4000 CMOS.

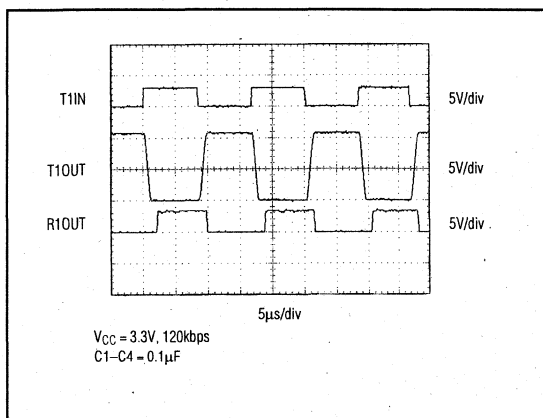


Figure 9. Loopback Test Result at 120kbps

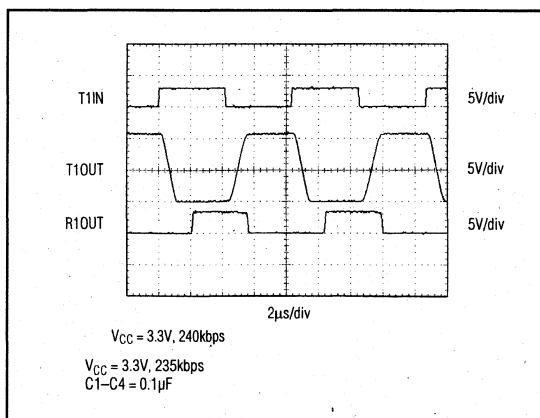
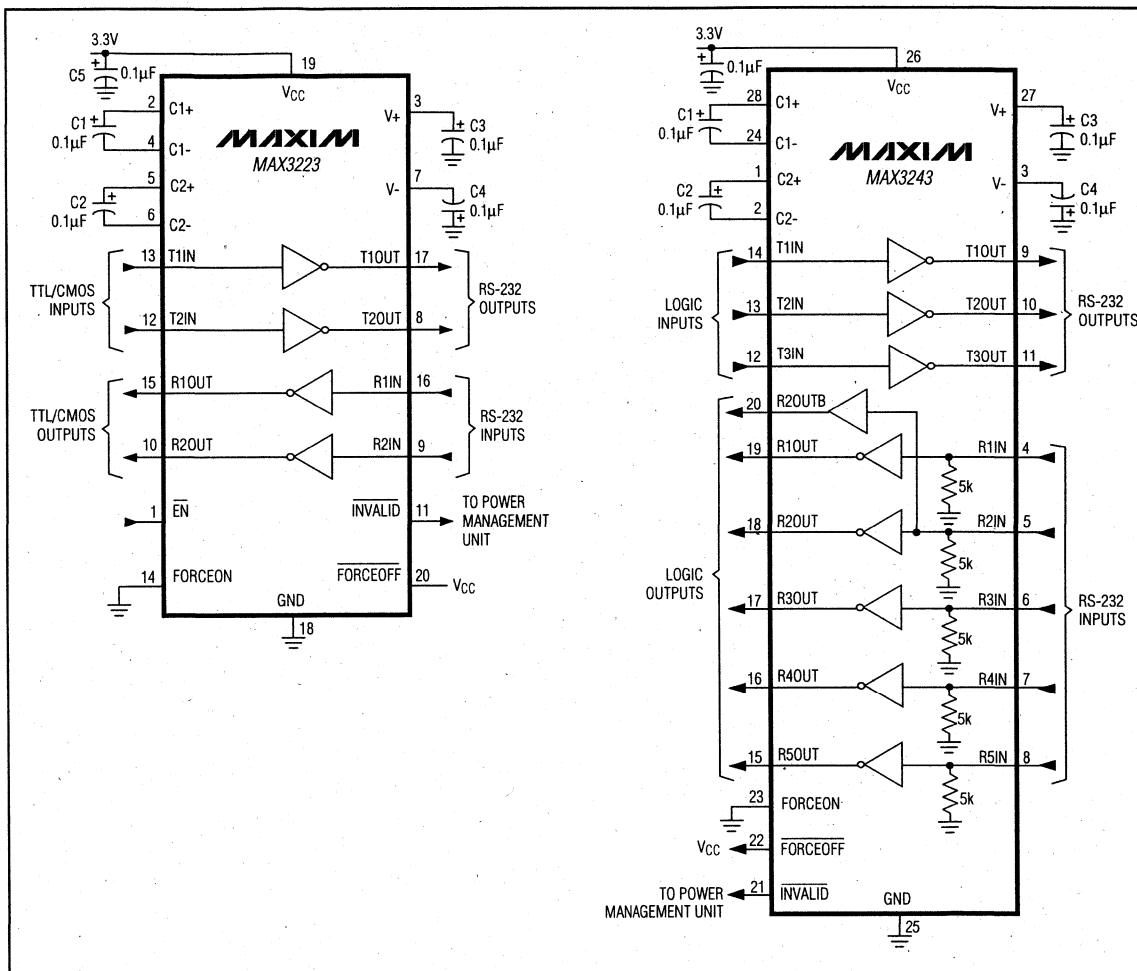


Figure 10. Loopback Test Result at 235kbps

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Typical Operating Circuits



MAX3223/MAX3243

2

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

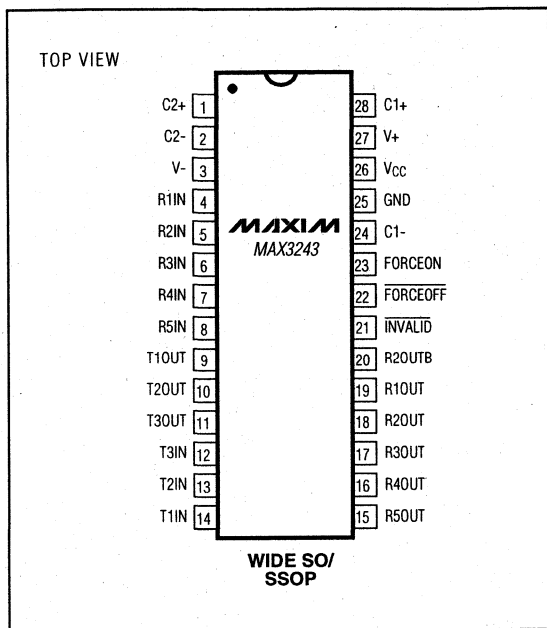
PART	POWER-SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	GUARANTEED DATA RATE (kbps)	EIA/TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	120	232	Drives mice
MAX218	1.8 to 4.25	2/2	2	120	232	Operates directly from batteries without a voltage regulator
MAX562	2.7 to 5.25	3/5	5	230	562	230kbps guaranteed data rate
MAX563	3.0 to 3.6	2/2	2	120	562	0.1 μ F capacitors
MAX3212	2.7 to 3.6	3/5	5	235	232	AutoShutdown™, complementary receiver, drives mice, transient detection
MAX3222	3.0 to 5.5	2/2	2	120	232	0.1 μ F capacitors, MAX242 pinout
MAX3223	3.0 to 5.5	2/2	2	120	232	0.1 μ F capacitors, AutoShutdown™
MAX3232	3.0 to 5.5	2/2	N/A	120	232	0.1 μ F capacitors, MAX232 pinout
MAX3241	3.0 to 5.5	3/5	5	120	232	0.1 μ F capacitors, 2 complementary receivers, drives mice
MAX3243	3.0 to 5.5	3/5	1	120	232	0.1 μ F capacitors, AutoShutdown™, complementary receiver, drives mice

1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

MAX3223/MAX3243

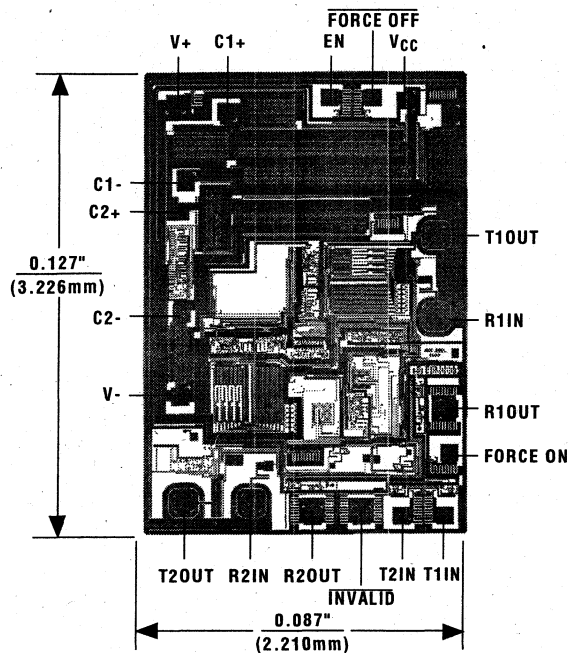
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Pin Configurations (continued)



1 μ A Supply Current, True +3V to +5.5V RS-232 Transceivers with AutoShutdown™

Chip Topography



MAX3223

TRANSISTOR COUNT: 339
SUBSTRATE CONNECTED TO GND

MAX3243

TRANSISTOR COUNT: 476



3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

General Description

The MAX3483, MAX3485, MAX3486, MAX3488, MAX3490, and MAX3491 are 3.3V, low-power transceivers for RS-485 and RS-422 communication. Each part contains one driver and one receiver. The MAX3483 and MAX3488 feature slew-rate-limited drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The partially slew-rate-limited MAX3486 transmits up to 2.5Mbps. The MAX3485, MAX3490, and MAX3491 transmit at up to 10Mbps.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if both inputs are open circuit.

The MAX3488, MAX3490, and MAX3491 feature full-duplex communication, while the MAX3483, MAX3485, and MAX3486 are designed for half-duplex communication.

Applications

Low-Power RS-485/RS-422 Transceivers
Telecommunications
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks

Features

- ◆ Operate from a Single 3.3V Supply—No Charge Pump!
- ◆ Interoperable with +5V Logic
- ◆ 8ns Max Skew (MAX3485/MAX3490/MAX3491)
- ◆ Slew-Rate Limited for Errorless Data Transmission (MAX3483/MAX3488)
- ◆ 2nA Low-Current Shutdown Mode (MAX3483/MAX3485/MAX3486/MAX3491)
- ◆ -7V to +12V Common-Mode Input Voltage Range
- ◆ Allows up to 32 Transceivers on the Bus
- ◆ Full-Duplex and Half-Duplex Versions Available
- ◆ Industry Standard 75176 Pinout (MAX3483/MAX3485/MAX3486)
- ◆ Current-Limiting and Thermal Shutdown for Driver Overload Protection

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3483CPA	0°C to +70°C	8 Plastic DIP
MAX3483CSA	0°C to +70°C	8 SO
MAX3483C/D	0°C to +70°C	Dice*
MAX3483EPA	-40°C to +85°C	8 Plastic DIP
MAX3483ESA	-40°C to +85°C	8 SO
MAX3485CPA	0°C to +70°C	8 Plastic DIP
MAX3485CSA	0°C to +70°C	8 SO
MAX3485C/D	0°C to +70°C	Dice*
MAX3485EPA	-40°C to +85°C	8 Plastic DIP
MAX3485ESA	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

Selection Table

PART NUMBER	GUARANTEED DATA RATE (Mbps)	SUPPLY VOLTAGE (V)	HALF/FULL DUPLEX	SLEW-RATE LIMITED	DRIVER/RECEIVER ENABLE	SHUTDOWN CURRENT (nA)	PIN COUNT
MAX3483	0.25	3.0 to 3.6	Half	Yes	Yes	2	8
MAX3485	10		Half	No	Yes	2	8
MAX3486	2.5		Half	Yes	Yes	2	8
MAX3488	0.25		Full	Yes	No	—	8
MAX3490	10		Full	No	No	—	8
MAX3491	10		Full	No	Yes	2	14

MAXIM

Maxim Integrated Products 2-87

Call toll free 1-800-998-8800 for free samples or literature.

MAX3483/MAX3485/MAX3486/MAX3488/MAX3490/MAX3491

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 7V
 Control Input Voltage (RE, DE) -0.3V to 7V
 Driver Input Voltage (DI) -0.3V to 7V
 Driver Output Voltage (A, B, Y, Z) -7.5V to 12.5V
 Receiver Input Voltage (A, B) -7.5V to 12.5V
 Receiver Output Voltage (RO) -0.3V to (V_{CC} + 0.3V)
 Continuous Power Dissipation (T_A = +70°C)
 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW

14-Pin Plastic DIP (derate 10mW/°C above +70°C) 800mW
 14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
 Operating Temperature Ranges
 MAX34_ _C_ _ 0°C to +70°C
 MAX34_ _E_ _ -40°C to +85°C
 Storage Temperature Range -65°C to +160°C
 Lead Temperature (soldering, 10sec) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Driver Output	V _{OD}	R _L = 100Ω (RS-422), Figure 4	2.0			V
		R _L = 54Ω (RS-485), Figure 4	1.5			
		R _L = 60Ω (RS-485), V _{CC} = 3.3V, Figure 5	1.5			
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States (Note 1)	ΔV _{OD}	R _L = 54Ω or 100Ω, Figure 4			0.2	V
Driver Common-Mode Output Voltage	V _{OC}	R _L = 54Ω or 100Ω, Figure 4			3	V
Change in Magnitude of Common-Mode Output Voltage (Note 1)	ΔV _{OC}	R _L = 54Ω or 100Ω, Figure 4			0.2	V
Input High Voltage	V _{IH}	DE, DI, RE	2.0			V
Input Low Voltage	V _{IL}	DE, DI, RE			0.8	V
Logic Input Current	I _{IN1}	DE, DI, RE			±2	μA
Input Current (A, B)	I _{IN2}	DE = 0V, V _{CC} = 0V or 3.6V	V _{IN} = 12V		1.0	mA
			V _{IN} = -7V		-0.8	
Output Leakage (Y, Z)	I _O	DE = 0V, RE = 0V, V _{CC} = 0V or 3.6V, MAX3491	V _{OUT} = 12V		20	μA
			V _{OUT} = -7V		-20	
Output Leakage (Y, Z) in Shutdown Mode	I _O	DE = 0V, RE = V _{CC} , V _{CC} = 0V or 3.6V, MAX3491	V _{OUT} = 12V		1	μA
			V _{OUT} = -7V		-1	
Receiver Differential Threshold Voltage	V _{TH}	-7V ≤ V _{CM} ≤ 12V	-0.2		0.2	V
Receiver Input Hysteresis	ΔV _{TH}	V _{CM} = 0V		50		mV
Receiver Output High Voltage	V _{OH}	I _{OUT} = -1.5mA, V _{ID} = 200mV, Figure 6	V _{CC} - 0.4			V
Receiver Output Low Voltage	V _{OL}	I _{OUT} = 2.5mA, V _{ID} = 200mV, Figure 6			0.4	V
Three-State (High Impedance) Output Current at Receiver	I _{OZR}	V _{CC} = 3.6V, 0V ≤ V _{OUT} ≤ V _{CC}			±1	μA
Receiver Input Resistance	R _{IN}	-7V ≤ V _{CM} ≤ 12V	12			kΩ

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±0.3V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I _{CC}	No load, DI = 0V or V _{CC}	DE = V _{CC} , RE = 0V or V _{CC}		1.1	2.2	mA
			DE = 0V, RE = 0V		0.95	1.9	
Supply Current in Shutdown Mode	I _{SHDN}	DE = 0V, RE = V _{CC} , DI = V _{CC} or 0V			0.002	1	μA
Driver Short-Circuit Output Current	I _{OSD}	V _{OUT} = -7V				-250	mA
		V _{OUT} = 12V				250	
Receiver Short-Circuit Output Current	I _{OSR}	0V ≤ V _{RO} ≤ V _{CC}			±8	±60	mA

DRIVER SWITCHING CHARACTERISTICS—MAX3485, MAX3490, and MAX3491

(V_{CC} = 3.3V, T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Differential Output Delay	t _{DD}	R _L = 60Ω, Figure 7	1	22	35	ns
Driver Differential Output Transition Time	t _{TD}	R _L = 60Ω, Figure 7	3	8	25	ns
Driver Propagation Delay, Low-to-High Level	t _{PLH}	R _L = 27Ω, Figure 8	7	22	35	ns
Driver Propagation Delay, High-to-Low Level	t _{PHL}	R _L = 27Ω, Figure 8	7	22	35	ns
t _{PLH} - t _{PHL} Driver Propagation Delay Skew (Note 2)	t _{PDS}	R _L = 27Ω, Figure 8			8	ns
DRIVER OUTPUT ENABLE/DISABLE TIMES (MAX3485/MAX3491 only)						
Driver Output Enable Time to Low Level	t _{PZL}	R _L = 110Ω, Figure 10		45	90	ns
Driver Output Enable Time to High Level	t _{PZH}	R _L = 110Ω, Figure 9		45	90	ns
Driver Output Disable Time from High Level	t _{PHZ}	R _L = 110Ω, Figure 9		40	80	ns
Driver Output Disable Time from Low Level	t _{PLZ}	R _L = 110Ω, Figure 10		40	80	ns
Driver Output Enable Time from Shutdown to Low Level	t _{PSL}	R _L = 110Ω, Figure 10		650	900	ns
Driver Output Enable Time from Shutdown to High Level	t _{PSH}	R _L = 110Ω, Figure 9		650	900	ns

DRIVER SWITCHING CHARACTERISTICS—MAX3486

(V_{CC} = 3.3V, T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Differential Output Delay	t _{DD}	R _L = 60Ω, Figure 7	24	48	70	ns
Driver Differential Output Transition Time	t _{TD}	R _L = 60Ω, Figure 7	15	35	60	ns
Driver Propagation Delay, Low-to-High Level	t _{PLH}	R _L = 27Ω, Figure 8	20	48	70	ns
Driver Propagation Delay, High-to-Low Level	t _{PHL}	R _L = 27Ω, Figure 8	20	48	70	ns
t _{PLH} - t _{PHL} Driver Propagation Delay Skew (Note 2)	t _{PDS}	R _L = 27Ω, Figure 8			11	ns
Driver Output Enable Time to Low Level	t _{PZL}	R _L = 110Ω, Figure 10	55		100	ns
Driver Output Enable Time to High Level	t _{PZH}	R _L = 110Ω, Figure 9	55		100	ns
Driver Output Disable Time from High Level	t _{PHZ}	R _L = 110Ω, Figure 9	45		80	ns
Driver Output Disable Time from Low Level	t _{PLZ}	R _L = 110Ω, Figure 10	45		80	ns
Driver Output Enable Time from Shutdown to Low Level	t _{PSL}	R _L = 110Ω, Figure 10	700		1000	ns
Driver Output Enable Time from Shutdown to High Level	t _{PSH}	R _L = 110Ω, Figure 9	700		1000	ns

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

DRIVER SWITCHING CHARACTERISTICS—MAX3483 and MAX3488

($V_{CC} = 3.3V$, $T_A = +25^\circ C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Differential Output Delay	t_{DD}	$R_L = 60\Omega$, Figure 7	600	900	1400	ns
Driver Differential Output Transition Time	t_{rD}	$R_L = 60\Omega$, Figure 7	400	700	1200	ns
Driver Propagation Delay, Low-to-High Level	t_{PLH}	$R_L = 27\Omega$, Figure 8	700	1000	1500	ns
Driver Propagation Delay, High-to-Low Level	t_{PHL}	$R_L = 27\Omega$, Figure 8	700	1000	1500	ns
$ t_{PLH} - t_{PHL} $ Driver Propagation Delay Skew (Note 2)	t_{PDS}	$R_L = 27\Omega$, Figure 8		100		ns
DRIVER OUTPUT ENABLE/DISABLE TIMES (MAX3483 only)						
Driver Output Enable Time to Low Level	t_{PZL}	$R_L = 110\Omega$, Figure 10		900	1300	ns
Driver Output Enable Time to High Level	t_{PZH}	$R_L = 110\Omega$, Figure 9		600	800	ns
Driver Output Disable Time from High Level	t_{PHZ}	$R_L = 110\Omega$, Figure 9		50	80	ns
Driver Output Disable Time from Low Level	t_{PLZ}	$R_L = 110\Omega$, Figure 10		50	80	ns
Driver Output Enable Time from Shutdown to Low Level	t_{PSL}	$R_L = 110\Omega$, Figure 10		1.9	2.7	μs
Driver Output Enable Time from Shutdown to High Level	t_{PSH}	$R_L = 110\Omega$, Figure 9		2.2	3.0	μs

RECEIVER SWITCHING CHARACTERISTICS

($V_{CC} = 3.3V$, $T_A = +25^\circ C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time to Shutdown	t_{SHDN}	MAX3483/MAX3485/MAX3486/MAX3491 only (Note 3)	80	190	300	ns
Receiver Propagation Delay, Low-to-High Level	t_{rPLH}	$V_{ID} = 0V$ to $3.0V$, $C_L = 15pF$, Figure 11	25	65	90	ns
		MAX3483/MAX3488	25	75	120	
Receiver Propagation Delay, High-to-Low Level	t_{rPHL}	$V_{ID} = 0V$ to $3.0V$, $C_L = 15pF$, Figure 11	25	65	90	ns
		MAX3483/MAX3488	25	75	120	
$ t_{PLH} - t_{PHL} $ Receiver Propagation Delay Skew	t_{rPDS}	$V_{ID} = 0V$ to $3.0V$, $C_L = 15pF$, Figure 11			10	ns
		MAX3483/MAX3488			20	
Receiver Output Enable Time to Low Level	t_{PPZL}	$C_L = 15pF$, Figure 12, MAX3483/MAX3485/MAX3486/MAX3491 only		25	50	ns
Receiver Output Enable Time to High Level	t_{PPZH}	$C_L = 15pF$, Figure 12, MAX3483/MAX3485/MAX3486/MAX3491 only		25	50	ns
Receiver Output Disable Time from High Level	t_{PRHZ}	$C_L = 15pF$, Figure 12, MAX3483/MAX3485/MAX3486/MAX3491 only		25	45	ns
Receiver Output Disable Time from Low Level	t_{PRLZ}	$C_L = 15pF$, Figure 12, MAX3483/MAX3485/MAX3486/MAX3491 only		25	45	ns
Receiver Output Enable Time from Shutdown to Low Level	t_{PRSL}	$C_L = 15pF$, Figure 12, MAX3483/MAX3485/MAX3486/MAX3491 only		720	1400	ns
Receiver Output Enable Time from Shutdown to High Level	t_{PRSH}	$C_L = 15pF$, Figure 12, MAX3483/MAX3485/MAX3486/MAX3491 only		720	1400	ns

Note 1: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

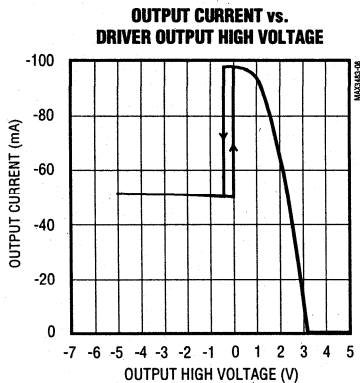
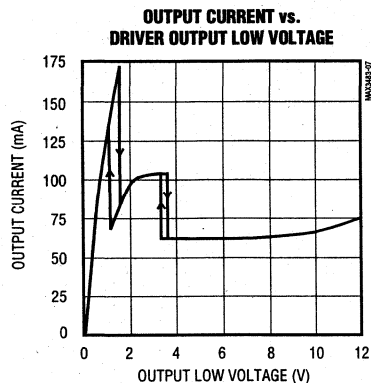
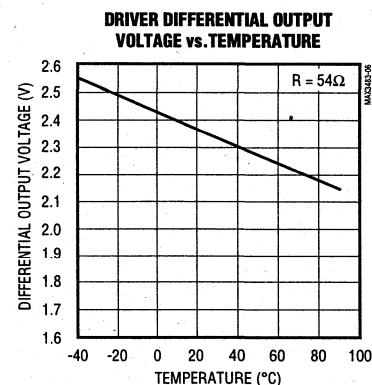
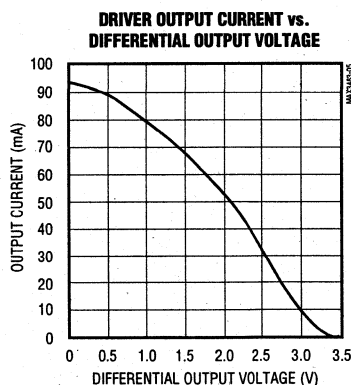
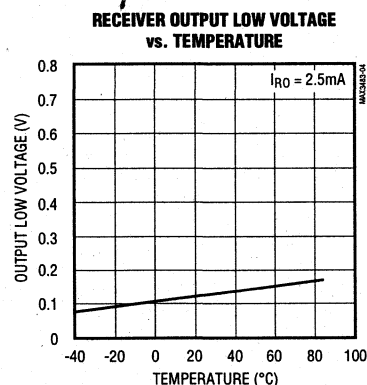
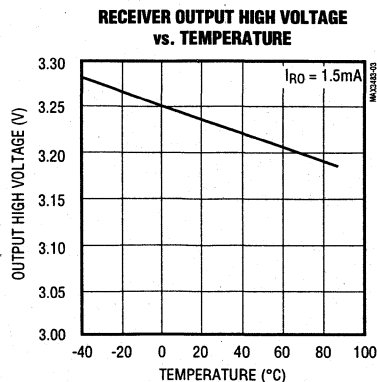
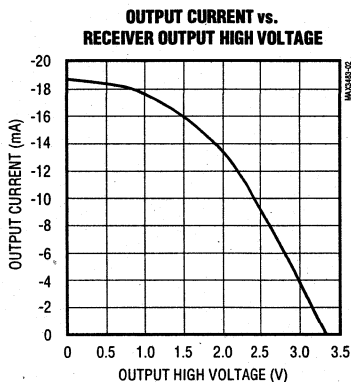
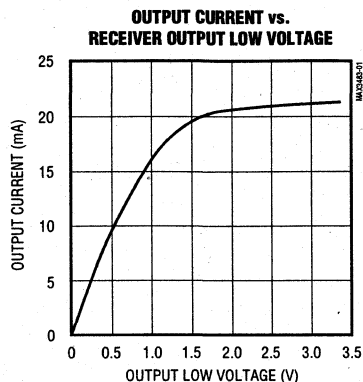
Note 2: Measured on $|t_{PLH}(Y) - t_{PHL}(Y)|$ and $|t_{PLH}(Z) - t_{PHL}(Z)|$.

Note 3: The transceivers are put into shutdown by bringing $\overline{RE}$ high and $\overline{DE}$ low. If the inputs are in this state for less than 80ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 300ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

Typical Operating Characteristics

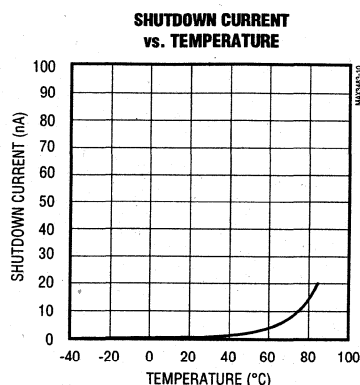
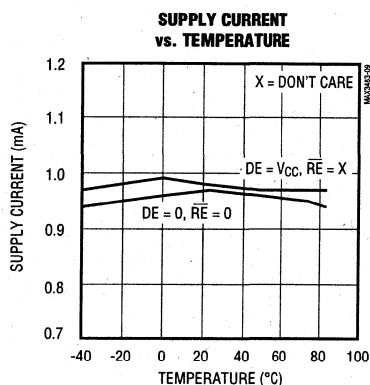
($V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX3483/MAX3485/MAX3486/MAX3488/MAX3490/MAX3491

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

Typical Operating Characteristics (continued)



Pin Description

PIN			NAME	FUNCTION
MAX3483/ MAX3485/ MAX3486	MAX3488/ MAX3490	MAX3491		
1	2	2	RO	Receiver Output. If $A > B$ by 200mV, RO will be high; if $A < B$ by 200mV, RO will be low.
2	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If $\overline{RE}$ is high and DE is low, the device will enter a low-power shutdown mode.
3	—	4	DE	Driver Output Enable. The driver outputs are enabled by bringing DE high. They are high impedance when DE is low. If $\overline{RE}$ is high and DE is low, the device will enter a low-power shutdown mode. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	3	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
—	5	9	Y	Noninverting Driver Output
—	6	10	Z	Inverting Driver Output
6	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	8	12	A	Noninverting Receiver Input
7	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	7	11	B	Inverting Receiver Input
8	1	13, 14	VCC	Positive Supply: $3.0V \leq V_{CC} \leq 3.6V$
—	—	1, 8	N.C.	No Connect—not internally connected

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

MAX3483/MAX3485/MAX3486/MAX3488/MAX3489/MAX3490/MAX3491

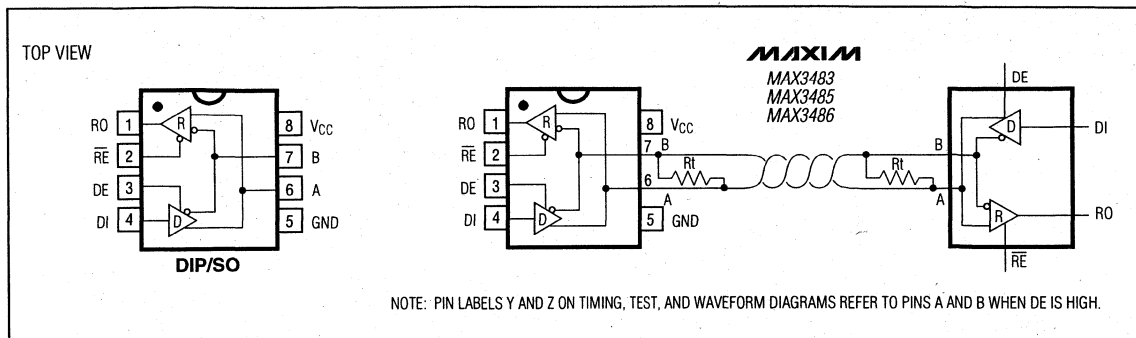


Figure 1. MAX3483/MAX3485/MAX3486 Pin Configuration and Typical Operating Circuit

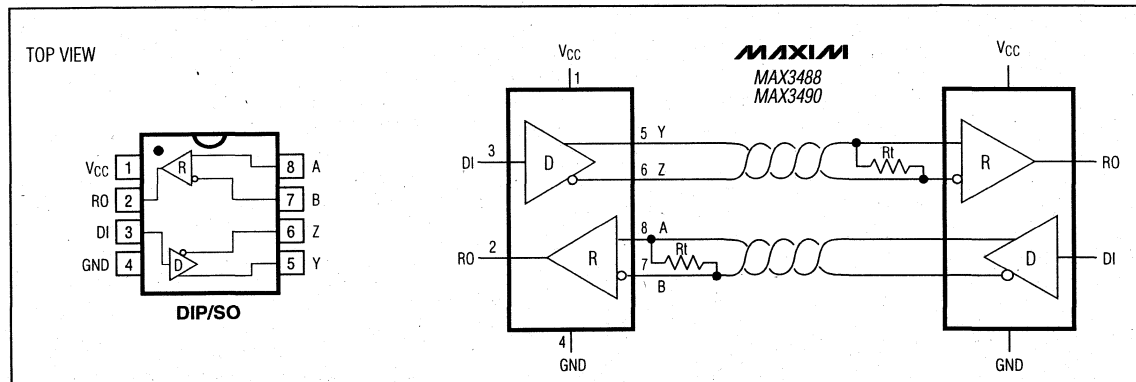


Figure 2. MAX3488/MAX3490 Pin Configuration and Typical Operating Circuit

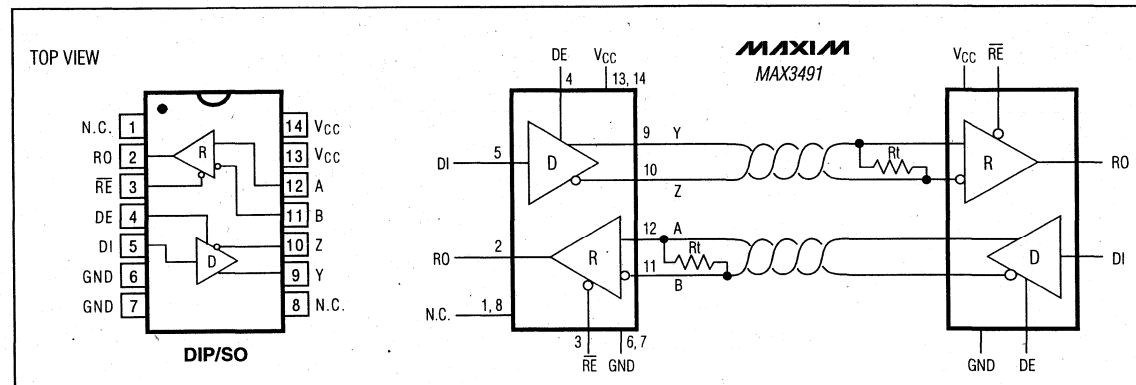


Figure 3. MAX3491 Pin Configuration and Typical Operating Circuit

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

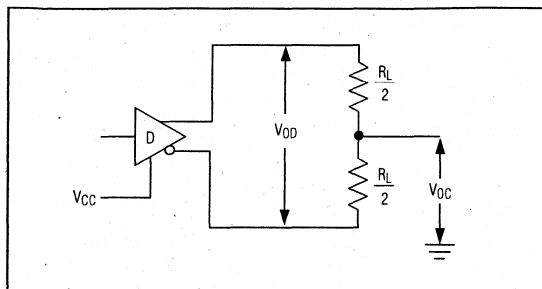


Figure 4. Driver V_{OD} and V_{OC}

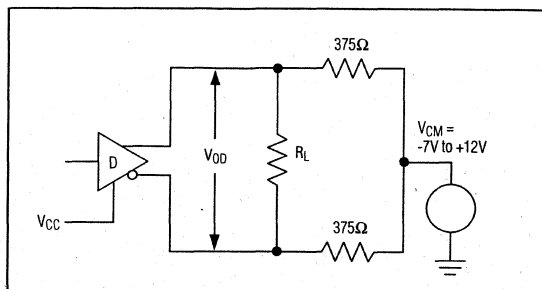


Figure 5. Driver V_{OD} with Varying Common-Mode Voltage

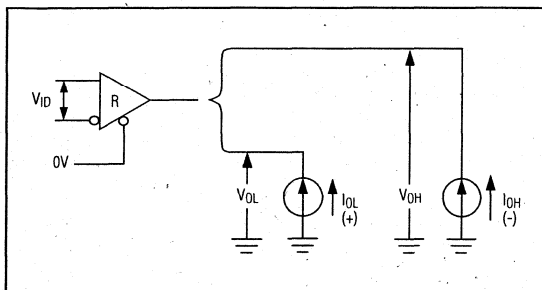


Figure 6. Receiver V_{OH} and V_{OL}

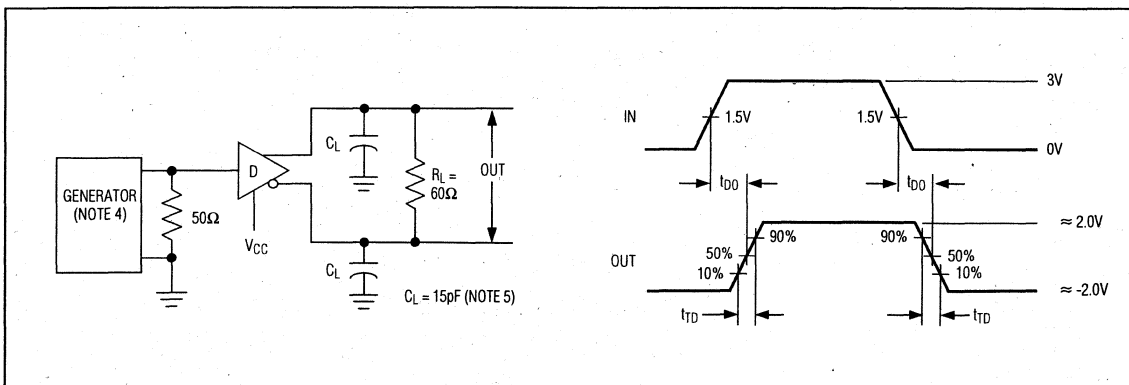


Figure 7. Driver Differential Output Delay and Transition Times

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

MAX3483/MAX3485/MAX3486/MAX3488/MAX3490/MAX3491

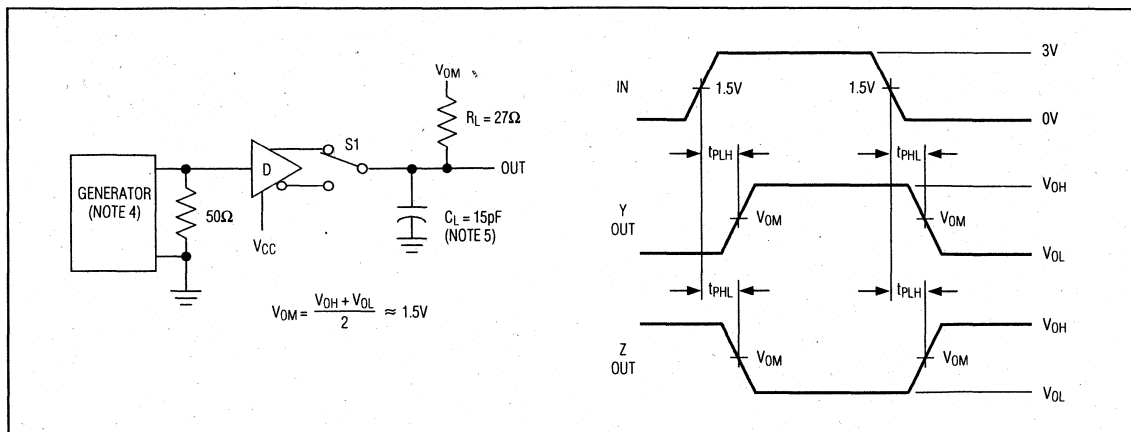


Figure 8. Driver Propagation Times

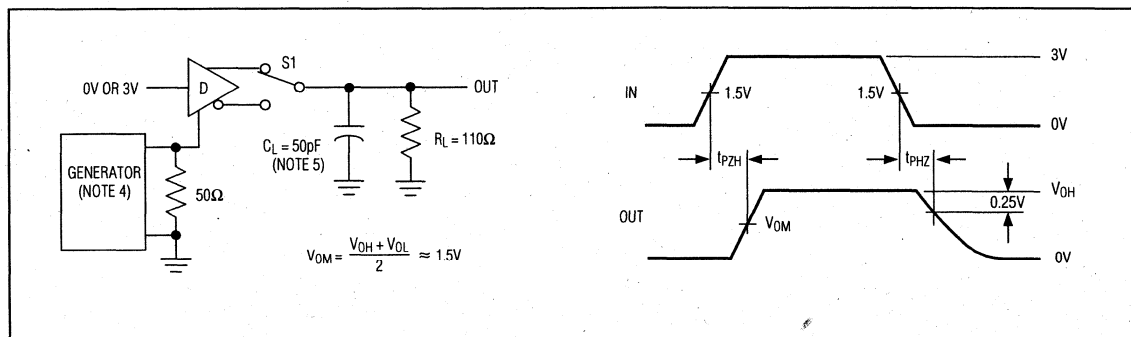


Figure 9. Driver Enable and Disable Times (t_{PZH} , t_{PSH} , t_{PHZ})

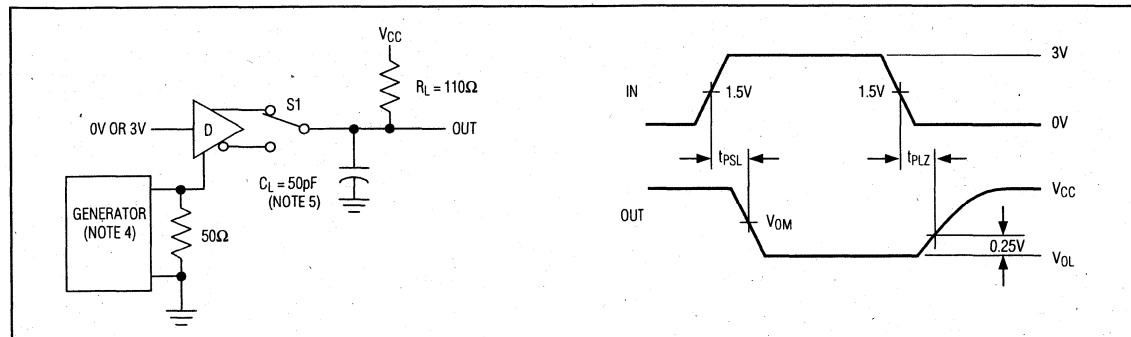


Figure 10. Driver Enable and Disable Times (t_{PZL} , t_{PSL} , t_{PLZ})

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

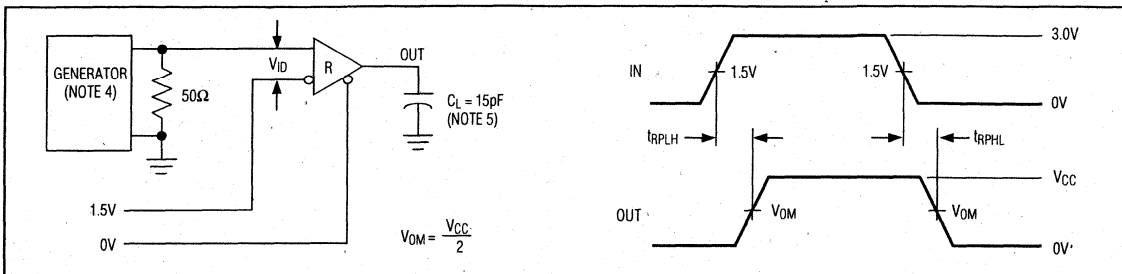


Figure 11. Receiver Propagation Delay

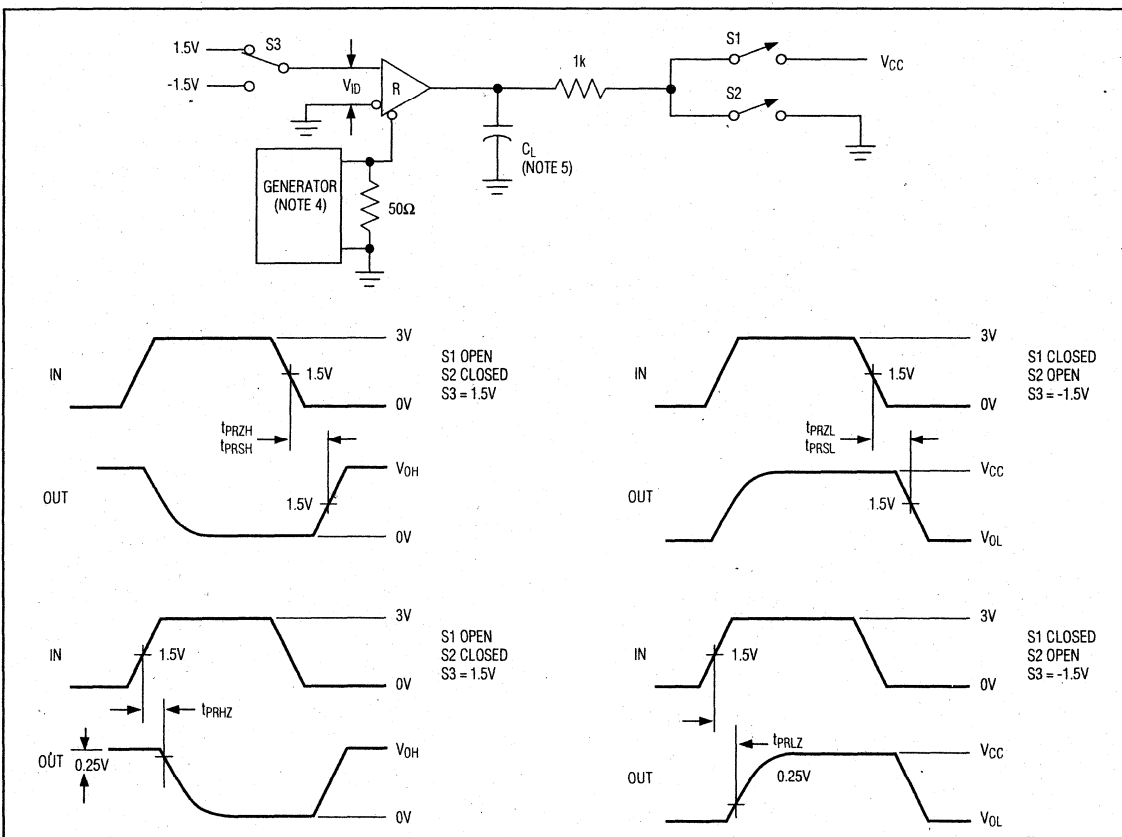


Figure 12. Receiver Enable and Disable Times

Note 4: The input pulse is supplied by a generator with the following characteristics: PRR = 250kHz, 50% duty cycle, $t_r \leq 6.0\text{ns}$, $Z_O = 50\Omega$.

Note 5: C_L includes probe and stray capacitance.

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

Function Tables

Devices with Receiver/Driver Enable (MAX3483/MAX3485/MAX3486/MAX3491)

Table 1. Transmitting

INPUTS			OUTPUTS		MODE
RE	DE	DI	B*	A*	
X	1	1	0	1	Normal
X	1	0	1	0	Normal
0	0	X	High-Z	High-Z	Normal
1	0	X	High-Z	High-Z	Shutdown

* B and A outputs are Z and Y, respectively, for full-duplex part (MAX3491).

X = Don't care; High-Z = High impedance

Table 2. Receiving

INPUTS			OUTPUTS	MODE
RE	DE	A, B	RO	
0	0*	$\geq +0.2V$	1	Normal
0	0*	$\leq -0.2V$	0	Normal
0	0*	Inputs Open	1	Normal
1	0	X	High-Z	Shutdown

* DE is a "don't care" (x) for the full-duplex part (MAX3491).

X = Don't care; High-Z = High impedance

Devices without Receiver/Driver Enable (MAX3488/MAX3490)

Table 3. Transmitting

INPUT	OUTPUTS	
DI	Z	Y
1	0	1
0	1	0

Table 4. Receiving

INPUTS	OUTPUT
A, B	RO
$\geq +0.2V$	1
$\leq -0.2V$	0
Inputs Open	1

Applications Information

The MAX3483/MAX3485/MAX3486/MAX3488/MAX3490/MAX3491 are low-power transceivers for RS-485 and RS-422 communications. The MAX3483 and MAX3488 can transmit and receive at data rates up to 250kbps, the MAX3486 at up to 2.5Mbps, and the MAX3485/MAX3490/MAX3491 at up to 10Mbps. The MAX3488/MAX3490/MAX3491 are full-duplex transceivers, while the MAX3483/MAX3485/MAX3486 are half-duplex. Driver Enable (DE) and Receiver Enable (RE) pins are included on the MAX3483/MAX3485/MAX3486/MAX3491. When disabled, the driver and receiver outputs are high impedance.

Reduced EMI and Reflections (MAX3483/MAX3486/MAX3488)

The MAX3483/MAX3488 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 13 shows both the driver output waveform of a MAX3485/MAX3490/MAX3491 transmitting a 125kHz signal and the Fourier analysis of that waveform. High-frequency harmonics with large amplitudes are evident. Figure 14 shows the same information, but for the slew-rate-limited MAX3483/MAX3488 transmitting the same signal. The high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power Shutdown Mode (MAX3483/MAX3485/MAX3486/MAX3491)

A low-power shutdown mode is initiated by bringing both RE high and DE low. The devices will not shut down unless both the driver and receiver are disabled (high impedance). In shutdown, the devices typically draw only 2nA of supply current.

For these devices, the t_{PSH} and t_{PSL} enable times assume the part was in the low-power shutdown mode; the t_{PZH} and t_{PZL} enable times assume the receiver or driver was disabled, but the part was not shut down.

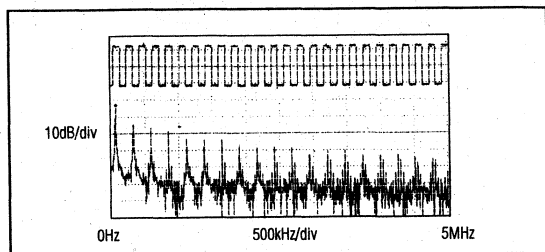


Figure 13. Driver Output Waveform and FFT Plot of MAX3485/MAX3490/MAX3491 Transmitting a 125kHz Signal

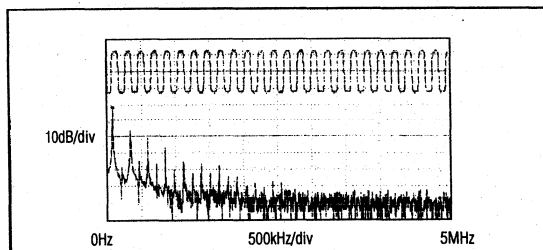


Figure 14. Driver Output Waveform and FFT Plot of MAX3483/MAX3488 Transmitting a 125kHz Signal

MAX3483/MAX3485/MAX3486/MAX3488/MAX3490/MAX3491

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

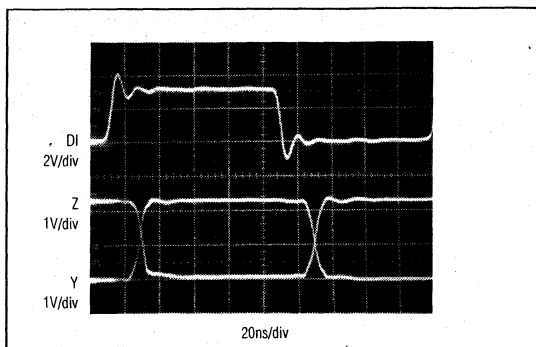


Figure 15. MAX3485/MAX3490/MAX3491 Driver Propagation Delay

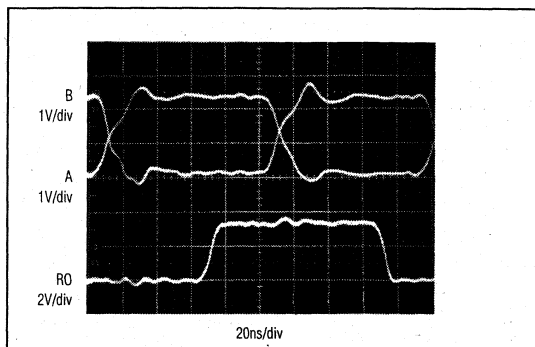


Figure 16. MAX3485/MAX3490/MAX3491 Receiver Propagation Delay Driven by External RS-485 Device

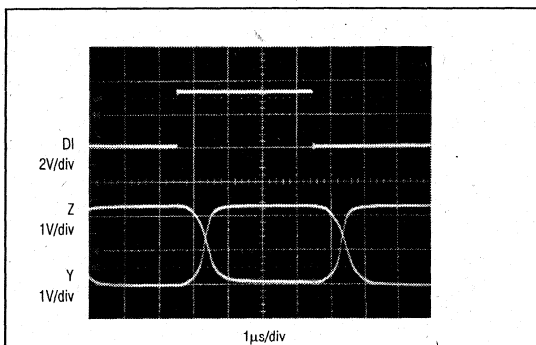


Figure 17. MAX3483/MAX3488 Driver Propagation Delay

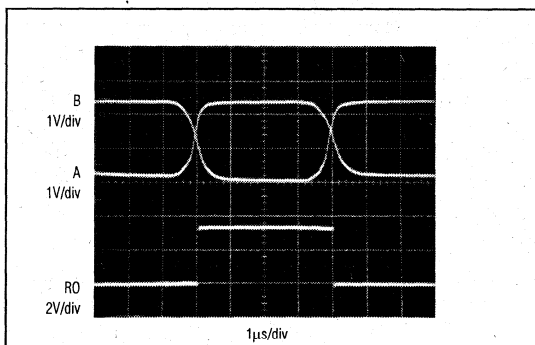


Figure 18. MAX3483/MAX3488 Receiver Propagation Delay

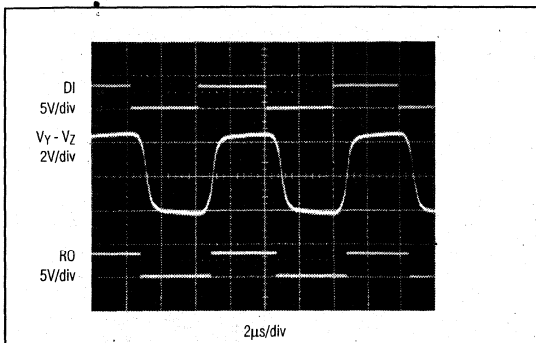


Figure 19. MAX3483/MAX3488 System Differential Voltage at 125kHz Driving 4000 ft of Cable

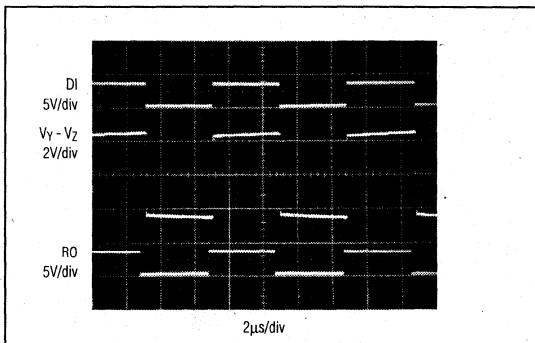


Figure 20. MAX3485/MAX3490/MAX3491 System Differential Voltage at 125kHz Driving 4000 ft of Cable

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

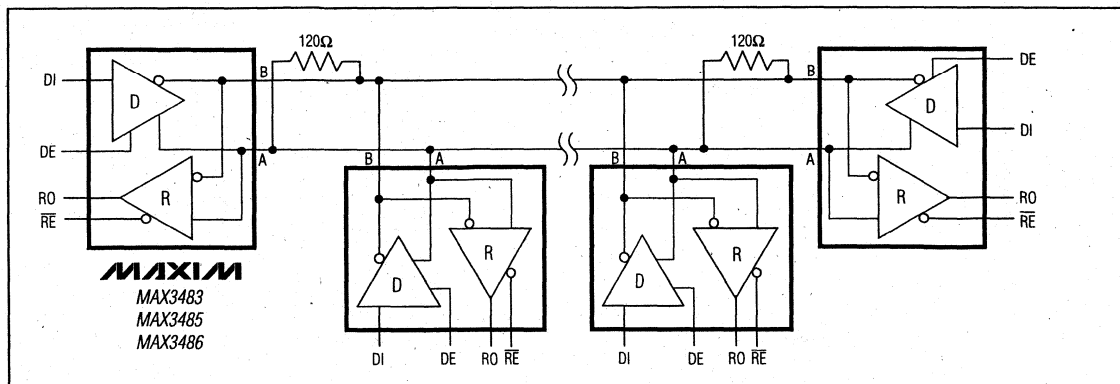


Figure 21. MAX3483/MAX3485/MAX3486 Typical RS-485 Network

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shut-down circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Figures 15–18 show the typical propagation delays. Skew time is simply the difference between the low-to-high and high-to-low propagation delay. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle).

The receiver skew time, $|t_{PRHL} - t_{PRHL}|$, is under 10ns (20ns for the MAX3483/MAX3488). The driver skew times are 8ns for the MAX3485/MAX3490/MAX3491, 11ns for the MAX3486, and typically under 100ns for the MAX3483/MAX3488.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 23.

Figures 19 and 20 show the system differential voltage for parts driving 4000 feet of 26AWG twisted-pair wire at 125kHz into 120Ω loads.

Typical Applications

The MAX3483, MAX3485, MAX3486, MAX3488, MAX3490, and MAX3491 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 21 and 22 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 23.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX3483/MAX3488 and the partially slew-rate-limited MAX3486 are more tolerant of imperfect termination.

MAX3483/MAX3485/MAX3486/MAX3488/MAX3489/MAX3490/MAX3491

3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

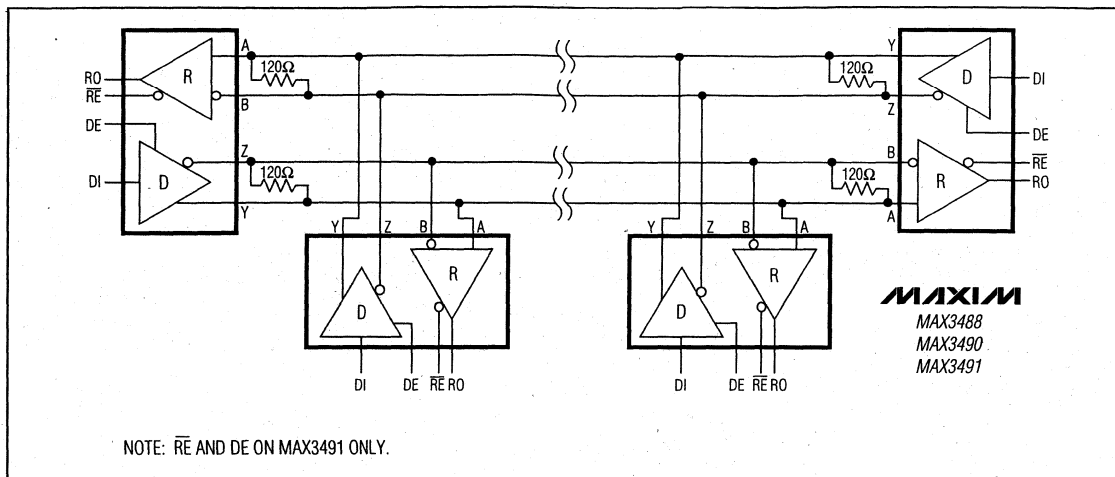


Figure 22. MAX3488/MAX3490/MAX3491 Full-Duplex RS-485 Network

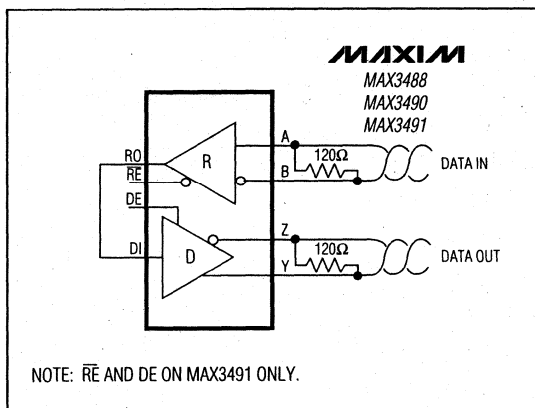


Figure 23. Line Repeater for MAX3488/MAX3490/MAX3491

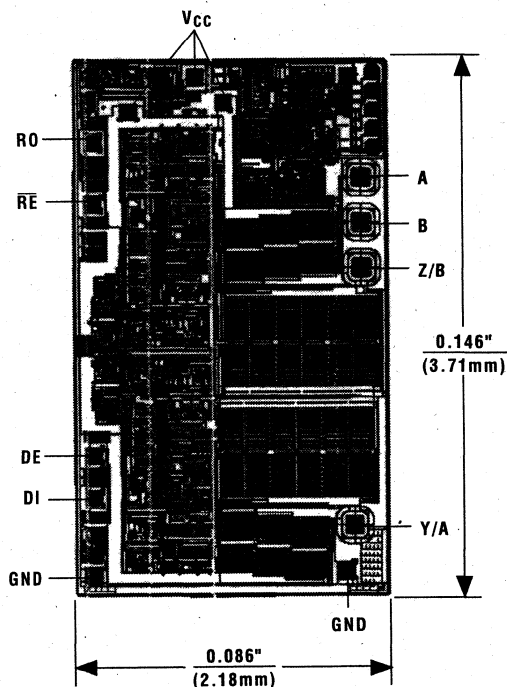
3.3V-Powered, 10Mbps and Slew-Rate-Limited True RS-485/RS-422 Transceivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX3486 CPA	0°C to +70°C	8 Plastic DIP
MAX3486CSA	0°C to +70°C	8 SO
MAX3486C/D	0°C to +70°C	Dice*
MAX3486EPA	-40°C to +85°C	8 Plastic DIP
MAX3486ESA	-40°C to +85°C	8 SO
MAX3488 CPA	0°C to +70°C	8 Plastic DIP
MAX3488CSA	0°C to +70°C	8 SO
MAX3488C/D	0°C to +70°C	Dice*
MAX3488EPA	-40°C to +85°C	8 Plastic DIP
MAX3488ESA	-40°C to +85°C	8 SO
MAX3490 CPA	0°C to +70°C	8 Plastic DIP
MAX3490CSA	0°C to +70°C	8 SO
MAX3490C/D	0°C to +70°C	Dice*
MAX3490EPA	-40°C to +85°C	8 Plastic DIP
MAX3490ESA	-40°C to +85°C	8 SO
MAX3491 CPD	0°C to +70°C	14 Plastic DIP
MAX3491CSD	0°C to +70°C	14 SO
MAX3491C/D	0°C to +70°C	Dice*
MAX3491EPD	-40°C to +85°C	14 Plastic DIP
MAX3491ESD	-40°C to +85°C	14 SO

* Contact factory for dice specifications.

Chip Topography



TRANSISTOR COUNT: 810

SUBSTRATE CONNECTED TO GROUND

MAX3483/MAX3485/MAX3486/MAX3488/MAX3490/MAX3491

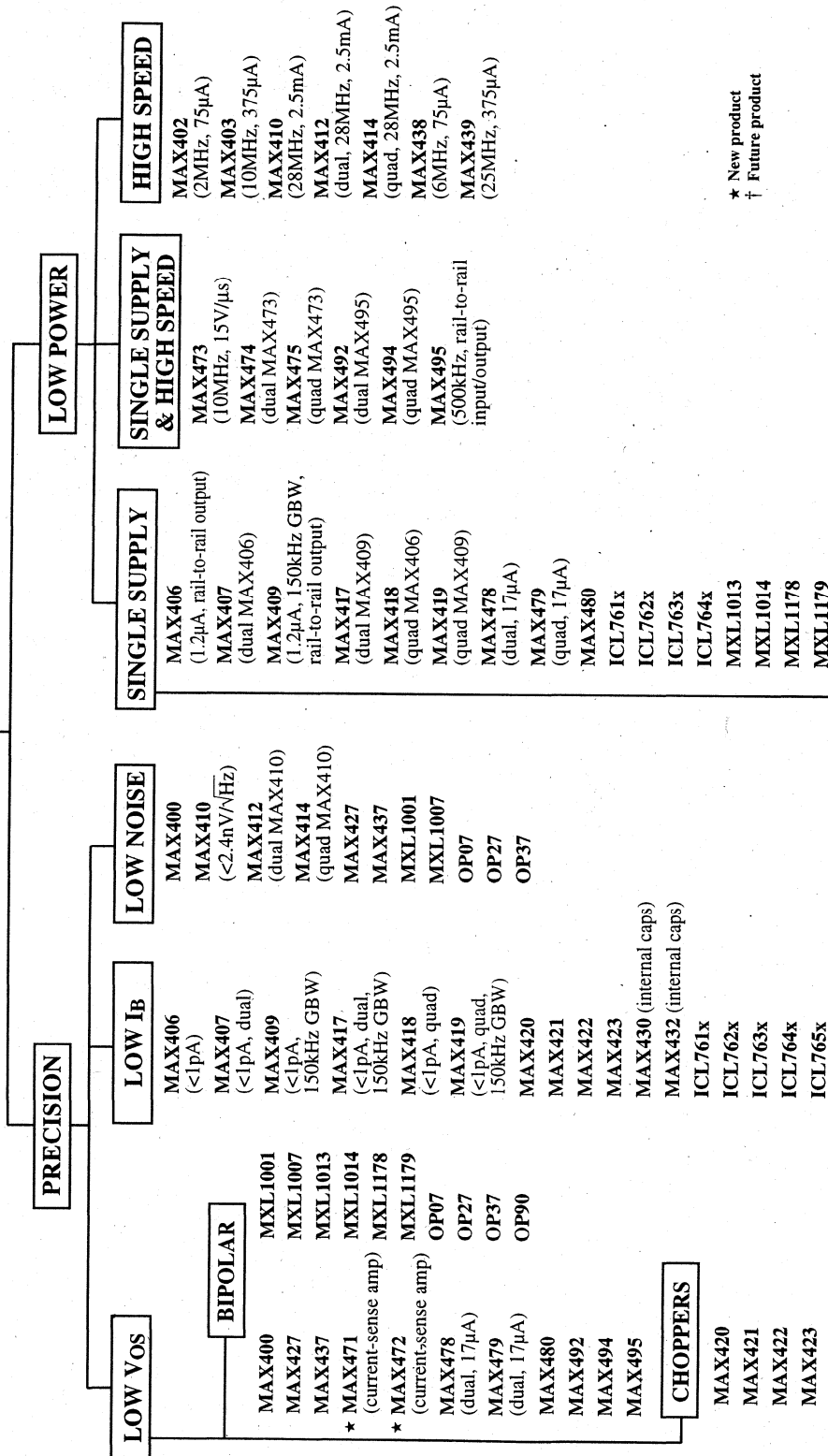


Op Amps/Comparators

Op Amps/Comparators, Product Tables and Trees	3-2
MAX471 Precision, High-Side Current-Sense Amp	3-7
MAX472 Precision, High-Side Current-Sense Amp	3-7
MAX473 Single, 10MHz, Single-Supply Op Amp	3-19
MAX474 Dual, 10MHz, Single-Supply Op Amp	3-19
MAX475 Quad, 10MHz, Single-Supply Op Amp	3-19
MAX492 Dual, Micropower, Single-Supply Op Amp w/ Rail-to-Rail I/O	3-31
MAX494 Quad, Micropower, Single-Supply Op Amp w/ Rail-to-Rail I/O	3-31
MAX495 Single, Micropower, Single-Supply Op Amp w/ Rail-to-Rail I/O	3-31
MAX951 Ultra-Low-Power, Single-Supply Op Amp and Comparator w/ Reference*	3-47
MAX952 Ultra-Low-Power, Single-Supply Op Amp and Comparator w/ Reference*	3-47
MAX953 Ultra-Low-Power, Single-Supply Op Amp and Comparator*	3-47
MAX954 Ultra-Low-Power, Single-Supply Op Amp and Comparator*	3-47

*Advance Information—first page of data sheet in preparation.

OP AMPS



★ New product
† Future product

† MAX951 (10μA, 20kHz op amp + comparator + reference)
† MAX952 (10μA, 125kHz op amp + comparator + reference)
† MAX953 (8μA, 20kHz op amp + comparator)
† MAX954 (8μA, 125kHz op amp + comparator)

Part Number	V _{os} (mV max)	TCV _{os} (μ V/°C max)	I _{bias} (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current per Op Amp (mA max)	Features	Price† 1000-up (\$)
MAX400	10 to 15 μ V	0.3	2	0.4	± 3 to ± 18	4	Ultra-low V _{os} & drift, non-chopper stabilized	5.16
MAX402	2	25 typ	5	2	± 3 to ± 5	75 μ A	High speed, micropower	1.98
MAX403	2	25 typ	25	10	± 3 to ± 5	375 μ A	High speed, micropower	2.75
MAX406/407/418	0.5 to 4	10	10pA	8 to 40kHz	± 2.5 to ± 10	1.2 μ A	Single/dual/quad, lowest power, single supply, rail-to-rail outputs, unity-gain stable	1.95/2.98/3.98
MAX409/417/419	0.5 to 4	10	10pA	150kHz (A _v ≥ 10 V/V)	± 2.5 to ± 10	1.2 μ A	Single/dual/quad, lowest power, decompensated (A _v ≥ 10 V/V)	1.95/2.98/3.98
MAX410/412/414	250 μ V (320 μ V MAX414)	1 typ	150	28	± 2.4 to ± 2.5	2.7	Single/dual/quad, high speed, low noise, < 2.4nV/Hz at 1kHz guaranteed, unity-gain stable	1.50/2.45/4.50
MAX420/422	5 to 10 μ V	0.05	0.03 to 0.10	0.125 to 0.5	± 15	0.5 to 2	± 15 V chopper stabilized	3.77/4.21
MAX421/423	5 to 10 μ V	0.05	0.03 to 0.10	0.125 to 0.5	± 15	0.5 to 2	± 15 V chopper stabilized with clamped output and INT/EXT clock option	4.21/5.57
MAX427/437	15 μ V	0.8	35	8/60	± 15	4	High speed, low noise 3.8nV/Hz precision	1.83
MAX430/432	5 μ V	0.05	0.1	0.125 to 0.5	± 15	0.5 to 2	± 15 V chopper stabilized with internal caps	4.80/5.29
MAX438	2	25 typ	5	6 (A _v ≥ 5 V/V)	± 3 to ± 5	75 μ A	High speed, micropower; 10V/ μ s slew rate	1.98
MAX439	2	25 typ	25	25 (A _v ≥ 5 V/V)	± 3 to ± 5	375 μ A	High speed, micropower; 48V/ μ s slew rate	2.75
MAX471	-	-	-	-	± 3 to ± 36	100 μ A	Precision, high-side current-sense amplifier with internal sense resistor, measures charge and discharge	2.50
MAX472	60 μ V	-	-	-	± 3 to ± 36	100 μ A (5 μ A SHDN)	Precision, high-side current-sense amplifier	2.05
MAX473/474/475	1 to 1.5	2 typ	150	10	± 2.7 to ± 6	3	Single/dual/quad, single or dual supply, wide output swing, 15V/ μ s min slew rate	1.45/2.25/3.60
MAX478/479	70 to 250 μ V	4.5	6	60kHz	± 2.2 to ± 36 ± 1.1 to ± 18	17 μ A	Micropower, precision dual 8-pin SO and quad 14-pin narrow SO, 3V, 5V, and ± 15 V specs	2.58/3.35
MAX480	70 μ V	1.5	3	20kHz	± 1.6 to ± 36 ± 0.8 to ± 18	15 μ A	Low V _{os} & drift, micropower, single supply, input/output extend to negative rail	3.68
MAX492/494/495	500 μ V	2 typ	60	500kHz	± 2.7 to ± 6	150 μ A	Single/dual/quad, precision, rail-to-rail input and output	2.25/3.60/1.45
ICL7611	2 to 15	10 to 25 typ	0.05	0.044 to 1.4	± 1.0 to ± 8	0.02 to 2.5	Programmable quiescent current	1.35
ICL7612	5 to 15	15 to 25 typ	0.05	0.044 to 1.4	± 1.0 to ± 8	0.02 to 2.5	Programmable quiescent current, rail-to-rail input and output	1.29
ICL7614	2 to 15	15 to 25 typ	0.05	0.48*	± 1.0 to ± 8	0.25	External compensation	0.95
ICL7616	2 to 15	15 to 25 typ	0.05	0.044 to 1.4	± 1.0 to ± 8	0.02 to 2.5	Programmable quiescent current, extended CMVR	1.62
ICL7621/7622	5 to 15	15 to 25 typ	0.05	0.48	± 1.0 to ± 8	0.25	Dual, low I _{bias} & I _{os}	1.06/1.48
ICL7631/7632	5 to 20	15 to 30 typ	0.05	0.044 to 1.4	± 1.0 to ± 8	0.022 to 2.5	Triple op amp, programmable quiescent current	2.27/2.12
ICL7641/7642	5 to 25	15 to 30 typ	0.05	0.044 to 1.4	± 1.0 to ± 8	0.015 to 2.5	ICL7632 is externally compensated	1.41/1.56
ICL7650	5 to 10 μ V	0.05 to 0.10	0.01 to 0.02	2	± 5	2	Quad, low power, CMOS	2.16
ICL7652	5 to 10 μ V	0.05	0.03	0.45	± 5	2	Industry standard, chopper stabilized	3.24
LH0101	3 to 10	10 typ	300 to 1k	5	± 5 to ± 15	35	Low noise, industry standard, chopper stabilized	18.98
MXL1001	15 to 60 μ V	0.6 to 1	2 to 4	0.8	± 3 to ± 18	2	5A peak power	1.73
MXL1007	25 to 60 μ V	0.6 to 1	35 to 55	8	± 15	4 to 4.7	Precision LT1001 second source	1.85
MXL1013/1014	150 to 800 μ V	2 to 5	20 to 30	0.6	± 4 to ± 36 ± 2 to ± 18	0.50 to 0.55	Low noise, precision LT1007 second source	1.57/3.06
MXL1178/1179	70 to 600 μ V	3 to 4.5	5 to 6	60kHz	± 2.2 to ± 36 ± 1.1 to ± 18	17 to 21 μ A	Dual/quad, precision, micropower LT1178/1179 second source	2.50/3.35

* External 39pF compensation capacitor added.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Op Amps (continued)

Part Number	Vos (mV max)	TCVos ($\mu\text{V}/^\circ\text{C}$ max)	I _{BIAS} (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current per Op Amp (mA max)	Features	Price† 1000-up (\$)
OP07	25 to 150 μV	0.6 to 2.5	2 to 12	0.6	± 3 to ± 18	4	Industry standard, precision	1.58
OP27	25 to 100 μV	0.6 to 1.8	40 to 80	8	± 3 to ± 18	4.6 to 5.6	Industry standard, low noise	2.06
OP37	25 to 100 μV	0.6 to 1.8	40 to 80	63 ($A_V \geq 5$)	± 3 to ± 18	4.6 to 5.6	Industry standard, low noise	2.06
OP90	150 to 450 μV	2 to 5	15 to 25	0.020	± 0.8 to ± 18	15 to 20 μA	Industry standard, micropower	1.60
					± 1.6 to ± 36			

Op Amp + Comparator + Reference ICs

Part Number	Op Amp Compensation	Op Amp GBW (kHz)	Comparator	Reference (1.2V $\pm 1\%$)	Supply Voltage (V min)	Supply Current (μA max)	Features	Price† 1000-up (\$)
MAX951	Unity-gain stable	20	✓	✓	2.8	10	Single supply, rail-to-rail outputs. 8-pin package. op amp drives capacitive loads	++
MAX952	Decompensated ($A_V \geq 10\text{V/V}$)	125	✓	✓	2.8	10	MAX951 with decompensated op amp for $A_V \geq 10\text{V/V}$	++
MAX953	Unity-gain stable	20	✓		2.4	8	MAX951 without the reference	++
MAX954	Decompensated ($A_V \geq 10\text{V/V}$)	125	✓		2.4	8	MAX953 with decompensated op amp for $A_V \geq 10\text{V/V}$	++

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++ Future product—contact factory for pricing and availability. Specifications are preliminary.

COMPARATORS

SPECIAL

- MAX516
(quad, programmable input threshold voltage)
- MAX910
(8ns, programmable input threshold voltage)
- MAX911
(4ns, programmable input threshold voltage)

HIGH-SPEED COMPARATORS

TTL OUTPUT Single/Dual Supply

<10ns

- MAX900
(quad, 8ns, single/dual supply)
- MAX901
(quad, 8ns, single/dual supply)
- MAX902
(dual, 8ns, single/dual supply)
- MAX903
(8ns, single/dual supply)
- MAX910
(8ns, programmable input threshold)

<50ns

- MAX907
(dual, 40ns, single supply)
- MAX908
(quad, 40ns, single supply)
- MAX909
(40ns, single/dual supply)

3V, HIGH SPEED

- MAX941
(350 μ A, 80ns, rail-to-rail inputs)
- MAX942
(dual MAX941)
- MAX944
(quad MAX941)

ECL OUTPUT

- MAX905
(master/slave, clocked)
- MAX906
(dual, master/slave, clocked)
- MAX911
(4ns, programmable input threshold voltage)
- MAX9685
(industry standard)
- MAX9687
(industry standard, dual)
- MAX9690 (8-pin SO)

MICROPOWER

- MAX921
(3.2 μ A comparator + 1% reference)
- MAX922
(dual, 3.2 μ A max supply current)
- MAX923
(dual, 4.5 μ A comparator + 1% reference)
- MAX924
(quad, 6.5 μ A comparator + 1% reference)
- MAX931
(3.2 μ A comparator + 2% reference)
- MAX932
(dual, 4.5 μ A comparator + 2% reference)
- MAX933
(dual, 4.5 μ A comparator + 2% reference, window comparator)
- MAX934
(quad, 6.5 μ A comparator + 2% reference)

SPECIAL

- MAX951
(10 μ A, 20kHz op amp + comparator + reference)
- MAX952
(10 μ A, 125kHz op amp + comparator + reference)
- MAX953
(8 μ A, 20kHz op amp + comparator)
- MAX954
(8 μ A, 125kHz op amp + comparator)

+ Future product

Comparators (High-Speed & Micropower)

Part Number	Comps. per Pkg.	Logic	Latched Outputs	Complementary Outputs	Single-Supply Operation	Supply Current per Comparator (mA max)	Tpd (ns)	Features	Price* 1000-up (\$)
HIGH SPEED									
MAX516	4	TTL/CMOS	No	No	Yes	10.01 (total pkg.)	800	Quad comparator + quad 8-bit DAC for independent threshold setting. single-supply capability, rail-to-rail input voltage ranges	3.00
MAX900	4	TTL	Yes	No	Yes	4 (I _{CC})	8	Single +5V capability, low power, CMVR extends to neg. rail. separate analog & digital supplies, internal pull-up resistors	7.01
MAX901	4	TTL	No	No	Yes	4 (I _{CC})	8	MAX900 without output latch	5.98
MAX902	2	TTL	Yes	No	Yes	4 (I _{CC})	8	Dual MAX900	4.01
MAX903	1	TTL	Yes	No	Yes	4 (I _{CC})	8	Dual MAX900	3.15
MAX905	1	ECL	Yes	Yes	No	24 (I _{EE})	1.8	Single MAX900 Edge-triggered master/slave architecture eliminates oscillations and resolves 3mV input voltages	3.54
MAX906	2	ECL	Yes	Yes	No	24 (I _{EE})	1.8	Dual MAX905	5.23
MAX907	2	TTL	No	No	Yes	1	30	High speed, ultra-low power, single +5V, 8-pin DIP/SO, built-in hysteresis	1.70
MAX908	4	TTL	No	No	Yes	1	30	High speed, ultra-low power, single +5V, 14-pin DIP/SO, built-in hysteresis	2.95
MAX909	1	TTL	Yes	Yes	Yes	1.8	30+	High speed, low power, single or dual supply, input range includes ground, complementary outputs	1.50
MAX910	1	TTL	Yes	No	No	30 (I _{CC})	8	TTL-compatible, 8-bit digitally programmable input voltage threshold, on-board reference	5.20
MAX911	1	ECL	Yes	Yes	No	30 (I _{EE})	4	MAX910 with differential ECL outputs	5.20
MAX912	2	TTL	Yes	Yes	Yes	10	10	Dual MAX913	3.90
MAX913	1	TTL	Yes	Yes	Yes	10	10	Lowest power, 10ns comparator with complementary outputs single/dual supply, CMVR extends below ground to V ₊ - 1.5V	2.55
MAX915	1	TTL	Yes	Yes	No	18 (I _{CC})	6	No oscillations, master/slave, clocked	2.55
MAX916	2	TTL	Yes	Yes	Yes	18 (I _{CC})	6	Dual MAX915	3.90
MAX941	1	TTL/CMOS	Yes	No	Yes	600μA	75	Low power, 3V or 5V single supply, rail-to-rail inputs (5μA SHDN)	1.40
MAX942	2	TTL/CMOS	No	No	Yes	600μA	75	Dual MAX941, 8-pin DIP/SO	1.50
MAX944	4	TTL/CMOS	No	No	Yes	600μA	75	Quad MAX941	2.50
MAX9685	1	ECL	Yes	Yes	No	32 (I _{EE})	1.3	Higher-speed industry standard	3.38
MAX9686	1	TTL	Yes	Yes	No	25 (I _{CC})	6	Higher-speed industry standard	2.31
MAX9687	2	ECL	Yes	Yes	No	68 (I _{EE})	1.4	Higher-speed industry standard	5.12
MAX9690	1	ECL	No	Yes	No	32 (I _{EE})	1.3	8-pin DIP/SO package	3.29
MAX9698	2	TTL	Yes	Yes	No	50 (I _{CC})	6	Higher-speed industry standard	3.92
MXL1016	1	TTL	Yes	Yes	Yes	35 (I _{CC})	10	High speed, complementary outputs, LTI016 second source	2.57
MXL1116	1	TTL	Yes	Yes	Yes	38 (I _{CC})	12	High speed, single supply, complementary outputs, LTI116 second source	2.57
MICROPOWER									
MAX921	1 + ref	TTL/CMOS	No	No	Yes	3.2μA (total pkg.)	12μs	Micropower comparator + 1% reference & hysteresis, single-supply capability, CMVR extends to GND	1.50
MAX922	2	TTL/CMOS	No	No	Yes	3.2μA (total pkg.)	12μs	Dual, single-supply micropower comparator, in 8-pin DIP/SO	1.50
MAX923	2 + ref	TTL/CMOS	No	No	Yes	4.5μA (total pkg.)	12μs	Dual, single-supply comparator with 1% voltage reference in 8-pin DIP/SO	1.95
MAX924	4 + ref	TTL/CMOS	No	No	Yes	6.5μA (total pkg.)	12μs	Quad, micropower comparator with 1% voltage reference	2.25
MAX931	1 + ref	TTL/CMOS	No	No	Yes	3.2μA (total pkg.)	12μs	Comparator + 2% reference & hysteresis, single-supply, CMVR extends to GND	0.98
MAX932	2 + ref	TTL/CMOS	No	No	Yes	4.5μA (total pkg.)	12μs	Dual, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO	1.26
MAX933	2 + ref	TTL/CMOS	No	No	Yes	4.5μA (total pkg.)	12μs	Dual, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO (window comparator input configuration)	1.26
MAX934	4 + ref	TTL/CMOS	No	No	Yes	6.5μA (total pkg.)	12μs	Quad comparator + 2%-accurate reference, single/dual supply	1.31
MAX951-954 (See Op Amp section for tables)									

* Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

MAXIM

Precision, High-Side Current-Sense Amplifiers

General Description

The MAX471/MAX472 are complete, bidirectional, high-side current-sense amplifiers for portable PCs, telephones, and other systems where battery/DC power-line monitoring is critical. High-side power-line monitoring is especially useful in battery-powered systems, since it does not interfere with the ground paths of the battery chargers or monitors often found in "smart" batteries.

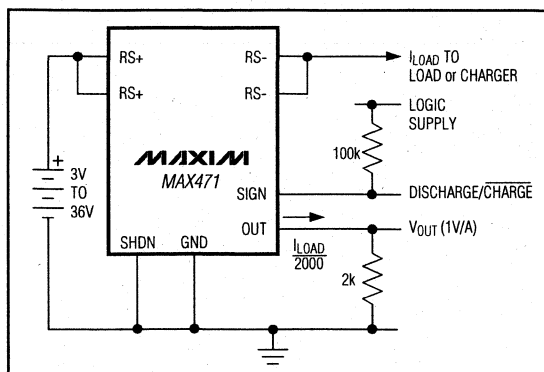
The MAX471 has an internal 35mΩ current-sense resistor and measures battery currents up to $\pm 3A$. For applications requiring higher current or increased flexibility, the MAX472 functions with external sense and gain-setting resistors. Both devices have a current output that can be converted to a ground-referred voltage with a single resistor, allowing a wide range of battery voltages and currents.

An open-collector SIGN output indicates current-flow direction, so the user can monitor whether a battery is being charged or discharged. Both devices operate from 3V to 36V, draw less than 100μA over temperature, and include a 5μA max shutdown mode.

Applications

Portable PCs:
Notebooks/Subnotebooks/Palmtops
Smart Battery Packs
Cellular Phones
Portable Phones
Portable Test/Measurement Systems
Battery-Operated Systems
Energy Management Systems

Typical Operating Circuit



Features

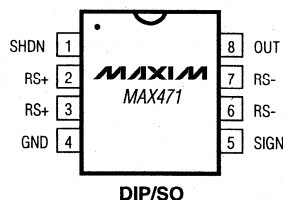
- ◆ Complete High-Side Current Sensing
- ◆ Precision Internal Sense Resistor (MAX471)
- ◆ 2% Accuracy Over Temperature
- ◆ Monitors Both Charge and Discharge
- ◆ 3A Sense Capability with Internal Sense Resistor (MAX471)
- ◆ Higher Current-Sense Capability with External Sense Resistor (MAX472)
- ◆ 100μA Max Supply Current
- ◆ 5μA Max Shutdown Mode
- ◆ 3V to 36V Supply Operation
- ◆ 8-Pin DIP/SO Packages

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX471CPA	0°C to +70°C	8 Plastic DIP
MAX471CSA	0°C to +70°C	8 SO
MAX471EPA	-40°C to +85°C	8 Plastic DIP
MAX471ESA	-40°C to +85°C	8 SO
MAX472CPA	0°C to +70°C	8 Plastic DIP
MAX472CSA	0°C to +70°C	8 SO
MAX472EPA	-40°C to +85°C	8 Plastic DIP
MAX472ESA	-40°C to +85°C	8 SO

Pin Configurations

TOP VIEW



MAX472 Pin Configuration continued on last page.

Precision, High-Side Current-Sense Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, RS+, RS-, VCC to GND-0.3V, +40V
 RMS Current, RS+ to RS- (MAX471 only)±3.3A
 Peak Current, (RS+ to RS-)see Figure 5
 Differential Input Voltage, RG1 to RG2 (MAX472 only)±0.3V
 Voltage at Any Pin Except SIGN
 MAX471 only-0.3V to (RS+ - 0.3V)
 MAX472 only-0.3V to (VCC + 0.3V)
 Voltage at SIGN-0.3V to +40V
 Current into SHDN, GND, OUT, RG1, RG2, VCC±50mA
 Current into SIGN+10mA, -50mA

Continuous Power Dissipation (T_A = +70°C)

MAX471 (Note 1):

Plastic DIP (derate 17.5mW/°C above +70°C)1.4W

SO (derate 9.9mW/°C above +70°C)791mW

MAX472:

Plastic DIP (derate 9.09mW/°C above +70°C)727mW

SO (derate 5.88mW/°C above +70°C)471mW

Operating Temperature Ranges

MAX47_C_A0°C to +70°C

MAX47_E_A-40°C to +85°C

Junction Temperature Range-60°C to +150°C

Storage Temperature Range-60°C to +160°C

Lead Temperature (soldering, 10sec)+300°C

Note 1: Due to special packaging considerations, MAX471 (DIP, SO) has a higher power dissipation rating than the MAX472. RS+ and RS- must be soldered to large copper traces to achieve this dissipation rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX471

(RS+ = +3V to +36V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V _{RS+}			3		36	V
Supply Current	I _{RS+}	I _{LOAD} = 0A, excludes I _{SIGN}			50	100	μA
Sense Current	I _{LOAD}					±3	ARMS
Sense Resistor	R _{SENSE}				35	70	mΩ
Current-Sense Ratio	I _{OUT} /I _{LOAD}	I _{LOAD} = 1A, RS+ = 10V	MAX471C	0.490	0.500	0.510	mA/A
			MAX471E	0.4875	0.500	0.5125	
No-Load OUT Error		I _{LOAD} = 0A, RS+ = 10V	MAX471C		2.5		μA
			MAX471E		3.0		
Low-Level OUT Error		I _{LOAD} = 30mA, RS+ = 10V	MAX471C		±2.5		μA
			MAX471E		±3.0		
Power-Supply Rejection Ratio	PSRR	3V ≤ RS+ ≤ 36V, I _{LOAD} = 1A				0.1	%/V
SIGN Threshold (I _{LOAD} required to switch SIGN)		MAX471C			±4.0	±6.0	mA
		MAX471E				±7.0	
SIGN Output Leakage Current		V _{SIGN} = 36V				1.0	μA
SIGN Sink Current	I _{OL}	V _{SIGN} = 0.3V		0.1			mA
Shutdown Supply Current	I _{RS+(SHDN)}	V _{SHDN} = 2.4V			1.5	5.0	μA
SHDN Input Low Voltage	V _{IL}					0.3	V
SHDN Input Low Current	I _{IL}	V _{SHDN} = 0V				1.0	μA
SHDN Input High Voltage	V _{IH}			2.4			V
SHDN Input High Current	I _{IH}	V _{SHDN} = 2.4V				1.0	μA
OUT Output Voltage Range	V _{OUT}			0	V _{RS+} - 1.5		V
OUT Output Resistance	R _{OUT}	I _{LOAD} = 3.0A, V _{OUT} = 0V to (V _{RS+} - 1.5V)		1	3		MΩ
OUT Rise, Fall Time	t _r , t _f	I _{LOAD} = 50mA to 3.0A, R _{OUT} = 2kΩ, C _{OUT} = 50pF, 10% to 90%			4		μs
OUT Settling Time to 1% of Final Value	t _s	I _{LOAD} = 100mA to 3.0A, R _{OUT} = 2kΩ, C _{OUT} = 50pF			15		μs

Precision, High-Side Current-Sense Amplifiers

MAX471/MAX472

3

ELECTRICAL CHARACTERISTICS—MAX472

($V_{CC} = +3V$ to $+36V$, $R_{G1} = R_{G2} = 200\Omega$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}			3		36	V
Supply Current	I_{CC}	$I_{LOAD} = 0A$, excludes I_{SIGN}			20	35	μA
Input Offset Voltage (Note 2)	V_{OS}	MAX472C				120	μV
		MAX472E				140	
Input Bias Current	I_{RG1}, I_{RG2}				20	35	μA
Input Bias-Current Matching	I_{OS}	$I_{RG1} - I_{RG2}$			± 0.4	± 3.0	μA
OUT Current Accuracy	I_{RG}/I_{OUT}	$V_{SENSE} = 100mV$, $V_{CC} = 10V$ (Note 3)	MAX472C			± 2	%
			MAX472E			± 2.5	
No-Load OUT Error		$V_{CC} = 10V$, $V_{SENSE} = 0V$	MAX472C			2.5	μA
			MAX472E			3	
Low-Level OUT Error		$V_{CC} = 10V$, $V_{SENSE} = 1mV$	MAX472C			± 2.5	μA
			MAX472E			± 3.0	
Power-Supply Rejection Ratio	PSRR	$3V \leq V_{CC} \leq 36V$, $V_{SENSE} = 100mV$				0.1	%/V
SIGN Threshold (V_{SENSE} required to switch SIGN)		$V_{CC} = 10V$	MAX472C		60	120	μV
			MAX472E		60	140	
SIGN Output Leakage Current		$V_{SIGN} = 36V$				1.0	μA
SIGN Output Sink Current		$V_{SIGN} = 0.3V$		0.1			mA
Shutdown Supply Current	$I_{CC}(SHDN)$	$V_{SHDN} = 2.4V$			1.5	5.0	μA
SHDN Input Low Voltage	V_{IL}					0.3	V
SHDN Input Low Current	I_{IL}	$V_{SHDN} = 0V$				1.0	μA
SHDN Input High Voltage	V_{IH}			2.4			V
SHDN Input High Current	I_{IH}	$V_{SHDN} = 2.4V$				1.0	μA
OUT Output Voltage Range	V_{OUT}			0	$V_{CC} - 1.5$		V
OUT Output Resistance	R_{OUT}	$I_{OUT} = 1.5mA$		1	3		$M\Omega$
OUT Rise, Fall Time	t_R, t_F	$V_{SENSE} = 5mV$ to $150mV$, $R_{OUT} = 2k\Omega$, $C_{OUT} = 50pF$, 10% to 90%			4		μs
OUT Settling Time to 1% of Final Value	t_s	$V_{SENSE} = 5mV$ to $150mV$, $R_{OUT} = 2k\Omega$, $C_{OUT} = 50pF$			15		μs
Maximum Output Current	I_{OUT}			1.5			mA

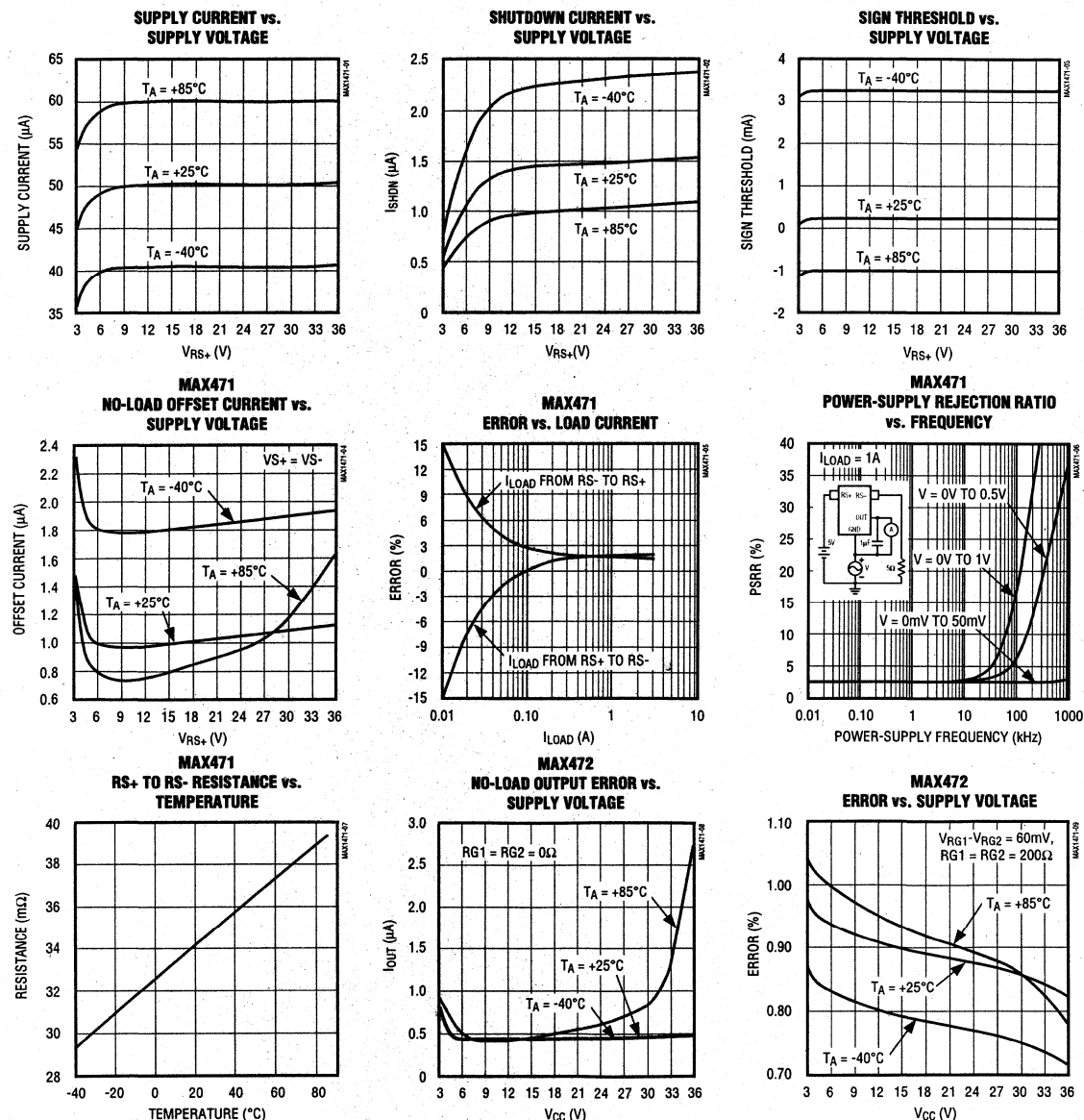
Note 2: V_{OS} is defined as the input voltage (V_{SENSE}) required to give minimum I_{OUT} .

Note 3: V_{SENSE} is the voltage across the sense resistor.

Precision, High-Side Current-Sense Amplifiers

Typical Operating Characteristics

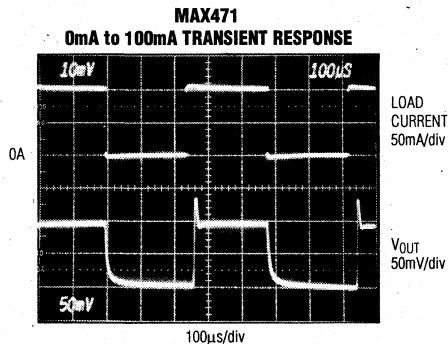
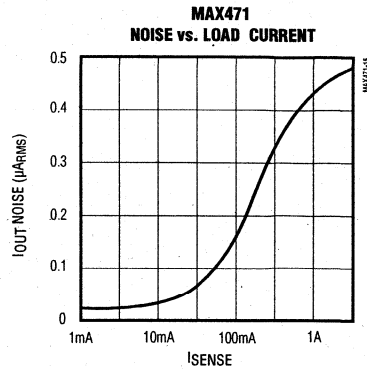
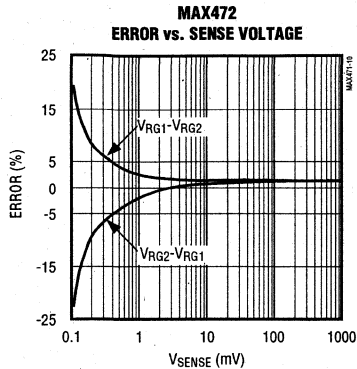
(Typical Operating Circuit (MAX471) or circuit of Figure 4, $R_{G1} = R_{G2} = 200\Omega$, $R_{OUT} = 2k\Omega$ (MAX472), $T_A = +25^\circ\text{C}$, unless otherwise noted.)



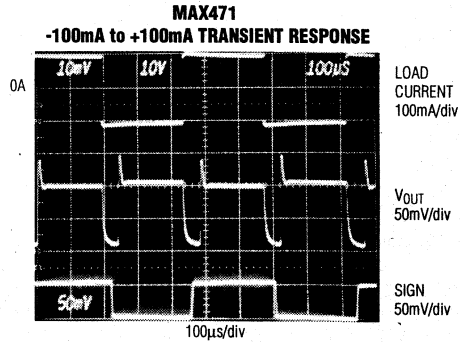
Precision, High-Side Current-Sense Amplifiers

Typical Operating Characteristics (continued)

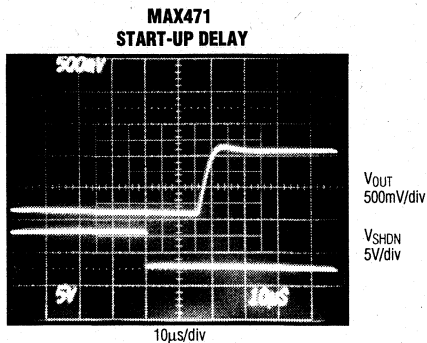
(Typical Operating Circuit (MAX471) or circuit of Figure 4, $R_{G1} = R_{G2} = 200\Omega$, $R_{OUT} = 2k\Omega$ (MAX472), $T_A = +25^\circ\text{C}$, unless otherwise noted.)



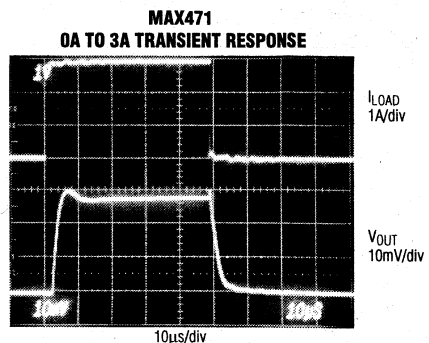
$V_{CC} = 10\text{V}$, $R_{OUT} = 2k\Omega$ 1%, SIGN PULL-UP = $50k\Omega$ 1%



$V_{CC} = 10\text{V}$, $R_{OUT} = 2k\Omega$ 1%, SIGN PULL-UP = $50k\Omega$ 1%



$I_{LOAD} = 1\text{A}$, $R_{OUT} = 2k\Omega$ 1%



$R_{OUT} = 2k\Omega$ 1%

MAX471/MAX472

3

Precision, High-Side Current-Sense Amplifiers

Pin Description

PIN		NAME	FUNCTION
MAX471	MAX472		
1	1	SHDN	Shutdown. Connect to ground for normal operation. When high, supply current is less than 5µA.
2, 3	—	RS+	Battery (or power) side of the internal current-sense resistor. The "+" indicates direction of flow for SIGN output only. Connect pins 2 and 3 together at the package.
—	2	N.C.	No Connect—no internal connection
—	3	RG1	Gain Resistor. Connect to battery side of current-sense resistor through the gain resistor.
4	4	GND	Ground or Battery Negative Terminal
5	5	SIGN	An open-collector logic output. For the MAX471, a low level indicates current is flowing from RS- to RS+. For the MAX472, a low level indicates a negative VSENSE (see Figure 2). SIGN is high impedance when SHDN is high. Leave open if SIGN is not needed.
6, 7	—	RS-	Load side of the internal current-sense resistor. The "-" indicates direction of flow for SIGN output only. Connect pins 6 and 7 together at the package.
—	6	RG2	Gain Resistor. Connect to load side of current-sense resistor through the gain resistor.
—	7	VCC	Power input for MAX472. Connect to sense resistor (RSENSE) junction with RG1.
8	8	OUT	Current output that is proportional to the magnitude of the sensed current flowing through RSENSE. A 2kΩ resistor from this pin to ground will result in a voltage equal to 1V/Amp of sensed current in the MAX471.

Detailed Description

The MAX471 and MAX472 current-sense amplifier's unique topology allows a simple design to accurately monitor current flow. The MAX471/MAX472 contain two amplifiers operating as shown in Figures 1 and 2. The battery/load current flows from RS+ to RS- (or vice versa) through RSENSE. Current flows through either RG1 and Q1 or RG2 and Q2, depending on the sense-resistor current direction. Internal circuitry, not shown in Figures 1 and 2, prevents Q1 and Q2 from turning on at the same time. The MAX472 is identical to the MAX471, except that RSENSE and gain-setting resistors RG1 and RG2 are external (Figure 2).

To analyze the circuit of Figure 1, assume that current flows from RS+ to RS- and that OUT is connected to GND through a resistor. In this case, amplifier A1 is active and output current I_{OUT} flows from the emitter of Q1. Since no current flows through RG2 (Q2 is off), the negative input of A1 is equal to V_{SOURCE} - (I_{LOAD} × RSENSE). The open-loop gain of A1 forces its positive input to essentially the same level as the negative input. Therefore, the drop across RG1 equals I_{LOAD} × RSENSE. Then, since I_{OUT} flows through Q1 and RG (ignoring the extremely low base currents), I_{OUT} × RG1 = I_{LOAD} × RSENSE, or:

$$I_{OUT} = (I_{LOAD} \times R_{SENSE}) / RG1$$

Current Output

The output voltage equation for the MAX471/MAX472 is given below. In the MAX471, the current-gain ratio has been preset to 500µA/A so that an output resistor (R_{OUT}) of 2kΩ yields 1V/A for a full-scale value of +3V at ±3A. Other full-scale voltages can be set with different R_{OUT} values, but the output voltage can be no greater than V_{RS+} - 1.5V for the MAX471 or V_{RG-} - 1.5V for the MAX472.

$$V_{OUT} = (R_{SENSE} \times R_{OUT} \times I_{LOAD}) / RG$$

where V_{OUT} = the desired full-scale output voltage, I_{LOAD} = the full-scale current being sensed, RSENSE = the current-sense resistor, R_{OUT} = the voltage-setting resistor, and RG = the gain-setting resistor (RG = RG1 = RG2).

The above equation can be modified to determine the R_{OUT} required for a particular full-scale range:

$$R_{OUT} = (V_{OUT} \times RG) / (I_{LOAD} \times R_{SENSE})$$

For the MAX471, this reduces to:

$$R_{OUT} = V_{OUT} / (I_{LOAD} \times 500\mu A/A)$$

OUT is a high-impedance current-source output that can be connected to other MAX471/MAX472 OUT pins

Precision, High-Side Current-Sense Amplifiers

MAX471/MAX472

3

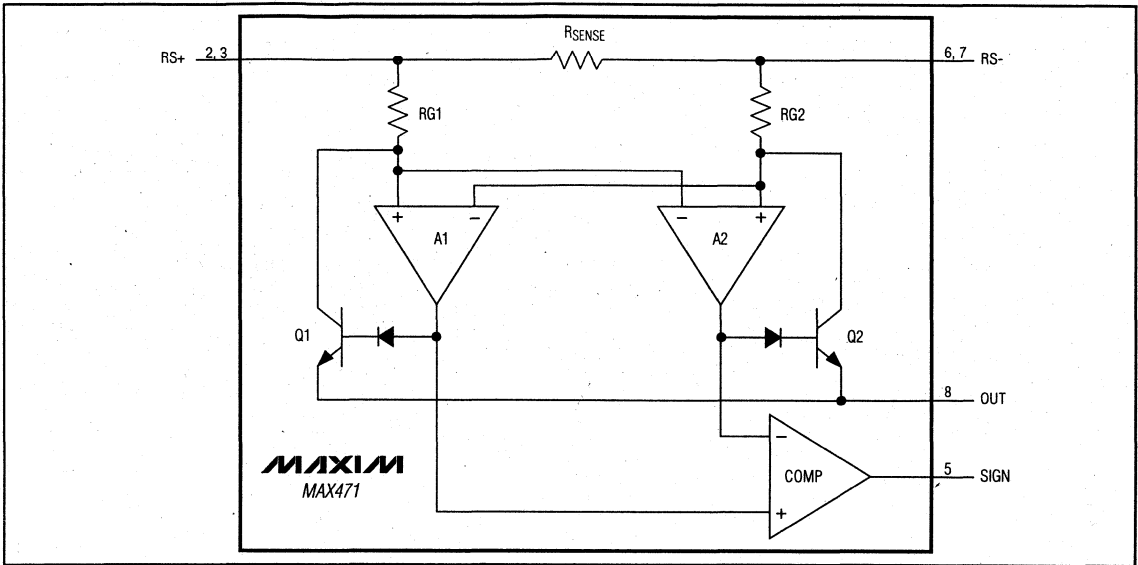


Figure 1. MAX471 Functional Diagram

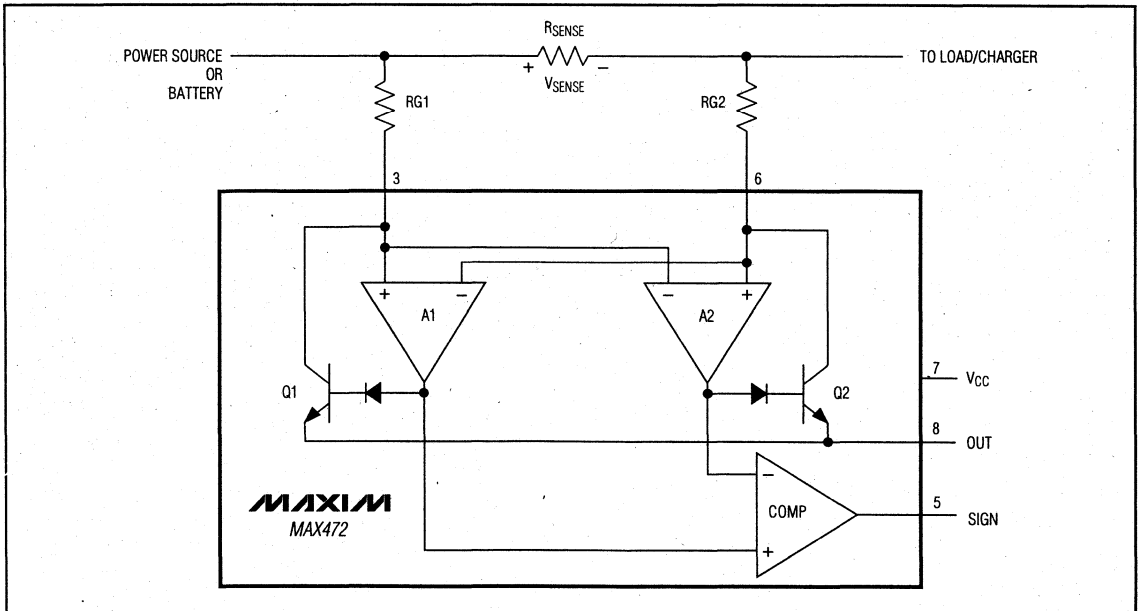


Figure 2. MAX472 Functional Diagram

Precision, High-Side Current-Sense Amplifiers

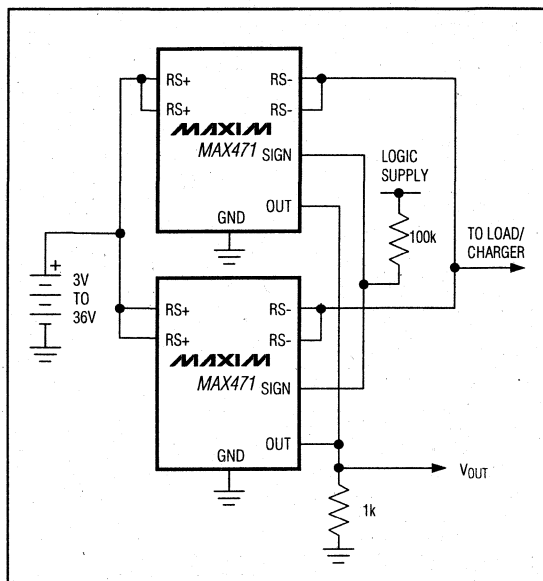


Figure 3. Paralleling MAX471s to Sense Higher Load Current

for current summing. A single scaling resistor is required when summing OUT currents from multiple devices (Figure 3). Current can be integrated by connecting OUT to a capacitive load.

SIGN Output

The current at OUT indicates magnitude. The SIGN output indicates the current's direction. Operation of the SIGN comparator is straightforward. When Q1 (Figures 1 and 2) conducts, the output of A1 is high while A2's output is zero. Under this condition, a high SIGN output indicates positive current flow (from RS+ to RS-). In battery-operated systems, this is useful for determining whether the battery is charging or discharging. The SIGN output may not correctly indicate if the load current is such that IOUT is less than 3.5µA. The MAX471's SIGN output accurately indicates the direction of current flow for load currents greater than 7mA.

SIGN is an open-collector output (sinks current only), allowing easy interface with logic circuits powered from any voltage. Connect a 100kΩ pull-up resistor from SIGN to the logic supply. The convention chosen for the polarity of the SIGN output ensures that it draws no current when the battery is being discharged. If current direction is not needed, float the SIGN pin.

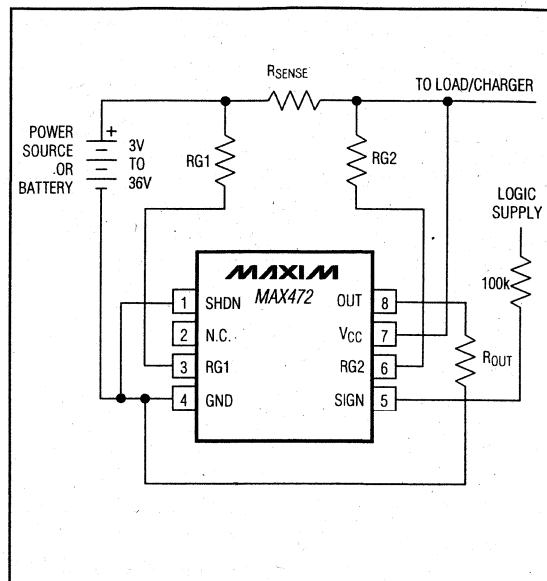


Figure 4. MAX472 Standard Application Circuit

Shutdown

When SHDN is high, the MAX471/MAX472 are shut down and consume less than 5µA. In shutdown mode, SIGN is high impedance and OUT turns off.

Applications Information

MAX471

The MAX471 obtains its power from the RS- pin. This includes MAX471 current consumption in the total system current measured by the MAX471. The small drop across RSENSE does not affect the MAX471's performance.

Resistor Selection

Since OUT delivers a current, an external voltage gain-setting resistor (ROUT to ground) is required at the OUT pin in order to get a voltage. RSENSE is internal to the MAX471. RG1 and RG2 are factory trimmed for an output current ratio (output current to load current) of 500µA/A. Since they are manufactured of the same material and in very close proximity on the chip, they provide a high degree of temperature stability. Choose ROUT for the desired full-scale output voltage up to RS- - 1.5V (see the *Current Output* section).

Precision, High-Side Current-Sense Amplifiers

Peak Sense Current

The MAX471's maximum sense current is $3I_{ARMS}$. For power-up, fault conditions, or other infrequent events, larger peak currents are allowed, provided they are short—that is, within a safe operating region, as shown in Figure 5.

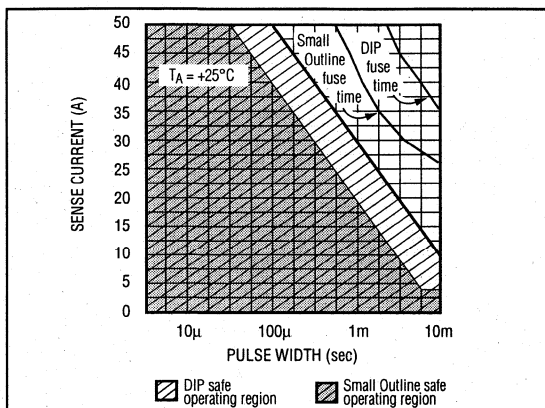


Figure 5. MAX471 Pulse Current Safe Operation for 10,000 Pulses and Fuse Time for Continuous Current. Pulse tests done with 250mW average power dissipation.

MAX472

R_{SENSE} , $RG1$, and $RG2$ are externally connected on the MAX472. V_{CC} can be connected to either the load/charge or power-source/battery side of the sense resistor. Connect V_{CC} to the load/charge side of R_{SENSE} if you want to include the MAX472 current drain in the measured current.

Suggested Component Values for Various Applications

The general circuit of Figure 4 is useful in a wide variety of applications. It can be used for high-current applications (greater than 3A), and also for those where the full-scale load current is less than the 3A of the MAX471.

Table 1. Suggested Component Values for the MAX472

FULL-SCALE LOAD CURRENT, I_{SENSE} (A)	CURRENT-SENSE RESISTOR, R_{SENSE} (m Ω)	GAIN-SETTING RESISTORS, $RG1 = RG2$ (Ω)	OUTPUT RESISTOR, R_{OUT} (k Ω)	FULL-SCALE OUTPUT VOLTAGE, V_{OUT} (V)	SCALE FACTOR, V_{OUT}/I_{SENSE} (V/A)	TYPICAL ERROR AT X% OF FULL LOAD (%)		
						1%	10%	100%
0.1	500	200	10	2.5	25	14	2.5	0.9
1	50	200	10	2.5	2.5	14	2.5	0.9
5	10	100	5	2.5	0.5	13	2.0	1.1
10	5	50	2	2	0.2	12	2.0	1.6

Table 1 shows suggested component values and indicates the resulting scale factors for various applications required to sense currents from 100mA to 10A.

Higher or lower sense-current circuits can also be built. Select components and calculate circuit errors using the guidelines and formulas in the following section.

R_{SENSE}

Choose R_{SENSE} based on the following criteria:

- Voltage Loss:** A high R_{SENSE} value will cause the power-source voltage to degrade through IR loss. For least voltage loss, use the lowest R_{SENSE} value.
- Accuracy:** A high R_{SENSE} value allows lower currents to be measured more accurately. This is because offsets become less significant when the sense voltage is larger.
- Efficiency and Power Dissipation:** At high current levels, the I^2R losses in R_{SENSE} may be significant. Take this into consideration when choosing the resistor value and power dissipation (wattage) rating. Also, if the sense resistor is allowed to heat up excessively, its value may drift.
- Inductance:** If there is a large high-frequency component to I_{SENSE} , you will want to keep inductance low. Wire-wound resistors have the highest inductance, while metal film is somewhat better. Low-inductance metal-film resistors are available. Instead of being spiral wrapped around a core, as in metal-film or wire-wound resistors, these are a straight band of metal. They are made in values under 1Ω .
- Cost:** If the cost of R_{SENSE} becomes an issue, you may want to use an alternative solution, as shown in Figure 6. This solution uses the PC board traces to create a sense resistor. Because of the inaccuracies of the copper "resistor," you will need to adjust the full-scale current value with a potentiometer. Also, the resistance temperature coefficient of copper is fairly high (approximately $0.4\%/^{\circ}\text{C}$), so systems that experience a wide temperature variance should take this into account.

Precision, High-Side Current-Sense Amplifiers

In Figure 6, assume the load current to be measured is 10A and that you have determined a 0.3 inch wide, 2 ounce copper to be appropriate. The resistivity of 0.1 inch wide, 2 ounce copper is 30mΩ/ft (see Note 4). For 10A you may want $R_{SENSE} = 5\text{m}\Omega$ for a 50mV drop at full scale. This resistor will require about 2 inches of 0.1 inch wide copper trace.

RG1 and RG2

Once R_{SENSE} is chosen, $RG1$ and $RG2$ can be chosen to define the current-gain ratio (R_{SENSE}/RG). Choose $RG = RG1 = RG2$ based on the following criteria:

- 1Ω Input Resistance.** The minimum RG value is limited by the 1Ω input resistance, and also by the output current limitation (see below). As RG is reduced, the input resistance becomes a larger portion of the total gain-setting resistance. With $RG = 50\Omega$, the input resistance produces a 2% difference between the expected and actual current-gain ratio. This is a gain error that does not affect linearity and can be removed by adjusting RG or R_{OUT} .
- Efficiency.** As RG is reduced, I_{OUT} gets larger for a given load current. Power dissipated in R_{OUT} is not going to the load, and therefore reduces overall efficiency. This is significant only when the sense current is small.
- Maximum Output Current Limitation.** I_{OUT} is limited to 1.5mA, requiring $RG \geq V_{SENSE} / 1.5\text{mA}$. For $V_{SENSE} = 60\text{mV}$, RG must be $\geq 40\Omega$.
- Headroom.** The MAX472 requires a minimum of 1.5V between the lower of the voltage at $RG1$ or $RG2$ ($V_{RG_}$) and V_{OUT} . As RG becomes larger, the voltage drop across RG also becomes larger for a given I_{OUT} . This voltage drop further limits the maximum full-scale V_{OUT} . Assuming the drop across R_{SENSE} is small and V_{CC} is connected to either side of R_{SENSE} , $V_{OUT}(\text{max}) = V_{CC} - (1.5\text{V} + I_{OUT}(\text{max}) \times RG)$.
- Output Offset Error at Low Load Currents.** Large RG values reduce I_{OUT} for a given load current. As I_{OUT} gets smaller, the 2.5μA max output offset-error current becomes a larger part of the overall output current. Keeping the gain high by choosing a low value for RG minimizes this offset error.
- Input Bias Current and Input Bias Current Mismatching.** The size of RG also affects the errors introduced by the input bias and input bias mismatching currents. After selecting the ratio, check to

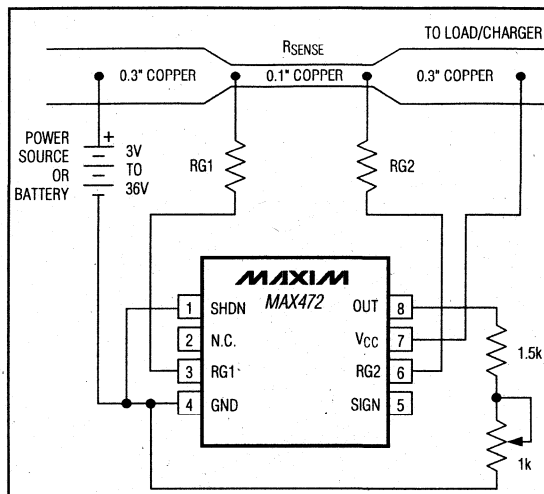


Figure 6. MAX472 Connections Showing Use of PC Board Trace

make sure RG is small enough that I_B and I_{OS} do not add any appreciable errors. The full-scale error is given by:

$$\% \text{ Error} = \frac{(RG1 - RG2) \times I_B + I_{OS} \times RG}{I_{FS} \times R_{SENSE}} \times 100$$

where $RG1$ and $RG2$ are the gain resistors, I_B is the bias current, I_{OS} is the bias-current mismatch, I_{FS} is the full-scale current, and R_{SENSE} is the sense resistor.

Assuming a 5A load current, 10mΩ R_{SENSE} , and 100Ω RG , the current-gain ratio is 100μA/A, yielding a full-scale I_{OUT} of 500μA. Using the maximum values for I_B (20μA) and I_{OS} (2μA), and 1% resistors for $RG1$ and $RG2$ ($RG1 - RG2 = 2\Omega$), the worst-case error at full scale calculates to:

$$\frac{2\Omega \times 20\mu\text{A} + 100\Omega \times 2\mu\text{A}}{5\text{m}\Omega \times 5\text{A}} = 0.48\%$$

The error may be reduced by: a) better matching of $RG1$ and $RG2$, b) increasing R_{SENSE} , or c) decreasing RG .

Current-Sense Adjustment (Resistor Range, Output Adjust)

Choose R_{OUT} after selecting R_{SENSE} , $RG1$, and $RG2$. Choose R_{OUT} to obtain the full-scale voltage you

Precision, High-Side Current-Sense Amplifiers

require, given the full-scale I_{OUT} determined by R_{SENSE} , R_{G1} , and R_{G2} . The high compliance of I_{OUT} permits using R_{OUT} values up to $10k\Omega$ with minimal error. Values above $10k\Omega$ are not usually recommended. The impedance of I_{OUT} 's load (e.g., the input of an op amp or ADC) must be much greater than R_{OUT} (e.g., $100 \times R_{OUT}$) to avoid degrading the measurement accuracy.

High-Current Measurement

The MAX472 can achieve higher current measurements than the MAX471 can. Low-value sense resistors may be paralleled to obtain even lower values, or the PC board trace may be adjusted for any value.

An alternative method is to connect several MAX471s in parallel and connect the high-impedance current-source I_{OUT} pins together to indicate the total system current (Figure 3). Pay attention to layout to ensure equal I_R drops in the paralleled connection. This is necessary to achieve equal current sharing.

Power-Supply Bypassing and Grounding

The MAX471 has been designed as a "high side" (positive terminal) current monitor to ease the task of grounding any battery charger, thermistor, etc. that may be a part of the battery pack. Grounding the MAX471 requires no special precautions; follow the same cautionary steps that apply to the system as a whole. High-current systems can experience large voltage drops across a ground plane, and this drop may add to or subtract from V_{OUT} . For highest current-measurement accuracy, use a single-point "star" ground.

The MAX471/MAX472 require no special bypassing, and respond quickly to transient changes in line current. If the noise at I_{OUT} caused by these transients is a problem, you may want to place a $1\mu F$ capacitor at the I_{OUT} pin to ground. You can also place a large capacitor at the $RS-$ terminal (or "load" side of the MAX472) to decouple the load and, thereby, reduce the current transients. These capacitors are not required for MAX471/MAX472 operation or stability, and their use will not degrade performance.

For the MAX472, the R_{G1} and R_{G2} inputs can be filtered by placing a capacitor (e.g., $1\mu F$) between them to average the sensed current.

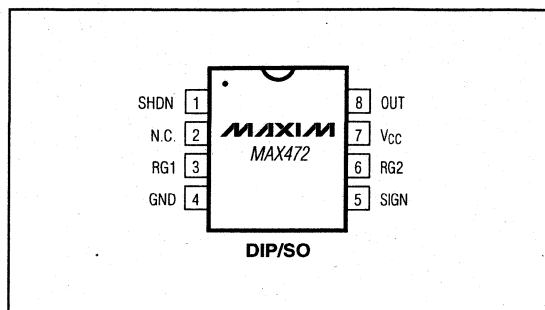
MAX471 Layout

The MAX471 must be soldered in place, since sockets can cause uneven current sharing between the $RS+$ pins (pins 2 and 3) and the $RS-$ pins (pins 6 and 7), resulting in typical errors of 0.5%.

In order to dissipate sense-resistor heat from large sense currents, solder the $RS+$ pins and the $RS-$ pins to large copper traces. Keep the part away from other heat-generating devices. This procedure will ensure continuous power dissipation rating.

Precision, High-Side Current-Sense Amplifiers

Pin Configurations (continued)



MAXIM

Single/Dual/Quad, 10MHz Single-Supply Op Amps

MAX473/MAX474/MAX475

General Description

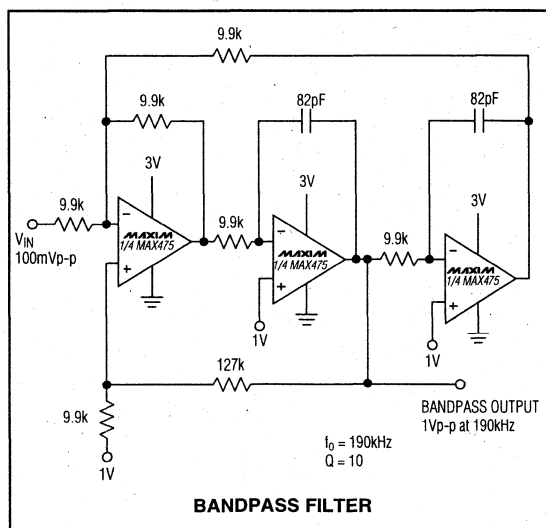
The single MAX473, dual MAX474, and quad MAX475 are single-supply (2.7V to 5.25V), unity-gain-stable op amps with rail-to-rail output swing. Each op amp guarantees a 10MHz unity-gain bandwidth, 15V/ μ s slew rate, and 600 Ω drive capability while typically consuming only 2mA supply current. In addition, the input range includes the negative supply rail and the output swings to within 50mV of each supply rail.

Single-supply operation makes these devices ideal for low-power and low-voltage portable applications. With their fast slew rate and settling time, they can replace higher-current op amps in large-signal applications. The MAX473/MAX474/MAX475 are available in DIP and SO packages in the industry-standard op-amp pin configurations. The MAX473 and MAX474 are also offered in the μ MAX package, the smallest 8-pin SO.

Applications

Portable Equipment
Battery-Powered Instruments
Signal Processing
Discrete Filters
Signal Conditioning
Servo-Loops

Typical Operating Circuit



Features

- ◆ 15V/ μ s Min Slew Rate
- ◆ +3V Single-Supply Operation
- ◆ Guaranteed 10MHz Unity-Gain Bandwidth
- ◆ 2mA Supply Current per Amplifier
- ◆ Input Range Includes Negative Rail
- ◆ Outputs Short-Circuit Protected
- ◆ Rail-to-Rail Output Swing (to within $\pm 50\text{mV}$)
- ◆ μ MAX Package (the smallest 8-pin SO)

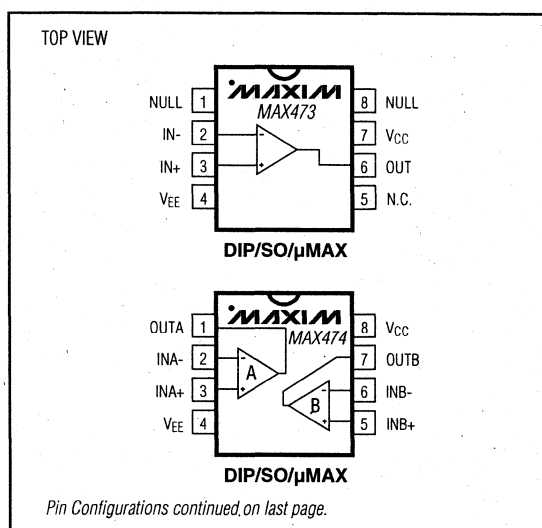
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX473CPA	0°C to +70°C	8 Plastic DIP
MAX473CSA	0°C to +70°C	8 SO
MAX473CUA	0°C to +70°C	8 μ MAX
MAX473C/D	0°C to +70°C	Dice*
MAX473EPA	-40°C to +85°C	8 Plastic DIP
MAX473ESA	-40°C to +85°C	8 SO
MAX473MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Pin Configurations


MAXIM

Maxim Integrated Products 3-19

Call toll free 1-800-998-8800 for free samples or literature.

Single/Dual/Quad, 10MHz Single-Supply Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC} - V_{EE}$).....	7V	14-Pin SO (derate 8.33mW/°C above +70°C).....	667mW
Input Voltage ($IN+$, $IN-$, $IN+$, $IN-$).....	($V_{CC} + 0.3V$) to ($V_{EE} - 0.3V$)	14-Pin Cerdip (derate 9.09mW/°C above +70°C).....	727mW
Output Short-Circuit Duration.....	Continuous	Operating Temperature Ranges	
Continuous Power Dissipation ($T_A = +70^\circ C$)		MAX47_C_ _	0°C to +70°C
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...	727mW	MAX47_E_ _	-40°C to +85°C
8-Pin SO (derate 5.88mW/°C above +70°C).....	471mW	MAX47_MJ	-55°C to +125°C
8-Pin μ MAX (derate 4.1mW/°C above +70°C).....	330mW	Junction Temperatures	
8-Pin Cerdip (derate 8.00mW/°C above +70°C).....	640mW	MAX47_C_ _/E_ _	+150°C
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)...	800mW	MAX47_MJ	+175°C
		Storage Temperature Range	-65°C to +160°C
		Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(+3V $\leq V_{CC} \leq +5V$, $V_{EE} = 0V$, $V_{CM} = 0.5V$, $V_{OUT} = 0.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473		± 0.70	± 2.0	mV
		MAX474		± 0.70	± 2.0	
		MAX475		± 0.80	± 2.5	
Input Bias Current	I_B	Current flows out of terminals	0	80	150	nA
Input Offset Current	I_{OS}			± 10	± 30	nA
Common-Mode Voltage	V_{CM}	High	$V_{CC} - 1.9$	$V_{CC} - 1.7$		V
		Low		$V_{EE} - 0.1$	V_{EE}	
Common-Mode Rejection Ratio	CMRR	$V_{EE} \leq V_{CM} \leq (V_{CC} - 1.9V)$	80	90		dB
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 2.7V$ to $6.0V$	80	90		dB
Input Noise-Voltage Density	e_n	$f = 10kHz$		40		nV/ $\sqrt{Hz}$
Large-Signal Gain (Note 1)	A_{VOL}	$0.3V \leq V_{OUT} \leq (V_{CC} - 0.5V)$	$R_L = \text{no load}$	110		dB
			$R_L = 10k\Omega$	94	105	
			$R_L = 600\Omega$	82	90	
		Sinking 5mA	$V_{CC} = 5V$	76		
			$V_{CC} = 3V$	100		
		Sourcing 5mA	$V_{CC} = 5V$	76		
			$V_{CC} = 3V$	90		
Output Voltage	V_{OH}	$V_{IN+} - V_{IN-} = +1V$, $R_L = \text{no load}$	$V_{CC} - 0.05$			V
	V_{OL}	$V_{IN+} - V_{IN-} = -1V$, $R_L = \text{no load}$			$V_{EE} + 0.05$	
Slew Rate	SR	$V_{CC} = 5V$, $R_L = 10k\Omega$, $C_L = 20pF$, $V_{IN+} - V_{IN-} = +1V$ step	15	17		V/ μs
Unity-Gain Bandwidth (Note 2)	GBW	$3V \leq V_{CC} \leq 5V$	10	12		MHz
		$V_{CC} = 2.7V$		10		

Single/Dual/Quad, 10MHz Single-Supply Op Amps

MAX473/MAX474/MAX475

ELECTRICAL CHARACTERISTICS (continued)

(+3V ≤ VCC ≤ +5V, VEE = 0V, VCM = 0.5V, VOUT = 0.5V, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Settling Time	ts	To 0.1%, CL = 20pF		400		ns
Power-Up Time	tPU	AV = +1, VIN = 1/2 VCC step, see <i>Typical Operating Characteristics</i>		700		ns
Overshoot		CL = 150pF		10		%
		CL = 20pF		5		
Phase Margin		RL = 10kΩ, VCC = 5V CL = 20pF		63		degrees
		VCC = 3V		58		
Gain Margin		RL = 10kΩ, VCC = 5V CL = 20pF		10		dB
		VCC = 3V		12		
Supply Current	IS	Per amplifier		2.0	3.0	mA
Operating Supply-Voltage Range		Single supply	2.7		5.25	V
		Dual supplies	±1.35		±2.625	

ELECTRICAL CHARACTERISTICS

(+3V ≤ VCC ≤ +5V, VEE = 0V, VCM = 0.5V, VOUT = 0.5V, TA = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	VOS	MAX473			±2.0	mV
		MAX474			±2.0	
		MAX475			±3.0	
Input Bias Current	IB	Current flows out of terminals	0		175	nA
Input Offset Current	IOS				±35	nA
Common-Mode Rejection Ratio	CMRR	VEE ≤ VCM ≤ (VCC - 1.9V)	78			dB
Power-Supply Rejection Ratio	PSRR	VCC = 2.7V to 6.0V	78			dB
Large-Signal Gain (Note 1)	AVOL	0.4V ≤ VOUT ≤ (VCC - 0.6V) RL = 10kΩ	94			dB
		RL = 600Ω	80			
Output Voltage	VOH	VIN+ - VIN- = +1V, RL = no load	VCC - 0.07			V
	VOL	VIN+ - VIN- = -1V, RL = no load		VEE + 0.07		
Slew Rate	SR	VCC = 5V, RL = 10kΩ, CL = 20pF, VIN+ - VIN- = +1V step	12			V/μs
Supply Current	IS	Per amplifier			3.3	mA
Operating Supply-Voltage Range		Single supply	2.7		5.25	V
		Dual supplies	±1.35		±2.625	

Single/Dual/Quad, 10MHz Single-Supply Op Amps

ELECTRICAL CHARACTERISTICS

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V _{OS}	MAX473			±2.3	mV
		MAX474			±2.3	
		MAX475			±3.3	
Input Bias Current	I _B	Current flows out of terminals	0		200	nA
Input Offset Current	I _{OS}				±50	nA
Common-Mode Rejection Ratio	CMRR	V _{EE} ≤ V _{CM} ≤ (V _{CC} - 2.0V)	72			dB
Power-Supply Rejection Ratio	PSRR	V _{CC} = 2.7V to 6.0V	72			dB
Large-Signal Gain (Note 1)	A _{VOL}	0.4V ≤ V _{OUT} ≤ (V _{CC} - 0.6V)		R _L = 10kΩ	94	dB
				R _L = 600Ω	72	
Output Voltage	V _{OH}	V _{IN+} - V _{IN-} = +1V, R _L = no load	V _{CC} - 0.08			V
	V _{OL}	V _{IN+} - V _{IN-} = -1V, R _L = no load		V _{EE} + 0.08		
Slew Rate	SR	V _{CC} = 5V, R _L = 10kΩ, C _L = 20pF, V _{IN+} - V _{IN-} = +1V step	10			V/μs
Supply Current	I _S	Per amplifier			3.4	mA
Operating Supply-Voltage Range		Single supply	2.7		5.25	V
		Dual supplies	±1.35		±2.625	

ELECTRICAL CHARACTERISTICS

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V _{OS}	MAX473			±2.8	mV
		MAX474			±2.8	
		MAX475			±4.0	
Input Bias Current	I _B	Current flows out of terminals	0		225	nA
Input Offset Current	I _{OS}				±60	nA
Common-Mode Rejection Ratio	CMRR	V _{EE} ≤ V _{CM} ≤ (V _{CC} - 2.15V)	70			dB
Power-Supply Rejection Ratio	PSRR	V _{CC} = 2.7V to 6.0V	70			dB
Large-Signal Gain (Note 1)	A _{VOL}	0.5V ≤ V _{OUT} ≤ (V _{CC} - 0.6V)		R _L = 10kΩ	90	dB
				R _L = 600Ω	70	
Output Voltage	V _{OH}	V _{IN+} - V _{IN-} = +1V, R _L = no load	V _{CC} - 0.1			V
	V _{OL}	V _{IN+} - V _{IN-} = -1V, R _L = no load		V _{EE} + 0.1		
Slew Rate	SR	V _{CC} = 5V, R _L = 10kΩ, C _L = 20pF, V _{IN+} - V _{IN-} = +1V step	9			V/μs
Supply Current	I _S	Per amplifier			3.6	mA
Operating Supply-Voltage Range		Single supply	2.7		5.25	V
		Dual supplies	±1.35		±2.625	

Note 1: Gain decreases to zero as the output swings beyond the specified limits.

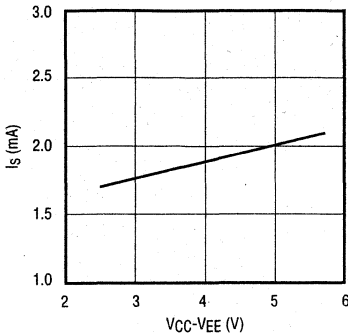
Note 2: Guaranteed by correlation to slew rate.

Single/Dual/Quad, 10MHz Single-Supply Op Amps

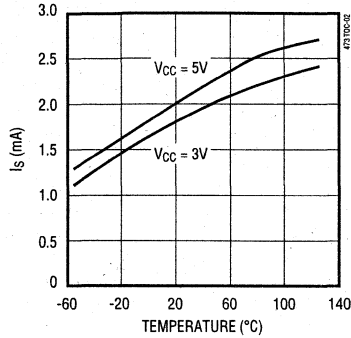
Typical Operating Characteristics

($V_{CC} = 5V$, $V_{EE} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

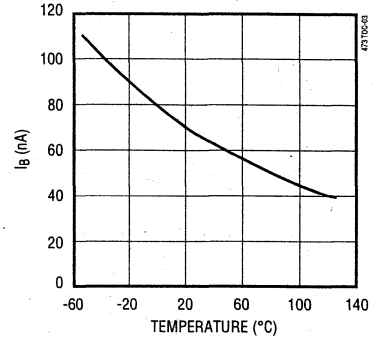
**SUPPLY CURRENT PER AMPLIFIER
vs. SUPPLY VOLTAGE**



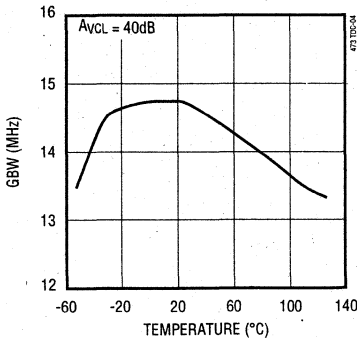
SUPPLY CURRENT vs. TEMPERATURE



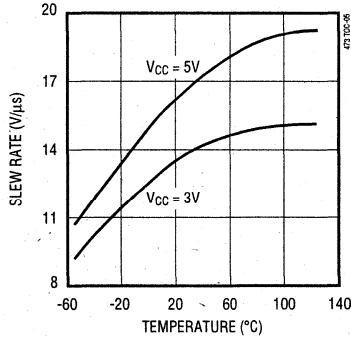
**INPUT BIAS CURRENT
vs. TEMPERATURE**



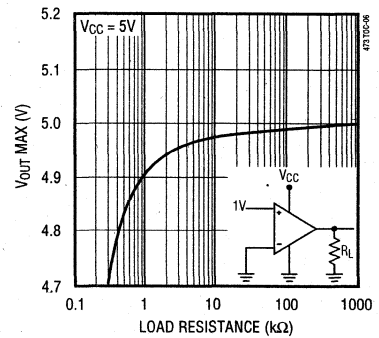
**GAIN-BANDWIDTH PRODUCT
vs. TEMPERATURE**



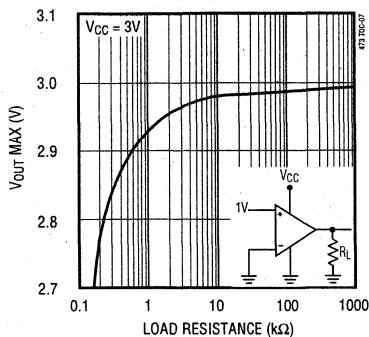
SLEW RATE vs. TEMPERATURE



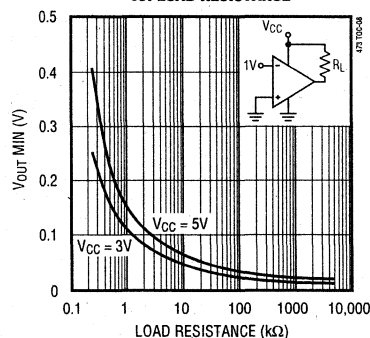
**MAXIMUM OUTPUT VOLTAGE
vs. LOAD RESISTANCE**



**MAXIMUM OUTPUT VOLTAGE
vs. LOAD RESISTANCE**



**MINIMUM OUTPUT VOLTAGE
vs. LOAD RESISTANCE**

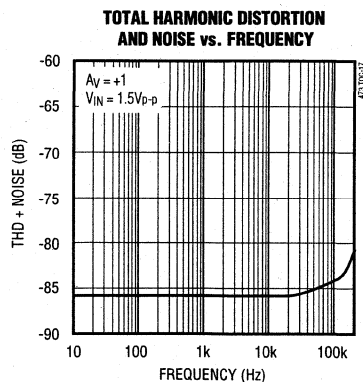
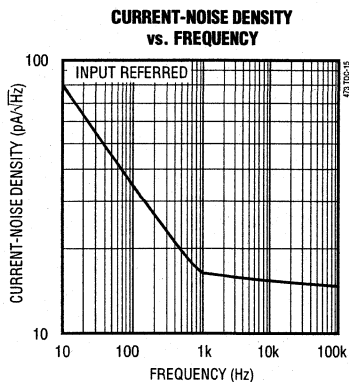
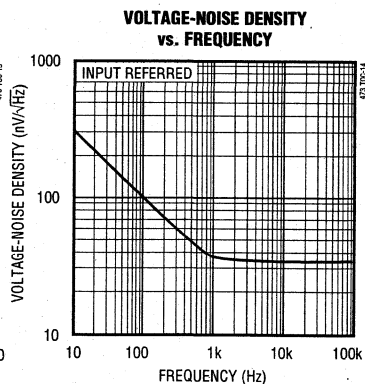
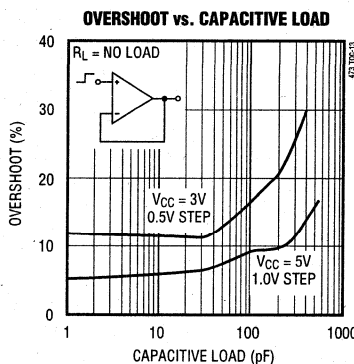
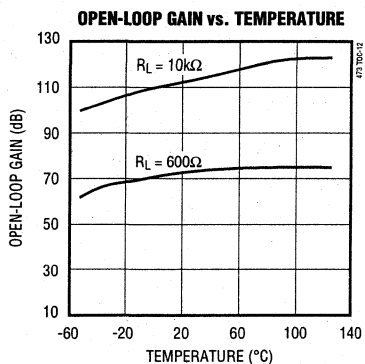
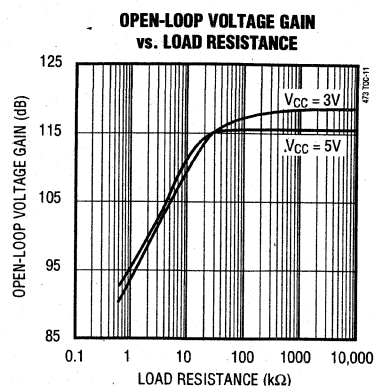
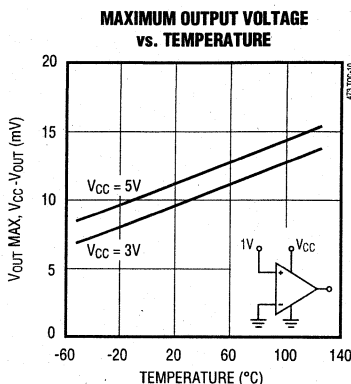
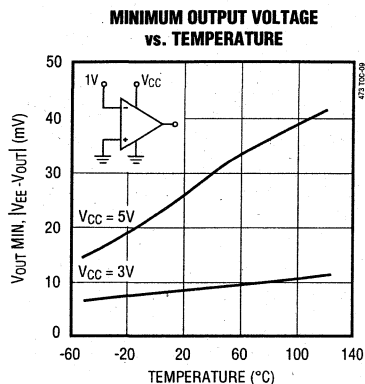


MAX473/MAX474/MAX475

Single/Dual/Quad, 10MHz Single-Supply Op Amps

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

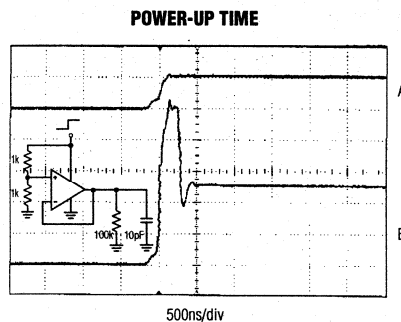
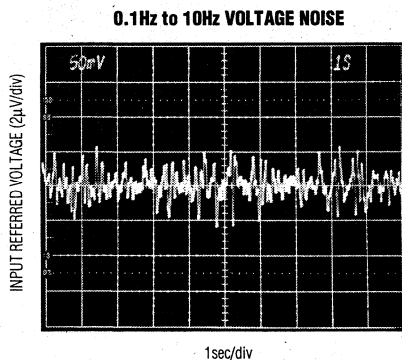
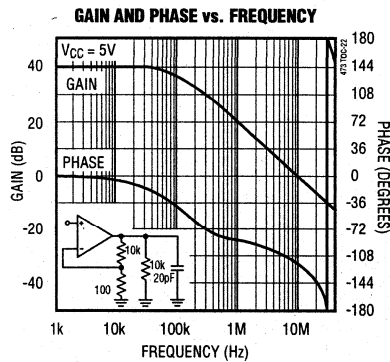
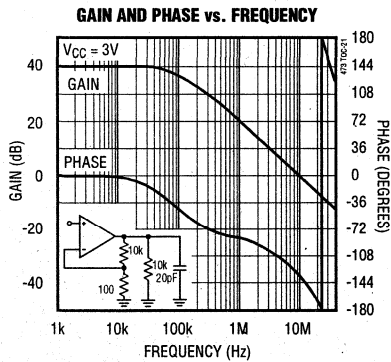
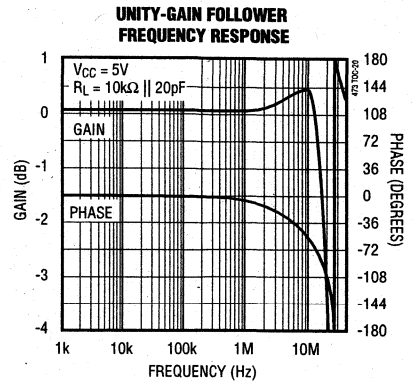
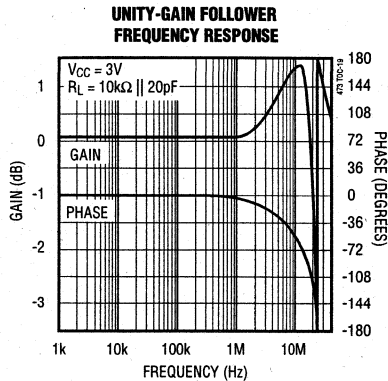
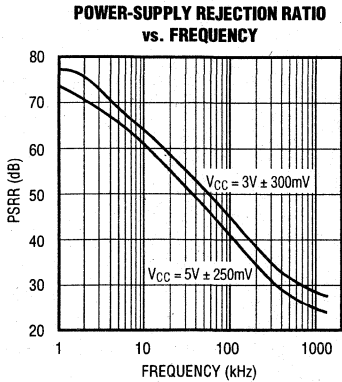


Single/Dual/Quad, 10MHz Single-Supply Op Amps

MAX473/MAX474/MAX475

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



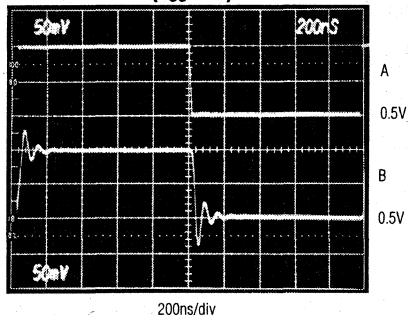
A: V_{CC} , 5V/div
B: V_{OUT} , 1V/div

Single/Dual/Quad, 10MHz Single-Supply Op Amps

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

SMALL-SIGNAL TRANSIENT RESPONSE
($V_{CC} = 5V$)

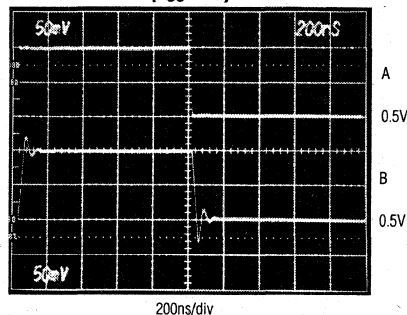


$V_{CC} = 5V$, $A_v = +1$, $R_L = 10k\Omega$, $C_L = 220pF$

A: V_{IN} , 50mV/div

B: V_{OUT} , 50mV/div

SMALL-SIGNAL TRANSIENT RESPONSE
($V_{CC} = 3V$)

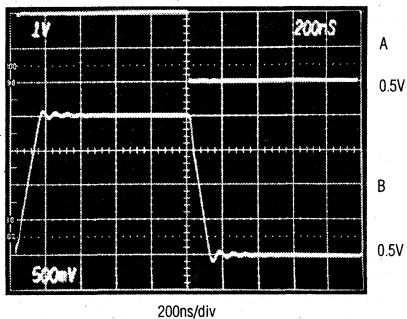


$V_{CC} = 3V$, $A_v = +1$, $R_L = 10k\Omega$, $C_L = 100pF$

A: V_{IN} , 50mV/div

B: V_{OUT} , 50mV/div

LARGE-SIGNAL TRANSIENT RESPONSE

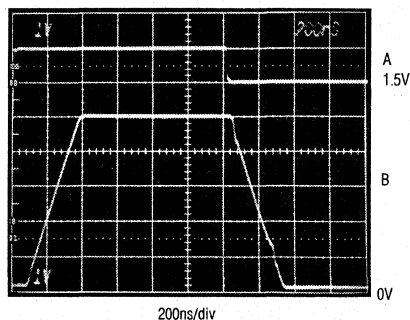


$V_{CC} = 5V$, $A_v = +1$, $R_L = 10k\Omega$, $C_L = 220pF$

A: V_{IN} , 1V/div

B: V_{OUT} , 500mV/div

OVERDRIVING THE OUTPUT



$V_{CC} = 5V$, $V_{IN-} = 2.0V$, $R_L = 10k\Omega$, $C_L = 33pF$

A: V_{IN+} , 1V/div

B: V_{OUT} , 1V/div

Single/Dual/Quad, 10MHz Single-Supply Op Amps

Pin Description

MAX473/MAX474/MAX475

PIN			NAME	FUNCTION
MAX473	MAX474	MAX475		
1, 8	—	—	NULL	Offset Null Input. Connect to one end of 2k Ω potentiometer for offset voltage trimming. Connect wiper to VEE. See Figure 1.
—	1	1	OUTA	Amplifier A Output
2	—	—	IN-	Inverting Input
—	2	2	INA-	Amplifier A Inverting Input
3	—	—	IN+	Noninverting Input
—	3	3	INA+	Amplifier A Noninverting Input
4	4	11	VEE	Negative Power-Supply Pin. Connect to ground or a negative voltage.
5	—	—	N.C.	No Connect—not internally connected
—	5	5	INB+	Amplifier B Noninverting Input
6	—	—	OUT	Amplifier Output
—	6	6	INB-	Amplifier B Inverting Input
—	7	7	OUTB	Amplifier B Output
7	8	4	VCC	Positive Power-Supply Pin. Connect to (+) terminal of power supply.
—	—	8	OUTC	Amplifier C Output
—	—	9	INC-	Amplifier C Inverting Input
—	—	10	INC+	Amplifier C Noninverting Input
—	—	12	IND+	Amplifier D Noninverting Input
—	—	13	IND-	Amplifier D Inverting Input
—	—	14	OUTD	Amplifier D Output

Applications Information

Power Supplies

The MAX473/MAX474/MAX475 operate from a single 2.7V to 5.25V power supply, or from dual supplies of $\pm 1.35V$ to $\pm 2.625V$. For single-supply operation, bypass the power supply with 0.1 μF . If operating from dual supplies, bypass each supply to ground. With 0.1 μF bypass capacitance, channel separation (MAX474/MAX475) is typically better than 120dB with signal frequencies up to 300kHz. Increasing the bypass capacitance (e.g. 10 μF || 0.1 μF) maintains channel separation at higher frequencies.

Minimizing Offsets

The MAX473's maximum offset voltage is $\pm 2mV$ ($T_A = +25^\circ C$). If additional offset adjustment is required, connect a 2k Ω trim potentiometer between pins 1, 8, and 4 (Figure 1). Input offset voltage for the dual MAX474 and quad MAX475 cannot be externally trimmed.

The MAX473/MAX474/MAX475 are bipolar op amps with low input bias currents. The bias currents at both inputs flow out of the device. Matching the resistance at the op amp's inputs significantly reduces the offset error caused by the bias currents. Place a resistor (R3) from the noninverting input to ground when using the inverting configuration (Figure 2a); place R3 in series with the noninverting input when using the noninverting configuration (Figure 2b). Select R3 such that the parallel combination of R2 and R1 equals R3. Adding R3 will slightly increase the op amp's voltage noise.

Output Loading and Stability

The MAX473/MAX474/MAX475 op amps are unity-gain stable. Any op amp's stability depends on the configuration, closed-loop gain, and load capacitance. The unity-gain, noninverting buffer is the most sensitive gain configuration, and driving capacitive loads decreases stability.

Single/Dual/Quad, 10MHz Single-Supply Op Amps

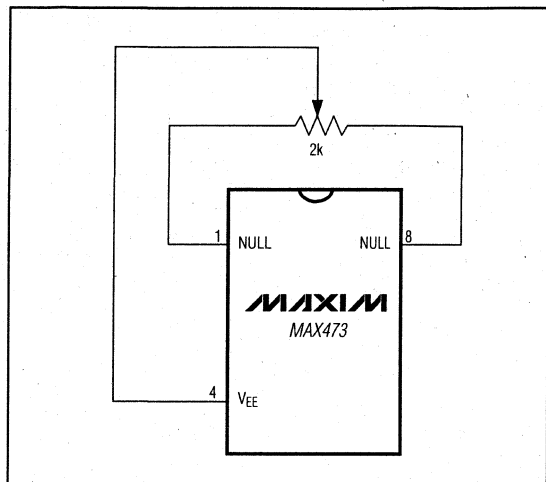


Figure 1. Offset Null Circuit

The MAX473/MAX474/MAX475 have excellent phase margin (the difference between 180° and the unity-gain phase angle). It is typically 63° with a load of 10kΩ in parallel with 20pF. Generally, higher phase margins indicate greater stability.

Capacitive loads form an RC network with the op amp's output resistance, causing additional phase shift that reduces the phase margin. Figure 3 shows the MAX473/MAX474/MAX475 output response when driving a 390pF load in parallel with 10kΩ.

When driving large capacitive loads, add an output isolation resistor, as shown in Figure 4. This resistor improves the phase margin by isolating the load capacitance from the amplifier output. Figure 5 shows the MAX473/MAX474/MAX475 driving a capacitive load of 1000pF using the circuit of Figure 4.

Feedback Resistors

The feedback resistors appear as a resistance network to the op amp's feedback input (Figure 2). This resistance, combined with the op amp's input and stray capacitance (total input capacitance), forms a pole that adds unwanted phase shift when either the total input capacitance or feedback resistance is too large. For example, using the noninverting configuration with a gain of 10, if the total capacitance at the negative input is 10pF and the effective resistance ($R1 \parallel R2$) is 9kΩ, this RC network introduces a pole at $f_0 = 1.8\text{MHz}$. At

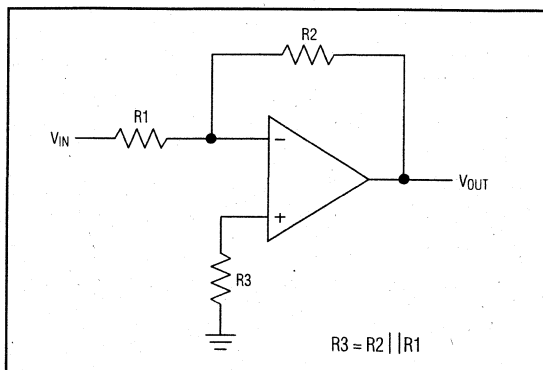


Figure 2a. Reducing Offset Error Due to Bias Current: Inverting Configuration

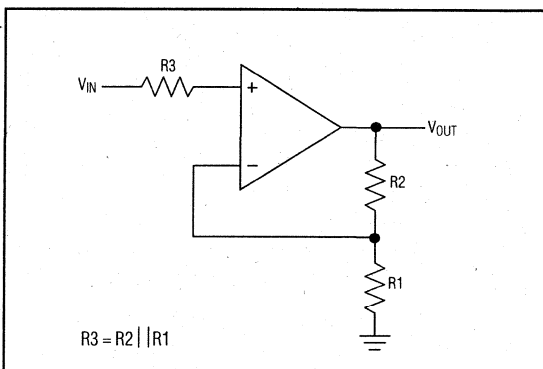


Figure 2b. Reducing Offset Error Due to Bias Current: Noninverting Configuration

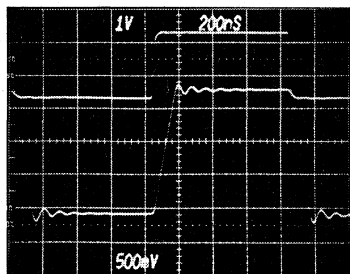
input frequencies above f_0 , the pole introduces additional phase shift, which reduces the overall bandwidth and adversely affects stability. Choose feedback resistors small enough so they do not adversely affect the op amp's operation at the frequencies of interest.

Overdriving the Outputs

The output voltage swing for specified operation is from ($V_{EE} + 0.3\text{V}$) to ($V_{CC} - 0.5\text{V}$) (see *Electrical Characteristics*). Exercising the outputs beyond these limits drives the output transistors toward saturation, resulting in bandwidth degradation, response-time increase, and gain decrease (which affects linearity). Operation in this region causes a slight distortion in the output waveform, but does not adversely affect the op amp.

Single/Dual/Quad, 10MHz Single-Supply Op Amps

MAX473/MAX474/MAX475



Driving 390pF in parallel with 10k Ω ,
V_{CC} = 5V, buffer configuration

Figure 3. MAX474 Driving 390pF

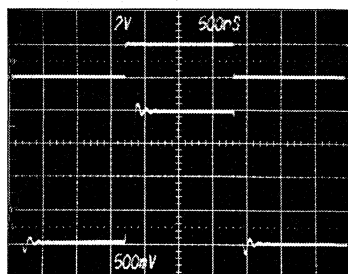


Figure 5. The MAX473 easily drives 1000pF using the
Capacitive-Load Driving Circuit (Figure 4).

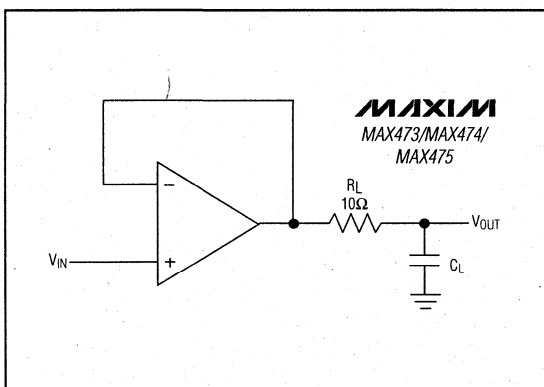


Figure 4. Capacitive-Load Driving Circuit

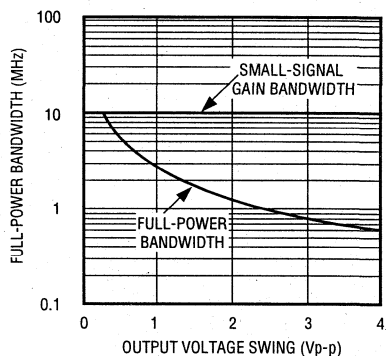


Figure 6. Full-Power Bandwidth vs. Peak-to-Peak AC Voltage

Full-Power Bandwidth

The MAX473/MAX474/MAX475's fast 15V/ μ s slew rate maximizes full-power bandwidth (FPBW). The FPBW is given by:

$$\text{FPBW (Hz)} = \frac{\text{SR}}{\pi [\text{V}_{\text{OUT peak-to-peak(max)}}]}$$

where the slew rate (SR) is 15V/ μ s min. Figure 6 shows the full-power bandwidth as a function of the peak-to-peak AC output voltage.

Layout

A good layout improves performance by decreasing the amount of stray capacitance at the amplifier's inputs and output. Since stray capacitance might be unavoidable, minimize trace lengths and resistor leads, and place external components as close to the pins as possible.

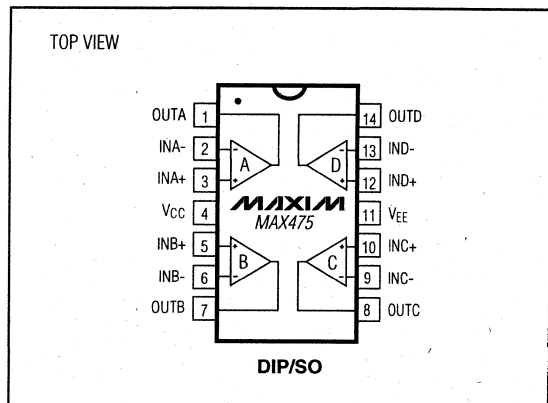
Single/Dual/Quad, 10MHz Single-Supply Op Amps

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX474CPA	0°C to +70°C	8 Plastic DIP
MAX474CSA	0°C to +70°C	8 SO
MAX474CUA	0°C to +70°C	8 μ MAX
MAX474C/D	0°C to +70°C	Dice*
MAX474EPA	-40°C to +85°C	8 Plastic DIP
MAX474ESA	-40°C to +85°C	8 SO
MAX474MJA	-55°C to +125°C	8 CERDIP
MAX475CPD	0°C to +70°C	14 Plastic DIP
MAX475CSD	0°C to +70°C	14 SO
MAX475EPD	-40°C to +85°C	14 Plastic DIP
MAX475ESD	-40°C to +85°C	14 SO
MAX475MJD	-55°C to +125°C	14 CERDIP

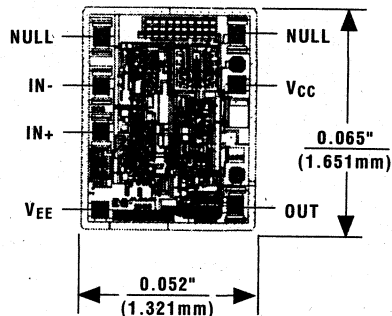
* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Pin Configurations (continued)



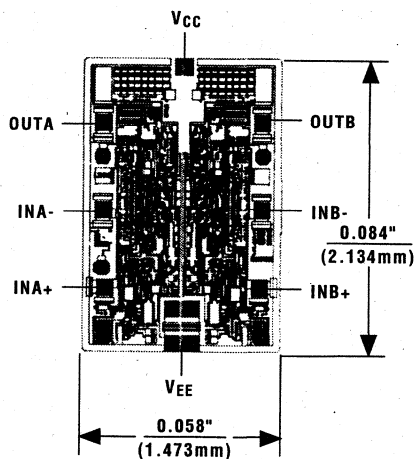
Chip Topographies

MAX473



TRANSISTOR COUNT: 185
SUBSTRATE CONNECTED TO VEE

MAX474



TRANSISTOR COUNT: 355
SUBSTRATE CONNECTED TO VEE

MAXIM

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

General Description

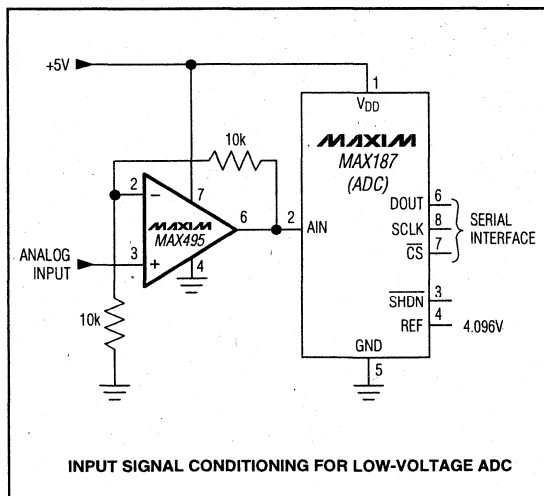
The dual MAX492, quad MAX494, and single MAX495 operational amplifiers combine excellent DC accuracy with rail-to-rail operation at the input and output. Since the common-mode voltage extends from VCC to VEE, the devices can operate from either a single supply (+2.7V to +6V) or split supplies ($\pm 1.35V$ to $\pm 3V$). Each op amp requires less than 150 μA supply current. Even with this low current, the op amps are capable of driving a 1k Ω load, and the input referred voltage noise is only 25nV/ $\sqrt{Hz}$. In addition, these op amps can drive loads in excess of 1nF.

The precision performance of the MAX492/MAX494/MAX495, combined with their wide input and output dynamic range, low-voltage single-supply operation, and very low supply current, makes them an ideal choice for battery-operated equipment and other low-voltage applications. The MAX492/MAX494/MAX495 are available in DIP and SO packages in the industry-standard op-amp pin configurations. The MAX495 is also available in the smallest 8-pin SO: the μ MAX package.

Applications

Portable Equipment
Battery-Powered Instruments
Data Acquisition
Signal Conditioning
Low-Voltage Applications

Typical Operating Circuit



Features

- ◆ Low-Voltage Single-Supply Operation (+2.7V to +6V)
- ◆ Rail-to-Rail Input Common-Mode Voltage Range
- ◆ Rail-to-Rail Output Swing
- ◆ 500kHz Gain-Bandwidth Product
- ◆ Unity-Gain Stable
- ◆ 150 μA Max Quiescent Current per Op Amp
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ 200 μV Offset Voltage
- ◆ High Voltage Gain (108dB)
- ◆ High CMRR (90dB) and PSRR (110dB)
- ◆ Drives 1k Ω Load
- ◆ Drives Large Capacitive Loads
- ◆ MAX495 Available in μ MAX Package—8-Pin SO

Ordering Information

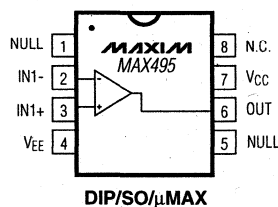
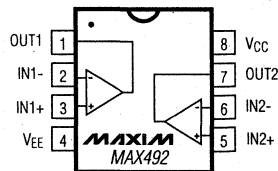
PART	TEMP. RANGE	PIN-PACKAGE
MAX492CPA	0°C to +70°C	8 Plastic DIP
MAX492CSA	0°C to +70°C	8 SO
MAX492C/D	0°C to +70°C	Dice*
MAX492EPA	-40°C to +85°C	8 Plastic DIP
MAX492ESA	-40°C to +85°C	8 SO
MAX492MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

* Dice are specified at $T_A = +25^\circ C$, DC parameters only.

Pin Configurations

TOP VIEW



Pin Configurations continued at end of data sheet.

MAXIM

Maxim Integrated Products 3-31

Call toll free 1-800-998-8800 for free samples or literature.

MAX492/MAX494/MAX495

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC to VEE)	7V
Common-Mode Input Voltage	(VCC + 0.3V) to (VEE - 0.3V)
Differential Input Voltage	±(VCC - VEE)
Input Current (IN+, IN-, NULL1, NULL2)	±10mA
Output Short-Circuit Duration	Indefinite short circuit to either supply
Voltage Applied to NULL Pins	VCC to VEE
Continuous Power Dissipation (TA = +70°C)	
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
8-Pin Cerdip (derate 8.00mW/°C above +70°C)	640mW
8-Pin µMAX (derate 4.1mW/°C above +70°C)	330mW

14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)	800mW
14-Pin SO (derate 8.33mW/°C above +70°C)	667mW
14-Pin Cerdip (derate 9.09mW/°C above +70°C)	727mW
Operating Temperature Ranges	
MAX49_C_ _ _	0°C to +70°C
MAX49_E_ _ _	-40°C to +85°C
MAX49_M_ _ _	-55°C to +125°C
Junction Temperatures	
MAX49_C_ _/E_ _	+150°C
MAX49_M_ _	+175°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(VCC = 2.7V to 6V, VEE = GND, VCM = 0V, VOUT = VCC / 2, TA = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	VCM = VEE to VCC			±200	±500	µV
Input Bias Current	VCM = VEE to VCC			±25	±60	nA
Input Offset Current	VCM = VEE to VCC			±0.5	±6	nA
Differential Input Resistance				2		MΩ
Common-Mode Input Voltage Range			VEE - 0.25		VCC + 0.25	V
Common-Mode Rejection Ratio	(VEE - 0.25V) ≤ VCM ≤ (VCC + 0.25V)		74	90		dB
Power-Supply Rejection Ratio	VCC = 2.7V to 6V		88	110		dB
Large-Signal Voltage Gain (Note 1)	VCC = 2.7V, RL = 100kΩ, VOUT = 0.25V to 2.45V	Sourcing	90	104		dB
		Sinking	90	102		
	VCC = 2.7V, RL = 1kΩ, VOUT = 0.5V to 2.2V	Sourcing	94	105		
		Sinking	78	90		
	VCC = 5.0V, RL = 100kΩ, VOUT = 0.25V to 4.75V	Sourcing	98	108		
		Sinking	92	100		
	VCC = 5.0V, RL = 1kΩ, VOUT = 0.5V to 4.5V	Sourcing	98	110		
		Sinking	86	98		
Output Voltage Swing (Note 1)	RL = 100kΩ	VOH	VCC - 0.075	VCC - 0.04		V
		VOL		VEE + 0.04	VEE + 0.075	
	RL = 1kΩ	VOH	VCC - 0.20	VCC - 0.15		
		VOL		VEE + 0.15	VEE + 0.20	
Output Short-Circuit Current				30		mA
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	VCM = VOUT = VCC / 2	VCC = 2.7V		135	150	µA
		VCC = 5V		150	170	

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

MAX492/MAX494/MAX495

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.7V$ to $6V$, $V_{EE} = GND$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	$R_L = 100k\Omega$, $C_L = 100pF$		500		kHz
Phase Margin	$R_L = 100k\Omega$, $C_L = 100pF$		60		degrees
Gain Margin	$R_L = 100k\Omega$, $C_L = 100pF$		10		dB
Total Harmonic Distortion	$R_L = 10k\Omega$, $C_L = 15pF$, $V_{OUT} = 2V_{p-p}$, $A_v = +1$, $f = 1kHz$		0.003		%
Slew Rate	$R_L = 100k\Omega$, $C_L = 15pF$		0.20		V/ μs
Settling Time	To 0.1%, 2V step		12		μs
Turn-On Time	$V_{CC} = 0V$ to 3V step, $V_{IN} = V_{CC}/2$, $A_v = +1$		5		μs
Input Noise-Voltage Density	$f = 1kHz$		25		nV/ $\sqrt{Hz}$
Input Noise-Current Density	$f = 1kHz$		0.1		pA/ $\sqrt{Hz}$
Amp-Amp Isolation	$f = 1kHz$		125		dB

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.7V$ to $6V$, $V_{EE} = GND$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_{CM} = V_{EE}$ to V_{CC}				± 650	μV
Input Offset Voltage Tempco				± 2		$\mu V/^\circ C$
Input Bias Current	$V_{CM} = V_{EE}$ to V_{CC}				± 75	nA
Input Offset Current	$V_{CM} = V_{EE}$ to V_{CC}				± 6	nA
Common-Mode Input Voltage Range			$V_{EE} - 0.20$		$V_{CC} + 0.20$	V
Common-Mode Rejection Ratio	$(V_{EE} - 0.20) \leq V_{CM} \leq (V_{CC} + 0.20)$		72			dB
Power-Supply Rejection Ratio	$V_{CC} = 2.7V$ to $6V$		86			dB
Large-Signal Voltage Gain (Note 1)	$V_{CC} = 2.7V$, $R_L = 100k\Omega$, $V_{OUT} = 0.25V$ to $2.45V$	Sourcing	88			dB
		Sinking	84			
	$V_{CC} = 2.7V$, $R_L = 1k\Omega$, $V_{OUT} = 0.5V$ to $2.2V$	Sourcing	92			
		Sinking	76			
	$V_{CC} = 5.0V$, $R_L = 100k\Omega$, $V_{OUT} = 0.25V$ to $4.75V$	Sourcing	92			
		Sinking	88			
	$V_{CC} = 5.0V$, $R_L = 1k\Omega$, $V_{OUT} = 0.5V$ to $4.5V$	Sourcing	96			
		Sinking	82			
Output Voltage Swing (Note 1)	$R_L = 100k\Omega$	V_{OH}	$V_{CC} - 0.075$			V
		V_{OL}		$V_{EE} + 0.075$		
	$R_L = 1k\Omega$	V_{OH}	$V_{CC} - 0.20$			
		V_{OL}		$V_{EE} + 0.20$		
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	$V_{CM} = V_{OUT} = V_{CC}/2$	$V_{CC} = 2.7V$			175	μA
		$V_{CC} = 5V$			190	

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.7V$ to $6V$, $V_{EE} = GND$, $V_{CM} = 0V$, $V_{OUT} = V_{CC} / 2$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_{CM} = V_{EE}$ to V_{CC}				± 950	μV
Input Offset Voltage Tempco				± 2		$\mu V/^{\circ}C$
Input Bias Current	$V_{CM} = V_{EE}$ to V_{CC}				± 100	nA
Input Offset Current	$V_{CM} = V_{EE}$ to V_{CC}				± 8	nA
Common-Mode Input Voltage Range			$V_{EE} - 0.15$	$V_{CC} + 0.15$		V
Common-Mode Rejection Ratio	$(V_{EE} - 0.15) \leq V_{CM} \leq (V_{CC} + 0.15)$		68			dB
Power-Supply Rejection Ratio	$V_{CC} = 2.7V$ to $6V$, $V_{CM} = 0V$		84			dB
Large-Signal Voltage Gain (Note 1)	$V_{CC} = 2.7V$, $R_L = 100k\Omega$, $V_{OUT} = 0.25V$ to $2.45V$	Sourcing	86			dB
		Sinking	84			
	$V_{CC} = 2.7V$, $R_L = 1k\Omega$, $V_{OUT} = 0.5V$ to $2.2V$	Sourcing	92			
		Sinking	76			
	$V_{CC} = 5.0V$, $R_L = 100k\Omega$, $V_{OUT} = 0.25V$ to $4.75V$	Sourcing	92			
		Sinking	86			
	$V_{CC} = 5.0V$, $R_L = 1k\Omega$, $V_{OUT} = 0.5V$ to $4.5V$	Sourcing	96			
		Sinking	80			
Output Voltage Swing (Note 1)	$R_L = 100k\Omega$	V_{OH}	$V_{CC} - 0.075$			V
		V_{OL}		$V_{EE} + 0.075$		
	$R_L = 1k\Omega$	V_{OH}	$V_{CC} - 0.20$			
		V_{OL}		$V_{EE} + 0.20$		
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	$V_{CM} = V_{OUT} = V_{CC} / 2$	$V_{CC} = 2.7V$			185	μA
		$V_{CC} = 5V$			200	

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

MAX492/MAX494/MAX495

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.7V$ to $6V$, $V_{EE} = GND$, $V_{CM} = 0V$, $V_{OUT} = V_{CC} / 2$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.)

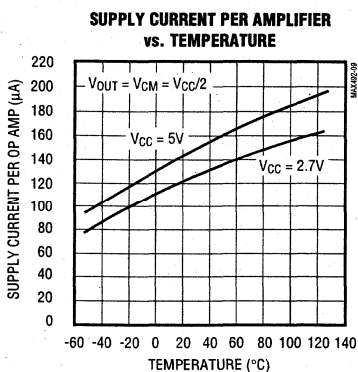
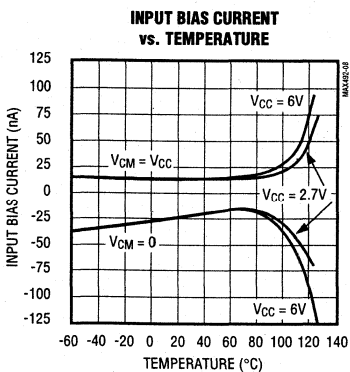
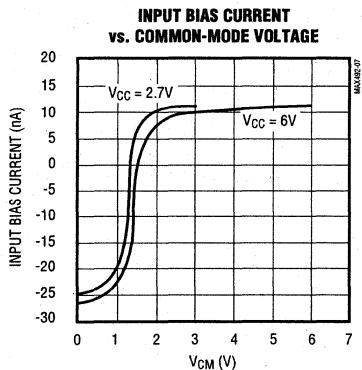
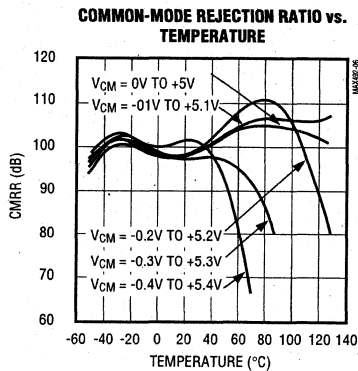
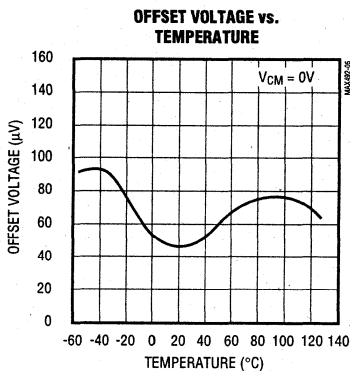
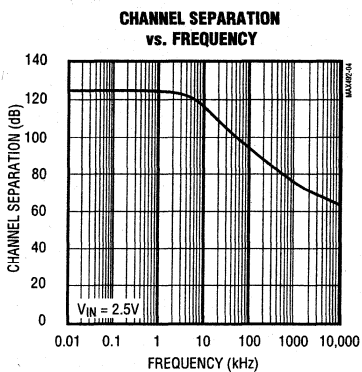
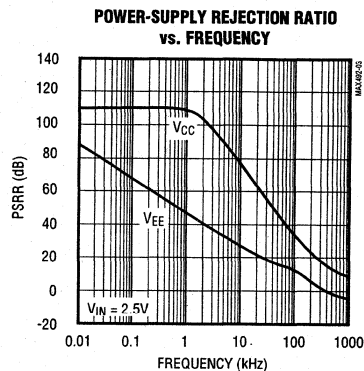
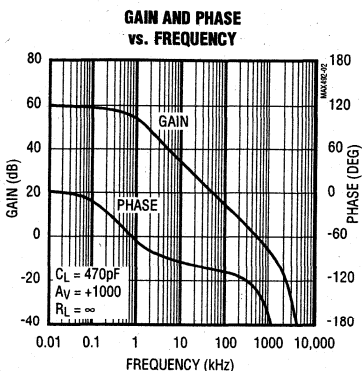
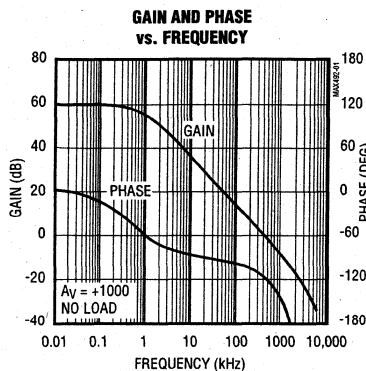
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_{CM} = V_{EE}$ to V_{CC}				± 1.2	mV
Input Offset Voltage Tempco				± 2		$\mu V/^{\circ}C$
Input Bias Current	$V_{CM} = V_{EE}$ to V_{CC}				± 200	nA
Input Offset Current	$V_{CM} = V_{EE}$ to V_{CC}				± 10	nA
Common-Mode Input Voltage Range			$V_{EE} - 0.05$	$V_{CC} + 0.05$		V
Common-Mode Rejection Ratio	$(V_{EE} - 0.05V) \leq V_{CM} \leq (V_{CC} + 0.05V)$		66			dB
Power-Supply Rejection Ratio	$V_{CC} = 2.7V$ to $6V$		80			dB
Large-Signal Voltage Gain (Note 1)	$V_{CC} = 2.7V$, $R_L = 100k\Omega$, $V_{OUT} = 0.25V$ to $2.45V$	Sourcing	82			dB
		Sinking	80			
	$V_{CC} = 2.7V$, $R_L = 1k\Omega$, $V_{OUT} = 0.5V$ to $2.2V$	Sourcing	90			
		Sinking	72			
	$V_{CC} = 5.0V$, $R_L = 100k\Omega$, $V_{OUT} = 0.25V$ to $4.75V$	Sourcing	86			
		Sinking	82			
	$V_{CC} = 5.0V$, $R_L = 1k\Omega$, $V_{OUT} = 0.5V$ to $4.5V$	Sourcing	94			
		Sinking	76			
Output Voltage Swing (Note 1)	$R_L = 100k\Omega$	V_{OH}	$V_{CC} - 0.075$			V
		V_{OL}		$V_{EE} + 0.075$		
	$R_L = 1k\Omega$	V_{OH}	$V_{CC} - 0.250$			
		V_{OL}		$V_{EE} + 0.250$		
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	$V_{CM} = V_{OUT} = V_{CC} / 2$	$V_{CC} = 2.7V$			200	μA
		$V_{CC} = 5V$			225	

Note 1: R_L to V_{EE} for sourcing and V_{OH} tests; R_L to V_{CC} for sinking and V_{OL} tests.

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{EE} = 0\text{V}$, unless otherwise noted.)

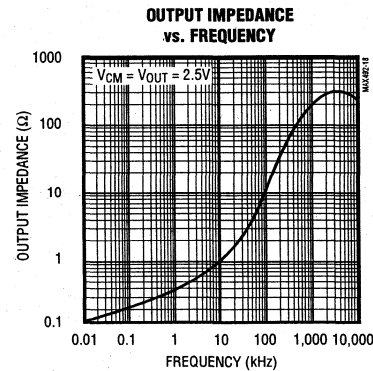
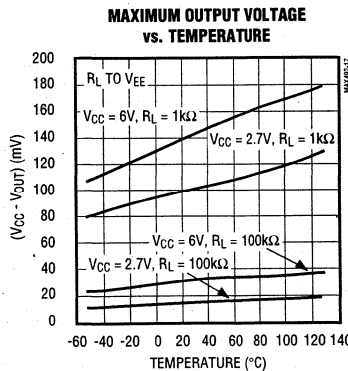
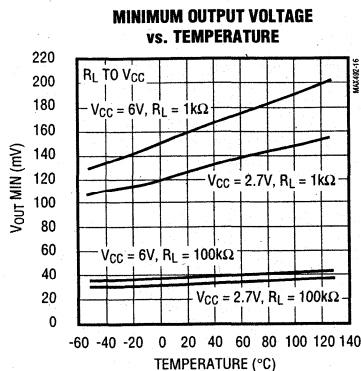
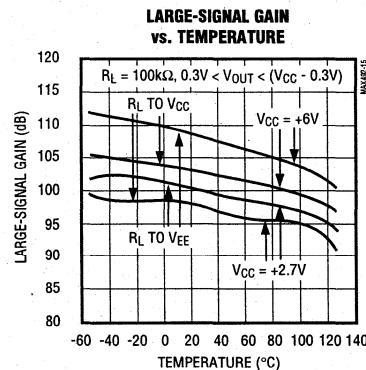
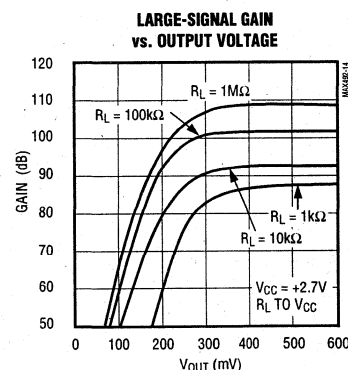
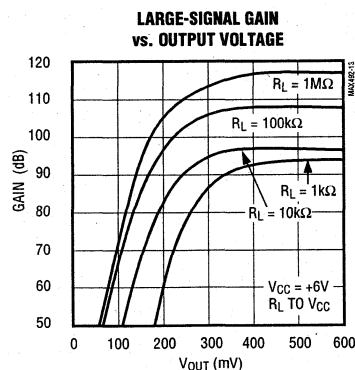
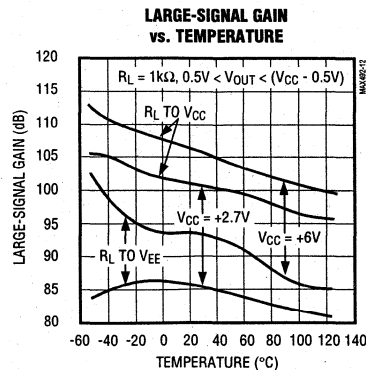
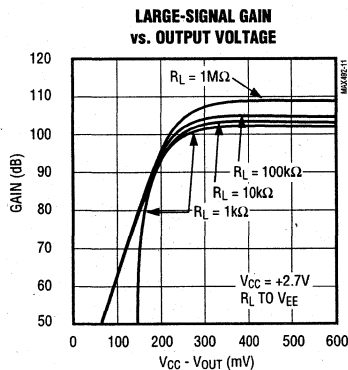
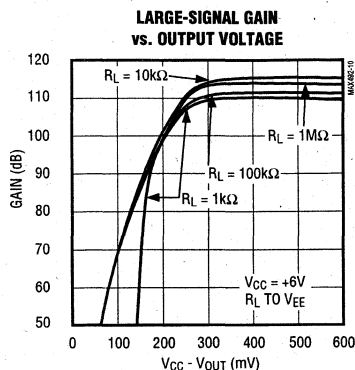


Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

Typical Operating Characteristics (continued)

(TA = +25°C, VCC = 5V, VEE = 0V, unless otherwise noted.)

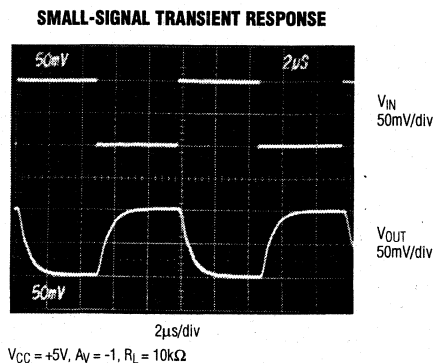
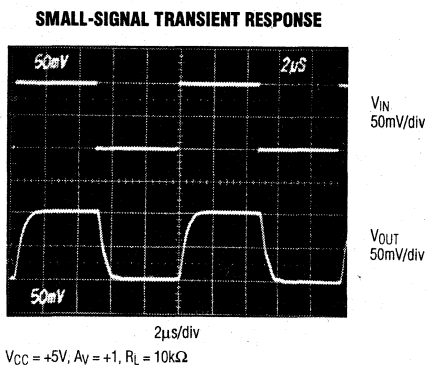
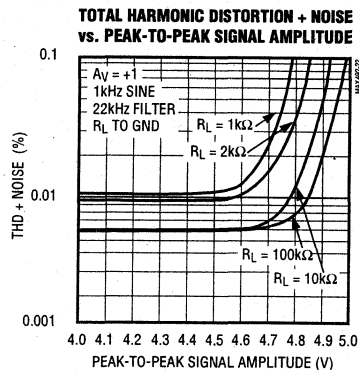
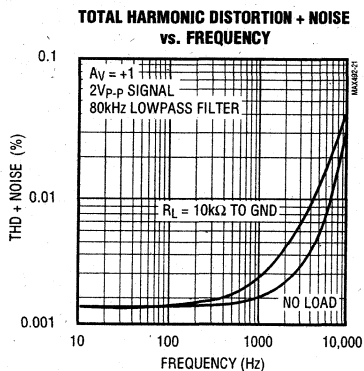
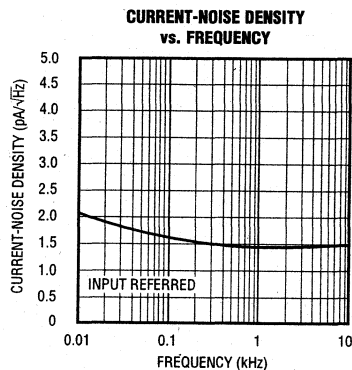
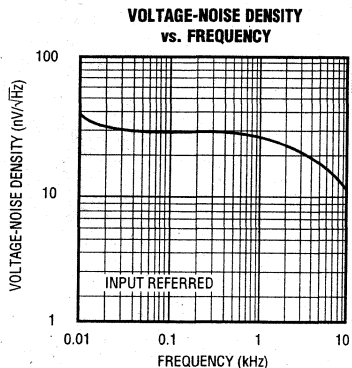
MAX492/MAX494/MAX495



Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

Typical Operating Characteristics (continued)

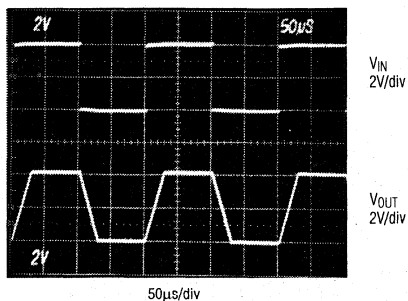
($T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{EE} = 0\text{V}$, unless otherwise noted.)



Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

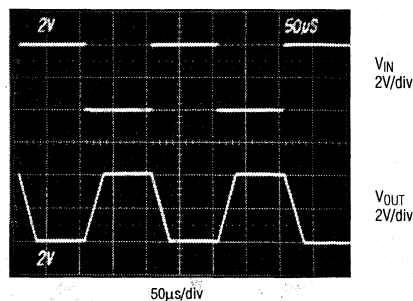
Typical Operating Characteristics (continued)

LARGE-SIGNAL TRANSIENT RESPONSE



V_{CC} = +5V, A_V = +1, R_L = 10kΩ

LARGE-SIGNAL TRANSIENT RESPONSE



V_{CC} = +5V, A_V = -1, R_L = 10kΩ

Pin Description

PIN			NAME	FUNCTION
MAX492	MAX494	MAX495		
1	1	—	OUT1	Amplifier 1 Output
—	—	1, 5	NULL	Offset Null Input. Connect to a 10kΩ potentiometer for offset-voltage trimming. Connect wiper to V _{EE} . See Figure 3.
—	—	2	IN-	Inverting Input
2	2	—	IN1-	Amplifier 1 Inverting Input
—	—	3	IN+	Noninverting Input
3	3	—	IN1+	Amplifier 1 Noninverting Input
4	11	4	V _{EE}	Negative Power-Supply Pin. Connect to ground or a negative voltage.
5	5	—	IN2+	Amplifier 2 Noninverting Input
—	—	6	OUT	Amplifier Output
6	6	—	IN2-	Amplifier 2 Inverting Input
7	7	—	OUT2	Amplifier 2 Output
8	4	7	V _{CC}	Positive Power-Supply Pin. Connect to (+) terminal of power supply.
—	8	—	OUT3	Amplifier 3 Output
—	9	—	IN3-	Amplifier 3 Inverting Input
—	10	—	IN3+	Amplifier 3 Noninverting Input
—	12	—	IN4+	Amplifier 4 Noninverting Input
—	13	—	IN4-	Amplifier 4 Inverting Input
—	14	—	OUT4	Amplifier 4 Output
—	—	8	N.C.	No Connect. Not internally connected.

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

Applications Information

The dual MAX492, quad MAX494, and single MAX495 op amps combine excellent DC accuracy with rail-to-rail operation at both input and output. With their precision performance, wide dynamic range at low supply voltages, and very low supply current, these op amps are ideal for battery-operated equipment and other low-voltage applications.

Rail-to-Rail Inputs and Outputs

The MAX492/MAX494/MAX495's input common-mode range extends 0.25V **beyond** the positive and negative supply rails, with excellent common-mode rejection. Beyond the specified common-mode range, the outputs are guaranteed not to undergo phase reversal or latchup. Therefore, the MAX492/MAX494/MAX495 can be used in applications with common-mode signals at or even beyond the supplies, without the problems associated with typical op amps.

The MAX492/MAX494/MAX495's output voltage swings to within 50mV of the supplies with a 100k Ω load. This rail-to-rail swing at the input and output substantially increases the dynamic range, especially in low supply-voltage applications. Figure 1 shows the input and output waveforms for the MAX492, configured as a unity-gain noninverting buffer operating from a single +3V supply. The input signal is 3.0V_{p-p}, 1kHz sinusoid centered at +1.5V. The output amplitude is approximately 2.95V_{p-p}.

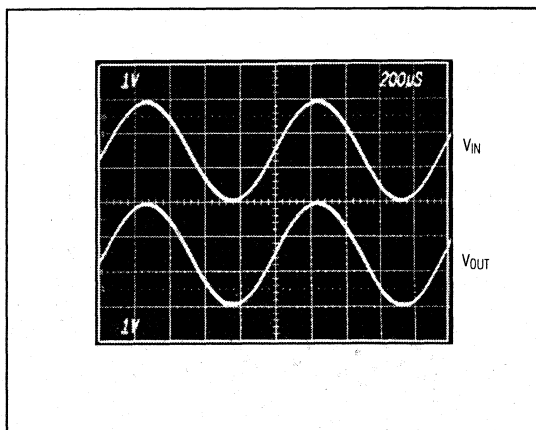


Figure 1. Rail-to-Rail Input and Output (Voltage Follower Circuit, VCC = +3V, VEE = 0V)

Input Offset Voltage

Rail-to-rail common-mode swing at the input is obtained by two complementary input stages in parallel, which feed a folded cascaded stage. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages close to the positive rail.

The offsets of the two pairs are trimmed, however there is some small residual mismatch between them. This mismatch results in a two-level input offset characteristic, with a transition region between the levels occurring at a common-mode voltage of approximately 1.3V. Unlike other rail-to-rail op amps, the transition region has been widened to approximately 600mV in order to minimize the slight degradation in CMRR caused by this mismatch.

To adjust the MAX495's input offset voltage (500 μ V max at +25°C), connect a 10k Ω trim potentiometer between the two NULL pins (pins 1 and 5), with the wiper connected to VEE (pin 4) (Figure 2). The trim range of this circuit is $\pm$ 6mV. External offset adjustment is not available for the dual MAX492 or quad MAX494.

The input bias currents of the MAX492/MAX494/MAX495 are typically less than 50nA. The bias current flows into the device when the NPN input stage is active, and it flows out when the PNP input stage is active. To reduce the offset error caused by input bias current flowing through external source resistances, match the effective resistance seen at each input. Connect resistor R3 between the noninverting input and ground when using

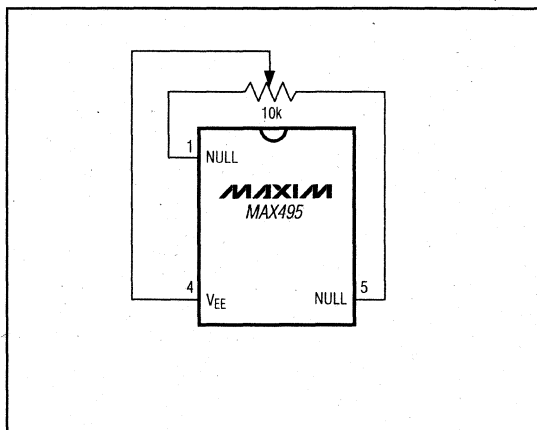


Figure 2. Offset Null Circuit

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

MAX492/MAX494/MAX495

the op amp in an inverting configuration (Figure 3a); connect resistor R3 between the noninverting input and the input signal when using the op amp in a noninverting configuration (Figure 3b). Select R3 to equal the parallel combination of R1 and R2. High source resistances will degrade noise performance, due to the thermal noise of the resistor and the input current noise (which is multiplied by the source resistance).

Output Loading and Stability

Even with their low quiescent current of less than 150µA per op amp, the MAX492/MAX494/MAX495 are well suited for driving loads up to 1kΩ while maintaining DC accuracy. Stability while driving heavy capacitive loads is another key advantage over comparable CMOS rail-to-rail op amps.

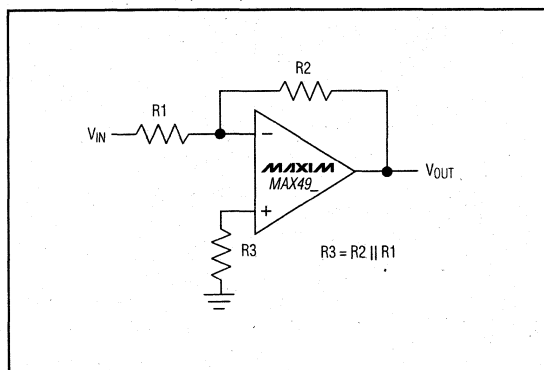


Figure 3a. Reducing Offset Error Due to Bias Current: Inverting Configuration

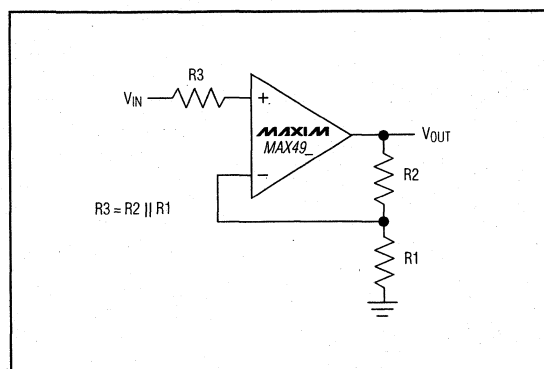


Figure 3b. Reducing Offset Error Due to Bias Current: Noninverting Configuration

In op amp circuits, driving large capacitive loads increases the likelihood of oscillation. This is especially true for circuits with high loop gains, such as a unity-gain voltage follower. The output impedance and a capacitive load form an RC network that adds a pole to the loop response and induces phase lag. If the pole frequency is low enough—as when driving a large capacitive load—the circuit phase margin is degraded, leading to either an under-damped pulse response or oscillation.

The MAX492/MAX494/MAX495 can drive capacitive loads in excess of 1000pF under certain conditions (Figure 4). When driving capacitive loads, the greatest potential for instability occurs when the op amp is sourcing approximately 100µA. Even in this case, sta-

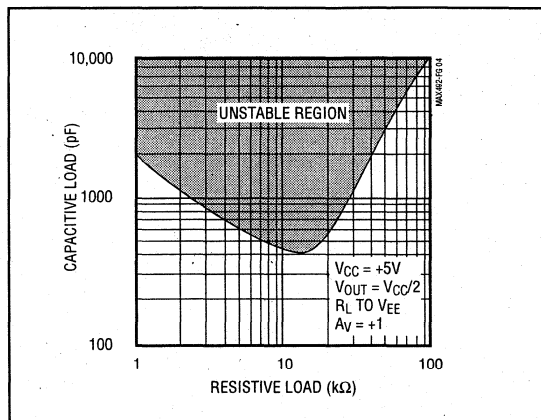


Figure 4. Capacitive-Load Stable Region Sourcing Current

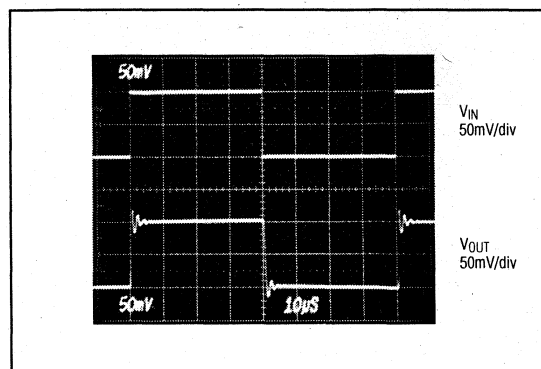


Figure 5. MAX492 Voltage Follower with 1000pF Load ($R_L = \infty$)

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

bility is maintained with up to 400pF of output capacitance. If the output sources either more or less current, stability is increased. These devices perform well with a 1000pF pure capacitive load (Figure 5). Figure 6 shows the performance with a 500pF load in parallel with various load resistors.

To increase stability while driving large capacitive loads, connect a pull-up resistor at the output to decrease the current that the amplifier must source. If the amplifier is made to sink current rather than source, stability is further increased.

Frequency stability can be improved by adding an output isolation resistor (R_S) to the voltage follower circuit (Figure 7). This resistor improves the phase margin of the circuit by isolating the load capacitor from the op amp's output. Figure 8a shows the MAX492 driving 10,000pF ($R_L \geq 100k\Omega$), while Figure 8b adds a 47 Ω isolation resistor.

Because the MAX492/MAX494/MAX495 have excellent stability, no isolation resistor is required, except in the most demanding applications. This is beneficial because an isolation resistor would degrade the low-frequency performance of the circuit.

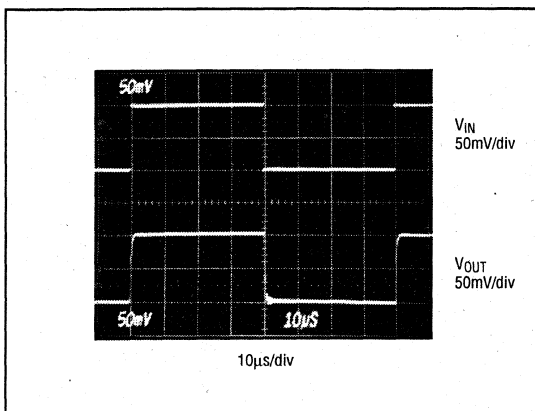


Figure 6a. MAX492 Voltage Follower with 500pF Load—
 $R_L = 5k\Omega$

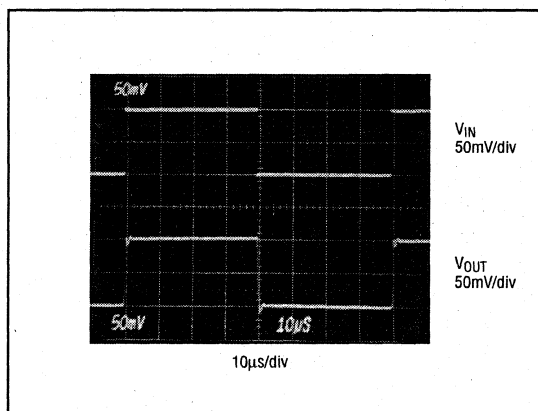


Figure 6c. MAX492 Voltage Follower with 500pF Load—
 $R_L = \infty$

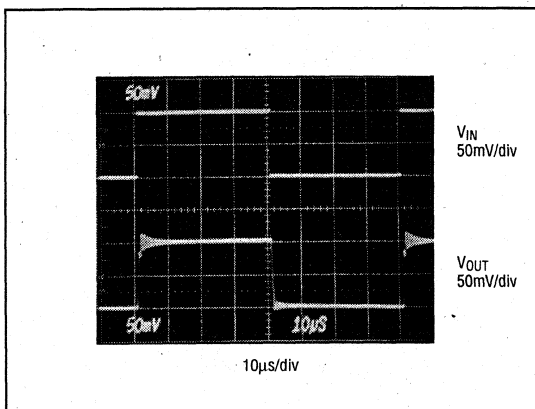


Figure 6b. MAX492 Voltage Follower with 500pF Load—
 $R_L = 20k\Omega$

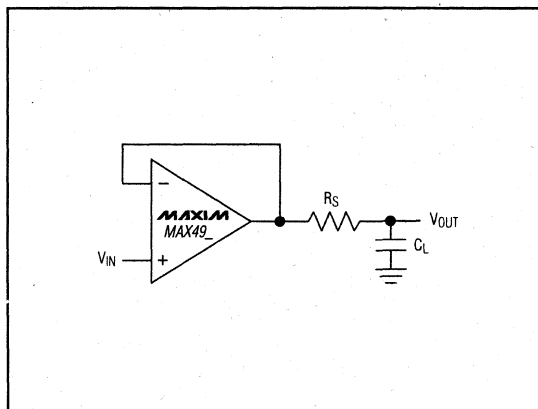


Figure 7. Capacitive-Load Driving Circuit

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

Power-Up Settling Time

The MAX492/MAX494/MAX495 have a typical supply current of 150 μ A per op amp. Although supply current is already low, it is sometimes desirable to reduce it further by powering down the op amp and associated ICs for periods of time. For example, when using a MAX494 to buffer the inputs to a multi-channel analog-to-digital converter (ADC), much of the circuitry could be powered down between data samples to increase battery life. If samples are taken infrequently, the op amps, along with the ADC, may be powered down most of the time.

When power is reapplied to the MAX492/MAX494/MAX495, it takes some time for the voltages on the supply pin and the output pin of the op amp to settle. Supply settling time depends on the supply voltage, the value of the bypass capacitor, the output impedance of the incoming supply, and any lead resistance or inductance between components. Op amp settling time depends primarily on the output voltage and is slew-rate limited. With the noninverting input to a voltage follower held at mid-supply (Figure 9), when the supply steps from 0V to V_{CC} , the output settles in approximately 4 μ s for $V_{CC} = +3$ V (Figure 10a) or 10 μ s for $V_{CC} = +5$ V (Figure 10b).

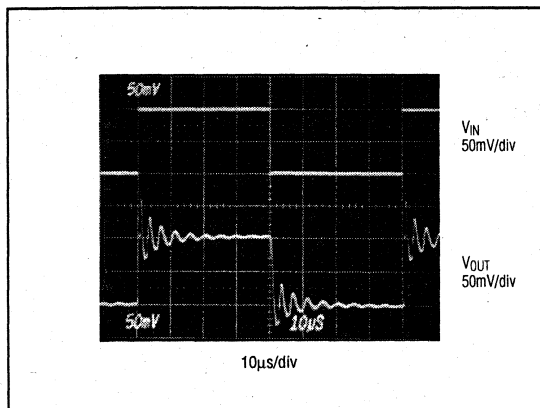


Figure 8a. Driving a 10,000pF Capacitive Load

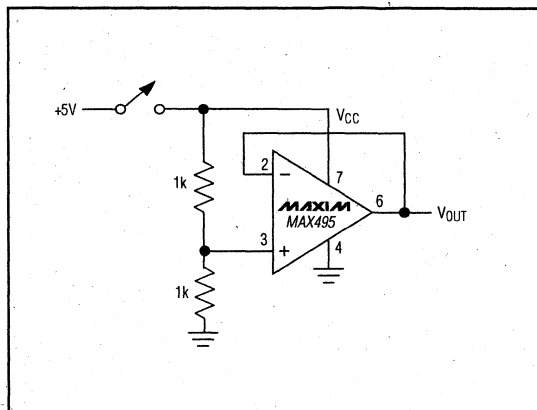


Figure 9. Power-Up Test Configuration

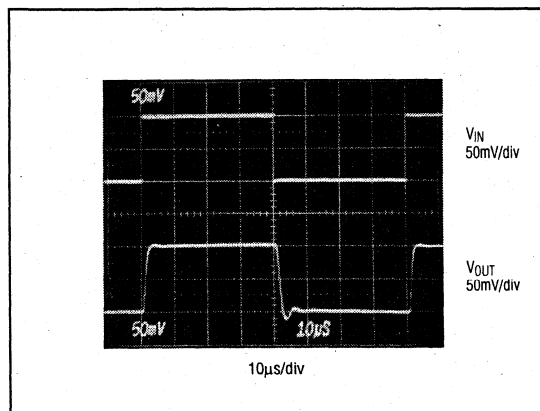


Figure 8b. Driving a 10,000pF Capacitive Load with a 47 Ω Isolation Resistor

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

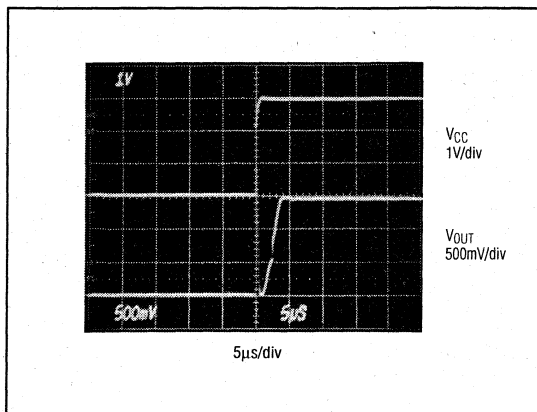


Figure 10a. Power-Up Settling Time ($V_{CC} = +3V$)

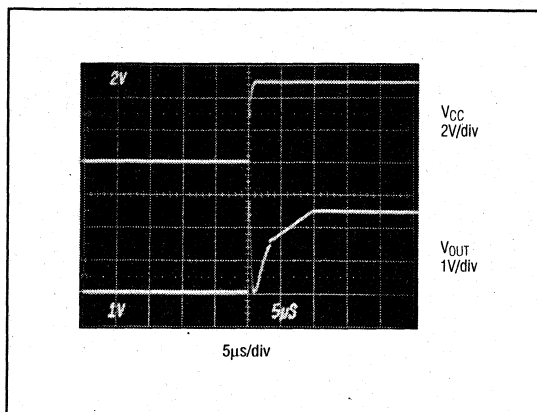


Figure 10b. Power-Up Settling Time ($V_{CC} = +5V$)

Power Supplies and Layout

The MAX492/MAX494/MAX495 operate from a single 2.7V to 6V power supply, or from dual supplies of $\pm 1.35V$ to $\pm 3V$. For single-supply operation, bypass the power supply with a $1\mu F$ capacitor in parallel with a $0.1\mu F$ ceramic capacitor. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize both trace lengths and resistor leads and place external components close to the op amp's pins.

Rail-to-Rail Buffers

The *Typical Operating Circuit* shows a MAX495 gain-of-two buffer driving the analog input to a MAX187 12-bit ADC. Both devices run from a single 5V supply, and the converter's internal reference is 4.096V. The MAX495's typical input offset voltage is $200\mu V$. This results in an error at the ADC input of $400\mu V$, or less than half of one least significant bit (LSB). Without offset trimming, the op amp contributes negligible error to the conversion result.

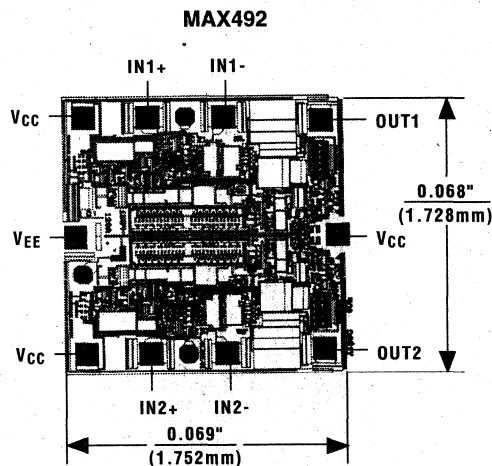
Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX494CPD	0°C to +70°C	14 Plastic DIP
MAX494CSD	0°C to +70°C	14 SO
MAX494EPD	-40°C to +85°C	14 Plastic DIP
MAX494ESD	-40°C to +85°C	14 SO
MAX494MJD	-55°C to +125°C	14 CERDIP
MAX495CPA	0°C to +70°C	8 Plastic DIP
MAX495CSA	0°C to +70°C	8 SO
MAX495CUA	0°C to +70°C	8 μ MAX
MAX495C/D	0°C to +70°C	Dice*
MAX495EPA	-40°C to +85°C	8 Plastic DIP
MAX495ESA	-40°C to +85°C	8 SO
MAX495MJA	-55°C to +125°C	8 CERDIP

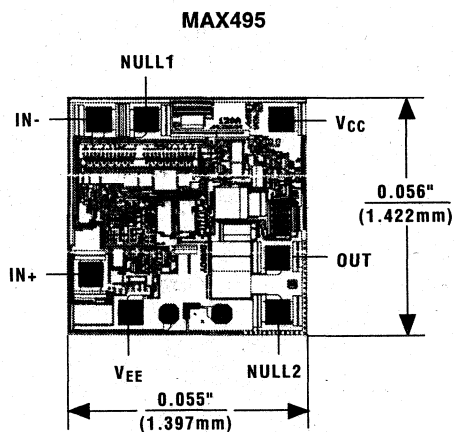
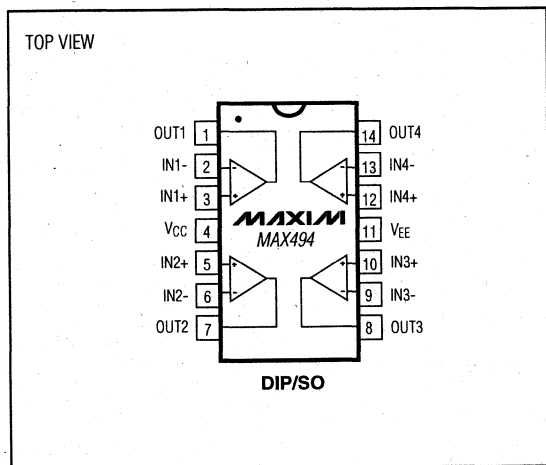
* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Chip Topographies



MAX492/MAX494/MAX495

Pin Configurations (continued)



TRANSISTOR COUNT: 134 (single MAX495)
268 (dual MAX492)
536 (quad MAX494)
SUBSTRATE CONNECTED TO VEE

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/95

MAXIM

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

General Description

The MAX951-MAX954 feature combinations of a micropower operational amplifier, comparator, and reference in an 8-pin package. In the MAX951 and MAX952, the comparator's inverting input is connected to an internal $1.2V \pm 1\%$ bandgap reference. The MAX953 and MAX954 are offered without an internal reference. The MAX951/MAX952 operate from a single $+2.8V$ to $+7V$ supply with a typical supply current of $6\mu A$, while the MAX953/MAX954 operate from $+2.4V$ to $+7V$ with a $4\mu A$ typical supply current. Both the op amp and comparator feature a common-mode input voltage range that extends from the negative supply rail to within $1.6V$ of the positive rail, as well as output stages that swing rail to rail.

The op amps in the MAX951/MAX953 are internally compensated to be unity-gain stable, while the op amps in the MAX952/MAX954 feature $125kHz$ typical bandwidth, $66V/ms$ slew rate, and stability for gains of $10V/V$ or greater. These op amps have a unique output stage that enables them to operate with an ultra-low supply current while maintaining linearity under loaded conditions. In addition, they have been designed to exhibit good DC characteristics over their entire operating temperature range, minimizing input referred errors.

The comparator output stage of these devices continuously sources as much as $40mA$. The comparators eliminate power-supply glitches that commonly occur when changing logic states, minimizing parasitic feedback and making the devices easier to use. In addition, they contain $\pm 3mV$ internal hysteresis to ensure clean output switching, even with slow-moving input signals.

Selection Table

PART	INTERNAL 1% PRECISION REFERENCE	MINIMUM GAIN STABILITY (V/V)	COMPARATOR	SUPPLY CURRENT (μA)
MAX951	Yes	1	Yes	6
MAX952	Yes	10	Yes	6
MAX953	No	1	Yes	4
MAX954	No	10	Yes	4

Features

- ◆ Op Amp + Comparator + Reference in an 8-Pin μMAX Package (MAX951/MAX952)
- ◆ $6\mu A$ Typical Supply Current (Op Amp + Comparator + Reference)
- ◆ Comparator and Op-Amp Input Range Includes Ground
- ◆ Outputs Swing Rail to Rail
- ◆ $+2.4V$ to $+7V$ Supply Voltage Range
- ◆ Unity-Gain Stable and Decompensated $A_v \geq 10V/V$ Op-Amp Options
- ◆ Internal $1.2V \pm 1\%$ Bandgap Reference
- ◆ Internal Fixed $\pm 3mV$ Comparator Hysteresis
- ◆ Op Amp Capable of Driving up to $1000pF$ Load

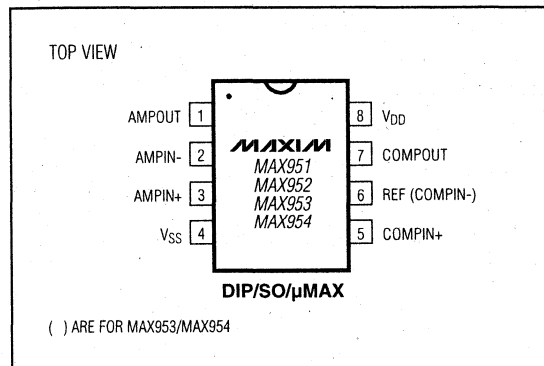
Applications

Instruments, Terminals, and Bar-Code Readers
Battery-Powered Systems
Automotive Keyless Entry
Low-Frequency, Local-Area Alarms/Detectors
Photodiode Preamps
Smart Cards
Infrared Receivers for Remote Controls
Smoke Detectors and Safety Sensors

MAX951-MAX954

3

Pin Configuration



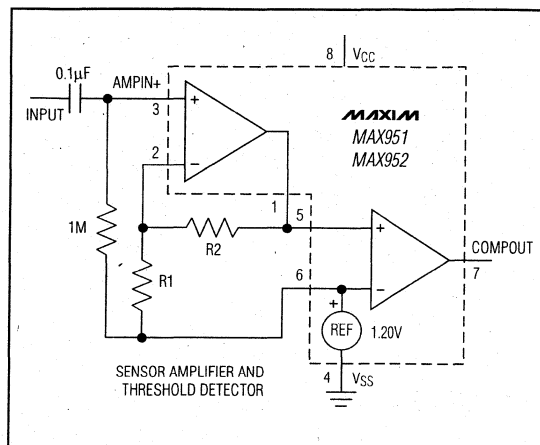
MAXIM

Maxim Integrated Products 3-47

Call toll free 1-800-998-8800 for free samples or literature.

Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

Typical Operating Circuit



Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX951C/D	+25°C	Dice*
MAX951EPA	-40°C to +85°C	8 Plastic DIP
MAX951ESA	-40°C to +85°C	8 SO
MAX951EUA	-40°C to +85°C	8 µMAX
MAX951MJA	-55°C to +125°C	8 Cerdip**
MAX952C/D	+25°C	Dice*
MAX952EPA	-40°C to +85°C	8 Plastic DIP
MAX952ESA	-40°C to +85°C	8 SO
MAX952EUA	-40°C to +85°C	8 µMAX
MAX952MJA	-55°C to +125°C	8 Cerdip**
MAX953C/D	+25°C	Dice*
MAX953EPA	-40°C to +85°C	8 Plastic DIP
MAX953ESA	-40°C to +85°C	8 SO
MAX953EUA	-40°C to +85°C	8 µMAX
MAX953MJA	-55°C to +125°C	8 Cerdip**
MAX954C/D	+25°C	Dice*
MAX954EPA	-40°C to +85°C	8 Plastic DIP
MAX954ESA	-40°C to +85°C	8 SO
MAX954EUA	-40°C to +85°C	8 µMAX
MAX954MJA	-55°C to +125°C	8 Cerdip**

* Dice are tested at $T_A = +25^\circ\text{C}$, DC parameters only.

** Contact factory for availability and processing to MIL-STD-883.



Power-Supply Circuits

Power-Supply Circuits, Product Tables and Trees	4-3
MAX1600 Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network*	4-11
MAX1601 Dual-Channel Cardbus and PCMCIA Power Switch w/ SMBus™ Serial Interface*	4-19
MAX1610 Digitally Controlled CCFL Backlight Power Supply*	4-31
MAX1611 Digitally Controlled CCFL Backlight Power Supply w/ SMBus™ Interface*	4-31
MAX1620 Digitally Adjustable LCD Bias Supply*	4-33
MAX1621 Digitally Adjustable LCD Bias Supply w/ SMBus™ Interface*	4-33
MAX1622 Digitally Adjustable LCD Bias Supply*	4-33
MAX1626 100% Duty Cycle, PFM, 5V or 3.3V Pin-Selectable, Step-Down DC-DC Controller*	4-35
MAX1627 100% Duty Cycle, PFM, Adjustable-Output, Step-Down DC-DC Controller*	4-35
MAX1649 5V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller	4-37
MAX1651 3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller	4-37
MAX2003 NiCd/NiMH Battery Fast-Charge Controller	4-49
MAX2003A NiCd/NiMH Battery Fast-Charge Controller w/ Pulse Trickle	4-49
MAX603 5V or Adjustable, Low-Dropout, Low IQ, 500mA Linear Regulator	4-69
MAX604 3.3V or Adjustable, Low-Dropout, Low IQ, 500mA Linear Regulator	4-69
MAX606 Low-Profile, 0.8MHz, Step-Up DC-DC Converter for Type 1 Flash Memory/ PCMCIA Cards*	4-79
MAX607 Low-Profile, 0.4MHz, Step-Up DC-DC Converter for Type 2 and 3 Flash Memory/ PCMCIA Cards*	4-79
MAX608 Low Input Voltage, High-Efficiency, Step-Up DC-DC Controller*	4-81
MAX624 Dual-Output, 1MHz, DC-DC Boost Converter for PCMCIA Applications	4-83
MAX687 3.3V, Low-Noise Linear Regulator Controller w/ Automatic Shutdown	4-99
MAX688 3.3V, Low-Noise Linear Regulator Controller	4-99
MAX689 3V, Low-Noise Linear Regulator Controller	4-99
MAX796 Step-Down PWM Controller with Synchronous Rectifier for CPU Power w/ Positive Secondary	4-109
MAX797 Step-Down PWM Controller with Synchronous Rectifier for CPU Power w/ Low-Noise Pin	4-109
MAX799 Step-Down PWM Controller with Synchronous Rectifier for CPU Power w/ Negative Secondary	4-109
MAX830 1A, Adjustable-Output, Step-Down, PWM DC-DC Converter—Surface Mountable	4-141
MAX831 1A, 5V, Step-Down, PWM DC-DC Converter—Surface Mountable	4-141
MAX832 1A, 3.3V, Step-Down, PWM DC-DC Converter—Surface Mountable**	4-141
MAX833 1A, 3V, Step-Down, PWM DC-DC Converter—Surface Mountable**	4-141
MAX840 Low-Noise, Regulated, -2V GaAsFET Bias	4-147
MAX843 Low-Noise, Regulated, -2V GaAsFET Bias w/ Adjustable Reference	4-147
MAX844 Low-Noise, Regulated, -2V GaAsFET Bias w/ LCD Output	4-147
MAX845 750mW Isolated Transformer Driver for PCMCIA Applications	4-157
MAX848 1 to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converter*	4-173
MAX849 1 to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converter*	4-173
MAX863 Dual-Output, PFM, Step-Up DC-DC Controller*	4-175
MAX864 Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter w/ Shutdown*	4-177

*Advance Information—first page of data sheet in preparation.

**Future Product.



Power-Supply Circuits (continued)

MAX865	Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter in μ MAX*	4-179
MAX866	3.3V/5V-Output, Single-Cell DC-DC Converter for Pagers.....	4-181
MAX867	Adjustable-Output, Single-Cell DC-DC Converter for Pagers.....	4-181
MAX882	3.3V or Adjustable, Low-Dropout, Low I_Q , 200mA Linear Regulator w/ Standby Mode	4-193
MAX883	5V or Adjustable, Low-Dropout, Low I_Q , 200mA Linear Regulator w/ Shutdown Mode	4-193
MAX884	3.3V or Adjustable, Low-Dropout, Low I_Q , 200mA Linear Regulator w/ Shutdown Mode	4-193

*Advance Information—first page of data sheet in preparation.

POWER MANAGEMENT

BATTERY CHARGERS

- ★ ☆ MAX2003
(NiCd/NiMH, temp. slope detection)
- † ☆ MAX2003A
(improved MAX2003)
- MAX471/472
(current-sense amp, fuel gauge) (see Op Amp table)
- ★ MAX712
(NiCd/NiMH, zero voltage-slope detection)
- ★ MAX713
(NiCd/NiMH, negative voltage-slope detection)

MULTI-FUNCTION SUPPLIES

- ★ ☆ MAX845
(750mW isolated transformer driver)

ISOLATED POWER

HIGH-SIDE MOSFET DRIVERS

- MAX620 (quad driver)
- MAX621 (quad driver, internal caps)
- MAX622 (VOUT = VIN + 11V)
- MAX623 (VOUT = VIN + 11V, internal caps)
- MAX625 (quad driver, internal MOSFETs & caps)

LOW-SIDE MOSFET DRIVERS

- MAX626 (2A, 4Q, dual inverting)
- MAX627 (2A, 4Q, dual noninverting)
- MAX628 (2A, 4Q, dual mixed)
- MAX4420 (6A, 1.5Q, single noninverting)
- MAX4426 (1.5A, 4Q, dual inverting)
- MAX4427 (1.5A, 4Q, dual noninverting)
- MAX4428 (1.5A, 4Q, dual mixed)
- MAX4429 (6A, 1.5Q, single inverting)
- ICL7667 (1.5A, 4Q, dual inverting)
- TSC426 (1.5A, 6Q, dual inverting)
- TSC427 (1.5A, 6Q, dual noninverting)
- TSC428 (1.5A, 6Q, dual mixed)

1-CELL PORTABLES

- † ☆ MAX848/849
(2.7V to 5V step-up)

2-OR 3-CELL PORTABLES

- MAX687 (3V and 3.3V LDO linear reg.)
- ★ MAX688 (3V and 3.3V LDO linear reg.)
- ★ MAX689 (3V and 3.3V LDO linear reg.)
- ★ MAX717 (3.3V & 12V flash prog.)
- ★ MAX718 (3.3V or 5V & 12V flash prog.)
- ★ MAX719 (3V or 5V & 12V flash prog.)
- MAX720 (3.3V or 5V & 12V flash prog.)
- MAX721 (3V or 5V & 12V flash prog.)
- ★ MAX722 (3.3V or 5VOUT, neg. LCD)
- ★ MAX723 (3V or 5VOUT, neg. LCD)
- † ☆ MAX863
(Dual PPM boost controller in small package)

5-OR 6-CELL PORTABLES

- MAX714 (2 at +5V, -26V LCD, μ P super.)
- MAX715 (3 at +5V, -26V LCD, -5V, +12V, μ P super.)
- ★ MAX716 (4 at +5V, -26V LCD, -5V, +12V, μ P super.)

5 to 12 CELL PORTABLES/NOTEBOOKS

- ★ MAX781 (3.3V, battery charger, PCMCIA)
- ★ MAX782 (3.3V, 5V, PCMCIA)
- ★ MAX783 (3.3V, 5V, PCMCIA, optimized for 6-cell inputs)
- ★ MAX786 (3.3V, 5V)

3V & 5V PCMCIA CARD & HOSTS

- † MAX1600 (dual card-slot power network with internal switches)
- † MAX1601 (dual card-slot power network with internal switches & SMBus serial interface)
- MAX613 (PCMCIA controller, dual Vpp)
- MAX614 (PCMCIA controller, single Vpp)
- ★ MAX624 (Dual output (5V & adj.), 1MHz switcher)
- MAX780 (PCMCIA controller, 4 level translators, dual Vpp, power ready)

- ★ New product
- † Future product
- ☆ Evaluation kit available

DC-DC CONVERTERS

LOW-DROPOUT LINEAR REGULATORS

POSITIVE

- ★ MAX603/604
(5V/3.3V or adj.,
500mA, 1.8V 8-pin SO)
- MAX663
(5V or adj., $I_Q = 6\mu A$)
- MAX666
(5V or adj., $I_Q = 6\mu A$,
low-battery detect)
- MAX667
(5V or adj., $I_Q = 20\mu A$, 120mV
dropout, 200mA, low-battery detect)
- MAX687
(3.3V ±3%, 0.073V dropout
at 500mA, 0.80V dropout at 4A)
- ★ MAX688/689
(3.3V/3V ±3%,
0.073V dropout at 500mA,
0.80V dropout at 4A)
- ★ MAX882
(3.3V or adj., P-Ch, 200mA,
low-battery detector,
1.5W 8-pin SO)
- ★ MAX883/884
(5V/3.3V or adj., P-Ch, 200mA,
low-battery detector,
1.3W 8-pin SO, 1µA OFF mode)
- ICL7663A (adj., 40mA)

NEGATIVE

- MAX664
(-3V or adj., $I_Q = 6\mu A$)
- ICL7664A (adj., 40mA)

SWITCHING REGULATORS

STEP-UP

- ★ MAX731 (2Vin to 5VOUT)
- ★ MAX732/733/752 (12V/5V/adj.)

PWM

- ★ MAX734 (12V, flash prog.)
- MAX848/849 (1-cell to 2.7V–5V step-up)

PFM

- ★ MAX1171 (12V or adj. controller)
- MAX1493 (adj.)
- ★ MAX606/607 (5V or 12V or adj.,
8-pin µMAX, for PCMCIA, 1MHz)
- ★ MAX608 (5V or adj., 2Vin, 300kHz)
- MAX630 (adj.)
- MAX631/632/633 (5V/12V/15V or adj.)
- MAX641/642/643 (5V/12V/15V or adj.
controller)
- ★ MAX756/757 (3.3V or 5V/adj.,
1.8Vin, 250mA)
- ★ MAX761 (12V, 120mA, flash prog.)
- ★ MAX762 (15V or adj.)

INVERTING

- ★ MAX4391 (adj.)
- MAX634 (adj.)
- MAX635/636/637 (-5V/-12V/-15V or adj.)
- ★ MAX749 (digital adj.)
- ★ MAX764/765/766 (-5V/-12V/-15V or adj.
controller)

PWM

- MAX735/755 (-5V/adj., max $\Delta V = 11.7V$)
- ★ MAX736/737/759
(-12V/-15V/-5V/adj., max $\Delta V = 22V$)

DUAL OUTPUT

- ★ MAX1610 (CCFL with digital adj.)
- ★ MAX1611 (CCFL with SMBus digital adj.)
- ★ MAX1620 (LCD bias supply with digital adj.)
- ★ MAX1621 (LCD bias supply with SMBus digital adj.)
- ★ MAX1622 (LCD bias supply)
- MAX753 (CCFL & -LCD, digital adj.)
- MAX754 (CCFL & +LCD, digital adj.)

PWM

- ★ MAX742 (±12V or ±15V controller)
- ★ MAX743 (±12V or ±15V)

STEP-DOWN

- ★ MAX724 (adj., 5A)
- ★ MAX727/728/729 (3.3V, battery charger,
adj./5V/3.3V/3V, 2A)
- ★ MAX740A (5V)
- ★ MAX782 (3.3V & 5V, PCMCIA)
- ★ MAX783 (3.3V & 5V, PCMCIA
for 6-cell inputs)
- ★ MAX744 (5V, optimized
for cellular comm.)
- ★ MAX746 (5V or adj.
controller; N-channel FET)
- ★ MAX747 (5V or adj.
controller; P-channel FET)
- ★ MAX748A (3.3V)
- ★ MAX750A (adj.)
- ★ MAX758A (adj.)
- ★ MAX763A (3.3V)

PFM

- ★ MAX1626/1627 (3.3V or 5V/adj., 100% duty cycle)
- ★ MAX1649/1651 (5V/3.3V or adj. controller)
- MAX638 (5V or adj.)
- ★ MAX639/640/653 (5V/3.3V/3V or adj., >90% efficiency)
- ★ MAX649/651/652 (5V/3.3V/3V or adj. controller)

STEP-UP/DOWN

- ★ MAX877/878/879 (5V/3V or 3.3V/adj.,
can start output from 1V to 6.2V input)
- ★ MAX761 (12V, 120mA, flash prog.)

CHARGE PUMPS

-VIN or (2 x VIN)

- MAX1044 (60kHz osc. freq. boost)
- MAX660 (100mA, VIN
up to 5V)
- MAX665 (100mA, VIN
up to 8V)
- MAX860/861 (50mA, VIN up to 5.5V,
250kHz osc. freq.)
- ICL7660 (VIN up to 10V)
- ICL7662 (VIN up to 20V)
- SI7661 (VIN up to 20V)

-VIN and (2 x VIN)

- MAX680
- MAX681 (internal caps)
- ★ MAX864 (5kHz to 200kHz, 1µF caps,
shutdown)
- ★ MAX865 (30kHz, µMAX package)

12V, 30mA

- ★ MAX662A (programs flash memories,
E² temp. range)

5V, 50mA

- ★ MAX649

-4.1V/Adj., 5mA

- ★ MAX850/851/852/853 (4.5Vin, low-noise,
neg. GaAsFET bias)

-2V/Adj., 4mA

- ★ MAX840/843/844 (2.5Vin, low-noise,
neg. GaAsFET bias)

DC-DC Switching Converters

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max.(typ)	Output (mA typ)	Control Scheme	Pins- Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up (\$)
STEP-UP SWITCHING REGULATORS										
MAX606/607	3 to 5.5	5 or 12 or adj.	0.6(0.4/0.3)(0.2)	75	PFM	8- μ MAX	CE	Yes	1MHz switching frequency fits Type I PCMCIA cards	††
MAX608	2 to 16.5	5 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	CE	Yes	Same as MAX1771, but accepts low input voltages	††
MAX624	3 to 5.5	5 & 12 or adj.	0.9(0.45)	200 @ 5V 80 @ 12V	PFM	16-NSO	I		1.2MHz switching frequency fits Type I PCMCIA cards	5.25
MAX731	1.8 to 5.25	5	4(2)	200	PWM	8-DIP, 16-WSO	C.E.M	Yes		2.60
MAX732	4 to 9.3	12	3(1.7)	200	PWM	8-DIP, 16-WSO	C.E.M	Yes		2.76
MAX733	4 to 11	15	3(1.7)	125	PWM	8-DIP, 16-WSO	C.E.M	Yes		2.60
MAX734	1.9 to 12	12	2.5(1.2)	120	PWM	8-DIP, 8-SO	C.E.M	Yes	12V flash memory, hot insert	2.23
MAX752	1.8 to 16	Adj.	3(1.7)	2.4W	PWM	8-DIP, 8-SO	C.E.M	Yes		2.94
MAX756/757	1.1 to 5.5	(3.3 or 5)/adj.	0.060(0.045)	250	PFM	8-DIP, 8-SO	CE	Yes	Best combination of low I_Q & high 86% efficiency	1.95
MAX761/762	2 to 16.5	12/15 or adj. to 16.5	0.1(0.080)	120	PFM	8-DIP, 8-SO	C.E.M	Yes	12V flash memory, lowest I_Q , 1.8V/3V/5V inputs	2.23
MAX770/771/772	2 to 16.5	5/12/15 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C.E.M	Yes	Controllers, high efficiency over wide I_{OUT} range	1.80
MAX1771	2 to 16.5	12 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C.E.M	Yes	Same as MAX771, but with single 100mV current-sense limit	1.80
MAX773	3 to 16.5	Adj.	0.1(0.085)	1A	PFM	14-DIP, 14-NSO	C.E.M	Yes	Controller, high-voltage applications	1.80
MAX777/778/779	1 to 6.2	5/3 or 3.3)/adj.	0.310(0.220)	300	PFM	8-DIP, 8-SO	C.E.M	Yes	On-chip active diode, true turn-off in shutdown	2.65
MAX848/849	0.8 to 5	2.7 to 5	TBD	200	PWM	16-NSO	CE	Yes	1-cell step-up, low-noise, fixed-frequency PWM	††
MAX856/857	0.5 to 6	(3.3 or 5)/adj.	0.060(0.025)	100	PFM	8-SO, 8- μ MAX	CE	Yes	Smallest, best combination of low I_Q & high 85% efficiency	1.72
MAX858/859	0.5 to 6	(3.3 or 5)/adj.	0.060(0.025)	25	PFM	8-SO, 8- μ MAX	CE	Yes	Smallest, best combination of low I_Q & high efficiency	1.72
MAX866/867	0.5 to 6	(3.3 or 5)/adj.	0.6(0.025)	90	PFM	8- μ MAX	E	Yes	Guaranteed 0.9V start-up, low I_Q	1.76
STEP-UP/DOWN SWITCHING REGULATORS										
MAX761	2.7 to 12	Adj. (1.5 to 6)	0.1(0.08)	200	PFM	8-DIP, 8-SO	C.E.M		No transformer	2.23
MAX877/878/879	1 to 6.2	5/3.3 or 3)/adj.	0.310(0.220)	240	PFM	8-DIP, 8-SO	C.E.M	Yes	Gives regulated output when input above and below the output. no transformer	2.95
STEP-DOWN SWITCHING REGULATORS										
MAX638	2.6 to 16.5	5, adj.	0.6(0.135)	75	PFM	8-DIP, 8-SO	C.E.M		Ultra-low I_Q	2.56
MAX639/640/653	4 to 11.5	5/3.3/3 or adj.	0.02(0.01)	225	PFM	8-DIP, 8-SO	C.E.M	Yes	Drives external P-channel FET, low I_Q	2.96
MAX649/651/652	4 to 16.5	5/3.3/3 or adj.	0.1(0.080)	2A	PFM	8-DIP, 8-SO	C.E.M	Yes	Same as MAX649/651, but with 96.5% duty cycle and single 100mV current-sense limit	1.60
MAX1649/1651	4 to 16.5	5/3.3 or adj.	0.1(0.080)	2A	PFM	8-DIP, 8-SO	C.E.M	Yes	Same as MAX1651, but with 100% duty cycle, high efficiency, and controller	††
MAX1626/1627	3 to 16.5	3.3 or 5)/adj.	0.080(0.060)	2A	PFM	8-SO	I, E	Yes		††
MAX724	0 to 60	Adj.	11(8.5)	5A	PFM	7-TO-220	CE			††
MAX726	0 to 40	Adj.	11(8.5)	2A	PFM	7-TO-220	CE			††
MAX727/728/729	0 to 40	5/3.3/3	11(8.5)	2A	PFM	7-TO-220	CE			††
MAX730A	5.2 to 11	5	3(1.7)	300	PWM	8-DIP, 8-SO	C.E.M	Yes	No subharmonic switching noise	2.15
MAX738A	6 to 16	5	3(1.7)	750	PWM	8-DIP, 16-WSO	C.E.M	Yes	No subharmonic switching noise	2.60
MAX744A	4.75 to 16	5	2.5(1.2)	750	PWM	8-DIP, 16-WSO	C.E.M	Yes	Optimized for cellular communications, no subharmonic switching noise	2.90
MAX746	4 to 15	5)/adj.	1	2.5A	PWM	16-DIP, 16-NSO	C.E.M		Lowest-cost 5V to 3.3V apps., drives external N-channel FET	2.25
MAX747	4 to 15	5)/adj.	1.3(0.8)	2.5A	PWM	14-DIP, 14-NSO	C.E.M	Yes	Lowest-cost 5V to 3.3V apps., drives external P-channel FET	2.25
MAX748A	3.3 to 16	3.3	3(1.7)	750	PWM	8-DIP, 16-WSO	C.E.M	Yes	No subharmonic switching noise	2.60
MAX750A	4 to 11	Adj.	3(1.7)	1.5W	PWM	8-DIP, 8-SO	C.E.M	Yes	No subharmonic switching noise	2.15
MAX758A	4 to 16	Adj.	3(1.7)	3.75W	PWM	8-DIP, 16-WSO	C.E.M	Yes	No subharmonic switching noise	2.60
MAX763A	3.3 to 11	3.3	2.5(1.4)	500	PWM	8-DIP, 8-SO	C.E.M	Yes	No subharmonic switching noise	2.15

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, μ MAX = Micro Max, TO— = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

DC-DC Switching Converters (continued)

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Control Scheme	Pins- Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up (\$)
MAX767	4.5 to 3.5	3.3, 3.45 (R), 5/3.3/3 or 3.6 (S)	0.75	1.5A to 10A	PWM	20-SSOP	C-E	Yes	Dedicated 5V-to-3.3V, high-efficiency, small size	3.40
MAX787/788/789	0 to 60	5/3.3/3	11(8.5)	5A	PFM	7-TQ-220	C-E			††
MAX796/797/799	4.5 to 30	5.05/3.3/2.9(adj.)	1(0.7)	50W	PWM	16-DIP, 16-NSO	C-E,M	Yes	Synchronous rectifier, secondary output regulation, high efficiency over full I _{OUT} range	3.65
MAX830/831	0 to 30	Adj./5	—	1A	PWM	16-SO	C	Yes	Small package	3.99
MAX832/833	0 to 30	3.3/3	—	1A	PWM	16-SO	C	Yes	Small package	††
INVERTING SWITCHING REGULATORS										
MAX735	4 to 6.2	-5	3(1.6)	275	PWM	8-DIP, 8-SO	C-E,M		>80% efficiencies	2.15
MAX736	4 to 8.6	-12	3(1.6)	125	PWM	14-DIP, 16-WSO	C-E,M	Yes	>80% efficiencies	2.75
MAX737	4 to 5.5	-15	4.5(2.5)	100	PWM	14-DIP, 16-WSO	C-E,M	Yes	>80% efficiencies	2.75
MAX739	4 to 15	-5	3(1.6)	500	PWM	14-DIP, 16-WSO	C-E,M	Yes	>80% efficiencies	2.75
MAX749	2 to 6	Adj.	0.06	5W	PFM	8-DIP, 8-SO	C-E,M	Yes	Digital adjust for negative LCD	2.49
MAX755	2.7 to 9	Adj.	3.5(1.8)	1.4W	PWM	8-DIP, 8-SO	C-E,M		>80% efficiencies	2.15
MAX759	4 to 15	Adj.	4(2.1)	1.5W	PWM	14-DIP, 16-WSO	C-E,M	Yes	LCD driver, >80% efficiencies	2.75
MAX764/765/766	3 to 16.5	-5/-12/-15 or adj. to 21AV	0.1	200	PFM	8-DIP, 8-SO	C-E,M	Yes	Lowest I _Q	2.38
MAX774/775/776	3 to 16.5	-5/-12/-15 or adj. to 21AV	0.1	1A	PFM	8-DIP, 8-SO	C-E,M	Yes	Controllers, high efficiency over wide I _{OUT} range	2.20
DUAL-OUTPUT SWITCHING REGULATORS										
MAX742	4.2 to 10	±12, ±15	15(8)	±15W	PWM	20-DIP, 20-WSO	C-E,M	Yes	Drives external MOSFETs	3.91
MAX743	4.2 to 6	±12, ±15	30(20)	±1.5W	PWM	16-DIP, 16-WSO	C-E,M	Yes	Internal power MOSFETs	4.49

DC-DC Charge-Pump Converters

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Pins- Package Options*	Temp. Ranges**	Features	Price† 1000-up (\$)
CHARGE-PUMP CONVERTERS—UNREGULATED								
MAX1044	1.5 to 10	-V _{IN} +2 x V _{IN}	0.200(0.03)	20	8-DIP, 8-SO	C-E,M	60kHz oscillator boost mode	1.19
MAX660	1.5 to 5.5	-V _{IN} +2 x V _{IN}	0.5(0.12)	100	8-DIP, 8-SO	C-E,M	8-pin SOIC	2.95
MAX665	1.5 to 8	-V _{IN} +2 x V _{IN}	0.5(0.12)	100	8-DIP, 16-WSO	C-E,M		3.96
MAX680	2 to 6	±2 x V _{IN}	2(1)	±10	8-DIP, 8-SO	C-E,M	Dual output	1.62
MAX681	2 to 6	±2 x V _{IN}	2(1)	±10	14-DIP	C-E	No external components (internal caps)	4.64
MAX860/861	1.5 to 5.5	-V _{IN} +2 x V _{IN}	0.33(0.18)	50	8-SO, 8-µMAX	C-E,M	Up to 250kHz oscillation frequency	1.45
MAX864	1.5 to 6.2	±2 x V _{IN}	0.3(0.2)	±10	16-QSOP	E	5kHz to 200kHz frequency select, 1µA shutdown	††
MAX865	1.5 to 6.2	±2 x V _{IN}	1.0(0.6)	±10	8-µMAX	E	Ultra-small µMAX package	††
ICL7660	1.5 to 10	-V _{IN} +2 x V _{IN}	0.175(0.110)	20	8-DIP, 8-SO, 8-TQ-99, 8-µMAX	C-E,M	µMAX package	1.09
ICL7662	4.5 to 20	-V _{IN} +2 x V _{IN}	0.6(0.25)	10	8-DIP, 8-SO, 8-TQ-99	C-I		1.86
SI7661	4.5 to 20	-V _{IN} +2 x V _{IN}	2(0.3)	10	8-DIP, 8-SO, 8-TQ-99	C-I		1.86

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TQ-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

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DC-DC Charge-Pump Converters (continued)

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output Current (mA typ)	Pins- Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up (\$)
CHARGE-PUMP CONVERTERS—REGULATED									
MAX619	2 to 3.6	5	0.15	60	8-DIP, 8-SO	C.E.M	Yes	No inductors, battery backup	1.60
MAX622	3.5 to 16.5	V _{IN} + 11V	0.5(0.07)	500µA	8-DIP, 8-SO	C.E		High-side switching	1.86
MAX623	3.5 to 16.5	V _{IN} + 11V	0.5(0.07)	500µA	16-DIP	C.E		No external capacitors, high-side switching	2.85
MAX662	Use MAX662A (pin-for-pin compatible upgrade)								
MAX662A	4.5 to 5.5	12	0.5(0.19)	30mA, guaranteed over temp.	8-DIP, 8-SO	C.E.M	Yes	World's smallest 12V flash memory programmer	2.09
MAX840/843/844	2.5 to 10	-2 or adj.	1(0.5)	4	8-SO	LE	Yes	Low-voltage negative GaAsFET bias, low noise, 1µA shutdown	1.75
MAX850-853	4.5 to 10	-4.1 or adj.	3(2)	5	8-SO	C.E	Yes	Negative GaAsFET bias, low noise, 1µA shutdown	1.65

Linear Voltage Regulators

Part Number	Input Voltage Range (V)	Output Voltage (V)	Dropout Voltage (V)	Quiescent Current (µA), max(typ)	Output Voltage Accuracy (%)	Shutdown	Pins- Package Options*	Temp. Ranges**	Price† 1000-up (\$)
DC LINEAR REGULATORS—POSITIVE OUTPUT									
MAX603	2.8 to 11.5	5 or adj. (1.3 to 11.5)	0.32 at 500mA	35(15)	±5	2µA off	8-DIP, 8-SO (P _{BISS} = 1.8W)	C.E.M	1.85
MAX604	2.8 to 11.5	3.3 or adj. (1.3 to 11.5)	0.48 at 400mA	35(15)	±5	2µA off	8-DIP, 8-SO (P _{BISS} = 1.8W)	C.E.M	1.85
MAX663	2 to 16.5	Fixed 5 or adj. (1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO	C.E.M	1.25
MAX666	2 to 16.5	Fixed 5 or adj. (1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO	C.E.M	1.38
MAX667	3.5 to 16.5	Fixed 5 or adj. (1.3 to 15)	0.15 at 200mA	25(20)	±4	Yes	8-DIP, 8-SO	C.E.M	2.35
MAX687	2.7 to 11	Fixed 3.3	0.073 at 500mA, 0.80 at 4A	250(150)	±3	Yes 25µA, off 1µA	8-DIP, 8-SO, 8-µMAX	C.E	1.60
MAX688/689	2.7 to 11	Fixed 3.3/3.0	0.073 at 500mA, 0.80 at 4A	250(150)	±3	Yes 25µA, off 1µA	8-DIP, 8-SO, 8-µMAX	C.E	1.60
MAX882	2.8 to 11.5	3.3 or adj. (1.5 to 11.5)	0.25 at 200mA	15(10)	±5	15µA standby	8-DIP, 8-SO (P _{BISS} = 1.5W)	C.E.M	1.45
MAX883	2.8 to 11.5	5 or adj. (1.5 to 11.5)	0.32 at 250mA	15(10)	±5	1µA off	8-DIP, 8-SO (P _{BISS} = 1.5W)	C.E.M	1.45
MAX884	2.8 to 11.5	3.3 or adj. (1.5 to 11.5)	0.25 at 200mA	15(10)	±5	1µA off	8-DIP, 8-SO (P _{BISS} = 1.5W)	C.E.M	1.45
ICL7663/A	1.5 to 16/2 to 16	Adj. (1.3 to 15)	0.9 at 40mA	10(3.5)	±8/±1.9	Yes	8-DIP, 8-SO, 8-TO-99	C.E.M	1.81/1.99
DC LINEAR REGULATORS—NEGATIVE OUTPUT									
MAX664	-2 to -16.5	Fixed -5 or -1.3 to -15	0.35 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO	C.E.M	1.75
ICL7664A	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±1	Yes	8-DIP, 8-SO, 8-TO-99	C.I.M	2.40
ICL7664B	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±5	Yes	8-DIP, 8-SO, 8-TO-99	C.I.M	1.85

Battery Chargers

Part Number	No. of Cells Charged	Cell Chemistry	Charge Rate	Charge Termination Method	Pins- Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up (\$)
MAX2003	1 to 16	NiCd and/ or NiMH	Fast, trickle, top-off	Temp slope, neg. ΔV, max temp, max time	16-DIP, 16-WSO	C	Yes	Linear or switcher, built-in term. algorithms, discharge-before-charge	3.25
MAX2003A	1 to 16	NiCd and/ or NiMH	Fast, trickle, top-off	Temp slope, neg. ΔV, max temp, max time	16-DIP, 16-WSO	C	Yes	Improved MAX2003, better loop response and pulse trickle-charge	††
MAX712	1 to 16	NiMH	Fast, trickle	neg. ΔV, max V, max temp, max time	16-DIP, 16-NSO	C.E.M	Yes	Linear or switcher, supplies load while charging, built-in term. algorithms	3.09
MAX713	1 to 16	NiCd	Fast, trickle	neg. ΔV, max V, max temp, max time	16-DIP, 16-NSO	C.E.M	Yes	Linear or switcher, supplies load while charging, built-in term. algorithms	3.09

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), TO = Can
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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

PCMCIA Switch Matrices

Part Number	Input Voltages (V)	Outputs	Controls	Plins- Package Options*	Temp. Ranges**	Features	Price† 1000-up (\$)
MAX1600	3.3/5/12	2 card slots	Std. PCMCIA	28-SSOP	C, E	Internal VCC and Vpp switches, current limit, thermal protection	++
MAX1601	3.3/5/12	2 card slots	SMBus	28-SSOP	C, E	Internal VCC and Vpp switches, current limit, thermal protection	++
MAX613	3.3/5/12	2 card slots	Std. PCMCIA	14-DIP, 14-SO	C, E	Internal Vpp switches, external VCC drivers	1.68
MAX614	3.3/5/12	1 card slot	Std. PCMCIA	8-DIP, 8-SO	C, E	Internal Vpp switches, external VCC drivers	1.48
MAX780A-C	3.3/5/12	2 card slots	Std. PCMCIA	24-DIP, 24-SSOP	C, E	Internal Vpp switches, external VCC drivers, Vpp valid output	2.25/2.00/2.05
MAX780D	3.3/5/12	2 card slots	Std. PCMCIA	20-DIP, 20-SSOP	C, E	Internal Vpp switches, external VCC drivers	1.80

Multiple-Output, System-Integrated Power Management Supplies

Part Number	Input Voltage Range (V)	Linear Output Voltage (V)	DC-DC Output Voltages (V)	Auxiliary Outputs (V)	Quiescent Supply Current, Over Temp. (µA max)	Plins- Package Options*	Temp. Ranges**	Features	Price† 1000-up (\$)
2 to 3 CELL INPUTS									
MAX717-721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	-	3.3 (MAX717), 3.3 or 5 (MAX718/720), 3 or 5 (MAX719/721)	5 or 12 (all)	60, 40 shutdown	16-NSO	C, E	Yes (MAX717- MAX719) Built-in switchover from main battery to plug-in adapter power, low-voltage warning, AC detect, clock & RAM keep-alive mini-switcher from backup battery	4.95
MAX722/723	0.85 to 5.5 (battery), 7 to 18 (plug-in adapter)	-	3.3 or 5 (MAX722), 3 or 5 (MAX723)	Neg. LCD (0 to -40)	60, 40 shutdown	16-NSO	C, E	Yes Built-in switchover from main battery to plug-in adapter power, low-voltage warning	4.63
MAX863	1.5 to 11	-	main = 3.3 or 5 or adj./1A second = adj./1A	LBI/LBO low-battery detector	45µA main ON, 65µA both ON, 5µA shutdown	16-QSOP	I, E	Yes Two high-efficiency boost controllers on one IC, for PDAs and organizers	++
5 to 16 CELL (30V) INPUTS									
MAX781	5 to 18	3.3 at 10mA 5.0 at 25mA	3.3, 14, battery charger	Battery charger, current source, dual Vpp outputs	100 shutdown, 750 standby, 2mA operating	36-SSOP	C, E	Yes High-power controller to 50W or more, dual PCMCIA Vpp outputs, analog mux, SPI interface	8.80
MAX782	5.5 to 30	3.3 at 5mA 5 at 25mA	3.3‡, 5, 14	Dual Vpp outputs	70 standby, 750 per output enabled	36-SSOP	C, E	Yes High-power dual controller to 50W or more, dual PCMCIA Vpp outputs, three precision voltage monitors	5.95
MAX783	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3‡, 5, 14	Dual Vpp outputs	70 standby, 750 per output enabled	36-SSOP	C, E	Yes High-power dual controller to 50W or more, dual PCMCIA Vpp outputs, three precision voltage monitors, optimized for 6-cell operation	5.95
MAX786	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3‡, 5	-	40 shutdown, 70 standby, 750 per output enabled	28-SSOP	C, E	Yes High-power dual controller to 50W or more, two precision voltage monitors	4.15

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

‡ Or 3.45V ("R" version), 3.6V ("S" version)

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

++ Future product—contact factory for pricing and availability. Specifications are preliminary.

LCD & CCFL Display Power Supplies

Part Number	Input Voltage Range (V)	DC-DC Output Voltages (V)	Quiescent Supply Current (μ A typ)	Pins- Package Options*	EV Kit	Features	Price† 1000-up (\$)
MAX1044	1.5 to 10	-V _{IN} or 2 x V _{IN}	30	8-DIP, 8-SO	Yes	No inductors, 60kHz boost pin, pager LCD supply	1.19
MAX1610	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital adjust, open and shorted lamp protection	††
MAX1611	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital SMBus adjust, open and shorted lamp protection	††
MAX1620	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP	Yes	Digital adjust, 32 levels	††
MAX1621	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP	Yes	SMBus adjust, 32 levels	††
MAX1622	4.5 to 24	Positive or negative LCD, configurable	500	8- μ MAX	Yes	Analog adjust	††
MAX1771	2 to 16.5	Positive LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5 μ A shutdown	1.80
MAX749	2 to 6	Negative LCD	60	8-DIP, 8-SO	Yes	Digital LCD adjustment	2.49
MAX753	6 to 24	CCFL drive, configurable; negative LCD, configurable	100	16-DIP, 16-NSO	Yes	Digital CCFT and LCD adjustment	4.45
MAX754	6 to 24	CCFL drive, configurable; positive LCD, configurable	100	16-DIP, 16-NSO	Yes	Digital CCFT and LCD adjustment	4.45
MAX759	4 to 15	Negative LCD, adjustable	1.2mA	14-DIP, 16-WSO	Yes	Internal MOSFET	2.75
MAX774/775/776	3 to 16.5	Negative LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5 μ A shutdown	2.20
MAX860/861	1.5 to 5.5	-V _{IN} or 2 x V _{IN}	180	8-SO, 8- μ MAX		No inductors, up to 250kHz oscillator, 2.2 μ F caps, smallest pager LCD supply	1.45
ICL7660	1.5 to 10	-V _{IN} or 2 x V _{IN}	110	8-DIP, 8-SO, 8- μ MAX		No inductors, low-cost pager LCD supply, μ MAX package	1.09

MOSFET Drivers

Part Number	Output Resistance (Ω)	Rise/Fall, T _A = +25°C (ns max)	Rise/Fall, Over Temp. (ns max)	Peak Output Current (A)	Supply Voltage (V)	Pins- Package Options*	Temp. Ranges**	Features	Price† 1000-up (\$)
MAX4420/4429	2.5(1.5)	30/30(2500pF)	60/60(2500pF)	6	4.5 to 18	8-DIP, 8-SO	C.E.M	Single noninverting/single inverting	1.71
MAX4426/4427/4428	10(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 18	8-DIP, 8-SO	C.E.M	Dual inverting/dual noninverting/dual mixed	1.61
MAX4626/627/628	15(4)	30/30(1000pF)	40/40(1000pF)	2	4.5 to 18	8-DIP, 8-SO	C.E.M	Dual inverting/dual noninverting/dual mixed	1.49
ICL7667	12(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 15	8-DIP, 8-SO	C.E.M	Dual inverting	1.12
TSC426/427/428	15(6)	30/30(1000pF)	60/40(1000pF)	1.5	4.5 to 18	8-DIP, 8-SO	C.E.M	Dual inverting/dual noninverting/dual mixed	1.06

Miscellaneous Power Supplies

Part Number	Description	Pins- Package Options*	Temp. Range**	EV Kit	Features	Price† 1000-up (\$)
MAX845	Isolated transformer driver	8-SO, 8- μ MAX	E	Yes	750mW output thin transformer, fits PCMCIA cards	1.55

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/95

MAXIM

Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

General Description

The MAX1600 DC power-switching IC contains a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two Cardbus or PCMCIA host sockets. Key features include very low-resistance switches, small packaging, soft-switching action, and compliance with PCMCIA specifications for 3V/5V switching. 3.3V-only power switching for fast, 32-bit Cardbus applications is supported in two ways: stiff, low-resistance 3.3V switches allow high 3.3V load currents (up to 1A); and completely independent internal charge pumps let the 3.3V switch operate normally, even if the 5V and 12V supplies are disconnected or turned off in order to conserve power. The internal charge pumps are regulating types that draw reduced input current when the VCC switches are static. Also, power consumption is automatically reduced to 10µA when the control logic inputs are programmed to high-Z or GND states, unlike other solutions that may require a separate shutdown control input.

Other key features include guaranteed specifications for output current limiting level, and guaranteed specifications for output rise/fall times (in compliance with PCMCIA specifications). Reliability is enhanced by thermal overload protection, accurate current limiting, overcurrent fault flag output, undervoltage lockout, and extra ESD protection at the VCC/VPP outputs. The CMOS/TTL-logic interface is flexible, and works properly with logic input levels in excess of the positive supply rail.

The MAX1600 fits two complete Cardbus/PCMCIA switches into a space-saving, narrow (0.2", 5mm wide) shrink small-outline package.

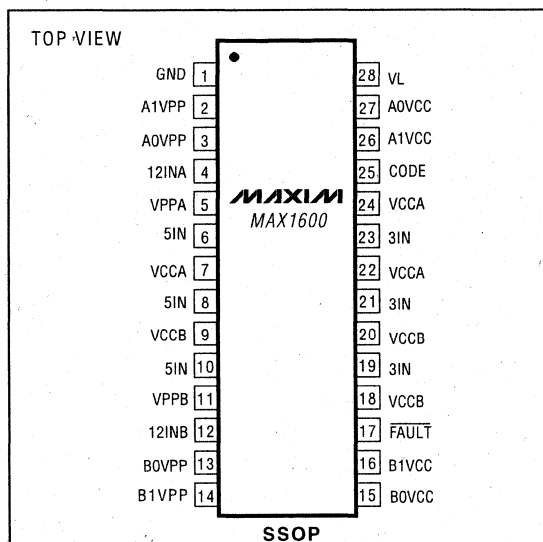
Features

- ◆ Supports Two PCMCIA/Cardbus Sockets
- ◆ 1A, 0.08Ω Max 3.3V VCC Switch
- ◆ 1A, 0.14Ω Max 5V VCC Switch
- ◆ Soft Switching for Low Inrush Surge Current
- ◆ Overcurrent Protection
- ◆ Overcurrent/Thermal Fault Flag Output
- ◆ Thermal Shutdown at $T_J = 150^{\circ}\text{C}$
- ◆ Independent Internal Charge Pumps
- ◆ Break-Before-Make Switching Action
- ◆ 10µA Max Standby Supply Current
- ◆ 5V and 12V Not Required for Low-RDS(ON) 3.3V Switching
- ◆ Complies with PCMCIA 3V/5V Switching Specifications
- ◆ Super-Small 28-Pin SSOP Package (0.2" or 5mm wide)
- ◆ Code Compatible with:
 - Cirrus CL-PD67XX Family
 - Databook DB86184
 - Intel 82365SL (industry-standard coding for most PCMCIA controller ICs)

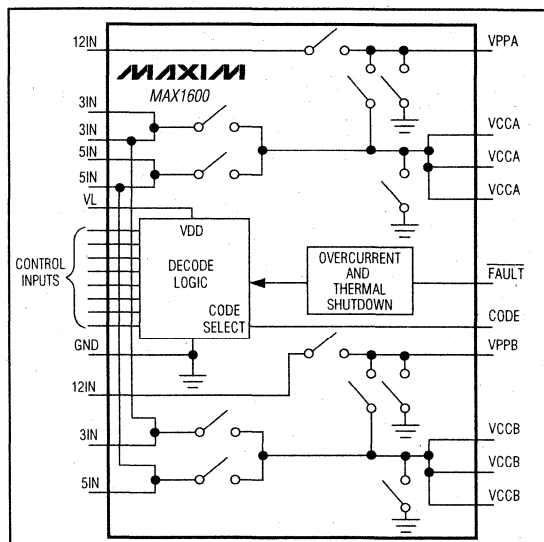
Applications

Desktop Computers	Data Loggers
Notebook Computers	Digital Cameras
Docking Stations	Printers
Handy-Terminals	PCMCIA Read/Write Drives

Pin Configuration



Simplified Block Diagram



MAXIM

Maxim Integrated Products 4-11

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MAX1600

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Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

ABSOLUTE MAXIMUM RATINGS

Inputs/Outputs to GND (VL, 3IN, 5IN, VCCA, VCCB) (Note 1)	-0.3V, +6V
VPP Inputs/Outputs to GND (12INA, 12INB, VPPA, VPPB) (Note 1)	-0.3V, +15V
Logic Inputs to GND (A0VCC, A1VCC, B0VCC, B1VCC, A0VPP, A1VPP, B0VPP, B1VPP) (Note 1)	-0.3V, +6V
CODE Input to GND	-0.3V, (VL + 0.3V)
VCCA, VCCB Output Current (Note 2)	2A
VPPA, VPPB Output Current (Note 2)	250mA
VCCA, VCCB Short Circuit to GND	Continuous
VPPA, VPPB Short Circuit to GND	Continuous
ESD Protection (VCC/VPP outputs)	4000V Minimum
ESD Protection (other pins)	2000V Minimum
Continuous Power Dissipation (T _A = +70°C)	
SSOP (derate 9.52mW/°C above +70°C)	762mW
Operating Temperature Ranges	
MAX1600CAI	0°C to +70°C
MAX1600EAI	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: There are no parasitic diodes between any of these pins, so there are no power-up sequencing restrictions (for example, logic input signals can be applied even if all of the supply voltage inputs are grounded).

Note 2: VCC and VPP outputs are internally current-limited to safe values. See the *Electrical Characteristics* table.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VL = 3IN = 3.3V, 5IN = 5V, 12INA = 12INB = 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION					
Input Voltage Range	3IN, 5IN or VL	3		5.5	V
	12INA, 12INB	11		13	
Undervoltage Lockout Threshold	Falling edge, hysteresis = 1%, 3IN or 5IN	2.3	2.5	2.8	V
Standby Supply Current	3IN or 5IN, all switches 0V or high-Z, control inputs = 0V or VL	T _A = +25°C	1	10	μA
		T _A = T _{MIN} to T _{MAX}	1	20	
3IN Quiescent Supply Current	Any combination of 3IN switches on, control inputs = 0V or VL, no VCC loads		30	200	μA
5IN Quiescent Supply Current	Any combination of 5IN switches on, control inputs = 0V or high-Z, no VCC loads		35	200	μA
12IN ₋ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL	T _A = +25°C	1	10	μA
		T _A = T _{MIN} to T _{MAX}		20	
12IN ₋ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads		15	100	μA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL		3.8	10	μA
VL Quiescent Supply Current	Any combination of switches on		25	300	μA
VL Fall Rate	When using VL as shutdown pin	0.25			V/sec
VCC SWITCHES					
Operating Output Current Range	VCCA or VCCB, 3IN = 5IN = 3V to 5.5V	0		1	A
On-Resistance, 3V Switches	3IN = VL = 3V, I _{SWITCH} = 1A, T _A = +25°C		0.06	0.08	Ω
On-Resistance, 5V Switches	5IN = 4.5V, 3IN = 3V to 3.6V, I _{SWITCH} = 1A, T _A = +25°C		0.10	0.14	Ω
Output Current Limit	VCCA or VCCB	1.5		3	A
Output Sink Current	VCCA or VCCB < 0.4V, programmed to 0V state	20			mA
Output Leakage Current	VCCA or VCCB forced to 0V, high-Z state			10	μA

Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

ELECTRICAL CHARACTERISTICS (continued)

(VL = 3IN = 3.3V, 5IN = 5V, 12INA = 12INB = 12V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Propagation Delay Plus Rise Time	VCCA or VCCB, 0V to 3IN or 5IN, CL = 30μF, RL = 25Ω, 50% of input to 90% of output (Note 3)			10	ms
Output Rise Time	VCCA or VCCB, 0V to 3IN or 5IN, CL = 1μF, RL = open circuit, 10% to 90% points (Note 3)	100			μs
Output Propagation Delay Plus Fall Time	VCCA or VCCB, 3IN or 5IN to 0V, CL = 30μF, RL = open circuit, 50% of input to 10% of output (Note 3)			60	ms
Output Fall Time	VCCA or VCCB, 3IN or 5IN to 0V, CL = 1μF, RL = 25Ω, 90% to 10% points (Note 3)	3			ms
VPP SWITCHES					
Operating Output Current Range	VPPA or VPPB	0		120	mA
On-Resistance, 12V Switches	12IN = 11.6V, ISWITCH = 100mA, TA = +25°C		0.65	1	Ω
On-Resistance, VPP = VCC Switches	Programmed to 5IN (5V) or 3IN (3.3V)		1	3	Ω
Output Current Limit	VPPA or VPPB	130	200	260	mA
Output Sink Current	VPPA or VPPB < 0.4V, programmed to 0V state	10			mA
Output Leakage Current	VPPA or VPPB forced to 0V, high-Z state			10	μA
Output Propagation Delay Plus Rise Time	VPPA or VPPB, 0V to 12IN, CL = 0.1μF, 50% of input to 90% of output (Note 3)			30	ms
Output Rise Time	VPPA or VPPB, 0V to 12IN, CL = 0.1μF, 10% to 90% points (Note 3)	1			ms
Output Propagation Delay Plus Fall Time	VPPA or VPPB, 12IN to 0V, CL = 0.1μF, 50% of input to 10% of output (Note 3)			60	ms
Output Fall Time	VPPA or VPPB, 12IN to 0V, CL = 0.1μF, 90% to 10% points (Note 3)	1			ms
INTERFACE AND LOGIC SECTION					
FAULT Signal Propagation Delay	VCC_ or VPP_, load step to FAULT output, 50% point to 50% point (Note 4)			2	μs
FAULT Output Low Voltage	ISINK = 1mA, low state			0.4	V
FAULT Output Leakage Current	VFAULT = 5.5V, high state	-0.5		0.5	μA
Thermal Shutdown Threshold	Hysteresis = 20°C		150		°C
Logic Input Low Voltage	__VCC, __VPP			0.6	V
Logic Input High Voltage	__VCC, __VPP	1.5			V
Code Input Low Voltage	"Cirrus" code	0		0.4	V
Code Input High Voltage	"Intel" code	VL - 0.4		VL	V
Code Input Mid-Level Voltage	"Databook" code	1.2		VL - 1.2	V
Logic Input Bias Current	__VCC, __VPP, code	-1		1	μA

Note 3: VCC/VPP timing specifications are 100% tested.

Note 4: Design target value, not production tested.

Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2, 3	A1VPP, A0VPP	VPP Control Inputs, channel A. See <i>Logic Truth Tables</i> .
4	12INA	12V Supply Voltage Input, internally connects to channel A VPP switch. Tie to VPPA if not used.
5	VPPA	0V/VCC/12V/high-Z VPP Output (channel A). Bypass to GND with 0.01 μ F for ESD protection.
6, 8, 10	5IN	5V Supply Voltage Inputs. 5IN pins must be connected together. Input range is 3V to 5.5V.
7, 22, 24	VCCA	0V/3.3V/5V/high-Z VCC Output (channel A). Bypass to GND with 0.01 μ F for ESD protection.
9, 18, 20	VCCB	0V/3.3V/5V/high-Z VCC Output (channel B). Bypass to GND with 0.01 μ F for ESD protection.
11	VPPB	0V/VCC/12V/high-Z VPP Output (channel B). Bypass to GND with 0.01 μ F for ESD protection.
12	12INB	12V Supply Voltage Input, internally connects to channel B VPP switch. Tie to VPPB if not used.
13, 14	B0VPP, B1VPP	VPP Control Inputs, channel B. See <i>Logic Truth Tables</i> .
15, 16	B0VCC, B1VCC	VCC Control Inputs, channel B. See <i>Logic Truth Tables</i> .
17	FAULT	Fault-Detection Output. FAULT goes low if either channel VCC or VPP switch is current limiting or if the thermal protection circuit is activated. FAULT is an open-drain output that requires an external pull-up resistor.
19, 21, 23	3IN	3.3V Supply Voltage Inputs. 3IN pins must be connected together. Input range is 3V to 5.5V.
25	CODE	Three-Level Code-Select Input. Reconfigures the logic decoder to one of three different code formats. See <i>Logic Truth Tables</i> . An additional 1 μ A (3 μ A max) of VL supply current will flow if CODE = mid-supply (VL/2). Low = Standard code (82365SL) High = "Cirrus" code Mid-supply = "Databook" code (tie CODE to a 1M Ω + 1M Ω resistor divider between VL and GND for "Databook" coding).
26, 27	A1VCC, A0VCC	VCC Control Inputs, channel A. See <i>Logic Truth Tables</i> .
28	VL	Logic Supply Voltage Input, usually connected to the 3.3V host system supply. Input range is 3V to 5.5V. If VL is disconnected or grounded, the device will enter standby mode. VL can be supplied via the output of a CMOS-logic gate, in order to produce an overriding shutdown. When being used as a shutdown input, VL should have an additional 0.01 μ F bypass capacitor to GND.

Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

Logic Truth Tables

**Table 1. "Standard" Code (82365SL),
CODE = GND**

_1VCC	_0VCC	_1VPP	_0VPP	VCC_	VPP_	MODE
0	0	0	0	GND	GND	STBY
0	0	0	1	GND	GND	STBY
0	0	1	0	GND	GND	STBY
0	0	1	1	GND	GND	STBY
0	1	0	0	3IN	GND	—
0	1	0	1	3IN	VCC_	—
0	1	1	0	3IN	12IN	—
0	1	1	1	3IN	High-Z	—
1	0	0	0	5IN	GND	—
1	0	0	1	5IN	VCC_	—
1	0	1	0	5IN	12IN	—
1	0	1	1	5IN	High-Z	—
1	1	0	0	3IN	GND	—
1	1	0	1	3IN	VCC_	—
1	1	1	0	3IN	12IN	—
1	1	1	1	3IN	High-Z	—

STBY = Standby Mode

**Table 2. "Cirrus" Code,
CODE = High (VL)**

_1VCC	_0VCC	_1VPP	_0VPP	VCC_	VPP_	MODE
0	0	0	0	High-Z	High-Z	STBY
0	0	0	1	High-Z	High-Z	STBY
0	0	1	0	High-Z	High-Z	STBY
0	0	1	1	High-Z	High-Z	STBY
0	1	0	0	5IN	GND	—
0	1	0	1	5IN	VCC_	—
0	1	1	0	5IN	12IN	—
0	1	1	1	5IN	High-Z	—
1	0	0	0	3IN	GND	—
1	0	0	1	3IN	VCC_	—
1	0	1	0	3IN	12IN	—
1	0	1	1	3IN	High-Z	—
1	1	0	0	GND	GND	STBY
1	1	0	1	GND	GND	STBY
1	1	1	0	GND	GND	STBY
1	1	1	1	GND	GND	STBY

STBY = Standby Mode

**Table 3. "Databook" Code,
CODE = Mid-Supply (VL/2)**

_1VCC	_0VCC	_1VPP	_0VPP	VCC_	VPP_	MODE
0	0	0	X	GND	High-Z	STBY
0	0	1	X	3IN	12IN	—
0	1	0	X	GND	GND	STBY
0	1	1	X	5IN	12IN	—
1	0	0	X	3IN	VCC_	—
1	0	1	X	3IN	GND	—
1	1	0	X	5IN	VCC_	—
1	1	1	X	5IN	GND	—

STBY = Standby Mode

Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

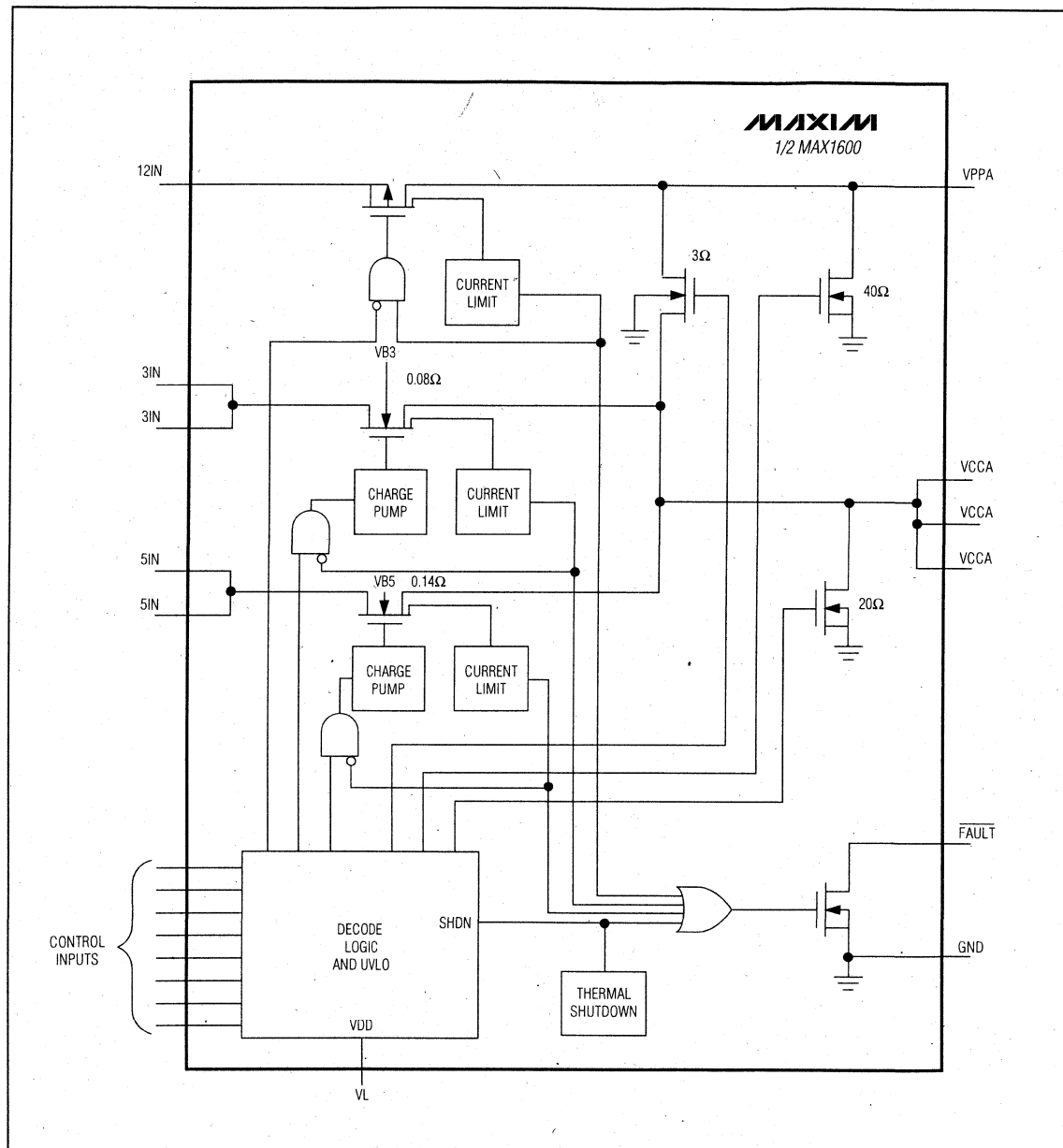


Figure 1. Detailed Block Diagram (one channel of two)

Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

MAX1600

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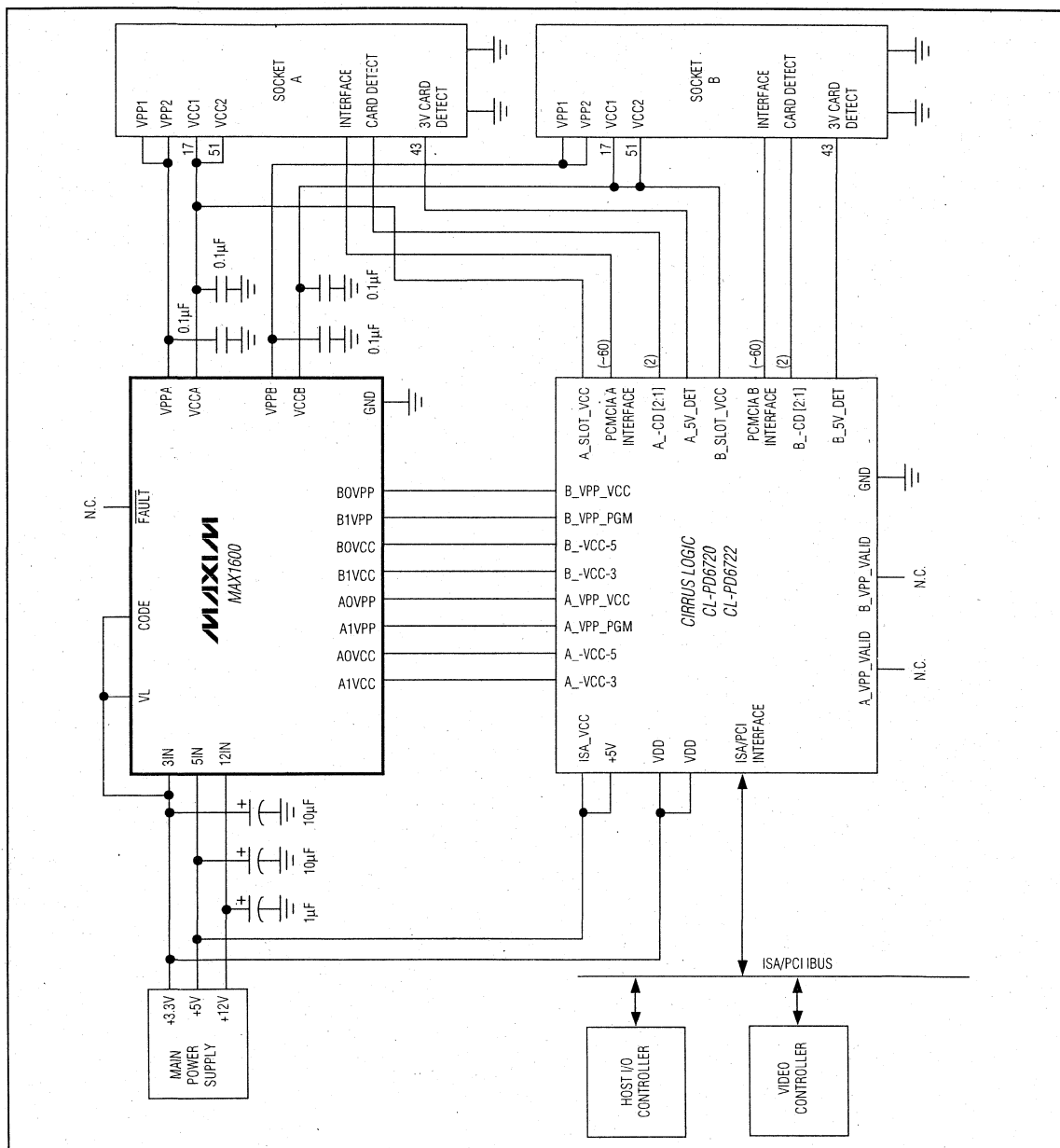


Figure 2. Application with Cirrus Logic Interface

Dual-Channel Cardbus and PCMCIA VCC/VPP Power-Switching Network

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1600CAI	0°C to +70°C	28 SSOP
MAX1600C/D	0°C to +70°C	Dice*
MAX1600EAI	-40°C to +85°C	28 SSOP

* Contact factory for dice specifications.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/95

MAXIM

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

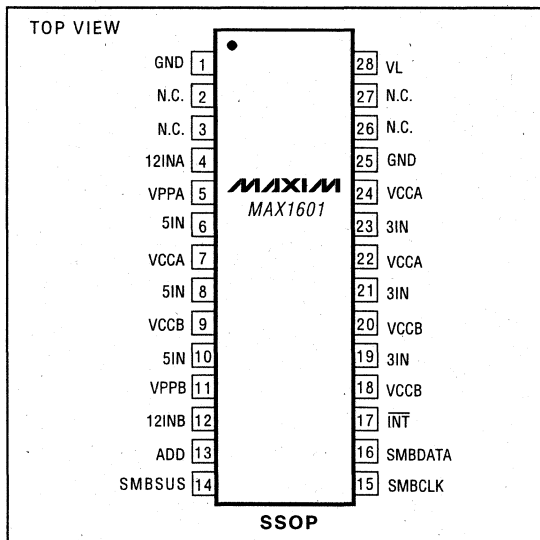
General Description

The MAX1601 DC power-switching IC contains a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two Cardbus or PCMCIA host sockets. Key features include very low-resistance switches, small packaging, soft-switching action, and compliance with PCMCIA specifications for 3V/5V switching. 3.3V-only power switching for fast, 32-bit Cardbus applications is supported in two ways: stiff, low-resistance 3.3V switches allow high 3.3V load currents (up to 1A); and completely independent internal charge pumps let the 3.3V switch operate normally, even if the 5V and 12V supplies are disconnected or turned off in order to conserve power. The internal charge pumps are regulating types that draw reduced input current when the VCC switches are static. Also, power consumption is automatically reduced to 10µA when the switches are programmed to high-Z or GND states over the serial interface, unlike other solutions that may require a separate shutdown control input.

Other key features include guaranteed specifications for output current limiting level, and guaranteed specifications for output rise/fall times (in compliance with PCMCIA specifications). Reliability is enhanced by thermal overload protection, accurate current limiting, overcurrent fault flag output, undervoltage lockout, and extra ESD protection at the VCC/VPP outputs. The SMBus serial interface is flexible, and can tolerate logic input levels in excess of the positive supply rail.

The MAX1601 fits two complete Cardbus/PCMCIA switches into a space-saving, narrow (0.2", 5mm wide) shrink small-outline package.

Pin Configuration



SMBus is a trademark of Intel Corp.

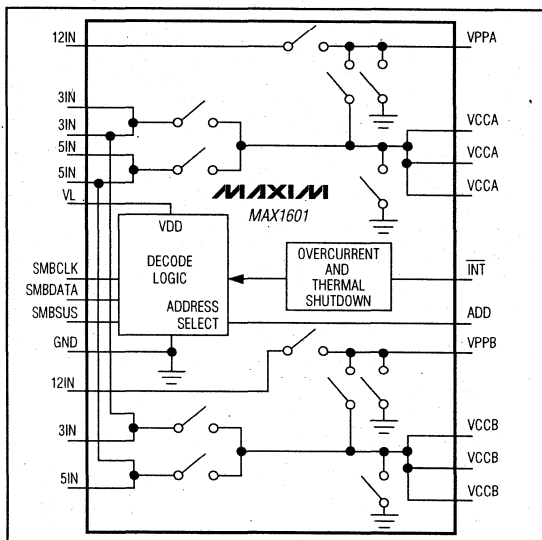
Features

- ♦ Supports Two PCMCIA/Cardbus Sockets
- ♦ 1A, 0.08Ω Max 3.3V VCC Switch
- ♦ 1A, 0.14Ω Max 5V VCC Switch
- ♦ Soft Switching for Low Inrush Surge Current
- ♦ Overcurrent Protection
- ♦ Overcurrent/Thermal Fault Flag Output
- ♦ Thermal Shutdown at $T_J = 150^{\circ}\text{C}$
- ♦ Independent Internal Charge Pumps
- ♦ Break-Before-Make Switching Action
- ♦ 10µA Max Standby Supply Current
- ♦ 5V and 12V Not Required for Low- $R_{DS(ON)}$ 3.3V Switching
- ♦ Complies with PCMCIA 3V/5V Switching Specifications
- ♦ Super-Small 28-Pin SSOP Package (0.2" or 5mm wide)
- ♦ System Management Bus (SMBus) Serial Interface

Applications

Desktop Computers	Data Loggers
Notebook Computers	Digital Cameras
Docking Stations	Printers
Handy-Terminals	PCMCIA Read/Write Drives

Simplified Block Diagram



MAX1601

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MAXIM

Maxim Integrated Products 4-19

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Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

ABSOLUTE MAXIMUM RATINGS

Inputs/Outputs to GND
(VL, 3IN, 5IN, VCCA, VCCB) (Note 1) -0.3V, +6V
VPP Inputs/Outputs to GND
(12INA, 12INB, VPPA, VPPB) (Note 1) -0.3V, +15V
Inputs and Outputs to GND (SMBCLK, SMBDATA,
SMBSUS, INT) (Note 1) -0.3V, +6V
ADD Input to GND -0.3V, (VL + 0.3V)
VCCA, VCCB Output Current (Note 2) 2A
VPPA, VPPB Output Current (Note 2) 250mA
VCCA, VCCB Short Circuit to GND Continuous

VPPA, VPPB Short Circuit to GND Continuous
ESD Protection (VCC/VPP outputs) 4000V Minimum
ESD Protection (other pins) 2000V Minimum
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX1600CAI 0°C to +70°C
MAX1600EAI -40°C to +85°C
Storage Temperature Range -65°C to +160°C
Lead Temperature (soldering, 10sec) +300°C

Note 1: There are no parasitic diodes between any of these pins, so there are no power-up sequencing restrictions (for example, logic input signals can be applied even if all of the supply voltage inputs are grounded).

Note 2: VCC and VPP outputs are internally current-limited to safe values. See the *Electrical Characteristics* table.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VL = 3IN = 3.3V, 5IN = 5V, 12INA = 12INB = 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION						
Input Voltage Range	3IN, 5IN or VL		3		5.5	V
	12INA, 12INB		11		13	
Undervoltage Lockout Threshold	Falling edge, hysteresis = 1%, 3IN or 5IN			2.5	2.8	V
Standby Supply Current	3IN or 5IN, all switches 0V or high-Z, control inputs = 0V or VL	T _A = +25°C		1	10	μA
		T _A = T _{MIN} to T _{MAX}		1	20	
3IN Quiescent Supply Current	Any combination of 3IN switches on, control inputs = 0V or VL, no VCC loads			30	200	μA
5IN Quiescent Supply Current	Any combination of 5IN switches on, control inputs = 0V or high-Z, no VCC loads			35	200	μA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL	T _A = +25°C		1	10	μA
		T _A = T _{MIN} to T _{MAX}			20	
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads			15	100	μA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL			3.8	10	μA
VL Quiescent Supply Current	Any combination of switches on			25	300	μA
VL Fall Rate	When using VL as shutdown pin		0.25			V/seq
VCC SWITCHES						
Operating Output Current Range	VCCA or VCCB, 3IN = 5IN = 3V to 5.5V		0		1	A
On-Resistance, 3V Switches	3IN = VL = 3V, I _{SWITCH} = 1A, T _A = +25°C			0.06	0.08	Ω
On-Resistance, 5V Switches	5IN = 4.5V, 3IN = 3V to 3.6V, I _{SWITCH} = 1A, T _A = +25°C			0.10	0.14	Ω
Output Current Limit	VCCA or VCCB		1.5		3	A
Output Sink Current	VCCA or VCCB < 0.4V, programmed to 0V state		20			mA

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

(VL = 3IN = 3.3V, 5IN = 5V, 12IN_A = 12IN_B = 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Current	VCCA or VCCB forced to 0V, high-Z state			10	μA
Output Propagation Delay Plus Rise Time	VCCA or VCCB, 0V to 3IN or 5IN, C _L = 30μF, R _L = 25Ω, 50% of input to 90% of output (Note 3)			10	ms
Output Rise Time	VCCA or VCCB, 0V to 3IN or 5IN, C _L = 1μF, R _L = open circuit, 10% to 90% points (Note 3)	100			μs
Output Propagation Delay Plus Fall Time	VCCA or VCCB, 3IN or 5IN to 0V, C _L = 30μF, R _L = open circuit, 50% of input to 10% of output (Note 3)			60	ms
Output Fall Time	VCCA or VCCB, 3IN or 5IN to 0V, C _L = 1μF, R _L = 25Ω, 90% to 10% points (Note 3)	3			ms
VPP SWITCHES					
Operating Output Current Range	VPPA or VPPB	0		120	mA
On-Resistance, 12V Switches	12IN = 11.6V, I _{SWITCH} = 100mA, T _A = +25°C		0.65	1	Ω
On-Resistance, VPP = VCC Switches	Programmed to 5IN (5V) or 3IN (3.3V)		1	3	Ω
Output Current Limit	VPPA or VPPB	130	200	260	mA
Output Sink Current	VPPA or VPPB < 0.4V, programmed to 0V state	10			mA
Output Leakage Current	VPPA or VPPB forced to 0V, high-Z state			10	μA
Output Propagation Delay Plus Rise Time	VPPA or VPPB, 0V to 12IN _A , C _L = 0.1μF, 50% of input to 90% of output (Note 3)			30	ms
Output Rise Time	VPPA or VPPB, 0V to 12IN _A , C _L = 0.1μF, 10% to 90% points (Note 3)	1			ms
Output Propagation Delay Plus Fall Time	VPPA or VPPB, 12IN _A to 0V, C _L = 0.1μF, 50% of input to 10% of output (Note 3)			60	ms
Output Fall Time	VPPA or VPPB, 12IN _A to 0V, C _L = 0.1μF, 90% to 10% points (Note 3)	1			ms
INTERFACE AND LOGIC SECTION					
INT Signal Propagation Delay	VCC _A or VPP _A , load step to INT output, 50% point to 50% point (Note 4)	0		10	μs
INT Output Low Voltage	I _{SINK} = 1mA, low state			0.4	V
INT Output Leakage Current	V _{INT} = 5.5V, high state	-0.1		0.1	μA
Thermal Shutdown Threshold	Hysteresis = 20°C		150		°C
Logic Input Low Voltage	SMBSUS, SMBCLK, SMBDATA, VL = 3V to 5.5V			0.6	V
Logic Input High Voltage	SMBSUS, SMBCLK, SMBDATA	VL = 3V to 3.6V		1.4	V
		VL = 3V to 5.5V		2.3	V
Logic Output Low Voltage	SMBDATA, I _{SINK} = 4mA			0.4	V

MAX1601

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Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

(VL = 3IN = 3.3V, 5IN = 5V, 12INA = 12INB = 12V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMB Input Capacitance	SMBSUS, SMBCLK, SMBDATA		5		pF
SMBCLK Clock Frequency	SMBus spec = 10kHz min	DC		100	kHz
SMBCLK Clock Low Time	TLOW 10% to 10% points	4.7			μs
SMBCLK Clock High Time	THIGH 90% to 90% points	4			μs
SMB Rise Time	SMBCLK, SMBDATA 10% to 90%			1	μs
SMB Fall Time	SMBCLK, SMBDATA 90% to 10%			300	ns
SMB Repeated Start-Condition Setup Time	TSU:STA 90% to 90% points	250			ns
SMB Start-Condition Hold Time	THD:STA 10% of SMBDATA to 90% of SMBCLK	4			μs
SMB Stop-Condition Setup Time	TSU:STO 90% of SMBCLK to 10% of SMBDATA	4			μs
SMB Data Valid to SMBCLK Rising-Edge Time	TSU:DAT 10% or 90% of SMBDATA to 10% of SMBCLK	250			ns
SMB Data Hold Time	THD:DAT (Note 5)	0			ns
Bus Free Time	TBUF between start and stop conditions	4.7			μs
ADD Input Low Voltage				0.6	V
ADD Input High Voltage		1.5			V
Logic Input Bias Current	ADD, SMBSUS, SMBCLK, SMBDATA	-1		1	μA
SCL Fall to SDA Valid (Master Clocking-In Data)				1000	ns
Start-Condition Setup		4.7			μs

Note 3: VCC/VPP timing specifications are 100% tested.

Note 4: Design target value, not production tested.

Note 5: Note that a transition must internally provide at least a hold time in order to bridge the undefined region (300ns max) of the falling edge of SMBCLK.

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2, 3, 26, 27	N.C.	No internal connection
4	12INA	12V Supply Voltage Input, internally connects to channel A VPP switch. Tie to VPPA if not used.
5	VPPA	0V/VCC/12V/High-Z VPP Output (channel A). Bypass to GND with 0.01μF for ESD protection.
6	5IN	5V Supply Voltage Input. Must be connected to other 5IN pins. Input range is 3V to 5.5V.
7, 22, 24	VCCA	0V/3.3V/5V/High-Z VCC Output (channel A). Bypass to GND with 0.01μF for ESD protection.
8, 10	5IN	5V Supply Voltage Input
9, 18, 20	VCCB	0V/3.3V/5V/High-Z VCC Output (channel B). Bypass to GND with 0.01μF for ESD protection.
11	VPPB	0V/VCC/12V/High-Z VPP Output (channel B). Bypass to GND with 0.01μF for ESD protection.
12	12INB	12V Supply Voltage Input, internally connects to channel B VPP switch. Tie to VPPB if not used.
13	ADD	Address Input, sets SMBus address location.
14	SMBSUS	SMBus Suspend-Mode Control Input. The device will execute commands previously stored in the normal-mode register if SMBSUS is high, or will execute commands previously stored in the suspend-mode register if SMBSUS is low.
15	SMBCLK	SMBus Clock Input
16	SMBDATA	SMBus Data Input/Output, open drain
17	INT	Fault-Detection Interrupt Output. INT goes low if either channel VCC or VPP switch is current limiting or if the thermal protection circuit is activated. INT is an open-drain output that requires an external pull-up resistor.
19	3IN	3.3V Supply Voltage Input. Must be connected to other 3IN pins. Input range is 3V to 5.5V.
21, 23	3IN	3.3V Supply Voltage Input
25	GND	Test-Mode Input, normally grounded
28	VL	Logic Supply Voltage Input, usually connected to the 3.3V host system supply. Input range is 3V to 5.5V. If VL is disconnected or grounded, the device will enter standby mode. VL can be supplied via the output of a CMOS-logic gate, in order to produce an overriding shutdown. When being used as a shutdown input, VL should have an additional 0.01μF bypass capacitor to GND. If VL is cycled, a power-on reset occurs, which resets all of the SMBus data registers.

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Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

SMBus Interface Operation

The SMBus serial interface is a two-wire interface with multi-mastering capability, intended to control low-speed peripheral devices in low-power portable equipment applications. SMBus is similar to I²C™ and AccessBus, but has slightly different logic threshold voltage levels (intended to accommodate future low-voltage systems that might have 2V VCC levels, for example), different fixed addresses, and a suspend-mode register capability. To obtain a complete set of specifications on the SMBus interface, call Intel at (800) 253-3696 and ask for product code SBS5220.

SMBus Addressing

These dual-channel PCMCIA switch devices respond to two of four different addresses, depending on the state of the ADD address pin. Normal writing to the device is done by transmitting one of four addresses, followed by a single data byte, to program the channel selected. Write transmissions to the interrupt pointer address are

not supported by these devices. Reading from the device is done by transmitting one of two addresses corresponding to either the A channel address (which will provide data about faults for both A and B channels) or to the interrupt pointer address (discussed later).

The normal start condition consists of a high-to-low transition on SMBDATA while SMBCLK is high. The 7-bit address is followed by a bit that designates a read or write operation; high = read, low = write. If the 7-bit address matches one of the supported function addresses, the IC issues an acknowledge pulse by pulling the SMBDATA line low. If the address is not a valid one, the IC stays off of the bus and ignores any data on the bus until a new start condition is detected. Once the IC receives a valid address that includes a write bit, it expects to receive one additional byte of data. If a stop condition or new start condition is detected before a complete byte of data is clocked in, the IC interprets this as an error and all of the data is rejected and lost.

Table 1. SMBus Addressing

SMB Address	ADD Pin	Write Function	Read Function
0001100	Don't care	N/A	Interrupt Pointer
1010000	Grounded	Channel A	Channel A/B faults
1010001	Grounded	Channel B	Channel A/B faults
1010010	Tied to VL	Channel A	Channel A/B faults
1010011	Tied to VL	Channel B	Channel A/B faults

SMBus Write Operations

If the IC receives a valid address immediately followed by a write bit, the IC becomes a slave receiver. The slave IC generates a first acknowledge after the address and write bit, and a second acknowledge after the command byte. A stop condition following the command (data) byte causes the immediate execution of the command, unless the data included a low SUS/OP bit. If the data included a low SUS/OP bit, the command is stored in the suspend-mode register, and is executed only when the SMSUS pin is pulled low.

Table 2. Command Format for Channel A Write Operations (address 1010000 or 1010010)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: High = normal, Low = suspend.
6	VCCAON	0	Turns on VCCA when high, pulls VCCA to GND when low.
5	VCCA3/5	0	If VCCA is on, a high forces 3.3V output, and a low forces 5V output.
4	VCCAHiZ	0	Puts VCCA in a high-impedance state when high. Overrides VCCAON.
3	VPPAON	0	Turns on VPPA when high, pulls VPPA to GND when low.
2	VPPAPGM	0	If VPPA is on, a high forces VPPA to 12V, and a low forces VPPA to equal VCCA.
1	VPPAHiZ	0	Puts VPPA in a high-impedance state when high. Overrides VPPAON.
0 (LSB)	MASKFLT	0	Masks fault interrupts from both channel A and channel B when high.

I²C is a trademark of Philips Corp.

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

MAX1601

Table 3. Command Format for Channel B Write Operations (address 1010001 or 1010011)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: High = normal, Low = suspend.
6	VCCBON	0	Turns on VCCB when high, pulls VCCB to GND when low.
5	VCCB3/5	0	If VCCB is on, a high forces 3.3V output, and a low forces 5V output.
4	VCCBHIZ	0	Puts VCCB in a high-impedance state when high. Overrides VCCBON.
3	VPPBON	0	Turns on VPPB when high, pulls VPPB to GND when low.
2	VPPBPGM	0	If VPPA is on, a high forces VPPB to 12V, and a low forces VPPB to equal VCCB.
1	VPPAHIZ	0	Puts VPPA in a high-impedance state when high. Overrides VPPAON.
0 (LSB)	RFU	0	Reserved for future use.

Table 4. Read Format for Interrupt Pointer Address (0001100)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	ADD7	0	ADD7 to ADD1 provide a return address for any interrupt query. For these devices, the return addresses are: 1010000 = Channel A, ADD = low 1010001 = Channel B, ADD = low 1010010 = Channel A, ADD = high 1010011 = Channel B, ADD = high
6	ADD6	0	
5	ADD5	0	
4	ADD4	0	
3	ADD3	0	
2	ADD2	0	
1	ADD1	0	
0 (LSB)	ADD0	0	

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Table 5. Read Format for Power Switch Address (1010000 or 1010010)

BIT	NAME	POR STATE	LATCHED?	FUNCTION
7 (MSB)	CATFAULT	0	Y	Indicates catastrophic (thermal or undervoltage lockout) fault when high.
6	FAULT1	0	Y	Indicates VCCA overcurrent fault when high.
5	FAULT2	0	Y	Indicates VPPA overcurrent fault when high.
4	FAULT3	0	Y	Indicates VCCB overcurrent fault when high.
3	FAULT4	0	Y	Indicates VPPB overcurrent fault when high.
2	SIG/DUAL	0	N	Indicates dual part (single-channel devices would read 1)
1	RFU	0	N	Reserved for future use.
0 (LSB)	RFU	0	N	Reserved for future use.

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

SMBus Read Operations

If the IC receives a valid address that includes a read bit, the IC becomes a slave transmitter. After receiving the address data, the IC generates an acknowledge during the acknowledge clock pulse and drives the SMBDATA line in sync with SMBCLK. The SMB protocol requires that the master end the read transmission by not acknowledging during the acknowledge bit of SMBCLK. These PCMCIA ICs support the repeated start-condition method for changing data transfer direction; that is, a write transmission followed by a repeated start instead of a stop condition prepares the IC for data reading.

SMBus Interrupts

These PCMCIA power-switch ICs are slave devices only, and never initiate communications except by asserting an interrupt (by pulling $\overline{\text{INT}}$ low). Interrupts are generated only for reporting fault conditions, including overcurrent at VCCA, VCCB, VPPA, or VPPB, plus IC thermal overload. If an interrupt occurs, it can be an indication of impending system failure. The host system can react by going into suspend mode or taking other action, and come back later to interrogate the IC via the interrupt pointer to determine status or perform corrective action (such as disabling the appropriate power switch that might be connected to a shorted PC card). The fastest method for turning off the switches in response to a fault condition is to cycle the voltage on VL in order to generate a power-on reset (which clears all of the SMBus registers). Note that the SMBus registers retain their data even if the main VCC supplies are turned off, provided that VL is kept powered.

When a fault occurs, $\overline{\text{INT}}$ is immediately asserted and latched low. If the fault is momentary and disappears before the IC is serviced, the data is still latched in the interrupt pointer and $\overline{\text{INT}}$ remains asserted. Normally, the master (host system or PCMCIA digital controller) now sends out the interrupt pointer address (0011000) followed by a read bit. $\overline{\text{INT}}$ is cleared and the PCMCIA IC responds by putting out its address on the bus. If the fault persists, $\overline{\text{INT}}$ is re-asserted, but the data in the fault registers is not re-loaded. The data in the fault latches only reflects the first time $\overline{\text{INT}}$ is asserted.

Normally, the master now sends out the appropriate PCMCIA switch address on the bus, followed by a read bit. The data in the fault registers is then clocked out onto the bus (an action which also clears the fault registers). If the fault still persists, the fault bits and $\overline{\text{INT}}$ are latched again.

The interrupt pointer address provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. The host can read the interrupt pointer to determine which slave device generated an $\overline{\text{INT}}$ interrupt signal. The interrupt pointer address can activate several different slave devices simultaneously, similar to an I²C general call. Any slave device that generated an interrupt will attempt to identify itself by putting its own address on the bus during the first read byte. If more than one slave attempts to respond, bus arbitration rules apply and the device with the lower address code wins. The losing device won't generate an acknowledge and will continue to hold the $\overline{\text{INT}}$ line low until serviced, which implies that the host interrupt input must be level-sensitive.

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

MAX1601

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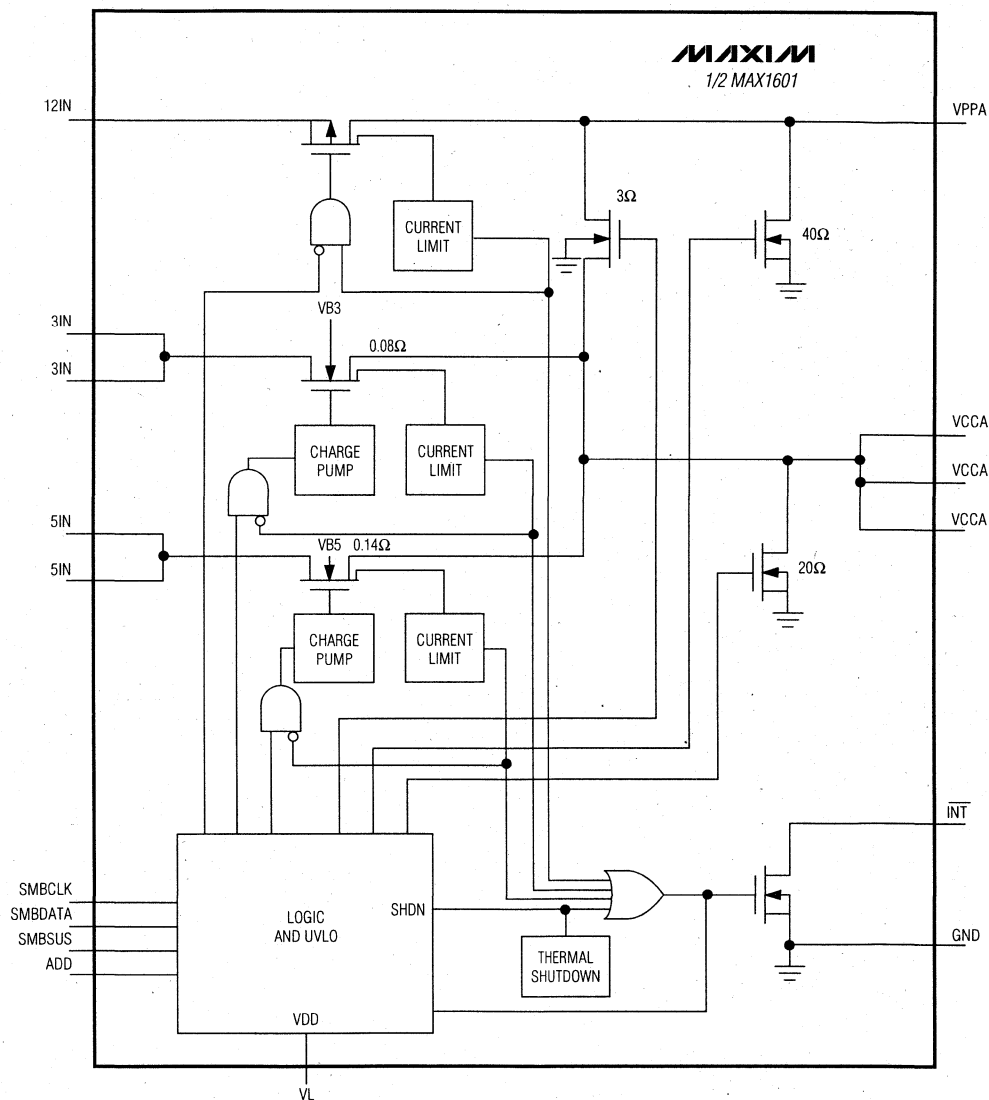


Figure 1. Detailed Block Diagram

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

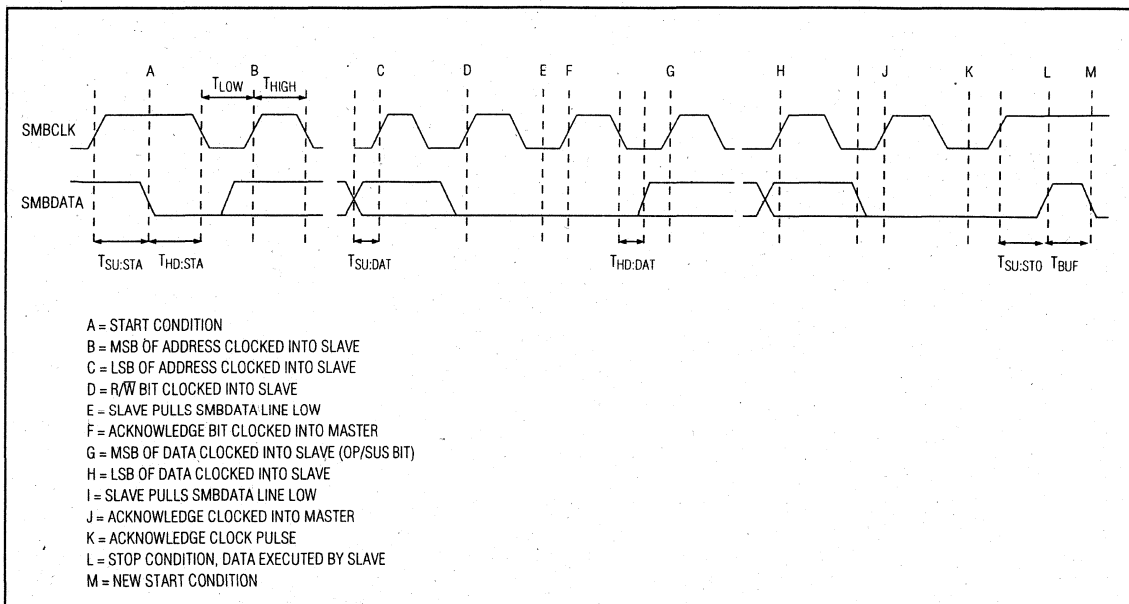


Figure 2. SMBus Write Timing Diagram

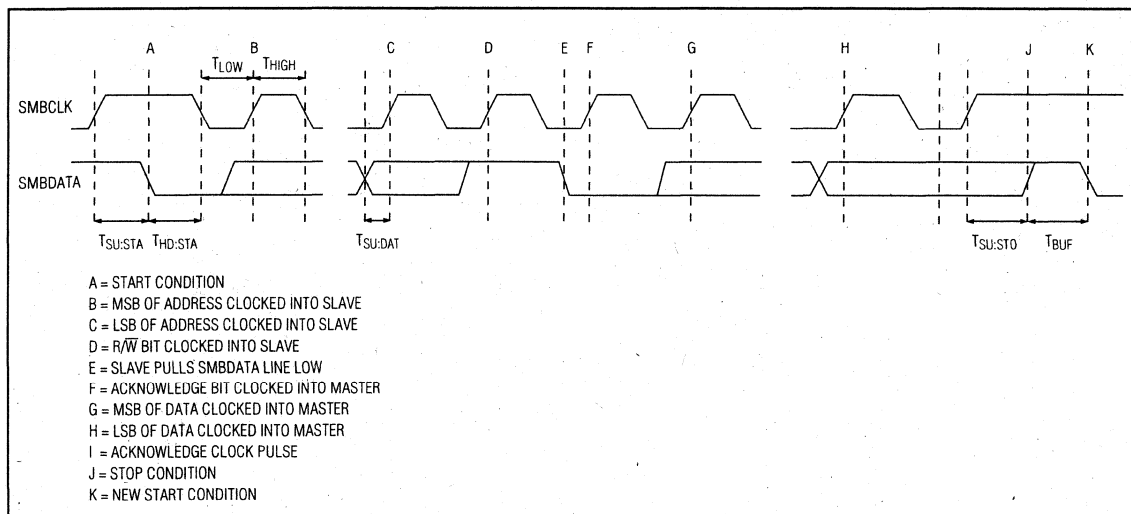


Figure 3. SMBus Read Timing Diagram

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1601CAI	0°C to +70°C	28 SSOP
MAX1601C/D	0°C to +70°C	Dice*
MAX1601EAI	-40°C to +85°C	28 SSOP

* Contact factory for dice specifications.

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ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Digitally Controlled CCFL Backlight Power Supplies

MAX1610/MAX1611

General Description

The MAX1610/MAX1611 are highly integrated power-supply subsystems for driving cold-cathode fluorescent lamps (CCFLs) from a 4.5V to 28V power source. They keep CCFL brightness constant with changing input voltage, and allow digital adjustment of the regulation point. An on-board power MOSFET with a high switching frequency reduces external component count and magnetics size. The MAX1610/MAX1611 are protected against both open and shorted lamp fault conditions. The CCFL can be driven from an isolated transformer secondary winding to improve efficiency, avoid flicker at dim tube settings, and lower the minimum input voltage required. Brightness is adjusted by scaling lamp current, or by operating with a fixed lamp current and chopping the CCFL on and off at a rate faster than the eye can detect.

The MAX1610 digital inputs increment, decrement, or clear an internal 5-bit up/down counter that sets CCFL brightness. The MAX1611 uses the Intel System Management Bus (SMBus™) two-wire serial interface to directly set CCFL brightness. Both devices include micropower shutdown and a linear regulator that eliminates the need for a separate logic supply.

Applications

Notebook Computers
Flat Panel Displays
LCD Televisions

Features

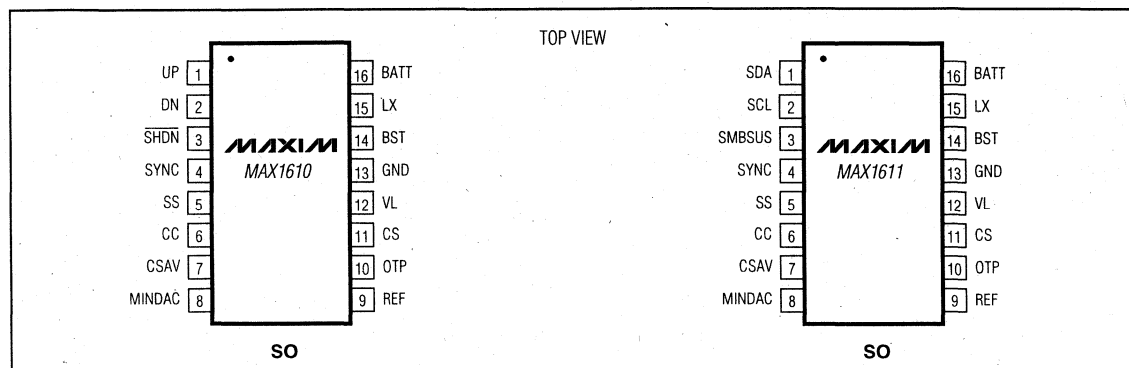
- ◆ Direct Digital Control of CCFL Brightness
- ◆ High Power-to-Light Efficiency
- ◆ Low-Voltage Operation (down to 4.5V)
- ◆ Internal 30V, 0.5Ω Power Switch
- ◆ Open Lamp and Shorted Lamp Protection
- ◆ CCFL Drive from Fully Isolated Transformer Secondary Winding
- ◆ No Flicker at Low Brightness
- ◆ 300kHz Switching Frequency
- ◆ Oscillator SYNC Input
- ◆ 16-Pin Narrow SO Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1610CSE	0°C to +70°C	16 Narrow SO
MAX1610ESE	-40°C to +85°C	16 Narrow SO
MAX1611CSE	0°C to +70°C	16 Narrow SO
MAX1611ESE	-40°C to +85°C	16 Narrow SO

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Pin Configurations



SMBus is a trademark of Intel Corp.

MAXIM

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Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Digitally Adjustable LCD Bias Supply

General Description

The MAX1620/MAX1621/MAX1622 convert a 4V to 24V battery voltage to a positive or negative LCD backplane bias voltage. Backplane bias voltage is automatically disabled when the display logic voltage is removed, protecting the display. These devices use very little PC board area: They come in ultra-small QSOP and μ MAX packages, and require only small, low-profile external components.

The output voltage can be preset to the desired positive or negative voltage range with simple applications resistors, and adjusted over that range with the on-board DAC or with a potentiometer. The MAX1620/MAX1621 include a 5-bit DAC, allowing digital software control of the bias voltage. The MAX1620 uses up/down digital signaling to adjust the DAC, and the MAX1621 uses the System Management Bus (SMBus™) two-wire serial interface. The MAX1622 is suitable for applications where digital control is not required.

These devices use low-cost, external N-channel or NPN power switches, and can be configured for positive or negative output voltages. Operating power is a low 500 μ A, provided from the display logic supply of 3.0V to 5.5V. The MAX1620/MAX1621 are available in a 16-pin QSOP package, and the MAX1622 is available in the 8-pin μ MAX package.

Applications

Notebook Computers Palmtop Computers
Laptop Computers Personal Digital Assistants
Portable Data-Collection Terminals

Features

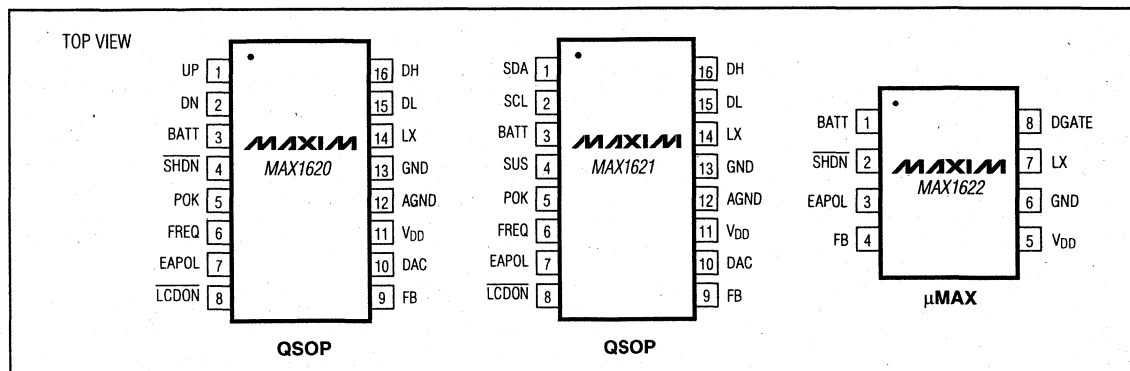
- ◆ 4V to 24V Battery Input Voltage
- ◆ Automatic Disable when Display Logic is Shut Down
- ◆ Extremely Small QSOP/ μ MAX Package
- ◆ 32-Level Internal DAC
- ◆ SMBus™ Serial Interface
- ◆ Positive or Negative Output Voltage

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1620CEE	0°C to +70°C	16 QSOP
MAX1620EEE	-40°C to +85°C	16 QSOP
MAX1621CEE	0°C to +70°C	16 QSOP
MAX1621EEE	-40°C to +85°C	16 QSOP
MAX1622CUA	0°C to +70°C	8 μ MAX
MAX1622EUA	-40°C to +85°C	8 μ MAX

MAX1620/MAX1621/MAX1622

Pin Configurations



SMBus is a trademark of Intel Corp.

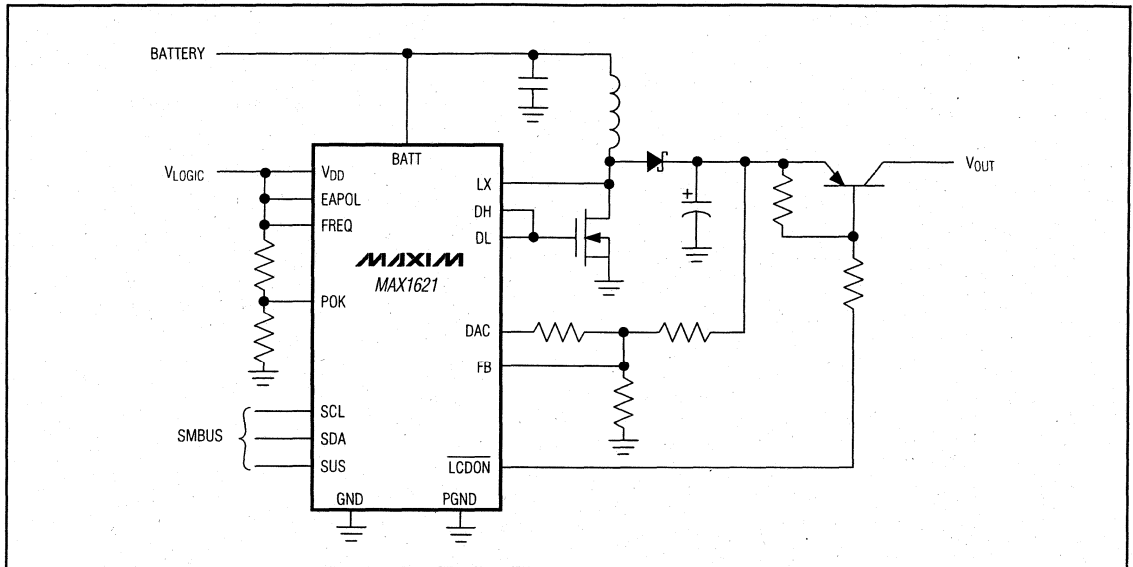
MAXIM

Maxim Integrated Products 4-33

Call toll free 1-800-998-8800 for free samples or literature.

Digitally Adjustable LCD Bias Supply

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

EVALUATION KIT WILL BE AVAILABLE

100% Duty Cycle, PFM, Step-Down DC-DC Controllers

MAXIM

MAX1626/MAX1627

General Description

The MAX1626/MAX1627 step-down, DC-DC switching controllers provide greater than 90% efficiency over loads ranging from 10mA to more than 2.5A. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives these devices the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using only 80µA (max) of supply current (vs. 2mA to 10mA for PWM converters).

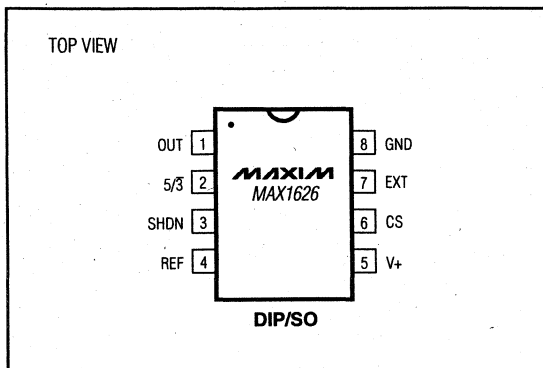
The MAX1626/MAX1627 have a high switch duty cycle of up to 100%, allowing the external P-channel transistor to fully turn on. The 100% duty cycle and a low 100mV current-sense voltage permit less than 0.3V dropout at 500mA. The MAX1626 output voltage is pin selectable to be either 5V or 3.3V. The MAX1627 output can be adjusted from 1.3V to the input voltage by using two external resistors. Both parts accept input voltages up to 16.5V.

High switching frequencies (up to 300kHz) and continuous-conduction mode operation allow minimum size coils and capacitors. The MAX1626/MAX1627 are improved-dropout upgrades for the MAX1649/MAX1651.

Applications

PDAs
Cellular Phones
PCMCIA
Handy Terminals
Notebook Computers
Scanners
Portable Equipment and Instruments

Pin Configuration



Features

- ◆ Greater than 90% Efficiency for 10mA to 2.5A Loads
- ◆ Up to 100% Duty Cycle for Lowest Dropout
- ◆ Less than 0.3V Dropout Voltage at 500mA
- ◆ 80µA (max) Quiescent Supply Current
- ◆ 5µA (max) Shutdown Supply Current
- ◆ Up to 16.5V Input Voltage
- ◆ 5V/3.3V (MAX1626) or Adjustable (MAX1627) Output Voltage
- ◆ Current-Limited Control Scheme Provides High Efficiency and Prevents Surge During Turn-On
- ◆ Up to 300kHz Switching Frequency

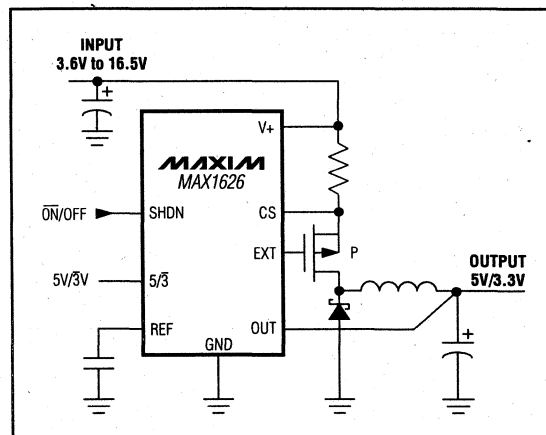
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1626C/D	0°C to +70°C	Dice*
MAX1626ISA	-25°C to +85°C	8 SO
MAX1627C/D	0°C to +70°C	Dice*
MAX1627ISA	-25°C to +85°C	8 SO

*Dice are specified at $T_A = +25^\circ\text{C}$.

4

Typical Operating Circuit



MAXIM

Maxim Integrated Products 4-35

Call toll free 1-800-998-8800 for free samples or literature.

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

General Description

The MAX1649/MAX1651 BiCMOS, step-down, DC-DC switching controllers provide high efficiency over loads ranging from 1mA to more than 2.5A. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives these devices the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using only 100µA of supply current (vs. 2mA to 10mA for PWM converters). Dropout performance down to 300mV is provided by a high switch duty cycle (96.5%) and a low current-sense threshold (110mV).

A high switching frequency (up to 300kHz) allows these devices to use miniature external components.

The MAX1649/MAX1651 have dropout voltages less than 0.3V at 500mA and accept input voltages up to 16V. Output voltages are preset at 5V (MAX1649), or 3.3V (MAX1651). They can also be adjusted to any voltage from 1.5V to the input voltage by using two resistors.

These step-down controllers drive external P-channel MOSFETs at loads greater than 12.5W. If less power is required, use the MAX639/MAX640/MAX653 step-down converters with on-chip FETs, which allow up to a 225mA load current.

Applications

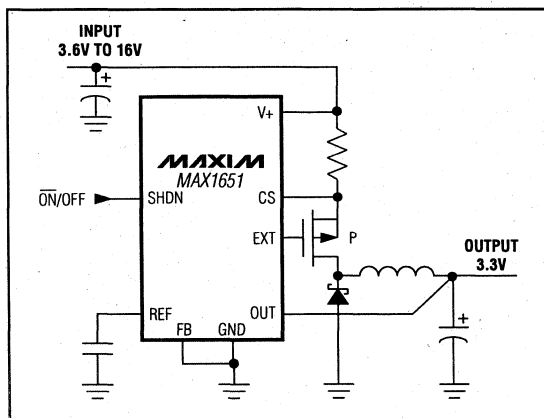
PDA's

High-Efficiency Step-Down Regulation

5V-to-3.3V Green PC Applications

Battery-Powered Applications

Typical Operating Circuit



Features

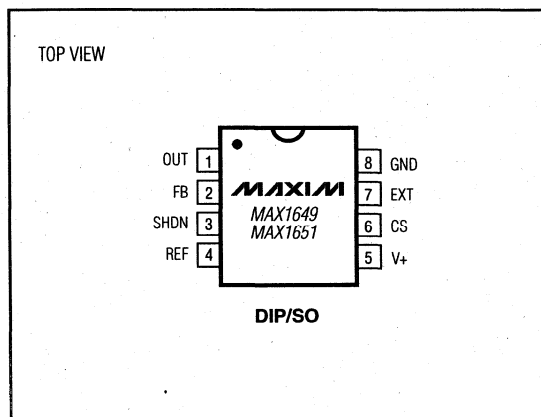
- ◆ More than 90% Efficiency (10mA to 1.5A Loads)
- ◆ More than 12.5W Output Power
- ◆ Less than 0.3V Dropout Voltage at 500mA
- ◆ 100µA Max Quiescent Supply Current
- ◆ 5µA Max Shutdown Supply Current
- ◆ 16V Max Input Voltage
- ◆ 5V (MAX1649), 3.3V (MAX1651), or Adjustable Output Voltage
- ◆ Current-Limited Control Scheme
- ◆ Up to 300kHz Switching Frequency
- ◆ Up to 96.5% Duty Cycle

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1649CPA	0°C to +70°C	8 Plastic DIP
MAX1649CSA	0°C to +70°C	8 SO
MAX1649C/D	0°C to +70°C	Dice*
MAX1649EPA	-40°C to +85°C	8 Plastic DIP
MAX1649ESA	-40°C to +85°C	8 SO
MAX1651CPA	0°C to +70°C	8 Plastic DIP
MAX1651CSA	0°C to +70°C	8 SO
MAX1651C/D	0°C to +70°C	Dice*
MAX1651EPA	-40°C to +85°C	8 Plastic DIP
MAX1651ESA	-40°C to +85°C	8 SO

* Dice are tested at $T_A = +25^\circ\text{C}$.

Pin Configuration



5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to GND -0.3V, +17V
 REF, SHDN, FB, CS, EXT, OUT -0.3V, (V+ + 0.3V)
 Continuous Power Dissipation (T_A = +70°C)
 Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
 SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Ranges
 MAX1649C_A, MAX1651C_A 0°C to +70°C
 MAX1649E_A, MAX1651E_A -40°C to +85°C
 Storage Temperature Range -65°C to +160°C
 Lead Temperature (soldering, 10sec) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	V _{OUT} < V+		3.0		16	V
Supply Current	I+	V+ = 16V, SHDN ≤ 0.4V (operating, switch off)			78	100	μA
		V+ = 16V, SHDN ≥ 1.6V (shutdown)			2		
		V+ = 10V, SHDN ≥ 1.6V (shutdown)			1	5	
FB Trip Point		MAX1649C, MAX1651C		1.470	1.5	1.530	V
		MAX1649E, MAX1651E		1.4625	1.5	1.5375	
FB Input Current	I _{FB}	MAX1649C, MAX1651C				±50	nA
		MAX1649E, MAX1651E				±70	
Output Voltage	V _{OUT}	Circuit of Figure 1	MAX1649, V+ = 5.5V to 16V	4.80	5.0	5.20	V
			MAX1651, V+ = 3.6V to 16V	3.17	3.3	3.43	
Reference Voltage	V _{REF}	MAX1649C, MAX1651C, I _{REF} = 0μA		1.470	1.5	1.530	V
		MAX1649E, MAX1651E, I _{REF} = 0μA		1.4625	1.5	1.5375	
REF Load Regulation		0μA ≤ I _{REF} ≤ 100μA, sourcing only			4	10	mV
REF Line Regulation		3V ≤ V+ ≤ 16V			40	100	μV/V
Output Voltage Line Regulation		Circuit of Figure 1	MAX1649, 5.5V ≤ V+ ≤ 16V, I _{LOAD} = 1A		2.6		mV/V
			MAX1651, 3.6V ≤ V+ ≤ 16V, I _{LOAD} = 1A		1.7		
Output Voltage Load Regulation		Circuit of Figure 1	MAX1649, 0A ≤ I _{LOAD} ≤ 1.5A, V _{IN} = 10V		-47		mV/A
			MAX1651, 0A ≤ I _{LOAD} ≤ 1.5A, V _{IN} = 5V		-45		
Efficiency		Circuit of Figure 1	MAX1649, V+ = 10V, I _{LOAD} = 1A		90		%
			MAX1651, V+ = 5V, I _{LOAD} = 1A		90		
SHDN Input Current		V+ = 16V, SHDN = 0V or V+				1	μA
SHDN Input Voltage High	V _{IH}	3V ≤ V+ ≤ 16V		1.6			V
SHDN Input Voltage Low	V _{IL}	3V ≤ V+ ≤ 16V				0.4	V

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

MAX1649/MAX1651

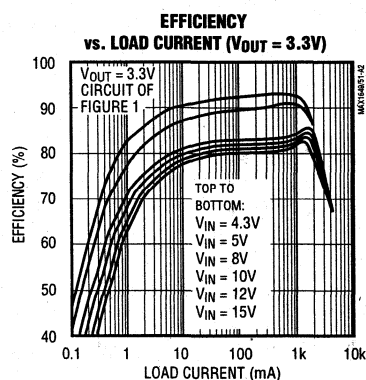
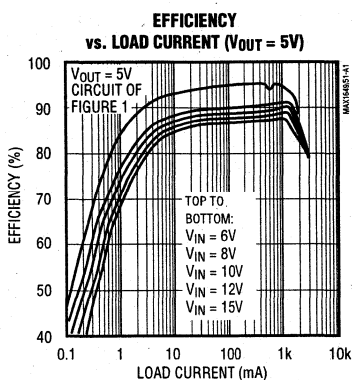
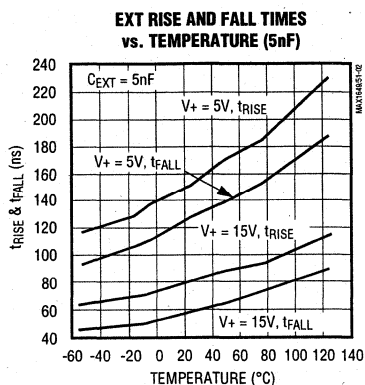
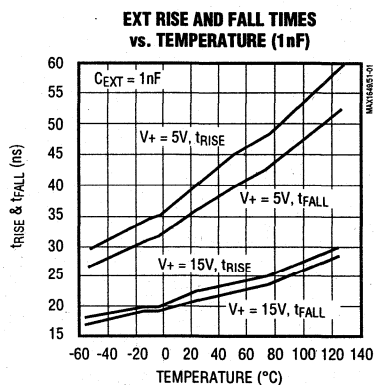
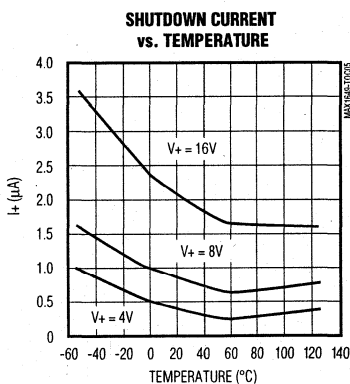
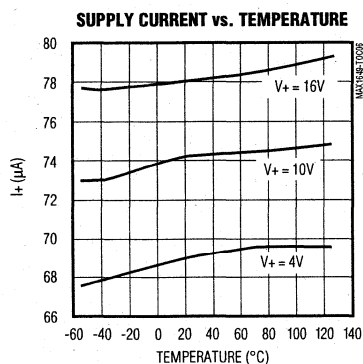
ELECTRICAL CHARACTERISTICS (continued)

($V_+ = 5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Trip Level (V_+ to CS)	V_{CS}	$3V \leq V_+ \leq 16V$	80	110	140	mV
CS Input Current		$3V \leq V_+ \leq 16V$			± 1	μA
Switch Maximum On-Time	$t_{ON} (max)$	$V_+ = 12V$	24	32	40	μs
Switch Minimum Off-Time	$t_{OFF} (min)$	$V_+ = 12V$	0.8	1.1	1.8	μs
EXT Rise Time		$C_{EXT} = 0.001\mu F$, $V_+ = 12V$		25		ns
EXT Fall Time		$C_{EXT} = 0.001\mu F$, $V_+ = 12V$		25		ns
Maximum Duty Cycle		$\frac{t_{ON}}{t_{ON} + t_{OFF}} \times 100\%$	95	96.5		%

Typical Operating Characteristics

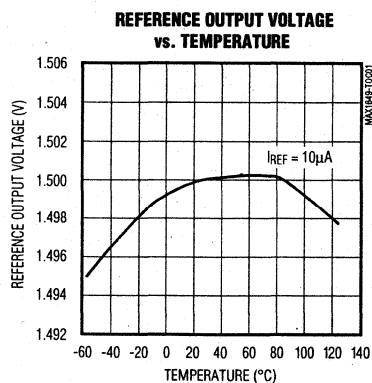
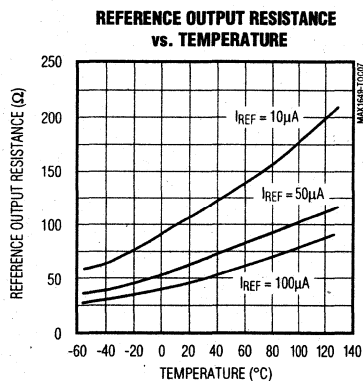
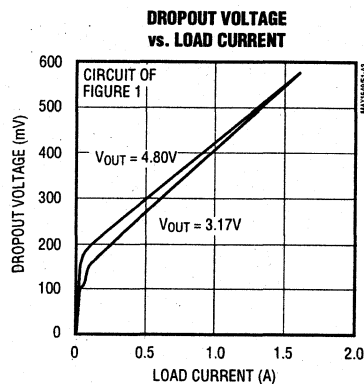
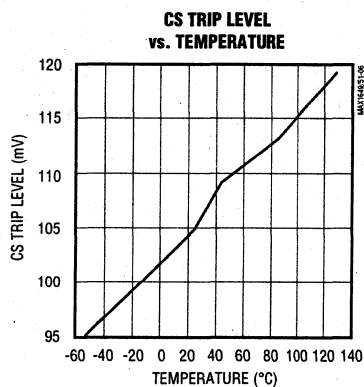
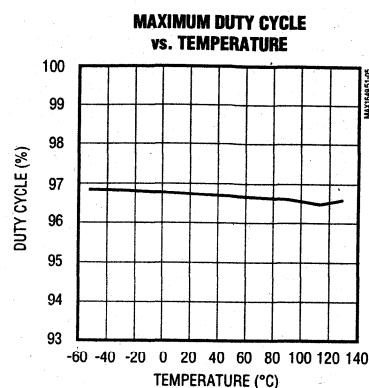
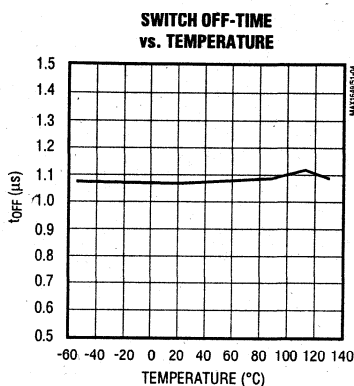
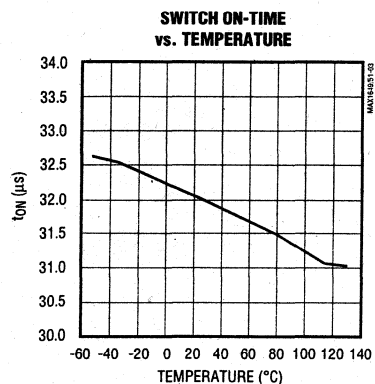
($T_A = +25^\circ C$, unless otherwise noted.)



5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

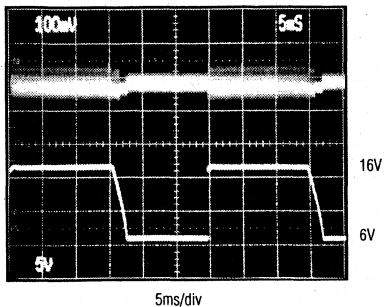


5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

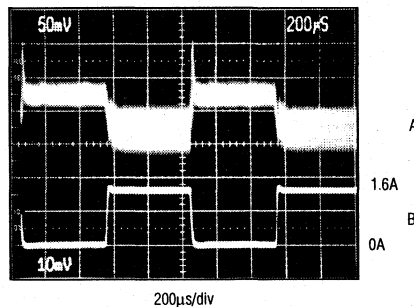
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

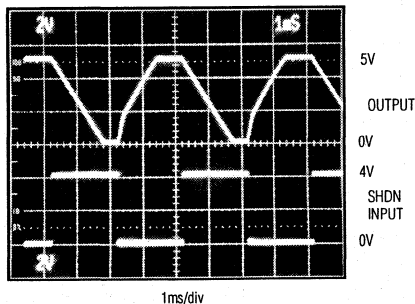
**MAX1649
LINE-TRANSIENT RESPONSE**



**MAX1649
LOAD-TRANSIENT RESPONSE**



**MAX1649
SHDN RESPONSE TIME**



MAX1649/MAX1651

4

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

Pin Description

PIN	NAME	FUNCTION
1	OUT	Sense Input for fixed 5V or 3.3V output operation. OUT is internally connected to the on-chip voltage divider. Although it is connected to the output of the circuit, the OUT pin does not supply current. Leave OUT unconnected for adjustable-output operation.
2	FB	Feedback Input. Connect to GND for fixed-output operation. Connect a resistor divider between OUT, FB, and GND for adjustable-output operation. See <i>Setting the Output Voltage</i> section.
3	SHDN	Active-High Shutdown Input. Part is placed in shutdown when SHDN is driven high. In shutdown mode, the reference, output, and external MOSFET are turned off. Connect to GND for normal operation.
4	REF	1.5V Reference Output that can source 100 μ A. Bypass with 0.1 μ F.
5	V+	Positive Power-Supply Input
6	CS	Current-Sense Input. Connect current-sense resistor between V+ and CS. When the voltage across the resistor equals the current-limit trip level, the external MOSFET is turned off.
7	EXT	Gate Drive for External P-Channel MOSFET. EXT swings between V+ and GND.
8	GND	Ground

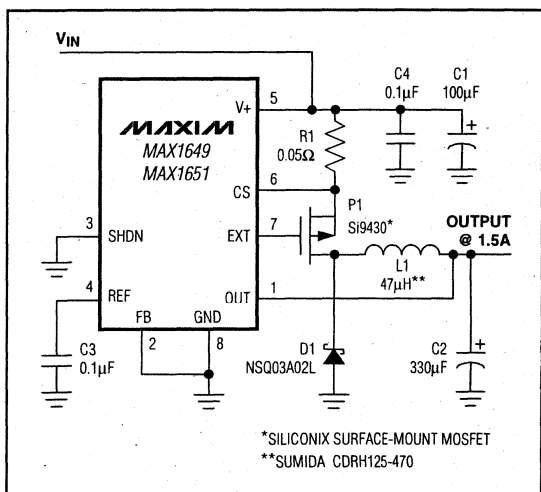


Figure 1. Test Circuit

Detailed Description

The MAX1649/MAX1651 are BiCMOS, step-down, switch-mode power-supply controllers that provide adjustable and fixed outputs of 5V and 3.3V, respectively. Their unique control scheme combines the advantages of pulse-frequency-modulation (low supply current) and pulse-width-modulation (high efficiency at high loads). An external P-channel power MOSFET allows peak currents in excess of 3A, increasing the output current capability over previous PFM devices. Figure 2 is the block diagram.

The MAX1649/MAX1651 offer four main improvements over prior solutions:

- 1) The converters operate with miniature surface-mount inductors, due to their 300kHz switching frequency.
- 2) The current-limited PFM control scheme allows greater than 90% efficiencies over a wide range of load currents (10mA to 1.5A).
- 3) Dropout voltage has been reduced to less than 300mV for many applications.
- 4) The quiescent supply current is only 100 μ A.

PFM Control Scheme

The MAX1649/MAX1651 use a proprietary, current-limited PFM control scheme. As with traditional PFM converters, the external power MOSFET is turned on when the voltage comparator senses that the output is out of regulation. However, unlike traditional PFM converters, switching is accomplished through the combination of a peak current limit and a pair of one-shots that set the maximum switch on-time (32 μ s) and minimum switch off-time (1.1 μ s). Once off, the off-time one-shot holds the switch off for 1.1 μ s. After this minimum time, the switch either 1) stays off if the output is in regulation, or 2) turns on again if the output is out of regulation.

The MAX1649/MAX1651 also limit the peak inductor current, which allows them to run in continuous-conduction mode and maintain high efficiency with heavy loads (Figure 3). This current-limiting feature is a key component of the control circuitry. Once turned on, the switch stays on until either 1) the maximum on-time one-shot turns it off (32 μ s later), or 2) the current limit is reached. EXT swings from V+ to GND and provides the drive output for an external P-channel power MOSFET.

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

MAX1649/MAX1651

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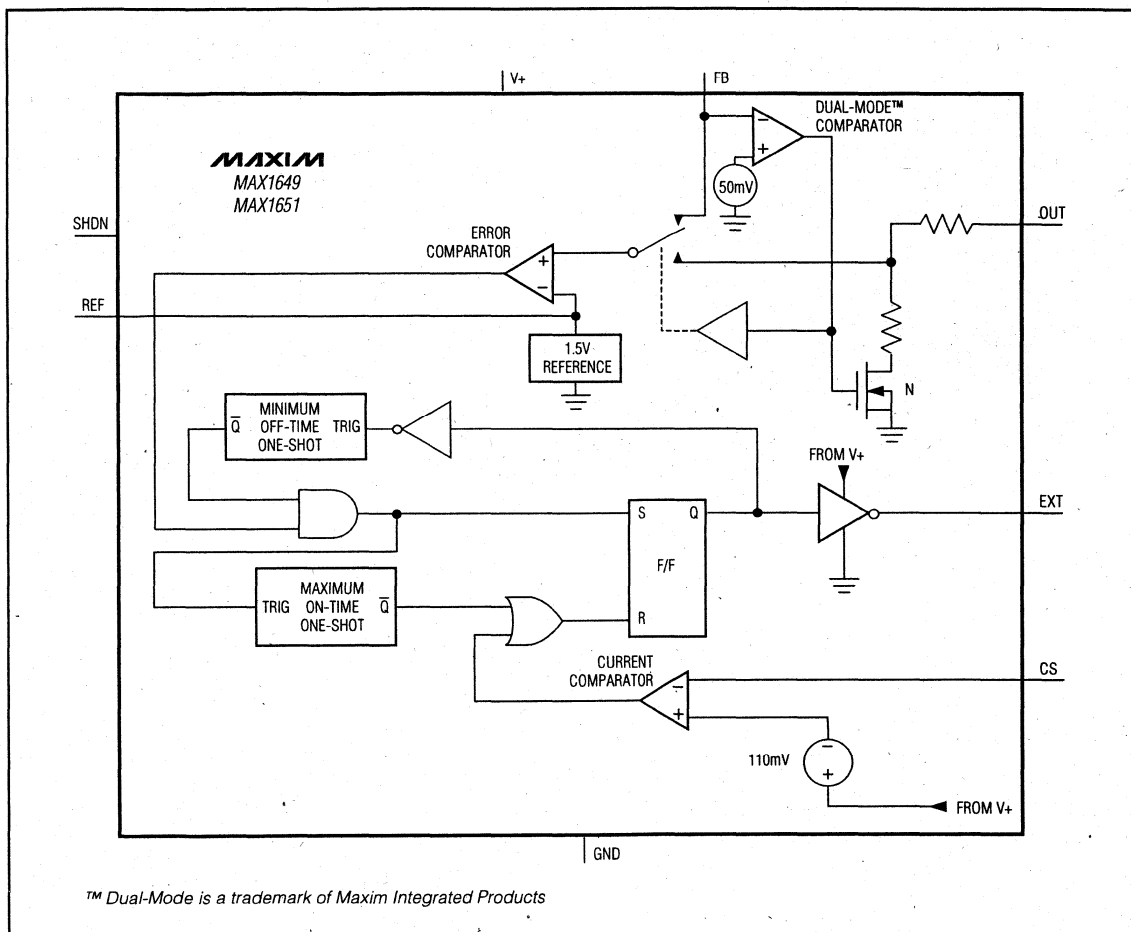


Figure 2. Block Diagram

Shutdown Mode

When SHDN is high, the MAX1649/MAX1651 enter shutdown mode. In this mode, the internal biasing circuitry is turned off (including the reference) and the supply current drops to less than 5 μ A. EXT goes high, turning off the external MOSFET. SHDN is a logic-level input. Connect SHDN to GND for normal operation.

Quiescent Current

In normal operation, the device's typical quiescent current is 78 μ A. In an actual application, even with no load, additional current is drawn to supply external feedback resistors (if used) and the diode and capacitor leakage currents. In the circuit of Figure 1, with V+ at 5V and VOUT at 3.3V, typical no-load supply current for the entire circuit is 90 μ A.

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

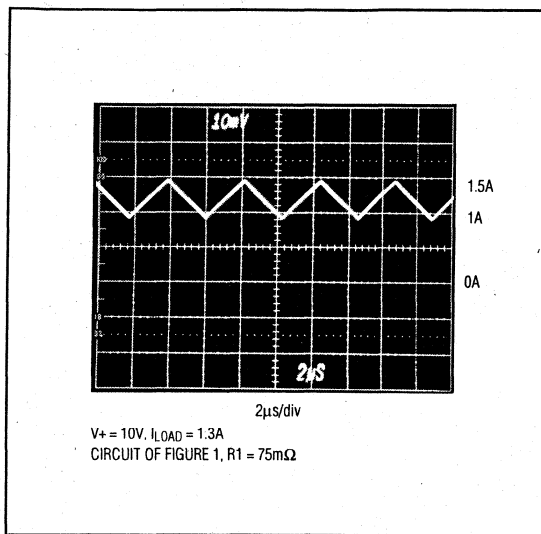


Figure 3. MAX1649 Continuous-Conduction Mode, Heavy Load-Current Waveform (500mA/div)

Modes of Operation

When delivering high output currents, the MAX1649/MAX1651 operate in continuous-conduction mode. In this mode, current always flows in the inductor, and the control circuit adjusts the switch duty cycle to maintain regulation without exceeding the switch current capability (Figure 3). This provides excellent load-transient response and high efficiency.

In discontinuous-conduction mode, current through the inductor starts at zero, rises to a peak value, then ramps down to zero. Although efficiency is still excellent, the output ripple increases slightly, and the switch waveform exhibits ringing (at the inductor's self-resonant frequency). This ringing is to be expected and poses no operational problems.

Dropout

The MAX1649/MAX1651 are in dropout when the input voltage (V_+) is low enough that the output drops below the minimum output voltage specification (see *Electrical Characteristics*). The dropout voltage is the difference between the input and output voltage when dropout occurs. See the *Typical Operating Characteristics* for the Dropout Voltage vs. Load Current and Dropout Voltage vs. Temperature graphs.

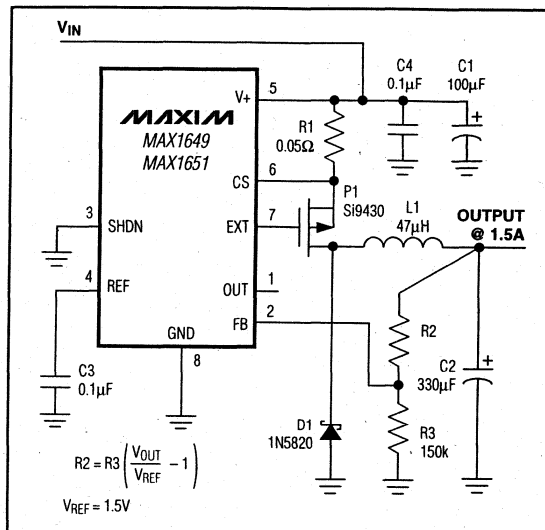


Figure 4. Adjustable-Output Operation

Design Procedure

Setting the Output Voltage

The MAX1649/MAX1651 are preset for 5V and 3.3V output voltages, respectively; tie FB to GND for fixed-output operation. They may also be adjusted from 1.5V (the reference voltage) to the input voltage, using external resistors R2 and R3 configured as shown in Figure 4. For adjustable-output operation, 150kΩ is recommended for resistor R3—high enough to avoid wasting energy, yet low enough to avoid RC delays caused by parasitic capacitance at FB. R2 is given by:

$$R2 = R3 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

where $V_{REF} = 1.5V$.

When using external resistors, it does no harm to connect OUT and the output together, or to leave OUT unconnected.

Current-Sense Resistor Selection

The current-sense resistor limits the peak switch current to $110mV/R_{SENSE}$, where R_{SENSE} is the value of the current-sense resistor, and 110mV is the current-limit trip level (see *Electrical Characteristics*).

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

To maximize efficiency and reduce the size and cost of external components, minimize the peak current. However, since the available output current is a function of the peak current, the peak current must not be too low.

To choose the proper current-sense resistor for a particular output voltage, determine the minimum input voltage and the maximum load current. Next, referring to Figures 5a or 5b, using the minimum input voltage, find the curve with the largest sense resistor that provides sufficient output current. It is not necessary to perform worst-case calculations. These curves take into account the sense-resistor ($\pm 5\%$) and inductor ($47\mu\text{H} \pm 10\%$) values, the diode drop (0.4), and the IC's current-sense trip level (85mV); an external MOSFET on-resistance of 0.07Ω is assumed for $V_{GS} = -5\text{V}$.

Standard wire-wound and metal-film resistors have an inductance high enough to degrade performance. Surface-mount (chip) resistors have very little inductance and are well suited for use as current-sense resistors. A U-shaped wire resistor made by IRC works well in through-hole applications. Because this resistor is a band of metal shaped as a "U", its inductance is less than 10nH (an order of magnitude less than metal film resistors). Resistance values between $5\text{m}\Omega$ and 0.1Ω are available (see Table 1).

Inductor Selection

The MAX1649/MAX1651 operate with a wide range of inductor values, although for most applications coils between $10\mu\text{H}$ and $68\mu\text{H}$ take best advantage of the con-

trollers' high switching frequency. With a high inductor value, the MAX1649/MAX1651 will begin continuous-current operation (see *Detailed Description*) at a lower fraction of full-load current. In general, smaller values produce higher ripple (see below) while larger values require larger size for a given current rating.

In both the continuous and discontinuous modes, the lower limit of the inductor is important. With a too-small inductor value, the current rises faster and overshoots the desired peak current limit because the current-limit comparator has a finite response time (300ns). This reduces efficiency and, more importantly, could cause the current rating of the external components to be exceeded. Calculate the minimum inductor value as follows:

$$L(\text{min}) = \frac{(V_{\text{in}}(\text{max}) - V_{\text{OUT}}) \times 0.3\mu\text{s}}{\Delta I \times I_{\text{LIM}}(\text{min})}$$

where ΔI is the inductor-current overshoot factor, $I_{\text{LIM}} = V_{\text{CS}}/R_{\text{SENSE}}$, and $0.3\mu\text{s}$ is the time it takes the comparator to switch. Set $\Delta I = 1.1$ for an overshoot of 10%.

For highest efficiency, use a coil with low DC resistance; a value smaller than $0.1\text{V}/I_{\text{LIM}}$ works best. To minimize radiated noise, use a toroid, pot core, or shielded-bobbin inductor. Inductors with a ferrite core or equivalent are recommended. Make sure the inductor's saturation-current rating is greater than $I_{\text{LIM}}(\text{max})$. However, it is generally acceptable to bias the inductor into saturation by about 20% (the point where the inductance is 20% below its nominal value).

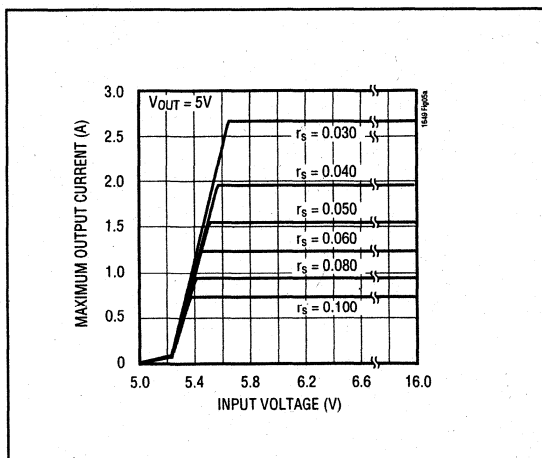


Figure 5a. MAX1649 Current-Sense Resistor Graph

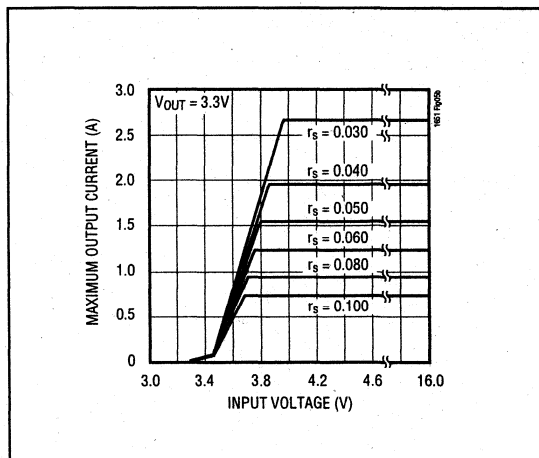


Figure 5b. MAX1651 Current-Sense Resistor Graph

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

Table 1. Component Selection Guide

PRODUCTION METHOD	INDUCTORS	CAPACITORS	DIODES	CURRENT-SENSE RESISTORS	MOSFETS
Surface Mount	Sumida CDRH125-470 (1.8A) CDRH125-220 (2.2A) CoilCraft DO3316-473 (1.6A) DO3340-473 (3.8A)	AVX TPS series Sprague 595D series	Motorola MBRS340T3 Nihon NSQ series	Dale WSL Series IRC LRC series	Siliconix Little Foot series Motorola medium-power surface-mount products
Miniature Through-Hole	Sumida RCH875-470M (1.3A)	Sanyo OS-CON series low-ESR organic semiconductor		IRC OAR series	Motorola
Low-Cost Through-Hole	CoilCraft PCH-45-473 (3.4A)	Nichicon PL series low-ESR electrolytics United Chemi-Con LXF series	Motorola 1N5817 to 1N5823		Motorola TMOS power MOSFETs

The peak current of Figure 1 is 2.35A for a 1.5A output. The inductor used in this circuit is specified to drop by 10% at 2.2A (worst case); a curve provided by the manufacturer shows that the inductance typically drops by 20% at 2.7A. Using a slightly underrated inductor can sometimes reduce size and cost, with only a minor impact on efficiency.

Table 1 lists inductor types and suppliers for various applications. The efficiencies of the listed surface-mount inductors are nearly equivalent to those of the larger size through-hole versions.

Diode Selection

The MAX1649/MAX1651's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5817 through 1N5823 (and their surface-mount equivalents), are recommended. Choose a diode with an average current rating equal to or greater than $I_{LIM(max)}$ and a voltage rating higher than $V_+(max)$.

External Switching Transistor

The MAX1649/MAX1651 drive P-channel enhancement-mode MOSFET transistors only. The choice of power transistor is primarily dictated by the input voltage and the peak current. The transistor's on-resistance, gate-source threshold, and gate charge must also be appropriately chosen. The drain-to-source and gate-to-source breakdown voltage ratings must be greater than V_+ . The total gate-charge specification is normally not

critical, but values should be less than 100nC for best efficiency. The MOSFET should be capable of handling the peak current and, for maximum efficiency, have a very low on-resistance at that current. Also, the on-resistance must be low for the minimum available V_{GS} , which equals $V_+(min)$. Select a transistor with an on-resistance between 50% and 100% of the current-sense resistor. The Si9430 transistor chosen for the *Typical Operating Circuit* has a drain-to-source rating of -20V and a typical on-resistance of 0.070Ω at 2A with $V_{GS} = -4.5V$. Tables 1 and 2 list suppliers of switching transistors suitable for use with these devices.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR), rather than high capacitance. An electrolytic capacitor with low enough ESR will automatically have high enough capacitance. The product of the inductor-current variation and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. When a $330\mu F$, 10V Sprague surface-mount capacitor (595D series) with $ESR = 0.15\Omega$ is used, 40mV of output ripple is typically observed when stepping down from 10V to 5V at 1A. The output filter capacitor's ESR also affects efficiency. Again, low-ESR capacitors perform best. Table 1 lists some suppliers of low-ESR capacitors.

5V/3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controllers

Table 2. Component Suppliers

COMPANY		PHONE	FAX
AVX	USA	(207) 282-5111 or (800) 282-4975	(207) 283-1941
Coiltronics	USA	(407) 241-7876	(407) 241-9339
CoilCraft	USA	(708) 639-6400	(708) 639-1469
Dale	USA	(402) 564-3131	(402) 563-1841
International Rectifier	USA	(310) 322-3331	(310) 322-3332
IRC	USA	(512) 992-7900	(512) 992-3377
Motorola	USA	(602) 244-3576 or (602) 244-5303	(602) 244-4015
Nichicon	USA Japan	(708) 843-7500 81-7-5231-8461	(708) 843-2798 81-7-5256-4158
Nihon	USA Japan	(805) 867-2555 81-3-3494-7411	(805) 867-2556 81-3-3494-7414
Sanyo	USA Japan	(619) 661-6835 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Siliconix	USA	(408) 988-8000 or (800) 554-5565	(408) 970-3950
Sprague	USA	(603) 224-1961	(603) 224-1430
Sumida	USA Japan	(708) 956-0666 81-3-3607-5111	(708) 956-0702 81-3-3607-5144
United Chemi-Con	USA	(714) 255-9500	(714) 255-9400

Input Bypass Capacitor

The input bypass capacitor reduces peak currents drawn from the voltage source, and also reduces the amount of noise at the voltage source caused by the switching action of the MAX1649/MAX1651. The input voltage source impedance determines the size of the capacitor required at the V+ input. As with the output filter capacitor, a low-ESR capacitor is recommended. Bypass the IC separately with a 0.1 μ F ceramic capacitor placed close to the V+ and GND pins.

Reference Capacitor

Bypass REF with a 0.1 μ F or larger capacitor.

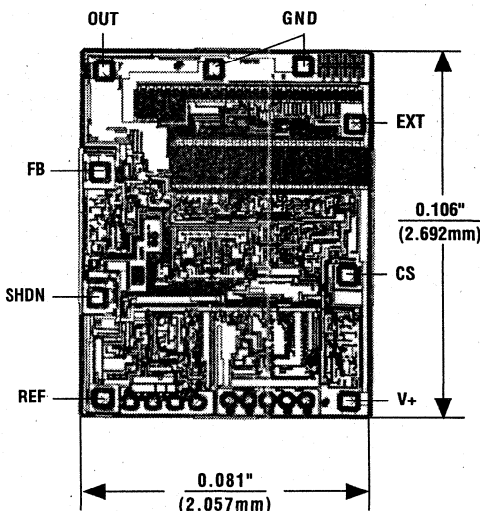
Layout Considerations

Proper PC board layout is essential because of high current levels and fast switching waveforms that radiate noise. Minimize ground noise by connecting the anode of the rectifier, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point ("star" ground configuration). A ground plane is recommended. Also minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. In particular, the traces connected to FB (if an external resistor divider is used) and EXT must be short. Place the 0.1 μ F ceramic bypass capacitor as close as possible to the V+ and GND pins.

MAX1649/MAX1651 vs. MAX649/MAX651

The MAX1649 and MAX1651 are pin compatible with the MAX649 and MAX651, but have been optimized for improved dropout performance and efficiency—particularly with low input voltages. The MAX1649/MAX1651 feature increased maximum switch duty cycle (96.5%) and reduced current-limit sense voltage (110mV). Their predecessors, the MAX649/MAX651, use a higher two-step (210mV/110mV) current-limit sense voltage to provide tighter current-sense accuracy and reduced inductor peak current at light loads.

Chip Topography



TRANSISTOR COUNT: 428
SUBSTRATE CONNECTED TO V+

NiCd/NiMH Battery Fast-Charge Controllers

General Description

The MAX2003/MAX2003A are fast-charge battery chargers (with conditioning) for NiCd (nickel cadmium) or NiMH (nickel-metal hydride) rechargeable batteries. The MAX2003A has the same features as the MAX2003 with an additional pulsed trickle-charge mode to prevent dendrite formation in NiMH batteries. Each can be configured as a switch-mode current regulator or as a gating controller for an external current source. Switch-mode current regulation provides efficient energy transfer, reducing power dissipation and the associated heating. Gating control of an external current source requires minimal components, saving space and cost.

On-chip algorithms determine charge termination, so the MAX2003/MAX2003A can be used as stand-alone chargers. Fast-charge termination is accomplished by five methods: temperature slope, negative voltage change, maximum temperature, maximum time, and maximum voltage. As a safety feature, the start of fast-charge is inhibited until battery voltage and temperature are within safe limits. By selecting the appropriate charge-termination method, a single circuit can be built with the MAX2003/MAX2003A to fast-charge both NiMH and NiCd batteries.

The MAX2003/MAX2003A provide a switch-activated discharge-before-charge option that allows for battery conditioning and more accurate capacity measurement. Other features include optional top-off charging and direct drivers for LED status lights.

The MAX2003, in DIP and wide SO packages, is a direct plug-in replacement for the bq2003. The MAX2003/MAX2003A also come in a space-saving narrow SO package. The MAX2003A evaluation kit (MAX2003A EVKIT-SO) is available to assist in designs.

Applications

- Battery-Powered Equipment:
 - Laptop, Notebook, and Palmtop Computers
 - Handy-Terminals
- Portable Consumer Products:
 - Portable Stereos
 - Cordless Phones
- Backup-Battery Applications:
 - Memory Hold-Up
 - Emergency Switchovers

Features

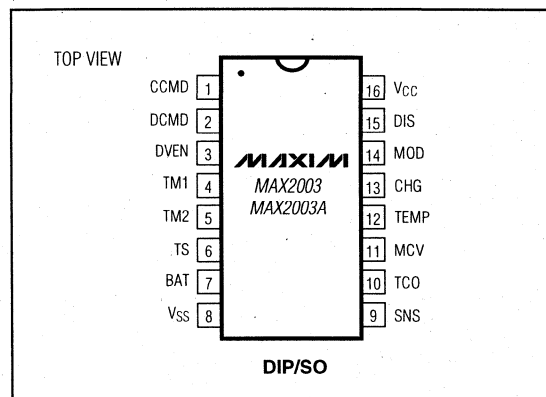
- ♦ Stand-Alone NiCd or NiMH Fast Chargers
- ♦ New Pulsed Trickle-Charge Mode (MAX2003A only)
- ♦ Provide Switch-Mode, Gated, or Linear Control Regulation
- ♦ Small, Narrow SOIC Package Available
- ♦ On-Chip Fast-Charge Termination Methods:
 - Temperature Slope
 - Maximum Voltage
 - Negative Delta Voltage
 - Maximum Time
 - Maximum Temperature
- ♦ Automatically Switch from Fast-Charge to Trickle-Charge or Top-Off Charge
- ♦ Optional Discharge-Before-Charge
- ♦ Directly Drive Status LEDs
- ♦ Optional Top-Off Charge

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2003CPE	0°C to +70°C	16 Plastic DIP
MAX2003CSE	0°C to +70°C	16 Narrow SO
MAX2003CWE	0°C to +70°C	16 Wide SO
MAX2003C/D	0°C to +70°C	Dice*
MAX2003ACPE	0°C to +70°C	16 Plastic DIP
MAX2003ACSE	0°C to +70°C	16 Narrow SO
MAX2003ACWE	0°C to +70°C	16 Wide SO
MAX2003AC/D	0°C to +70°C	Dice*

* Contact factory for dice specifications.

Pin Configuration



NiCd/NiMH Battery Fast-Charge Controllers

ABSOLUTE MAXIMUM RATINGS

All Pins to V_{SS} -0.3V, +6.0V
 Continuous Power Dissipation (T_A = +70°C)
 Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
 Narrow SO (derate 8.70mW/°C above +70°C) 696mW
 Wide SO (derate 9.52mW/°C above +70°C) 762mW

Operating Temperature Range 0°C to +70°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10sec) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Figure 1, all measurements are with respect to V_{SS}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V _{CC}		4.5	5.0	5.5	V
Supply Current	I _{CC}	No load		0.75	2.2	mA
Cell Potential	V _{CELL}	V _{BAT} - V _{SNS}	0.0		V _{CC}	V
Battery Voltage Input	V _{BAT}		0.0		V _{CC}	V
Temperature Potential	V _{TEMP}	V _{TS} - V _{SNS}	0.0		V _{CC}	V
Temperature Sense Input Voltage	V _{TS}		0.0		V _{CC}	V
End-of-Discharge Voltage	V _{EDV}	V _{CC} = 5V	0.2V _{CC} - 30mV	0.2V _{CC}	0.2V _{CC} + 30mV	V
Maximum Cell Voltage	V _{MCV}	V _{CC} = 5V	V _{EDV}		V _{EDV} + 0.2V _{CC}	V
Low-Temperature Trip Threshold	V _{LTF}	V _{CC} = 5V	0.4V _{CC} - 30mV	0.4V _{CC}	0.4V _{CC} + 30mV	V
Temperature Cutoff Voltage	V _{TCO}	V _{CC} = 5V	V _{LTF} - 0.2V _{CC}		V _{LTF}	V
High-Temperature Trip Threshold	V _{HTF}	V _{CC} = 5V, V _{TCO} = 1.4V	(V _{LTF} /8) + (7V _{TCO} /8) - 30mV (V _{LTF} /8) + 7V _{TCO} /8 (V _{LTF} /8) + (7V _{TCO} /8) + 30mV			V
Sense Trip Threshold High	V _{SNSHI}	V _{CC} = 5V	0.05V _{CC} - 25mV	0.05V _{CC}	0.05V _{CC} + 25mV	V
Sense Trip Threshold Low	V _{SNSLO}	V _{CC} = 5V	0.044V _{CC} - 25mV	0.044V _{CC}	0.044V _{CC} + 25mV	V
Delta Sense Voltage (Note 1)	V _{SNSHI} - V _{SNSLO}			30		mV
Negative Delta Voltage (Note 2)	-ΔV	V _{CC} = 5V		12		mV
Thermistor Input Resolution (Note 2)	V _{THERM}	V _{CC} = 5V		16		mV
Logic-High Threshold	V _{OH}	For DIS, TEMP and CHG, 0mA ≤ I _{LOAD} ≤ 5mA; For MOD, 0mA ≤ I _{LOAD} ≤ 10mA	V _{CC} - 0.5			V
Logic-Low Threshold	V _{OL}	For DIS, TEMP and CHG, 0mA ≤ I _{LOAD} ≤ 5mA; For MOD, 0mA ≤ I _{LOAD} ≤ 10mA	0.5			V

NiCd/NiMH Battery Fast-Charge Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, Figure 1, all measurements are with respect to V_{SS}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic Voltage High	V _{IH}	CCMD, DCMD, DVEN	V _{CC} - 1.0			V
		TM1, TM2	V _{CC} - 0.3			
Input Logic Voltage Low	V _{IL}	CCMD, DCMD, DVEN			1.0	V
		TM1, TM2			0.3	
Input Logic Leakage	I _{LKG}	CCMD, DCMD, DVEN at V _{CC} and V _{SS}	-1.0		1.0	μA
Input Logic Current High	I _{IH}	TM1, TM2 = V _{CC}	-70.0			μA
Input Logic Current Low	I _{IL}	TM1, TM2 = V _{SS}			70.0	μA
Input Logic Current High-Z	I _{IZ}	TM1, TM2 = tri-state	-2.0		2.0	μA
Input Impedance		BAT, MCV, TCO, SNS, TS	50			MΩ

TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Figure 1, all measurements are with respect to V_{SS}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Pulse Width	t _{MPW}	CCMD, DCMD	1.0			μs
Variation of Fast-Charge Timeout		(Note 3)	0.84	1.00	1.16	
MOD Switching Frequency	f _{MAX}	MOD pin in fast-charge mode, V _{CC} = 5V			100	kHz
Battery Replacement Timeout (Note 4)	t _{BTO}		200	250	300	ms

Note 1: The sense trip levels are determined by an internal resistor divider network that provides a typical difference of 30mV from SNSHI to SNSLO. Slight variation in this delta is seen if there is a resistor mismatch in the network.

Note 2: Typical variations of Negative Delta Voltage and Thermistor Input Resolution parameters are less than ±4mV.

Note 3: Ratio of actual versus expected timeout (see Table 4). Tested with TM1 = TM2 = floating.

Note 4: To recognize a battery insert signal, V_{BAT} must be greater than V_{MCV} for at least t_{BTO}.

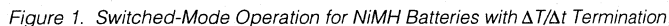
NiCd/NiMH Battery Fast-Charge Controllers

Pin Description

PIN	NAME	FUNCTION
1	CCMD	Charge-Enabled Mode Input—initiates fast-charge on a digital signal (see <i>Detailed Description</i> for operating conditions).
2	DCMD	Discharge-Enable Mode Input—initiates discharge-before-charge on a digital signal (see <i>Detailed Description</i> for operating conditions).
3	DVEN	Negative Delta Voltage ($-\Delta V$) Enable Input—enables $-\Delta V$ charge-termination mode. If DVEN is high, the controller uses negative-voltage change detection to terminate charge. If DVEN is low, this mode is disabled.
4, 5	TM1, TM2	These inputs are used to program the fast-charge and hold-off times, and to enable the top-off charge mode. The inputs can be high, low, or floating. See Table 4 for details.
6	TS	Temperature Sense-Voltage Input from external thermistor. The thermistor temperature coefficient is negative, so the higher the temperature, the lower the voltage at this pin (See <i>Detailed Description</i> for conditions of operation).
7	BAT	Input Voltage of Single Battery Cell. If more than one cell is present, a resistor divider is needed to divide the voltage down to a single cell voltage.
8	VSS	Ground
9	SNS	Current-Sense Input—connected to the negative battery terminal. TS and BAT are referenced to this pin. The voltage at SNS is directly proportional to the current through the battery and is used to determine how and when MOD switches.
10	TCO	Temperature Cutoff-Voltage Input. If the voltage from TS to SNS is less than the voltage at TCO, a hot thermistor (negative coefficient) is detected and fast or top-off charging is terminated.
11	MCV	Maximum Cell Voltage Input. If the voltage from BAT to SNS exceeds the voltage at MCV, fast or top-off charging is terminated.
12	TEMP	Temperature Status Output. This push/pull LED driver indicates that the temperature is outside the acceptable limits, and fast-charge and top-off are inhibited (see <i>Maximum Temperature Termination</i> section in <i>Detailed Description</i>).
13	CHG	Charge Status Output. This push/pull LED driver indicates charge status (see <i>Detailed Description</i>).
14	MOD	Modulation Output. This push/pull output switches to enable or disable charging current. If MOD is high, current is enabled. If it is low, current is disabled. For a 5V supply, if the voltage at the SNS pin is less than 220mV, MOD is high. If the voltage is above 250mV, MOD is low.
15	DIS	Discharge-Switch Control Output. This push/pull output turns on the FET that discharges the battery.
16	VCC	Power-Supply Voltage Input (+5V nominal)

MAX2003/MAX2003A

* COMPONENT USED FOR MAX2003.



NiCd/NiMH Battery Fast-Charge Controllers

Detailed Description

The MAX2003/MAX2003A is a fast-charge battery charger that uses several methods of charge termination. The device constantly monitors your choice of the following conditions to determine termination of fast-charge:

- Negative Delta Voltage ($-\Delta V$)
- Rate-of-Change of Temperature ($\Delta T/\Delta t$)
- Maximum Voltage
- Maximum Time
- Maximum Temperature

Figure 2 shows the block diagram for the MAX2003/MAX2003A.

The first step in creating a fast-charge battery-charger circuit is to determine what type of battery will be used and what conditions the battery manufacturer recommends for termination of fast-charge. The type of battery (NiCd or NiMH) and charge rate determine which method(s) of termination should be used.

The charging characteristics of NiMH batteries are similar to those of NiCd batteries, but there are some key differences that affect the choice of charge-termination method. Since the type of charge termination can be different for NiCd and NiMH batteries, it may not always be possible to use the same circuit for both battery types.

A comparison of the voltage profiles for NiCd and NiMH batteries (shown in Figure 3) reveals that NiCd batteries display a larger negative drop in voltage at the end of charge than do NiMH batteries. Therefore, the negative delta voltage detection ($-\Delta V$) method of terminating fast-charge should only be used for NiCd batteries. This termination method can cause errors in NiMH batteries, since the drop in voltage at full capacity is not as great, and may lead to an overcharged battery.

Figure 4 shows the temperature profiles of the two types of batteries. During the first 80% of the charge cycle, the NiCd battery temperature slowly rises. The NiMH battery temperature rises more rapidly during this period. As the cells approach 90% of capacity, the temperature of the NiCd cells rises more rapidly. When the cells approach full capacity, the rates-of-rise of temperature are comparable for both battery types. The rate of temperature change ($\Delta T/\Delta t$) can therefore be used to terminate fast-charge for both NiCd and NiMH batteries; fast-charge is terminated when the rate of temperature rise exceeds a preset rate.

Table 1 provides some guidelines to help in the selection of the proper fast-charge termination method, but the manufacturer's recommendations take priority in case of conflict.

Table 1a. Fast-Charge Termination Methods for NiMH Batteries

Charge Rate	$\Delta T/\Delta t$	Negative ΔV	Max Voltage	Max Time	Max Temp.
$>C/2$	Yes	No	Yes	Yes	Yes

Table 1b. Fast-Charge Termination Methods for NiCd Batteries

Charge Rate	$\Delta T/\Delta t$	Negative ΔV	Max Voltage	Max Time	Max Temp.
$>2C$	Yes	Yes	Yes	Yes	Yes
$2C$ to $C/2$	*	*	Yes	Yes	Yes

* Use one or both of these termination methods.

Figure 1 shows a standard application circuit for a switched-mode battery charger that charges NiMH batteries at a rate of C. Though this circuit is shown for NiMH batteries, it can be used for NiCd batteries (see Table 1b). The description below will use this standard application to explain, in detail, the functionality of the MAX2003/MAX2003A.

Battery Sense Voltage

The BAT pin measures the per-cell voltage of the battery pack; this voltage is used to determine fast-charge initiation and termination. The voltage is determined by the resistor-divider combination R_{B1} and R_{B2} , shown in Figure 1, where:

$$\text{Total Number of Cells} = (R_{B1} / R_{B2}) + 1$$

Since BAT has extremely high input impedance (50M Ω minimum), reasonable values can be selected for resistors R_{B1} and R_{B2} . These values, however, must not be low enough to drain the battery or high enough to unduly lengthen the time constant of the signal going to the BAT pin. The total resistance value from the positive to negative terminal of the battery ($R_{B1} + R_{B2}$) should be between 100k Ω and 500k Ω to prevent these problems.

A simple RC lowpass filter (R_B , C_B) may be needed to give a more accurate reading by removing any noise that may be present. Remember that the RC time delay from the cell to BAT must not exceed 200ms or the battery detection logic might not function properly ($R_B \times C_B < 200\text{ms}$).

NiCd/NiMH Battery Fast-Charge Controllers

MAX2003/MAX2003A

4

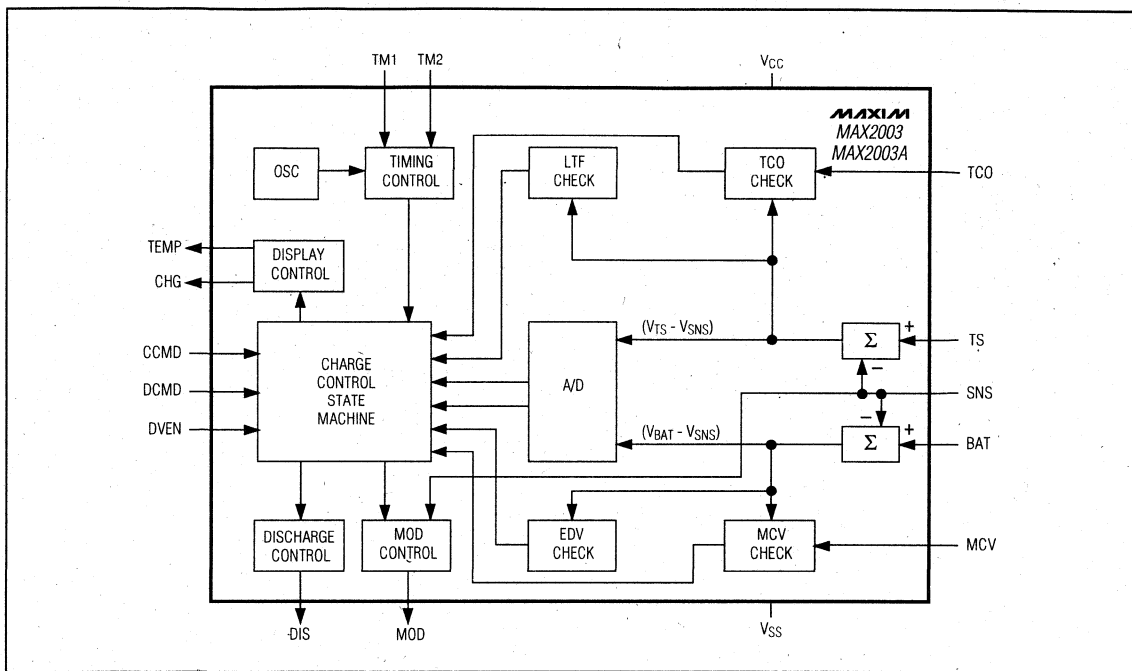


Figure 2. Block Diagram

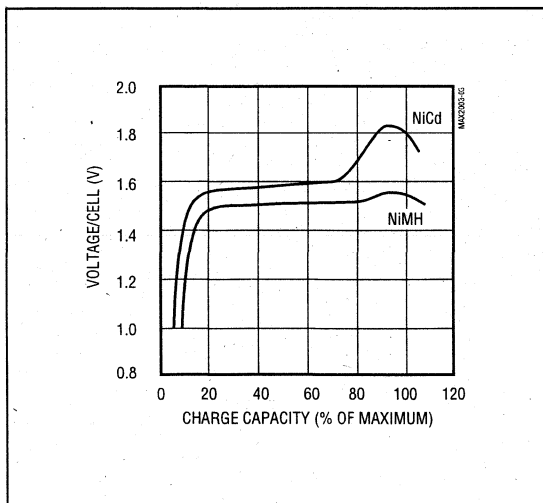


Figure 3. Voltage-Charge Characteristics of NiCd and NiMH Batteries

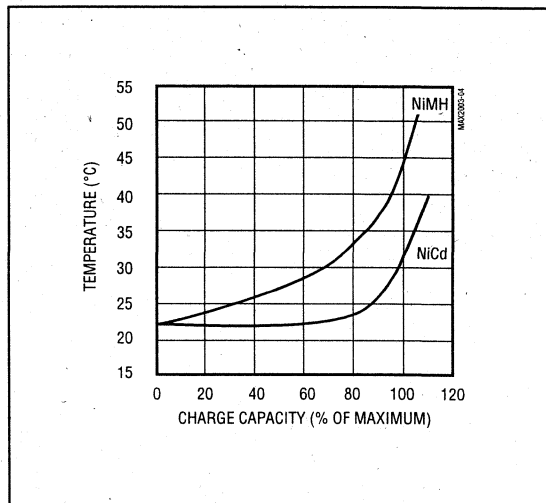


Figure 4. Temperature-Charge Characteristics of NiCd and NiMH Batteries

NiCd/NiMH Battery Fast-Charge Controllers

Temperature Measurement

The MAX2003/MAX2003A employs a negative temperature-coefficient (NTC) thermistor to measure the battery's temperature. This temperature value can be used to determine start and termination of fast-charge. The two temperature conditions that can be used for fast-charge termination are:

- Maximum Temperature
- Rate-of-Change of Temperature ($\Delta T/\Delta t$)

Figure 5 shows the various temperature cutoff points and the typical voltages that the device will see at the TS pin.

VLTF (low-temperature fault voltage) refers to the voltage at TS when the battery temperature is too low, and VHTE (high-temperature fault voltage) refers to the high-temperature cutoff. If the voltage is outside these limits, the MAX2003/MAX2003A will not enter fast-charge mode. After fast-charge is initiated, the termination point for high-temperature termination is VTCO (temperature cutoff voltage), rather than VHTE. See Figure 5 for TEMP LED status.

VLTF is set internally at $0.4V_{CC}$, so (with a 5V supply) VLTF is 2V. VTCO is set up using external resistors to determine the high-temperature cutoff after fast-charge begins. VHTE is internally set to be $(VLTF - VTCO) / 8$ above VTCO.

Thermistors are inherently nonlinear with respect to temperature. This nonlinearity is especially noticed when $\Delta T/\Delta t$ measurements are made to determine charge termination. The simplest way around this is to place a resistor-divider network in parallel with the thermistor (Figure 6) to reduce the effects of nonlinearity.

The lowpass filter (R_T , C_T) placed on the TS pin attenuates high-frequency noise on the signal seen by TS.

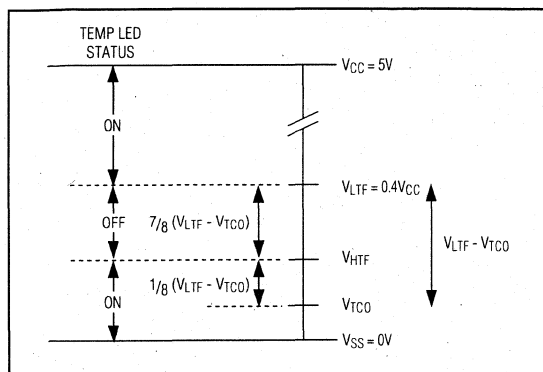


Figure 5. Temperature Measurement Scale

Charge Pending

Before fast-charge is initiated, the cell voltage and temperature of the battery pack must be within the assigned limits. If the voltage or temperature is outside these limits, the device is said to be in a "charge-pending" state. During this mode, the CHG pin will cycle low (LED on) for 0.125sec and high (LED off) for 1.375sec.

Fast-charge is normally initiated if the cell voltage is greater than VEDV (end-of-discharge voltage). If the cell voltage is too low (below VEDV), the device waits until the trickle current brings the voltage up before fast-charge is initiated. VEDV is set internally at $0.2V_{CC}$, so (for a 5V supply) VEDV is 1V.

If the temperature of the cell is not between VLTF and VHTE the device is also in a charge-pending state (see Temperature Measurement section).

Initiate Fast-Charge

If the MAX2003/MAX2003A are out of the charge-pending state, fast-charge can be initiated upon one of the following conditions:

- Battery Replacement
- Applying Power to the MAX2003/MAX2003A (battery already present)
- Digital Control Signal

During fast-charge, the CHG pin will be continuously low (LED on). For the initial period of fast-charge (the hold-off time), the voltage charge-termination methods are disabled. The hold-off time is a function of the charge rate selected by TM1 and TM2 (see Table 4).

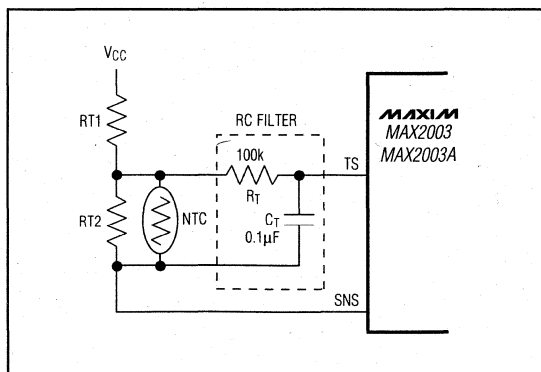


Figure 6. Thermistor Configuration for Temperature Measurement

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Table 2. Device Status on Power-Up if Battery is Already Present

CCMD	DCMD	MAX2003/MAX2003A Status when Power is Applied
Low	Low	• Fast-charge is initiated on power-up.
Low	High	• The device does not enter fast-charge immediately. • Fast-charge is initiated by the falling edge of a pulse on CCMD.
High	Low	• The device does not enter fast-charge immediately. • Fast-charge is initiated by the rising edge of a pulse on CCMD.
High	High	• Fast-charge is initiated on power-up.

Battery Replacement

Before a battery is inserted, the BAT pin is pulled higher than the maximum cell voltage (MCV) by the resistor (R_{TR}) and the divider network (R_{B1}/R_{B2}) (Figure 1). When the battery is inserted, the voltage per cell at BAT falls from the default voltage to the battery voltage. Fast-charge is initiated on a falling edge when the BAT voltage crosses the voltage on MCV.

Applying Power to the MAX2003/MAX2003A (battery already present)

There may be some cases where a battery is connected before power is applied to the MAX2003/MAX2003A. When power is applied, the device goes into reset mode for approximately 1.5sec and then samples the CCMD and DCMD pins. Its charge status is determined by the voltage at both the CCMD and DCMD pins. Table 2 summarizes the various conditions the MAX2003/MAX2003A might see on power-up.

Table 2 shows that the MAX2003/MAX2003A can be set-up for fast-charge on power-up by making sure CCMD and DCMD are at the same potential. If fast-charge on power-up is not desired, make sure CCMD and DCMD are at different logic levels during power-up, and use a digital signal to control fast-charge (see *Digital Control* section).

Digital Control

The CCMD pin can be used to initiate fast-charge. This is useful when neither the power supply nor the battery can be removed from the charger. The CCMD signal needed to initiate fast-charge depends on the potential at DCMD. If DCMD is low, a rising edge on CCMD initiates fast-charge. If DCMD is high, a falling edge on CCMD provides the fast-charge signal. Table 3 summarizes the conditions used to start fast-charge.

Table 3. Digital Control of Fast-Charge (VCC and battery present)

CCMD	DCMD	CCMD Status to Initiate Fast-Charge
	Low	• Fast-charge is initiated by a rising edge on CCMD.
	High	• Fast-charge is initiated by a falling edge on CCMD.

Discharge-Before-Charge (optional)

The discharge-before-charge function is optional and can be used to condition old batteries. It is especially useful in NiCd batteries, since it alleviates the voltage depression problems associated with partially discharged NiCd cells. The discharge-before-charge function is initiated by a rising edge into DCMD.

When the digital signal is applied, the DIS pin will be pulled high, turning on the attached circuit and discharging its battery. The discharge process continues until the single cell voltage drops below 0.2V_{CC}. During the discharge phase, the CHG pin will be low (LED on) for 1.375sec and high (LED off) for 0.125sec.

The MAX2003/MAX2003A does not control the current during discharge-before-charge. If the discharge rate is too great, the battery could overheat and be damaged. The battery manufacturer will be able to specify a safe discharge rate, but a rate of C or slower is typically acceptable. It is also important to choose components (Q2, R_{DIS}) that are rated for that particular discharge rate. Since the gate-source drive for Q2 can be as low as 4.5V, use a logic-level MOSFET.

Fast-Charge Current

The fast-charge current can be generated using two categories of circuits:

- Circuits with a sense resistor (R_{SNS})
- Circuits without sense resistor (SNS tied to V_{SS})

Circuits with SNS Resistor

The standard application circuit of Figure 1 uses an inductor and a switched mode of operation to supply the current. The charge current is determined by the sense resistor placed between the negative terminal of the battery (SNS) and ground (V_{SS}).

The SNS pin is the input to a comparator with hysteresis. If the voltage at SNS drops below 0.044V_{CC}, the MOD pin is turned on. If the SNS voltage is above 0.050V_{CC}, MOD is turned off. In the switched mode of operation, the SNS voltage ramps between 0.044V_{CC} and 0.050V_{CC}, which is 220mV and 250mV when V_{CC}

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is 5V (Figure 7). The average voltage at SNS, therefore, is 235mV, and can be used to calculate the charge current as follows:

$$I_{\text{CHARGE}} = 0.235V / R_{\text{SNS}}$$

where R_{SNS} is the sense resistor and I_{CHARGE} is the charge current required.

Circuits without SNS Resistor

In some applications (shown later), SNS is tied directly to ground. In these cases, the MOD pin remains on until any one charge-termination condition is exceeded (Figure 8). A reasonable external current limit (such as a current-limited DC source) must be provided for these applications, to prevent battery damage due to excessive charge currents.

Charge Termination

The MAX2003 has several charge-termination methods. The termination method selected depends on the type of battery and charge rate used. Table 1 summarizes the conditions used to terminate fast-charge with different battery types and charge rates.

Temperature Rate Termination

The Temperature Rate Termination ($\Delta T/\Delta t$) method terminates fast-charge when a particular rate-of-change in temperature is exceeded. As the battery begins fast-charge, its temperature increases at a slow rate. When the battery nears full capacity, this rate of temperature change increases. When the rate of temperature change exceeds a preset number, fast-charge is terminated. This method of fast-charge termination can be used for both NiCd and NiMH batteries.

The MAX2003 samples the voltage at the TS pin every 34 seconds and compares it with a value taken 68 seconds earlier. Since an NTC thermistor is used for temperature measurements, a gradual rise in temperature will result in successively lower voltage readings. If the new reading is more than $0.0032V_{\text{CC}}$ (16mV for $V_{\text{CC}} = 5V$) below the old reading, fast-charge is terminated.

The MAX2003A varies the sampling interval as a function of charge rate (Table 4). As the charge rate increases, the sampling interval decreases, thereby allowing more accurate termination of fast charge.

Note: This method of charge termination is valid only when the battery's temperature is between V_{LTF} and V_{TCO} (Figure 5).

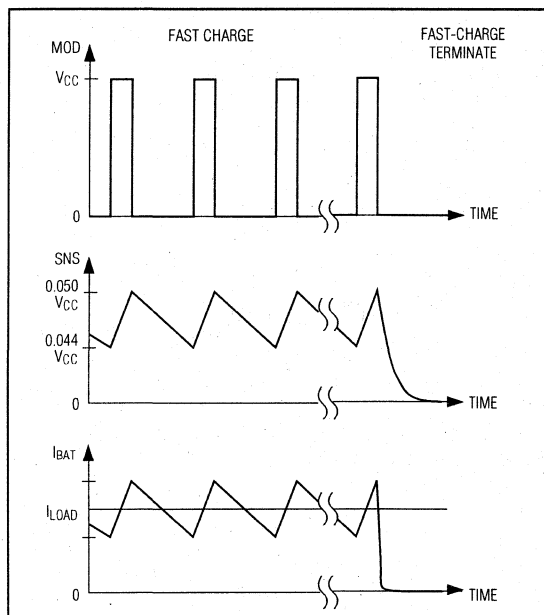


Figure 7. Current Regulation with an SNS Resistor

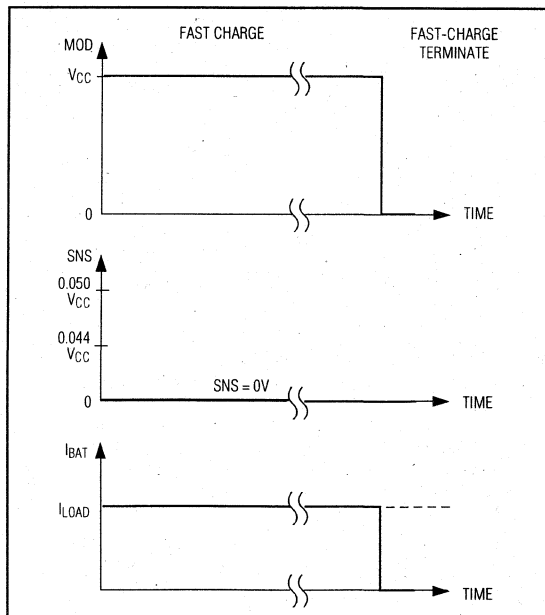


Figure 8. Current Regulation without an SNS Resistor

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Negative Delta Voltage Termination

The Negative Delta Voltage Termination ($-\Delta V$) method measures a negative delta voltage to determine termination of fast-charge. After maximum charge is reached, the terminal voltage of NiCd batteries declines significantly, whereas the terminal voltage of NiMH batteries does not. Hence, the $-\Delta V$ method of fast-charge termination is suitable for NiCd batteries, but not for NiMH batteries.

The MAX2003/MAX2003A sample the BAT pin every 34 seconds and compare it with all previous values. If the new value is less than any of the previous values by more than 12mV, a negative delta voltage has been detected and fast-charge is terminated.

Note: This method of charge termination is valid only when the voltage at BAT is between V_{MCV} and $V_{MCV} - 0.2V_{CC}$.

The $-\Delta V$ method is inhibited during the hold-off time to prevent false termination of fast-charge. The hold-off time depends on the charge rate used, and is selected by the inputs TM1 and TM2 (as shown in Table 4). After the hold-off time has expired, the device begins to monitor BAT for a voltage drop.

Maximum Temperature Termination

The Maximum Temperature Termination method is used as a safety net to prevent problems, and should never be needed under normal operation of the charger. The maximum temperature that the battery can reach during fast-charge has a corresponding voltage—the temperature cutoff voltage (V_{TCO}), as seen in Figure 5. This voltage is set externally at the TCO pin using a resistor divider from V_{CC} . Although rarely experienced, an excessively low temperature will also terminate fast-charge. The minimum temperature is the low temperature fault (V_{LTF}). This value is internally set at $0.4V_{CC}$.

When the thermistor exceeds these temperature limits, fast-charge is terminated. The thermistor configuration shown in Figure 5 is used to measure the battery's temperature and scale it to operate from V_{LTF} to V_{TCO} . Resistors R_{T1} and R_{T2} are calculated to provide the required cutoff at V_{TCO} . See the *Design Guide* section for a detailed design example.

Maximum Voltage Termination

The Maximum Voltage Termination method is another safety feature designed to work if something is drastically wrong. Under normal operation of the charger, this condition should only be reached when the battery is removed.

The maximum cell voltage expected is applied at the MCV pin using a resistor-divider network. If the cell volt-

age measured at BAT exceeds that at MCV, fast-charge is terminated. For most applications using both NiCd and NiMH batteries, this voltage (V_{MCV}) can be set to 1.9V.

The MAX2003/MAX2003A do not terminate fast-charge if the maximum voltage is reached before the hold-off time has expired. If the cell voltage is greater than the MCV during the hold-off time, the device will continue fast-charge until the hold-off time has expired, and then it will terminate fast-charge. The hold-off time is determined by the inputs TM1 and TM2, as shown in Table 4.

Maximum Timeout Termination

The final method is Maximum Timeout Termination, which (like the maximum voltage and maximum temperature methods) is another backup safety feature. The timeout time depends on the charge rate selected and is set by the control signals TM1 and TM2. Table 4 shows a list of different timeout periods available for different control-signal inputs. If the timeout is reached before any other termination method is seen, fast-charge is terminated to protect the charger and battery.

Top-Off Charge

Top-off charge is used to provide the last bit of charge needed to reach full capacity after fast-charge is terminated. Top-off charging puts slightly more energy into the battery than simple trickle charging, and can be used for both NiCd and NiMH batteries. Select it by choosing the appropriate control signals on TM1 and TM2 (Table 4).

Table 4. Programmable Inputs for Timeout/Hold-Off/Fast-Charge/Top-Off/Pulse Trickle ($V_{CC} = 5V$)

TM1	TM2	Fast-Charge Rate	Fast-Charge Timeout (min)	Hold-Off Time $\Delta V/MCV$ (sec)	Top-Off Charge	MAX2003A Trickle Charge (s) On/Off	
GND	GND	C/4	360	140	Disable	Disable	
Open	GND	C/2	180	820	Disable	1	16
V_{CC}	GND	C	90	410	Disable	1	32
GND	Open	2C	45	200	Disable	1	64
Open	Open	4C	23	100	Disable	1	128
V_{CC}	Open	C/2	180	820	*Enable	0.5	16
GND	V_{CC}	C	90	410	*Enable	0.5	32
Open	V_{CC}	2C	45	200	*Enable	0.5	64
V_{CC}	V_{CC}	4C	23	100	*Enable	0.5	128

* MAX2003 is on for 4sec and off for 30sec.

MAX2003A is on for 0.5sec and off for 3.5sec.

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Table 5. Charge Status

Charge State	CHG LED Status
Battery Absent	LED off
Charge Pending	LED on for 0.125sec, off for 1.375sec
Discharge-Before-Charge	LED on for 1.375sec, off for 0.125sec
Fast-Charge	LED on
Charge Complete and Top-Off	LED on for 0.125sec, off for 0.125sec

The top-off charge is done at 1/8 the fast-charge rate. For the MAX2003, the MOD pin is activated in every 34 second period to supply current to the battery for 4 seconds (MOD oscillates for 4 seconds and stays low for 30 seconds) (Figure 7). If external regulation is used (SNS tied to ground), MOD stays high for 4 seconds and low for 30 seconds (Figure 8). This top-off process continues until the fast-charge timeout (Table 4) is exceeded, or if a maximum temperature or maximum voltage condition is detected. The MAX2003A is slightly modified to turn the MOD pin on for 0.5sec in every 4 second period. This shorter on-time reduces battery heat and increases charge acceptance. During the top-off charge, the CHG pin will cycle low (LED on) for 0.125sec and high (LED off) for 0.125sec.

Trickle-Charge

A trickle-charge is applied to the battery after fast-charge and top-off charge have terminated to compensate for self discharge. There are two methods of trickle charge: constant and pulsed.

Pulsed Trickle-Charge (MAX2003A)

The MAX2003A provides a pulsed trickle-charge to the battery by turning on the MOD pin briefly during a fixed period of time. The duty cycle of the pulse is a function of the programmable inputs TM1 and TM2 (Table 4). The MAX2003A does not use the trickle resistor to provide the trickle charge. However, the trickle resistor cannot be entirely omitted because it is also used for the battery-detect circuitry.

Constant Trickle-Charge (MAX2003)

The MAX2003 provides a steady trickle-charge to the battery by connecting a resistor from the DC supply to the positive battery terminal. This resistor has a dual purpose, in that it provides a trickle-charge and pulls the BAT pin above the MCV when the battery is absent.

The trickle-charge rate depends on the type of battery used. For NiCd batteries, a nominal trickle-charge rate

would be C/16, and NiMH batteries could use a rate of C/40. The resistor value used depends on the maximum DC voltage and the typical battery voltage. For example, a six-cell 800mAh NiCd pack with a nominal voltage of 1.2V per cell would have a total voltage of $1.2V \times 6V = 7.2V$. If the DC supply voltage used is 14V, the voltage across the trickle resistor would be $14.0V - 7.2V = 6.8V$. The trickle current needed would be $C/16 = 800 / 16 = 50mA$. The trickle resistor would therefore be $R_{TR} = 6.8V / 50mA = 150\Omega$. Similar calculations should be made for NiMH batteries using C/40 as the trickle-charge rate.

If a trickle-charge is not needed, a higher value of trickle resistor (like 100k Ω) can be selected to sense the battery insertion.

Charge Status

The CHG pin is connected to a LED that indicates the operating mode. Table 5 summarizes the different charge conditions.

Design Guide

Using the circuit of Figure 1 as an example, the following nine steps show how to design a 1.7A switch-mode fast-charger that can charge a Duracell DR17 (NiMH six-cell battery pack with a 1700mAh capacity).

1) Select DC Power Supply. The first step is to select the DC power supply (such as a wall cube). The minimum supply voltage should have a supply equal to about 2V per cell, plus 1V headroom for external circuitry ($(2V/cell) + 1V$). The minimum supply voltage must be greater than 6V. If, as in our example, there are six cells, a minimum supply of about 13V is needed ($(6 \text{ cells} \times 2V) + 1V$).

2) Determine Charge Rate. The charge rate, or fast-charge current (I_{FAST}), is determined by two factors: the capacity of the battery, and the time in which the user wants the battery to be charged. The battery manufacturer recommends a maximum fast-charge rate, which must not be exceeded.

$$I_{FAST} \text{ (mA)} = \frac{\text{Capacity of Battery (mAh)}}{\text{Charge Time (h)}}$$

For example, if a 1700mAh battery needs to be charged in two hours (C/2), a fast-charge current of at least 850mA is needed. A charge rate of C/2 will ideally charge a battery in two hours but, because of inefficiencies in a battery's chemical processes, the time could be 30% to 40% more. Our example circuit (Figure 1) charges the Duracell battery pack at a C rate of 1.7A, which should fully charge a discharged battery in approximately 80 minutes.

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3) Select Sense Resistor. The sense resistor determines the rate at which the battery is fast-charged. The sense pin, SNS, has an average voltage of 235mV (see *Detailed Description*) and, since the charge current (IFAST) is known from above, the resistor can be calculated by:

$$R_{SNS} = V_{SNS} / I_{FAST} = 0.235 / I_{FAST}$$

In this example, a fast-charge current of 1.7A requires a sense resistor of about 0.14Ω (1 watt).

4) Select TM1 and TM2. Once the charge rate is determined, Table 4 can be used to select the TM1 and TM2 inputs. TM1 and TM2 set the safety timeout, hold-off time, and top-off enable (see *Fast-Charge Termination* section in the *Detailed Description*).

In Figure 1, a fast-charge rate of C with top-off would require TM1 to be GND and TM2 to be VCC.

5) Select RB1 and RB2. The MAX2003A requires the user to select RB1 and RB2 to indicate the number of cells in the battery. The total resistance value (RB1 + RB2) should be between 100kΩ and 500kΩ to prevent any problems with noise. In Figure 1 (with six cells) RB1 is selected to be 100kΩ and, from the following equation:

$$R_{B2} = R_{B1} / (\text{Number of Cells} - 1) = 100k\Omega / (6 - 1)$$

RB2 can be calculated to be 20kΩ.

6) Select Temperature-Control Components. Most sealed rechargeable battery packs have a built-in thermistor to prevent air currents from corrupting the accurate temperature measurements. The thermistor size and temperature characteristics can be obtained from the battery-pack manufacturer, to help in designing the rest of the circuit. Three-terminal battery packs that incorporate a thermistor generally share a common connection for the thermistor and the battery negative terminal. Large charging currents may produce voltage drops across the common negative connector, causing errors in thermistor readings. Using separate contacts for the thermistor ground sense and the battery ground sense at the negative battery terminal will reduce these errors. If an external thermistor is to be used, take care to ensure that it is placed in direct contact with the battery, and that the battery/thermistor set-up is placed in a sealed container.

Neither NiCd nor NiMH batteries should be fast-charged outside the maximum and minimum temperature limits. However, some applications also require termination using the $\Delta T/\Delta t$ criterion. The resistors RT1 and RT2 (Figure 1) will determine the temperature cutoff (VTCO) and the rate-of-change of temperature ($\Delta T/\Delta t$). Though NiCd batteries do not always require termination using the $\Delta T/\Delta t$ feature, it is not possible to isolate and disable this mode. It is therefore recommended

that NiCd and NiMH batteries use the same $\Delta T/\Delta t$ termination parameters.

The Duracell DR17 battery pack used in our example circuit recommended a low fault temperature (VLTF) of +10°C and a maximum temperature cutoff (VTCO) of +50°C. These maximum temperature values will never be reached in most cases, but are used as a safety net to prevent battery damage. According to Duracell, the 10kΩ thermistor inside the pack varies from 17.96kΩ at +10°C to 4.16kΩ at +50°C.

The circuit in Figure 1 will be designed so that a battery temperature change of 1°C/min will result in fast-charge termination. At 1°C/min, the battery will take 40 minutes to change 40°C (10°C to 50°C). Since a charge rate of C is used for this example, Table 4 shows that the MAX2003A samples the TS pin every 68 seconds and compares it with a value taken 136 seconds earlier. The device will terminate fast-charge if the voltage at TS changes by more than 0.0032VCC (16mV for VCC = 5V). At a charge rate of 16mV every 136 seconds, the TS pin will charge 280mV in 40 minutes (40min x 60sec/min x 16mV/136sec).

The low fault temperature (VLTF) is set internally at 0.4VCC, which is 2.0V for a supply of 5V. The temperature cutoff voltage (VTCO) will be 280mV below VLTF, or:

$$V_{TCO} = (2.00V - 0.28V) = 1.72V$$

Figure 5 shows that, at any given temperature:

$$V_{TS} = V_{CC} (R_{T2} \parallel R_{NTC}) / [(R_{T2} \parallel R_{NTC}) + R_{T1}]$$

When the battery temperature is +10°C, the voltage is:

$$V_{TS10} = V_{CC} (R_{T2} \parallel R_{NTC10}) / [(R_{T2} \parallel R_{NTC10}) + R_{T1}]$$

And at +50°C:

$$V_{TS50} = V_{CC} (R_{T2} \parallel R_{NTC50}) / [(R_{T2} \parallel R_{NTC50}) + R_{T1}]$$

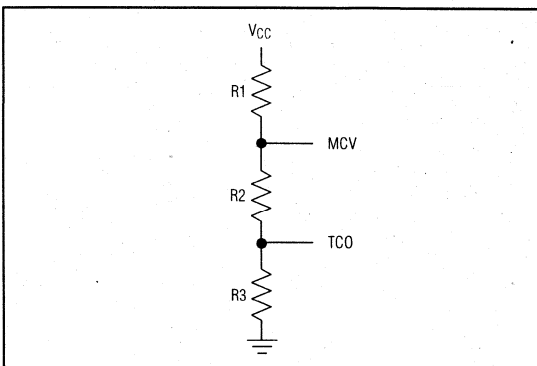


Figure 9. Resistor Configuration for MCV and TCO

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From solving these simultaneous equations:

$$RT_2 = [(X) (R_{NTC10}) - (R_{NTC50})] / (1 - X)$$

$$RT_1 = [(RT_2) (R_{NTC10}) (V_{CC} - V_{TS10})] / [V_{TS10} (RT_2 + R_{NTC10})]$$

$$\text{where } X = \frac{[(R_{NTC50})(V_{TS10})(V_{CC} - V_{TS50})]}{[(R_{NTC10})(V_{TS50})(V_{CC} - V_{TS10})]}$$

Using $R_{NTC50} = 4.16k\Omega$, $R_{NTC10} = 17.96k\Omega$, $V_{TS50} = 1.72V$, and $V_{TS10} = 2.00V$, it can be calculated that $RT_1 = 1.599k\Omega$ and $RT_2 = 2.303k\Omega$.

Select preferred resistor values for R_{T1} (2.21k Ω) and R_{T2} (1.62k Ω). The actual voltages on MCV and TCO can be verified as follows:

$$\begin{aligned} V_{TS10} &= \frac{V_{CC}(R_{T2} \parallel R_{NTC10})}{[(R_{T2} \parallel R_{NTC10}) + R_{T1}]} \\ &= \frac{5(1.62k\Omega \parallel 17.96k\Omega)}{[(1.62k\Omega \parallel 17.96k\Omega) + 2.21k\Omega]} \\ &= 2.01V \\ V_{TS50} &= \frac{V_{CC}(R_{T2} \parallel R_{NTC50})}{[(R_{T2} \parallel R_{NTC50}) + R_{T1}]} \\ &= \frac{5(1.62k\Omega \parallel 4.16k\Omega)}{[(1.62k\Omega \parallel 4.16k\Omega) + 2.21k\Omega]} \\ &= 1.72V. \end{aligned}$$

7) Select Maximum Cell Voltage (MCV) and Temperature Cutoff (TCO). The MCV and TCO can be selected with a resistor-divider combination (Figure 9). In our example, TCO has been set to +10°C, which corresponds to a voltage of 1.72V at the TS pin. The MCV for most fast-charge batteries can be set to about 1.9V. To minimize the current load on VCC, choose R1 in the range of 20k Ω to 200k Ω . In this example, choose $R_1 = 60.4k\Omega$, then calculate R3 and R2 as follows:

$$R_3 = (V_{TCO} \times R_1) / (V_{CC} - V_{MCV}) = 33.5k\Omega \text{ (1\%)} \\ \text{and}$$

$$R_2 = (V_{MCV} \times R_1) / (V_{CC} - V_{MCV}) - R_3 = 3.51k\Omega \text{ (1\%)}$$

Select preferred resistor values for R_2 (3.48k Ω) and R_3 (33.2k Ω). The actual voltages on MCV and TCO can be verified as follows:

$$V_{TCO} = V_{CC} (R_3) / (R_1 + R_2 + R_3) = 1.71V \\ \text{and}$$

$$V_{MCV} = V_{CC} (R_2 + R_3) / (R_1 + R_2 + R_3) = 1.89V.$$

8) Select Trickle Resistor (MAX2003 only). The trickle resistor (R_{TR}) is selected to allow a trickle-charge rate of C/16 to C/40. The resistor value is given by:

$$R_{TR} = (V_{DC} - V_{BAT}) / I_{TR}$$

where I_{TR} is the required trickle current, V_{DC} is the DC supply voltage, and V_{BAT} is the number of cells times the cell voltage after fast-charge.

In our example, the 1700mAh NiMH battery needs a trickle current of C/40; i.e., 42mA (1700mAh/40h). Therefore, the minimum voltage (from the formula above) is as follows:

$$R_{TR} = [13.0V - (6 \times 1.2V)] / 42mA \approx 150\Omega$$

The maximum power dissipated in the resistor can be calculated by:

$$\text{Power} = (V_{DC} - V_{BAT(MIN)})^2 / R_{TR}$$

where $V_{BAT(MIN)}$ is the minimum cell voltage, V_{DC} is the DC supply voltage, and R_{TR} is the trickle resistor value.

Since a shorted battery could have 0V, this must be the minimum cell voltage possible. Therefore the power dissipated in the trickle resistor would be:

$$\text{Power} = (13 - 0)^2 / 150 = 1.2W$$

A 2W, 150 Ω resistor should be sufficient for the trickle-charge resistor. For the MAX2003A, refer to *Trickle-Charge* section.

9) Select Inductor. The inductor value can be calculated using the formula:

$$V_L = L \delta i / \delta t$$

where V_L is the maximum voltage across the inductor, L is the minimum inductor value, δi is the change in inductor current, and t is the minimum on-time of the switch.

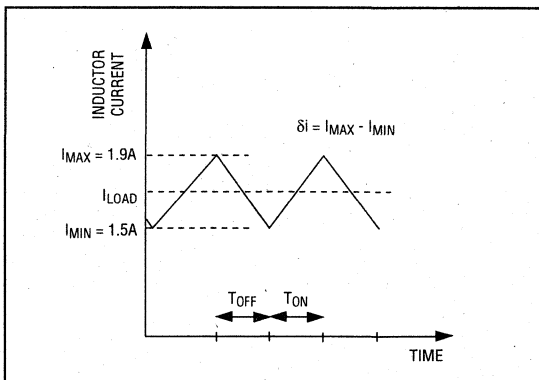


Figure 10. Inductor-Current Waveform in Continuous-Conduction Mode

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In order to provide high currents with minimum ripple, the device must function in the continuous-conduction mode. Figure 10 shows a current waveform of an inductor in the continuous-conduction mode (where the coil current never falls to zero).

The average load current (I_{LOAD}) through the inductor must be 1.7A, so a peak current (I_{MAX}) of 1.9A should give a fairly low ripple while keeping the inductor size minimal. This means that the total current change (Figure 10) across the inductor is $\delta i = 2 (1.9 - 1.7) = 0.4A$.

The maximum voltage across the inductor is present when the battery voltage is at its minimum. The minimum cell voltage at the start of fast-charge will be 1V per cell, giving a battery voltage of 6V for 6 cells. The maximum voltage (V_L) across the inductor is therefore:

$$V_L = (\text{input voltage} - \text{minimum battery voltage})$$

The input voltage for this application is 13V, so the maximum voltage is:

$$V_L = (13V - 6V) = 7V$$

The minimum on-time δt of the switch is given by:

$$\delta t = (V_{OUT} / V_{IN}) \times \text{PERIOD}$$

where V_{OUT} is the minimum battery voltage, V_{IN} is the maximum input voltage, and PERIOD is the period of the switching signal.

The maximum input voltage for this application will be 14V, and the maximum allowed switching frequency of 100kHz gives a period of 10 μ s. The minimum on-time will therefore be:

$$\delta t = (V_{OUT} / V_{IN}) \times \text{PERIOD} = (6V / 13V) \times 10\mu s = 4.62\mu s$$

The inductor value can be calculated from:

$$L = V \delta t / \delta i = (7V \times 4.62\mu s) / 0.4A = 81\mu H.$$

Table 6. External Component Sources

Device	Manufacturer	Phone Number	Fax Number
Power Supply	Advanced Power Solutions	(510) 734-3060	(510) 460-5498
Thermistor	Alpha Thermistor	(800) 235-5445	(619) 549-4791
Power MOSFET & Darlington Transistor	Motorola	(602) 244-3742	(602) 244-4015
Battery	Duracell	(800) 431-2658	(203) 791-3273
	Energizer Power Systems	(904) 462-3911	(904) 462-4726

If this inductor value is used, the actual switching frequency will be lower than the 100kHz expected, due to comparator delays and variations in the duty cycle. The inductor value selected for our application will be 100 μ H—a preferred value just above the calculated value. It is important to choose the saturation current rating of the inductor to be a little higher than the peak currents, to prevent the inductor from saturating during operation. The inductor must be selected to ensure that the switching frequency of the MOD pin will not exceed the 100kHz maximum.

Additional Applications Information

The MAX2003/MAX2003A can use several other circuits to charge batteries. Figure 9 shows a circuit that uses a Darlington transistor to regulate the current a six-cell NiCd battery pack receives. Figure 10 shows a gated current-limited supply being used to charge a Duracell NiMH battery pack. Table 6 lists the external components used in these two application configurations.

Linear Regulation of Charge Current

The circuit in Figure 11 uses an inexpensive transistor to provide the charge current. Since the input for the MAX667 can tolerate up to 16V, this circuit can charge up to 7 cells. The MAX667 can be replaced with a different regulator if more cells need to be charged. The DC source must supply a voltage equal to 2x the number of cells, plus 2V overhead to accommodate the drop across external components.

When fast-charge is initiated, the voltage at the SNS pin is sampled and compared to the trip levels (220mV low and 250mV high). If the voltage at SNS is below 220mV, the MOD pin will switch high, and the 10k/1 μ F RC lowpass filter will pull high, turning-on the NPN transistor. This will pull the base of the Darlington TIP115 low, turning it on and allowing current to flow into the battery. When the current through the battery and SNS resistor are high enough, the voltage at SNS will exceed 250mV and the MOD pin will turn off.

The amount of current the battery receives depends on the resistor between SNS and V_{SS} . In our example circuit, the average current through the SNS resistor will be:

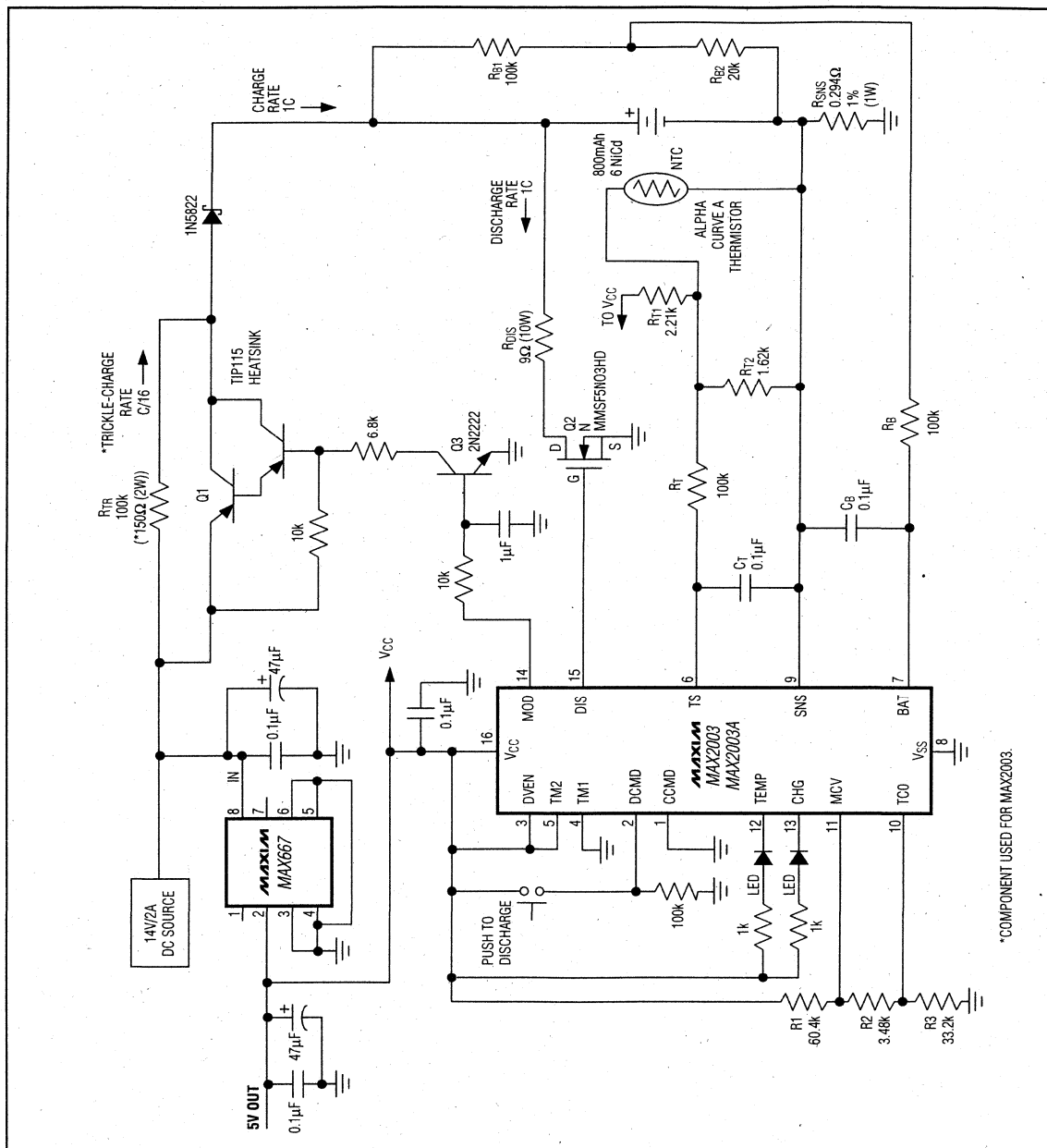
$$I_{SNS(AVG)} = V_{SNS(AVG)} / R_{SNS} = 0.235 / 0.28 = 0.84A$$

The maximum current the resistor will receive is:

$$I_{SNS(MAX)} = V_{SNS(MAX)} / R_{SNS} = 0.25 / 0.28 = 0.90A$$

The Darlington transistor must be biased to ensure that a minimum of 0.90A will be supplied. This minimum

NiCd/NiMH Battery Fast-Charge Controllers



*COMPONENT USED FOR MAX2003.

NiCd/NiMH Battery Fast-Charge Controllers

MAX2003/MAX2003A

4

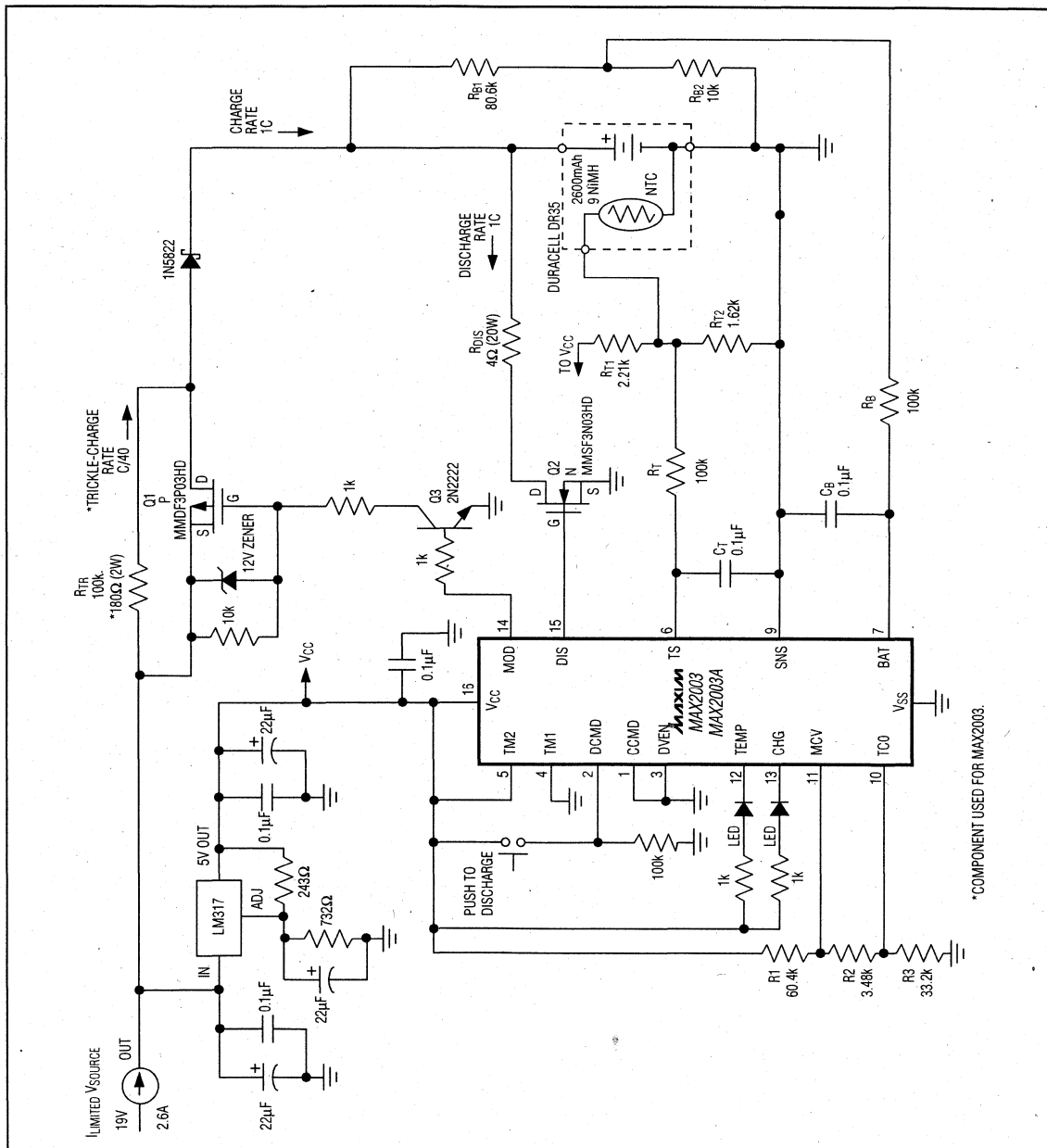


Figure 12. Current-Limited Mode for NiMH Batteries with $\Delta T/\Delta t$ Termination

NiCd/NiMH Battery Fast-Charge Controllers

current value must be sufficiently guardbanded to ensure the limiting factor is the SNS resistor, and not the transistor. In our example, the maximum current supplied by the Darlington will be guardbanded to 1.8A. Since the beta of the Darlington is typically 1000, the base current needed will be:

$$I_B = I_C / \text{BETA} = 1.8A / 1000 = 1.8mA$$

The emitter of the TIP115 will see 14V, so the base will see about 12.6V. When the MOD pin is high, the 2N2222 transistor is on and the base resistor will be:

$$R_B = V_B / I_B = 12.6V / 1.8mA \approx 6.8k\Omega$$

This 1.8A current will never be reached because MOD will be off when the SNS voltage reaches 0.25V (0.9A).

Current-Limited Supply

The circuit in Figure 12 is set up to charge a Duracell DR35 battery pack (nine cells, 2.6Ah) using a 19V, 2.6A current-limited power supply provided by Advanced Power Solutions. Since many power supplies have built-in current limiting, very few external components are required for this charging method.

The SNS pin in this circuit is tied directly to V_{SS}. This signals the MOD pin to stay high until a termination condition is met. When MOD is high, the NPN transistor is turned on, hence pulling the gate of the MOSFET low. This turns the MOSFET on and supplies current to the battery at the current limit of the source (2.6A). The 12V zener diode is placed between the source and gate of the FET to ensure the FET's maximum source-drain voltage is not exceeded.

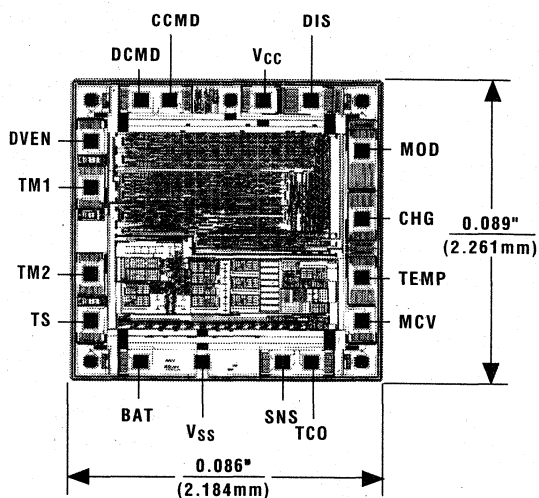
When a termination condition is reached, the MOD pin goes low to turn off the FET and terminate the fast-charge current.

Table 7. Operation Summary

Charge Status	Conditions	MOD Status	DIS Status	CHG LED Status	
				LED On (Low) (sec)	LED Off (High) (sec)
Battery Absent	$(V_{BAT} - V_{SNS}) \geq V_{MCV}$	Low	Low	—	Continuous
Initiate Discharge	Rising edge on DCMD	Low	Low	—	Continuous
Initiate Fast-Charge	a) Power applied and voltage at CCMD = DCMD b) DCMD = Low, CCMD = Rising Edge (power already present) c) DCMD = High, CCMD = Falling Edge (power already present)	Low	Low	—	Continuous
Charge Pending	Fast-charge initiated and temperature or voltage outside the set limits.	Low	Low	0.125	1.375
Discharge	Discharge initiated with temperature and voltage within set limits.	Low	High	1.375	0.125
Fast-Charge	Fast-charge initiated with temperature and voltage within set limits.	If $V_{SNS} > 0.050V_{CC}$, MOD = Low If $V_{SNS} > 0.044V_{CC}$, MOD = High	Low	Continuous	—
Charge Complete	Exceed one of the five termination conditions.	Low	Low	0.125	0.125
Top-Off Charge	Charge complete and top-off enabled without exceeding temperature and voltage limits.	MAX2003A: Activate for 0.5sec in every 4sec period. MAX2003: Active for 4sec in every 34sec period.	Low	0.125	0.125
Constant Trickle-Charge (MAX2003)	Trickle current provided by external resistor after fast-charge/top-off.	Low	Low	0.125	0.125
Pulsed Trickle-Charge (MAX2003A)	Pulse current provided by pulsing MOD pin after fast-charge/top-off.	Pulsed according to charge rate (Table 4).	Low	0.125	0.125

NiCd/NiMH Battery Fast-Charge Controllers

Chip Topography



TRANSISTOR COUNT: 5514
SUBSTRATE CONNECTED TO VSS

MAX2003/MAX2003A

4

MAXIM

5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

General Description

The MAX603/MAX604 low-dropout, low quiescent current, linear regulators supply 5V, 3.3V, or an adjustable output for currents up to 500mA. They are available in a 1.8W SO package. Typical dropouts are 320mV at 5V and 500mA, or 240mV at 3.3V and 200mA. Quiescent currents are 15 μ A typ and 35 μ A max. Shutdown turns off all circuitry and puts the regulator in a 2 μ A off mode. A unique protection scheme limits reverse currents when the input voltage falls below the output. Other features include foldback current limiting and thermal overload protection.

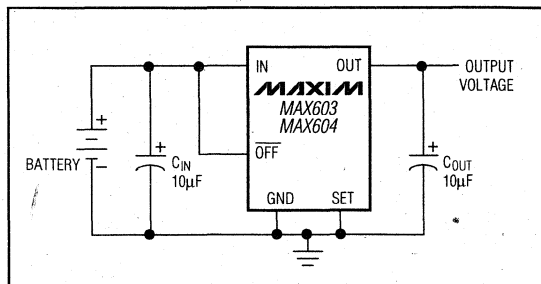
The output is preset at 3.3V for the MAX604 and 5V for the MAX603. In addition, both devices employ Dual Mode™ operation, allowing user-adjustable outputs from 1.25V to 11V using external resistors. The input voltage supply range is 2.7V to 11.5V.

The MAX603/MAX604 feature a 500mA P-channel MOSFET pass transistor. This transistor allows the devices to draw less than 35 μ A over temperature, independent of the output current. The supply current remains low because the P-channel MOSFET pass transistor draws no base currents (unlike the PNP transistors of conventional bipolar linear regulators). Also, when the input-to-output voltage differential becomes small, the internal P-channel MOSFET does not suffer from excessive base current losses that occur with saturated PNP transistors.

Applications

5V and 3.3V Regulators
1.25V to 11V Adjustable Regulators
Battery-Powered Devices
Pagers and Cellular Phones
Portable Instruments
Solar-Powered Instruments

Typical Operating Circuit



™ Dual Mode is a trademark of Maxim Integrated Products.

Features

- ♦ 500mA Output Current, with Foldback Current Limiting
- ♦ High-Power (1.8W) 8-Pin SO Package
- ♦ Dual Mode™ Operation: Fixed or Adjustable Output from 1.25V to 11V
- ♦ Large Input Range (2.7V to 11.5V)
- ♦ Internal 500mA P-Channel Pass Transistor
- ♦ 15 μ A Typical Quiescent Current
- ♦ 2 μ A (Max) Shutdown Mode
- ♦ Thermal Overload Protection
- ♦ Reverse-Current Protection

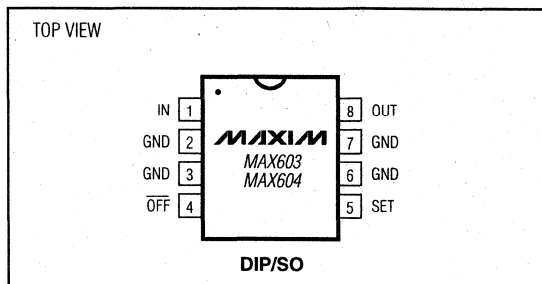
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX603CPA	0°C to +70°C	8 Plastic DIP
MAX603CSA	0°C to +70°C	8 SO
MAX603C/D	0°C to +70°C	Dice*
MAX603EPA	-40°C to +85°C	8 Plastic DIP
MAX603ESA	-40°C to +85°C	8 SO
MAX603MJA	-55°C to +125°C	8 CERDIP**
MAX604CPA	0°C to +70°C	8 Plastic DIP
MAX604CSA	0°C to +70°C	8 SO
MAX604C/D	0°C to +70°C	Dice*
MAX604EPA	-40°C to +85°C	8 Plastic DIP
MAX604ESA	-40°C to +85°C	8 SO
MAX604MJA	-55°C to +125°C	8 CERDIP**

* Dice are tested at $T_A = +25^\circ\text{C}$, DC parameters only.

** Contact factory for availability.

Pin Configuration


MAX603/MAX604
4
MAXIM

Maxim Integrated Products 4-69

Call toll free 1-800-998-8800 for free samples or literature.

5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IN or OUT to GND).....-0.3V to +12V
 Output Short-Circuit Duration1 min
 Continuous Output Current600mA
 SET, OFF Input Voltages-0.3V to the greater of
 (IN + 0.3V) or (OUT + 0.3V)
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 Plastic DIP (derate 9.09mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)727mW
 SO (derate 23.6mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)1.8W
 CERDIP (derate 8.00mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)640mW

Operating Temperature Ranges

MAX60_C_A 0°C to $+70^\circ\text{C}$
 MAX60_E_A -40°C to $+85^\circ\text{C}$
 MAX60_MJA -55°C to $+125^\circ\text{C}$
 Junction Temperature $+150^\circ\text{C}$
 Storage Temperature Range -65°C to $+160^\circ\text{C}$
 Lead Temperature (soldering, 10sec) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN} = 6\text{V}$ (MAX603) or 4.3V (MAX604), $C_{IN} = C_{OUT} = 10\mu\text{F}$, $\overline{\text{OFF}} = V_{IN}$, SET = GND, $T_J = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Typical values are at $T_J = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V _{IN}	SET = OUT, R _L = 1kΩ	MAX60_C	2.7		11.5	V
			MAX60_E	2.9		11.5	
			MAX60_M	3.0		11.5	
Output Voltage (Note 2)	V _{OUT}	I _{OUT} = 20μA to 500mA, 6.0V < V _{IN} < 11.5V	MAX603	4.75	5.00	5.25	V
		I _{OUT} = 20μA to 300mA, 4.3V < V _{IN} < 11.5V	MAX604	3.15	3.30	3.45	
Load Regulation	ΔV _{LDR}	I _{OUT} = 1mA to 500mA	MAX603C/E		60	100	mV
			MAX603M			150	
		I _{OUT} = 1mA to 300mA	MAX604		30	100	
Line Regulation	ΔV _{LNR}	(V _{OUT} + 0.5V) ≤ V _{IN} ≤ 11.5V, I _{OUT} = 25mA			7	40	mV
Dropout Voltage (Note 3)	ΔV _{DO}	I _{OUT} = 200mA	MAX603		130	220	mV
		I _{OUT} = 500mA			320	550	
		I _{OUT} = 200mA	MAX604		240	410	
		I _{OUT} = 400mA			480	820	
Quiescent Current	I _Q	3.0V ≤ V _{IN} ≤ 11.5V, SET = OUT	MAX60_C/E		15	35	μA
			MAX60_M			40	
OFF Quiescent Current	I _{Q OFF}	OFF ≤ 0.4V, R _L = 1kΩ, (V _{OUT} + 1V) ≤ V _{IN} ≤ 11.5V	MAX60_C		0.01	2	μA
			MAX60_E			10	
			MAX60_M			20	
Minimum Load Current	I _{OUT MIN}	V _{IN} = 11.5V, SET = OUT	MAX60_C			2	μA
			MAX60_E			6	
			MAX60_M			20	
Foldback Current Limit (Note 4)	I _{LIM}	V _{OUT} < 0.8V			350		mA
		V _{OUT} > 0.8V and V _{IN} - V _{OUT} > 0.7V			1200		
Thermal Shutdown Temperature	T _{SD}				160		°C
Thermal Shutdown Hysteresis	ΔT _{SD}				10		°C

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 6V (MAX603) or 4.3V (MAX604), C_{IN} = C_{OUT} = 10μF, $\overline{\text{OFF}}$ = V_{IN}, SET = GND, T_J = T_{MIN} to T_{MAX}, unless otherwise noted.

Typical values are at T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse-Current Protection Threshold (Note 5)	ΔV_{RTH}	V _{OUT} = 4.5V	MAX603	6	20		mV
		V _{OUT} = 3.0V	MAX604	6	20		
Reverse Leakage Current	I _{RVL}	V _{IN} = 0V, V _{OUT} = 4.5V (MAX603) V _{OUT} = 3.0V (MAX604)	MAX60_C	0.01	10		μA
			MAX60_E		20		
			MAX60_M		100		
Start-Up Overshoot	V _{OSSH}	R _L = 1kΩ, C _{OUT} = 10μF, $\overline{\text{OFF}}$ rise time ≤ 1μs		2			%V _{OUT}
Time Required to Exit Shutdown	t _{START}	V _{IN} = 9V, R _L = 18Ω, V $\overline{\text{OFF}}$ switched from 0V to V _{IN} , time from 0% to 95% of V _{OUT}		200			μs
Dual-Mode SET Threshold	V _{SET TH}	For internal feedback		80	30		mV
		For external feedback		150	80		
SET Reference Voltage	V _{SET}	SET = OUT, R _L = 1kΩ		1.16	1.20	1.24	V
SET Input Leakage Current	I _{SET}	V _{SET} = 1.5V or 0V		±0.01	±10		nA
OUT Leakage Current	I _{OUT LKG}	V _{IN} = 11.5V, V _{OUT} = 2V, SET = OUT	MAX60_C	0.01	2		μA
			MAX60_E		6		
			MAX60_M		20		
$\overline{\text{OFF}}$ Threshold Voltage	V _{IL $\overline{\text{OFF}}$}	Off			0.4		V
	V _{IH $\overline{\text{OFF}}$}	On, SET = OUT, V _{IN} = 4V		2.0			
		On, SET = OUT, V _{IN} = 6V		3.0			
		On, SET = OUT, V _{IN} = 11.5V		4.0			
$\overline{\text{OFF}}$ Input Leakage Current	I $\overline{\text{OFF}}$	V $\overline{\text{OFF}}$ = V _{IN} or GND		±0.01	±10		nA
Output Noise (Note 6)	e _n	10Hz to 10kHz, SET = OUT, R _L = 1kΩ, C _{OUT} = 10μF		250			μV _{RMS}

Note 1: Electrical specifications are measured by pulse testing and are guaranteed for a junction temperature (T_J) equal to the operating temperature range. C and E grade parts may be operated up to a T_J of +125°. Expect performance similar to M grade specifications. For T_J between +125°C and +150°C, the output voltage may drift more.

Note 2: (V_{IN} - V_{OUT}) is limited to keep the product (I_{OUT} × (V_{IN} - V_{OUT})) from exceeding the package power dissipation limits.

Note 3: Dropout Voltage is (V_{IN} - V_{OUT}) when V_{OUT} falls to 100mV below its nominal value at V_{IN} = V_{OUT} + 2V. For example, the MAX603 is tested by measuring the V_{OUT} at V_{IN} = 7V, then V_{IN} is lowered until V_{OUT} falls 100mV below the measured value. The difference (V_{IN} - V_{OUT}) is then measured and defined as ΔV_{DO}.

Note 4: Foldback Current Limit was characterized by pulse testing to remain below the maximum junction temperature.

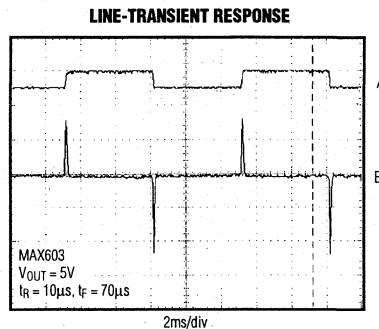
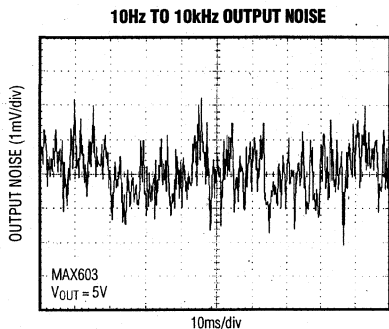
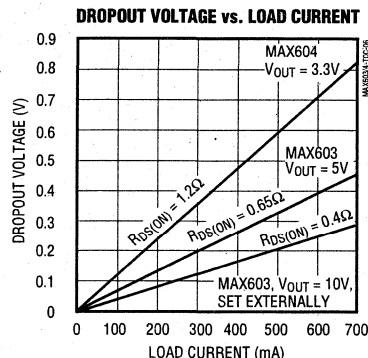
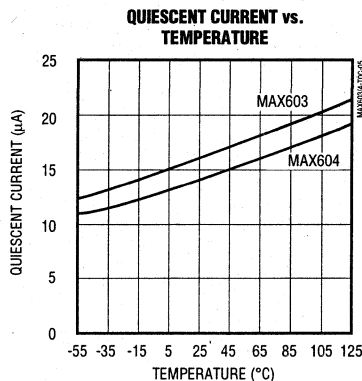
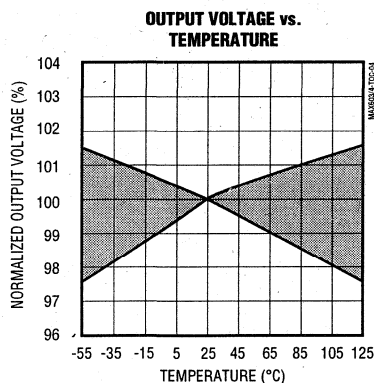
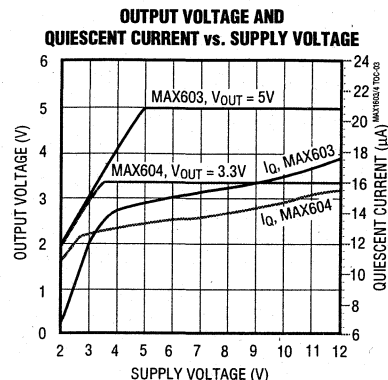
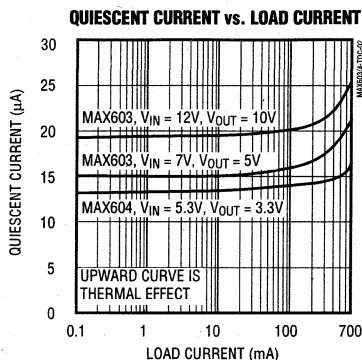
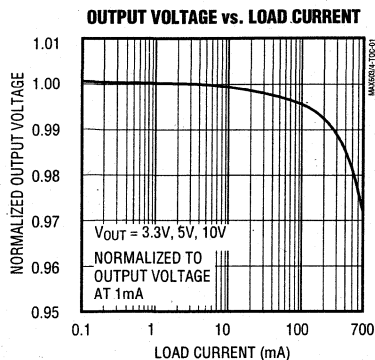
Note 5: The Reverse-Current Protection Threshold is the output/input differential voltage (V_{OUT} - V_{IN}) at which reverse-current protection switchover occurs and the pass transistor is turned off.

Note 6: Noise is tested using a bandpass amplifier with two poles at 10Hz and two poles at 10kHz.

5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

Typical Operating Characteristics

($V_{IN} = 7V$ for MAX603, $V_{IN} = 5.3V$ for MAX604, $\overline{OFF} = V_{IN}$, SET = GND, $C_{IN} = C_{OUT} = 10\mu F$, $R_L = 1k\Omega$, $T_J = +25^\circ C$, unless otherwise noted.)

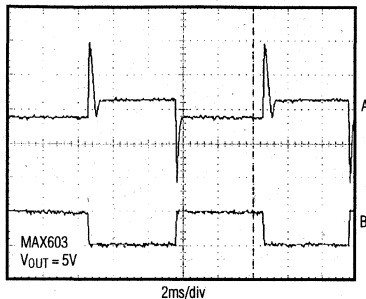


5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

Typical Operating Characteristics (continued)

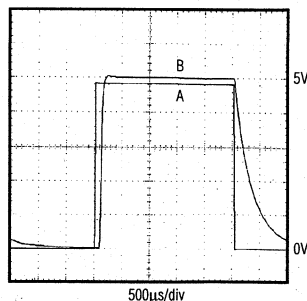
($V_{IN} = 7V$ for MAX603, $V_{IN} = 5.3V$ for MAX604, $\overline{OFF} = V_{IN}$, SET = GND, $C_{IN} = C_{OUT} = 10\mu F$, $R_L = 1k\Omega$, $T_J = +25^\circ C$, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE



A: OUTPUT VOLTAGE (100mV/div)
B: $I_{OUT} = 500mA$ (HIGH), $I_{OUT} = 5mA$ (LOW)

OVERSHOOT AND TIME EXITING SHUTDOWN MODE



A: OFF PIN VOLTAGE (1V/div)
RISE TIME = $13\mu s$
B: MAX603 OUTPUT VOLTAGE (1V/div)
DELAY = $4.936ms$, OVERSHOOT = 1%, RISE TIME = $55\mu s$

Pin Description

PIN	NAME	DESCRIPTION
1	IN	Regulator Input. Supply voltage can range from 2.7V to 11.5V.
2, 3, 6, 7	GND	Ground. These pins function as heatsinks, only in the SOIC package. All GND pins must be soldered to the circuit board for proper power dissipation. Connect to large copper pads or planes to channel heat from the IC.
4	$\overline{OFF}$	Shutdown, active low. Switch logic levels in less than $1\mu s$ with the high level above the $\overline{OFF}$ threshold.
5	SET	Feedback for Setting the Output Voltage. Connect to GND to set the output voltage to the preselected 3.3V or 5V. Connect to an external resistor network for adjustable output operation.
8	OUT	Regulator Output. Fixed or adjustable from 1.25V to 11.0V. Sources up to 500mA for input voltages above 4V.

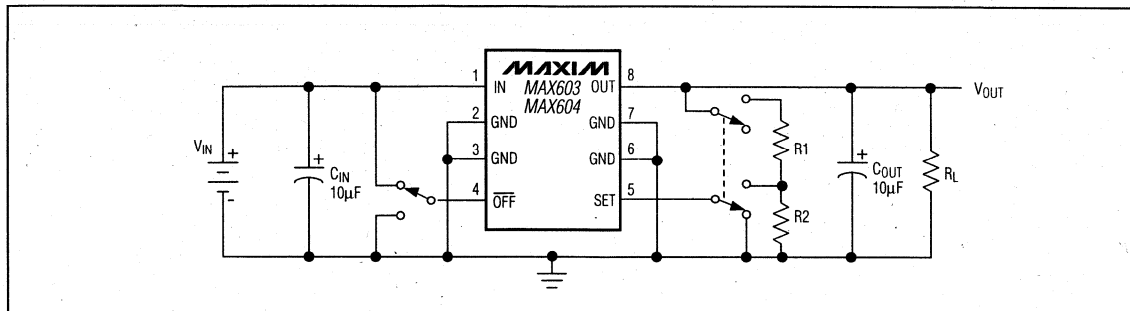


Figure 1. Test Circuit

5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

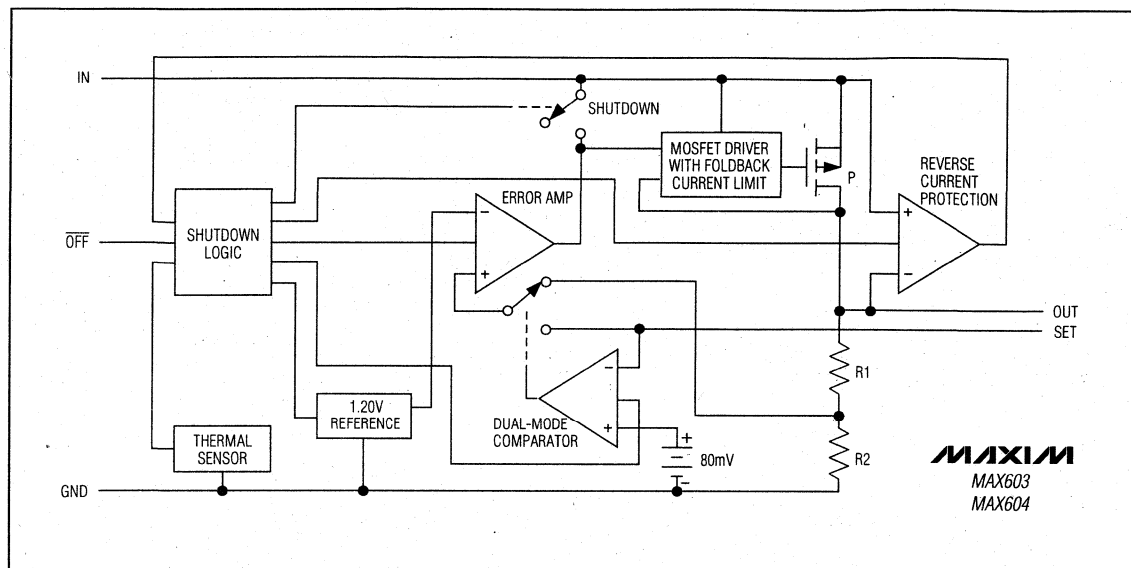


Figure 2. Functional Diagram

Detailed Description

The MAX603/MAX604 are low-dropout, low-quiescent-current linear regulators designed primarily for battery-powered applications. They supply an adjustable 1.25V to 11V output or a preselected 5V (MAX603) or 3.3V (MAX604) output for load currents up to 500mA. As illustrated in Figure 2, they consist of a 1.20V reference, error amplifier, MOSFET driver, P-channel pass transistor, dual-mode comparator, and internal feedback voltage divider.

The 1.20V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback voltage is lower than the reference, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage divider connected to the OUT pin, or an external resistor network connected to the SET pin. The dual-mode comparator examines the SET voltage and selects the feedback path used. If SET is below 80mV, internal feedback is used and the output voltage is regulated to 5V for the MAX603 or 3.3V for the MAX604. Additional blocks include a foldback current limiter, reverse current protection, thermal sensor, and shutdown logic.

Internal P-Channel Pass Transistor

The MAX603/MAX604 feature a 500mA P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The P-channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable amounts of current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The MAX603/MAX604 do not suffer from these problems and consume only 15 μ A of quiescent current under light and heavy loads, as well as in dropout.

5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

Output Voltage Selection

The MAX603/MAX604 feature dual-mode operation. In preset voltage mode, the output of the MAX603 is set to 5V and the output of the MAX604 is set to 3.3V using internal, trimmed feedback resistors. Select this mode by connecting SET to ground.

In adjustable mode, an output between 1.25V and 11V is selected using two external resistors connected as a voltage divider to SET (Figure 3). The output voltage is set by the following equation:

$$V_{OUT} = V_{SET} \left(1 + \frac{R_1}{R_2} \right)$$

where $V_{SET} = 1.20V$. To simplify resistor selection:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{SET}} - 1 \right)$$

Since the input bias current at SET is nominally zero, large resistance values can be used for R_1 and R_2 to minimize power consumption without losing accuracy. Up to $1.5M\Omega$ is acceptable for R_2 . Since the V_{SET} tolerance is less than $\pm 40mV$, the output can be set using fixed resistors instead of trim pots.

In preset voltage mode, impedances between SET and ground should be less than $10k\Omega$. Otherwise, spurious conditions could cause the voltage at SET to exceed the 80mV dual-mode threshold.

Shutdown

A low input on the $\overline{OFF}$ pin shuts down the MAX603/MAX604. In the off mode, the pass transistor, control circuit, reference, and all biases are turned off, reducing the supply current below $2\mu A$. $\overline{OFF}$ should be connected to IN for normal operation.

Use a fast comparator, Schmitt trigger, or CMOS or TTL logic to drive the $\overline{OFF}$ pin in and out of shutdown. Rise times should be shorter than $1\mu s$. Do not use slow RC circuits, leave $\overline{OFF}$ open, or allow the input to linger between thresholds; these measures will prevent the output from jumping to the positive supply rail in response to an indeterminate input state.

Since the $\overline{OFF}$ threshold varies with input supply voltage (see *Electrical Characteristics*), do not derive the drive voltage from 3.3V logic. With V_{IN} at 11.5V, the high $\overline{OFF}$ logic level needs to be above 4V.

Foldback Current Limiting

The MAX603/MAX604 also include a foldback current limiter. It monitors and controls the pass transistor's gate voltage, estimating the output current and limiting it to 1.2A for output voltages above 0.8V and $V_{IN} - V_{OUT}$

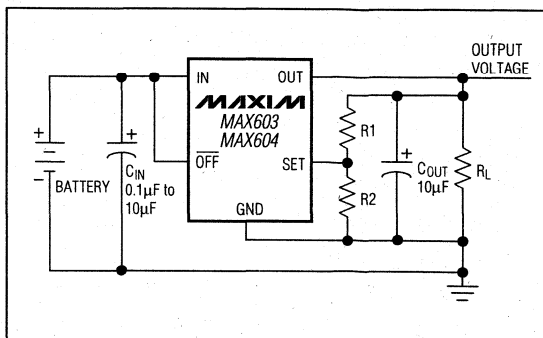


Figure 3. Adjustable Output Using External Feedback Resistors

> 0.7V. For $V_{IN} - V_{OUT} < 0.7V$ (dropout operation), there is no current limit. If the output voltage drops below 0.8V, implying a short-circuit condition, the output current is limited to 350mA. The output can be shorted to ground for one minute without damaging the device if the package can dissipate $V_{IN} \times 350mA$ without exceeding $T_J = +150^\circ C$.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX603/MAX604. When the junction temperature exceeds $T_J = +160^\circ C$, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor will turn the pass transistor on again after the IC's junction temperature cools by $10^\circ C$, resulting in a pulsed output during thermal overload conditions.

Thermal overload protection is designed to protect the MAX603/MAX604 in the event of fault conditions. For continual operation, the absolute maximum junction temperature rating of $T_J = +150^\circ C$ should not be exceeded.

Operating Region and Power Dissipation

Maximum power dissipation of the MAX603/MAX604 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. The resulting maximum power dissipation is:

$$P_{MAX} = \left(\frac{(T_J - T_A)}{(\theta_{JB} + \theta_{BA})} \right)$$

where $(T_J - T_A)$ is the temperature difference between the MAX603/MAX604 die junction and the surrounding

5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

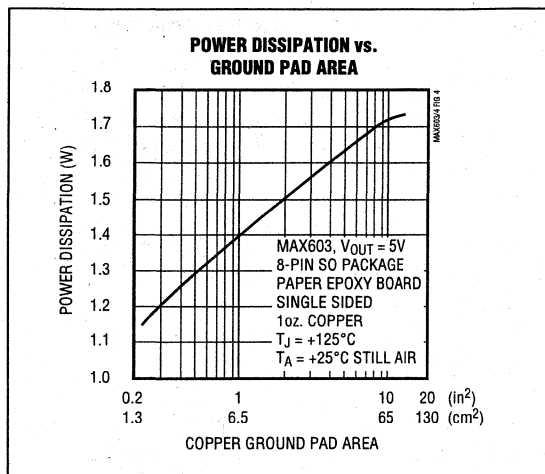


Figure 4. Typical Maximum Power Dissipation vs. Ground Pad Size.

air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package chosen, and θ_{BA} is the thermal resistance through the printed circuit board, copper traces and other materials to the surrounding air. The 8-pin SOIC package for the MAX603/MAX604 features a special lead frame with a lower thermal resistance and higher allowable power dissipation. The thermal resistance of this package is $\theta_{JB} = 42^\circ\text{C/W}$, compared with $\theta_{JB} = 110^\circ\text{C/W}$ for an 8-pin plastic DIP package and $\theta_{JB} = 125^\circ\text{C/W}$ for an 8-pin ceramic DIP package.

The GND pins of the MAX603/MAX604 SOIC package perform the dual function of providing an electrical connection to ground and channeling heat away. Connect all GND pins to ground using a large pad or ground plane. Where this is impossible, place a copper plane on an adjacent layer. The pad should exceed the dimensions in Figure 4.

Figure 4 assumes the IC is an 8-pin SOIC package, is soldered directly to the pad, has a $+125^\circ\text{C}$ maximum junction temperature and a $+25^\circ\text{C}$ ambient air temperature, and has no other heat sources. Use larger pad sizes for other packages, lower junction temperatures, higher ambient temperatures, or conditions where the IC is not soldered directly to the heat-sinking ground pad.

The MAX603/MAX604 can regulate currents up to 500mA and operate with input voltages up to 11.5V, but not simultaneously. High output currents can only be sustained when input-output differential voltages are

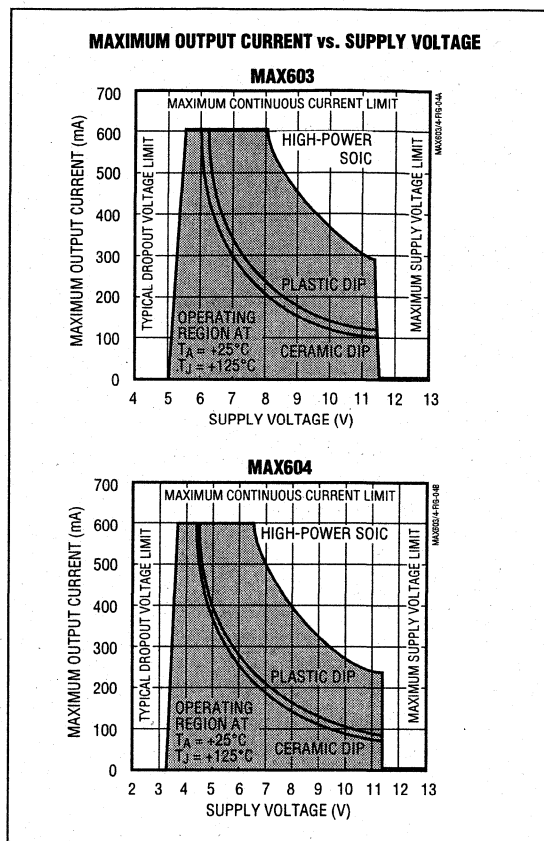


Figure 5. Power Operating Regions: Maximum Output Current vs. Differential Supply Voltage

low, as shown in Figure 5. Maximum power dissipation depends on packaging, board layout, temperature, and air flow. The maximum output current is:

$$I_{OUT(max)} = \frac{P_{MAX} \times (T_J - T_A)}{(V_{IN} - V_{OUT}) \times 100^\circ\text{C}}$$

where P_{MAX} is derived from Figure 4.

Reverse-Current Protection

The MAX603/MAX604 has a unique protection scheme that limits reverse currents when the input voltage falls below the output. It monitors the voltages on IN and OUT and switches the IC's substrate and power bus to

5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

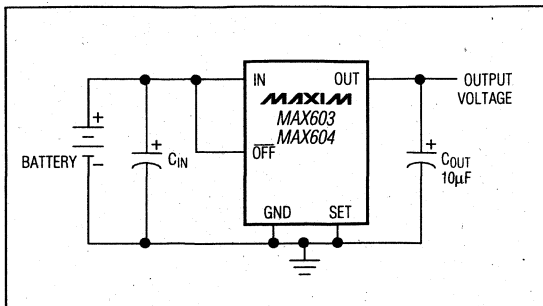


Figure 6. 3.3V or 5V Linear-Regulator Application

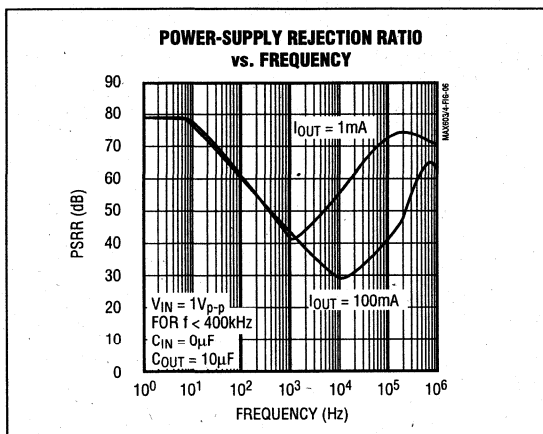


Figure 7. Power-Supply Rejection Ratio vs. Ripple Frequency

the more positive of the two. The control circuitry can then remain functioning and turn the pass transistor off, limiting reverse currents back through the device. This feature allows a backup regulator or battery pack to maintain V_{OUT} when the supply at IN fails.

Reverse-current protection activates when the voltage on IN falls 6mV (20mV maximum) below the voltage on OUT. Before this happens, currents as high as several milliamperes can flow back through the device. After switchover, typical reverse currents are limited to 0.01μA for as long as the condition exists.

Applications Information

Figure 6 illustrates the typical application for the MAX603/MAX604.

Capacitor Selection and Regulator Stability

Normally, use 0.1μF to 10μF capacitors on the input and 10μF on the output of the MAX603/MAX604. The larger input capacitor values provide better supply-noise rejection and line-transient response. Improve load-transient response, stability, and power-supply rejection by using large output capacitors. For stable operation over the full temperature range and with load currents up to 500mA, 10μF is recommended. Using capacitors smaller than 3.3μF can result in oscillation.

Noise

The MAX603/MAX604 exhibit 3mVp-p to 4mVp-p of noise during normal operation. This is negligible in most applications. When using the MAX603/MAX604 in applications that include analog-to-digital converters of greater than 12 bits, consider the ADC's power-supply rejection specifications. Refer to the output noise plot in the *Typical Operating Characteristics*.

PSRR and Operation from Sources Other than Batteries

The MAX603/MAX604 are designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Achieving these objectives requires trading off power-supply noise rejection and swift response to supply variations and load transients. Power-supply rejection is 80dB at low frequencies and rolls off above 10Hz. As the frequency increases above 10kHz, the output capacitor is the major contributor to the rejection of power-supply noise (Figure 7). Do not use power supplies with ripple above 100kHz, especially when the ripple exceeds 100mVp-p. When operating from sources other than batteries, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors, and through passive filtering techniques. The *Typical Operating Characteristics* show the MAX603/MAX604 supply and load-transient responses.

Transient Considerations

The *Typical Operating Characteristics* show the MAX603/MAX604 load-transient response. Two components of the output response can be observed on the load-transient graphs—a DC shift from the output impedance due to the different load currents, and the transient response. Typical transients for step changes in the load current from 5mA to 500mA are 0.2V. Increasing the output capacitor's value attenuates transient spikes.

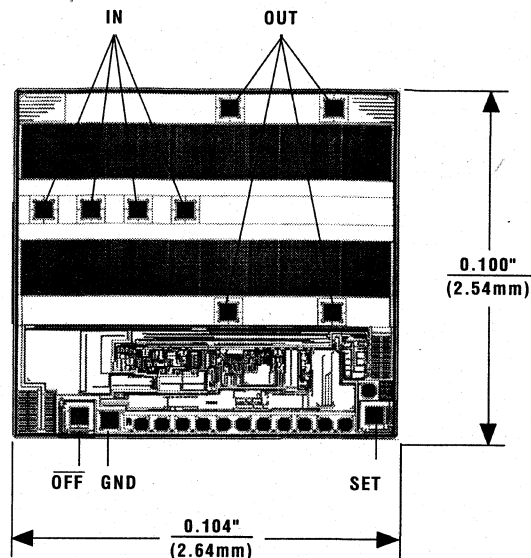
5V/3.3V or Adjustable, Low-Dropout, Low I_Q , 500mA Linear Regulators

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential, or dropout voltage, determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the MAX603/MAX604 use a P-channel MOSFET pass transistor, their dropout voltage is a function of $r_{DS(ON)}$ multiplied by the load current (see *Electrical Characteristics*).

Quickly stepping up the input voltage from the dropout voltage can result in overshoot. This occurs when the pass transistor is fully on at dropout and the IC is not given time to respond to the supply voltage change. Prevent this by slowing the input voltage rise time.

Chip Topography



TRANSISTOR COUNT: 111

NO DIRECT SUBSTRATE CONNECTION. THE N-SUBSTRATE IS INTERNALLY SWITCHED BETWEEN THE MORE POSITIVE OF IN OR OUT.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.
6/95

MAXIM

Low-Profile, Step-Up DC-DC Converters for Flash Memory and PCMCIA Cards

General Description

The MAX606/MAX607 are ultra-small, CMOS, DC-DC step-up converters. An extremely high 0.8MHz switching frequency allows the MAX606 to use the smallest available external inductors and capacitors, so the entire circuit fits in Type 1 (minimum height) flash memory and PCMCIA cards. The MAX607 is intended for Type 2 and 3 cards, as well as hand-held host devices. It operates at 0.4MHz. This device requires slightly larger external components but consumes less quiescent supply current than the MAX606.

These devices convert a 3V to 5.5V input to either a preset 5V or 12V output, or an adjustable output. The 12V output current is 60mA, guaranteed. Typical quiescent currents are 200µA for the MAX606, and 150µA for the MAX607.

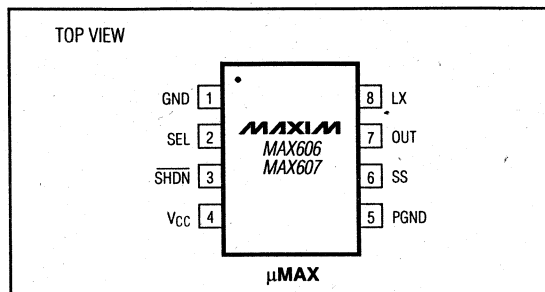
Both devices employ a unique, current-limiting, pulse-frequency-modulation (PFM) control scheme that optimizes performance over all input and output voltages and guarantees output voltage accuracy to $\pm 4\%$. Other features include a logic-controlled 1µA shutdown, and soft-start capability to minimize inrush surge currents.

The MAX606/MAX607 come in a 1.1mm high 8-pin µMAX package. The µMAX package occupies approximately one-half the area of a standard 8-pin SOIC and, when combined with small external components, requires a fraction of the board space of similar memory card devices.

Applications

PCMCIA Cards
Flash Memory Cards
5V and 12V Flash Memory Programming
Single-Slot PCMCIA Programming
Hand-Held Equipment
Miniature DC-DC Power Supplies
Low-Power DC-DC Power Supplies

Pin Configuration



Features

- ♦ 0.8MHz Switching Frequency (MAX606)
- ♦ Very Small External Components
- ♦ 1.11mm High µMAX Package
- ♦ Regulated 12V $\pm 4\%$ Output at 60mA, Guaranteed
- ♦ 3V to 5.5V Input Voltage Range
- ♦ 5V, 12V, or Adjustable (V_{IN} to 12.5V) Output
- ♦ Low 150µA Quiescent Current (MAX607)
- ♦ 1µA Typical Shutdown Current

Ordering Information

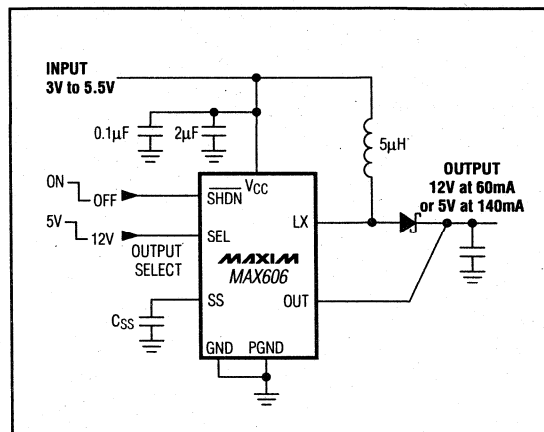
PART	TEMP. RANGE	PIN-PACKAGE
MAX606C/D	0°C to +70°C	Dice*
MAX606IUA	-25°C to +85°C	8 µMAX
MAX607C/D	0°C to +70°C	Dice*
MAX607IUA	-25°C to +85°C	8 µMAX

*Contact factory for dice specifications.

MAX606/MAX607

4

Typical Operating Circuit



MAXIM

Maxim Integrated Products 4-79

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

EVALUATION KIT WILL BE AVAILABLE

MAXIM

Low Input Voltage, High-Efficiency, Step-Up DC-DC Controller

General Description

The MAX608 step-up, DC-DC switching controller provides high efficiency over loads ranging from 10mA to more than 1A. A unique, current-limited, pulse-frequency modulated (PFM) control scheme gives this device the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using only 110µA of supply current (vs. 2mA to 10mA for PWM converters).

The MAX608 uses miniature external components. Its high switching frequency (up to 300kHz) allows surface-mount magnetics only 5mm high and 9mm wide.

The MAX608 must be run in bootstrapped mode with the IC powered by the output of the device. Bootstrapping and a low current-sense threshold (100mV) allows the circuit to start up from input voltages as low as 1.8V, operating with 80% efficiency. The MAX608 output voltage is set for 5V $\pm$ 3%, or can be adjusted using two external resistors.

For a similar part with 2.7V undervoltage lockout, see the MAX1771 data sheet.

Applications

- 2 or 3 Cells to 5V DC-DC Converter
- 2 or 3 Cell Palmtops/Handy-Terminals
- 2 or 3 Cell Portable Communicators
- 2 or 3 Cell Positive LCD-Bias Generators

Features

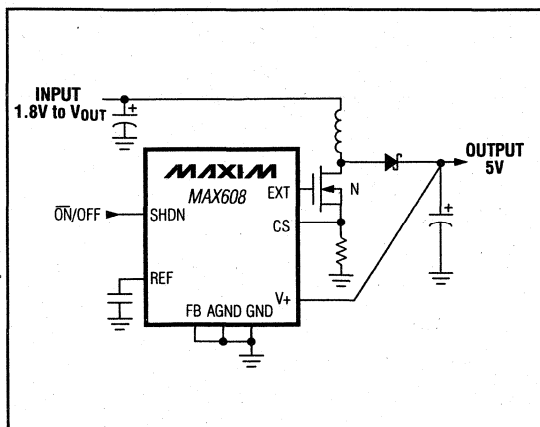
- ◆ Starts Up from 1.8V Input Voltage
- ◆ 80% Efficiency for 10mA to 1A Load Currents
- ◆ 110µA (max) Quiescent Supply Current
- ◆ 5µA (max) Shutdown Supply Current
- ◆ 5V or Adjustable Output Voltage
- ◆ Current-Limited PFM Control Scheme
- ◆ Up to 300kHz Switching Frequency

Ordering Information

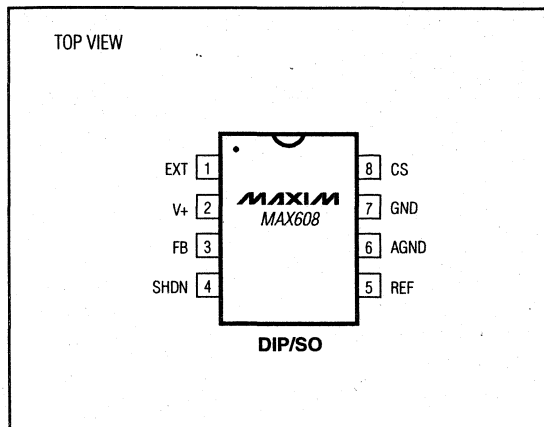
PART	TEMP. RANGE	PIN-PACKAGE
MAX608C/D	0°C to +70°C	Dice*
MAX608IPA	-25°C to +85°C	8 Plastic DIP
MAX608ISA	-25°C to +85°C	8 SO
MAX608EPA	-40°C to +85°C	8 Plastic DIP
MAX608ESA	-40°C to +85°C	8 SO

*Dice are specified at $T_A = +25^\circ\text{C}$.

Typical Operating Circuit



Pin Configuration



MAXIM

Maxim Integrated Products 4-81

Call toll free 1-800-998-8800 for free samples or literature.

MAX608

4



Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

General Description

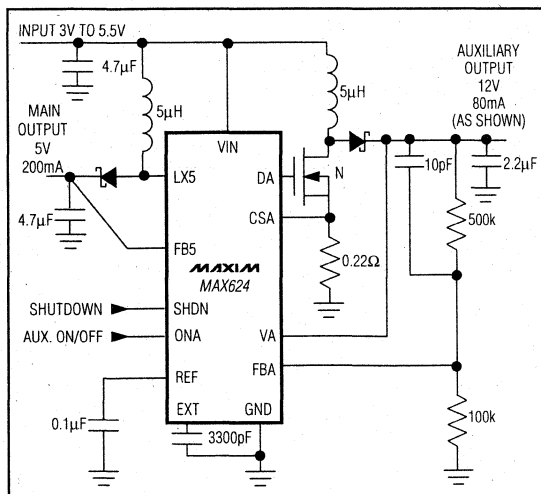
The MAX624 is a dual DC-DC converter intended for size-constrained applications, such as power supplies that must fit inside PCMCIA memory cards. At the heart of the MAX624 are two boost-topology converters, plus auxiliary functions including a start-up inrush surge-current limiter and a power-on reset output with timer (power-good signal). The MAX624 accepts input voltages from 3V to 5.5V and generates two outputs: a fixed 5V $\pm 4\%$ output at 200mA (guaranteed), and an adjustable auxiliary output that is configurable for various loads with an external power transistor. The auxiliary output is typically set to 12V $\pm 2\%$ for flash memory applications, but can be adjusted via a resistor divider from V_{IN} to 30V or more.

The MAX624's high switching frequency (1MHz) reduces external component sizes. High-frequency switching losses have minimal impact on efficiency, which is 85% for the main 5V supply. Small ceramic filter capacitors, together with the soft-start function, reduce start-up inrush current surges.

Applications

PCMCIA Memory Cards
Solid-State Disk Drives
Host-Side PCMCIA Adapters
LCD Bias Power Supplies

Typical Operating Circuit



Features

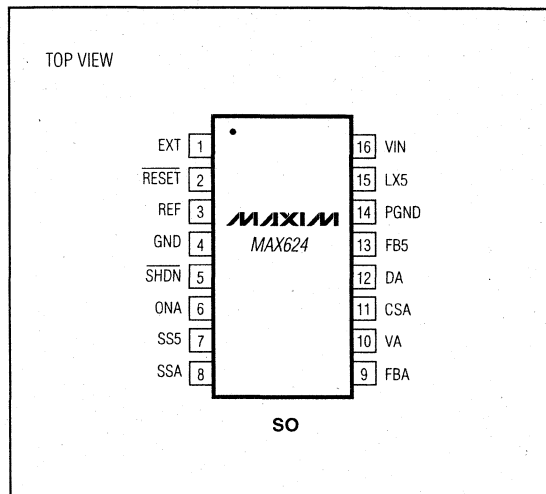
- ◆ 1MHz Switching Frequency for Small Components
- ◆ 5V $\pm 4\%$ Boost Converter with Internal Power Switch
- ◆ Adjustable $\pm 2\%$ Output Boost Converter with External Power Switch
- ◆ Optional Inrush Surge-Current Limiting
- ◆ 40µA Shutdown Current
- ◆ 0.5mA Quiescent Current
- ◆ 3.0V to 5.5V Input Range
- ◆ 85% Main 5V SMPS Efficiency
- ◆ Independent Soft-Start for Each Supply
- ◆ Reset Output with 2.8V $\pm 3\%$ Threshold and 4ms Timeout

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX624C/D	0°C to +70°C	Dice*
MAX624ISE	-25°C to +85°C	16 Narrow SO

* Dice are tested at $T_A = +25^\circ\text{C}$. Contact factory for dice specifications.

Pin Configuration



Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

ABSOLUTE MAXIMUM RATINGS

V _{IN} , FB5, LX5, SHDN, ONA to GND	-0.3V to 7V	Continuous Power Dissipation (T _A = +70°C)	
EXT to GND	-0.3V to 12V	SO (derate 8.70mW/°C above +70°C)	696mW
RESET, REF to GND	-0.3V to (V _{IN} + 0.3V)	Operating Temperature Range	
PGND to GND	±0.3V	MAX624ISE	-25°C to +85°C
SS5, SSA, DA, CSA, FBA to GND	-0.3V to (FB5 + 0.3V)	Lead Temperature (soldering, 10sec)	+300°C
VA to GND	-0.3V to 17V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, GND = PGND = 0V, SHDN = V_{IN}, EXT open, FBA feedback resistors set for 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range		3.0		5.5	V
OUTPUT VOLTAGES					
5V Output Voltage		4.80		5.20	V
FBA Regulation Point		1.96		2.04	V
SUPPLY CURRENTS					
V _{IN} Shutdown Current	V _{IN} = 5.5V, SHDN = ONA = 0V		40	60	μA
V _{IN} Quiescent Current	Circuit of Figure 1, V _{IN} = 3.3V, ONA = 0V		500		μA
FB5 Quiescent Current	FB5 = 5.5V, SHDN = 3V, ONA = 0V		200	400	μA
VA Quiescent Current	FB5 = 5.5V, VA = 12.5V		30	60	μA
FB5 Shutdown Discharge Current	FB5 = 5V, V _{IN} = 3V, SHDN = 0V, internal V _{IN} to FB5 discharge switch	100	5000		μA
VA Shutdown Discharge Current	VA = 12V, V _{IN} = 3V, ONA = 0V, internal V _{IN} to VA discharge switch	5	15		μA
FBA Leakage Current	VA = 12V, FBA = 2.1V			100	nA
5V MAIN SMPS					
Line Regulation	3V < V _{IN} < 5.5V (Note 1)		0.03	0.2	%
Switch On-Resistance			0.33	0.6	Ω
Switch Leakage Current	LX5 = 7V			10	μA
Switch Current Limit		0.7	0.9	1.1	A
Switch On-Time Constant (K5)	3V < V _{IN} < 5V, t _{ON5} = K5 / V _{IN}	0.8	1.3	1.7	μs-V
Switch Off-Time Ratio (SR5)	3V < V _{IN} < 5V, FB5 = 5V (Note 2)	0.2		0.8	
Efficiency	Circuit of Figure 1, I _{LOAD} = 100mA		85		%
AUXILIARY SMPS CONTROLLER					
Line Regulation	3V < V _{IN} < 5.5V (Note 1)		0.03	0.2	%
Enable Trip Voltage Level	ONA input will be inhibited until FB5 rises above this level	3.5	4.0	4.5	V
CSA Bias Current				10	μA
CSA Current-Limit Threshold		180		220	mV
DA On-Resistance	FB5 = 5.5V		4	15	Ω
DA Drive Current	DA = 2.5V		0.5		A
Switch On-Time Constant (KA)	3V < V _{IN} < 5V, t _{ONA} = KA / V _{IN}	1.5	2.2	3.0	μs-V
Switch Off-Time Ratio (SRA)	3V < V _{IN} < 5V, 7V < FBA < 11V (Note 3)	0.2		0.9	
Efficiency	Circuit of Figure 1, I _{LOAD} = 60mA		75		%

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

MAX624

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 3V$, $GND = PGND = 0V$, $\overline{SHDN} = V_{IN}$, EXT open, FBA feedback resistors set for 12V, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START CONTROL					
Source Resistance	SS5, SSA; $\overline{SHDN} = ONA = 3V$	14	20	28	k Ω
Discharge Resistance	SS5, SSA; $\overline{SHDN} = ONA = 0V$		50	300	Ω
LOGIC INPUTS AND OUTPUTS					
Input Low Voltage	$\overline{SHDN}$, ONA			0.8	V
Input High Voltage	$\overline{SHDN}$, ONA	2			V
Input Leakage	$\overline{SHDN}$, ONA			± 1	μA
Output Low Voltage	RESET, $I_{SINK} = 2mA$, $V_{IN} = 2.6V$			0.4	V
Output High Voltage	RESET, $I_{SINK} = 1mA$, $V_{IN} = 3V$	$V_{IN} - 0.8$			V
RESET Trip Level	Rising V_{IN} edge, typical hysteresis = 1%	2.7		2.9	V
RESET Timeout		2		10	ms
EXT Output Voltage	$V_{IN} = 2.9V$, $I_{SOURCE} = 2\mu A$	6.5			V
	$V_{IN} = 5.5V$, $I_{SOURCE} = 0\mu A$			11.8	
EXT Output Voltage in Reset	$V_{IN} = 2V$, $I_{SINK} = 0.1mA$			1	V

Note 1: Line Regulation is tested by measuring the reference line regulation, since both converters are supplied from the regulated 5V output.

Note 2: Switch off-time ratio guarantees that the inductor will go into continuous conduction. The ratio is tested for two cases for the main SMPS:

- 1) $V_{IN} = 5V$, $FB5 = 5V$ $SR5 = 0.120 \times t_{OFF} / t_{ON}$
- 2) $V_{IN} = 3V$, $FB5 = 5V$ $SR5 = 0.867 \times t_{OFF} / t_{ON}$

Note that the constants are calculated from: $(FB5 + 0.6V - V_{IN}) / V_{IN}$

Note 3: Switch off-time ratio guarantees that the inductor will go into continuous conduction. The ratio is tested for two cases for the auxiliary SMPS:

- 1) $V_{IN} = 5V$, $VA = 7V$ $SRA = 0.520 \times t_{OFF} / t_{ON}$
- 2) $V_{IN} = 3V$, $VA = 11V$ $SRA = 2.867 \times t_{OFF} / t_{ON}$

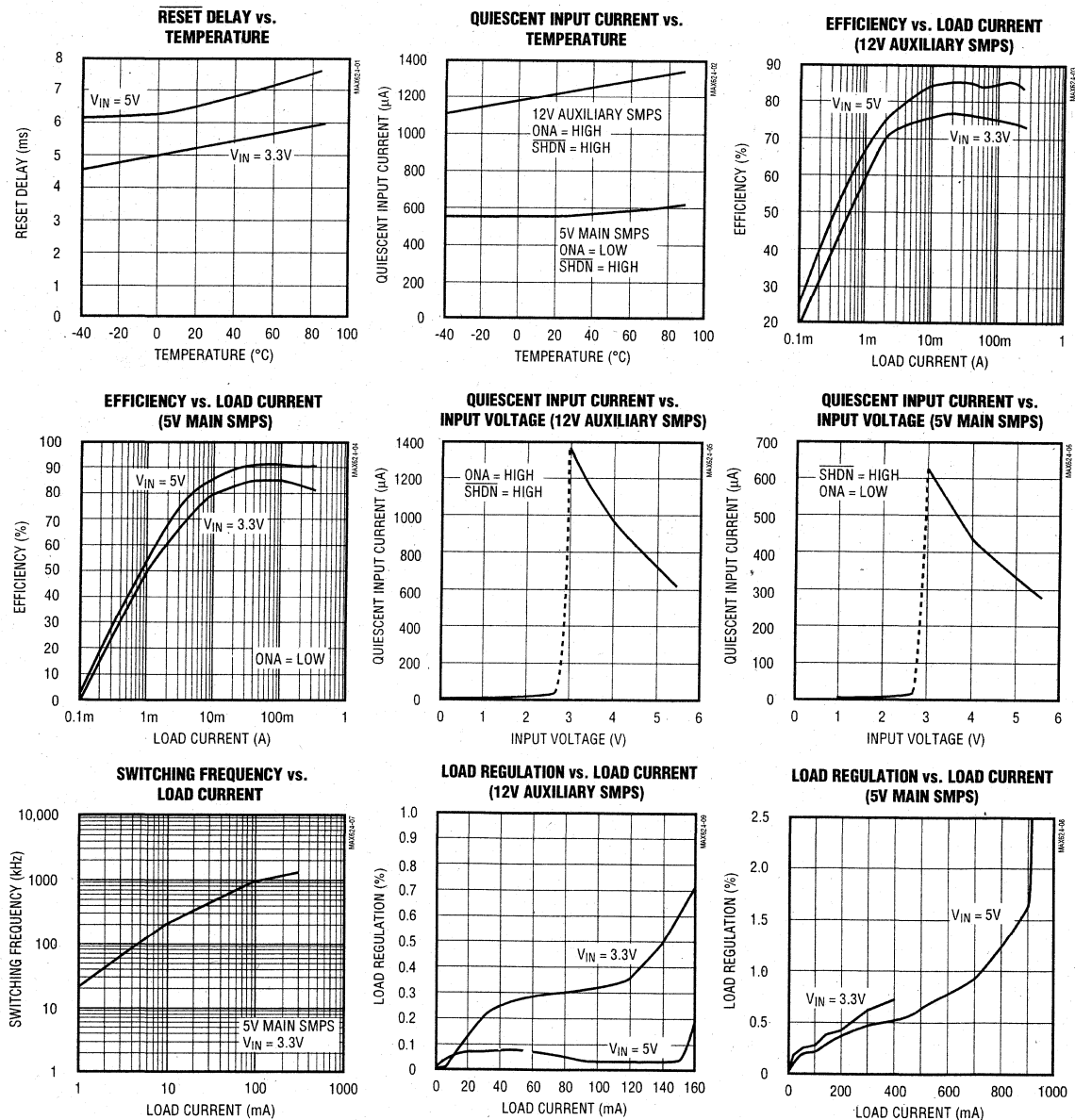
Note that the constants are calculated from: $(VA + 0.6V - V_{IN}) / V_{IN}$

4

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Typical Operating Characteristics

(Circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

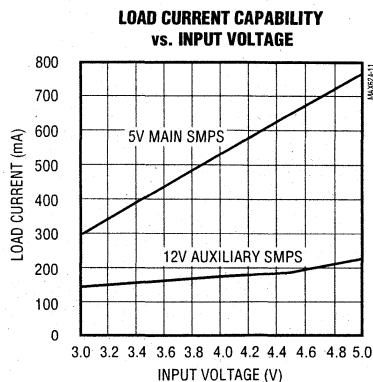
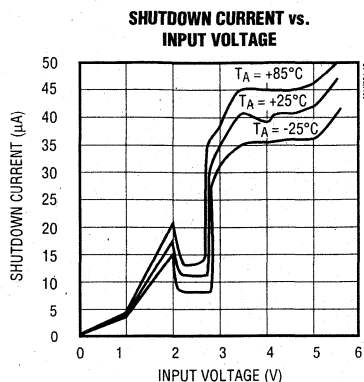


Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

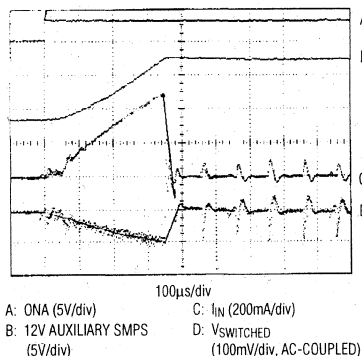
MAX624

Typical Operating Characteristics (continued)

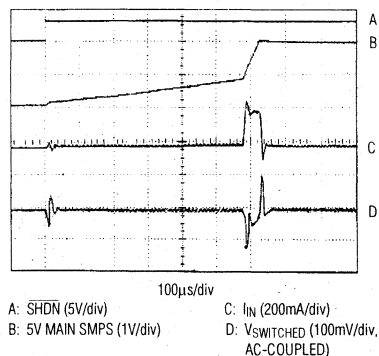
(Circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



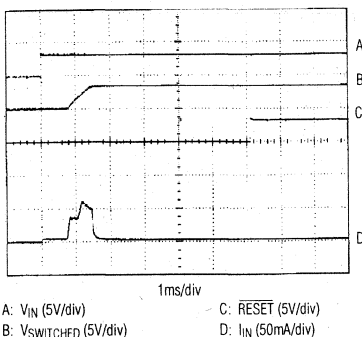
START-UP WAVEFORMS (12V AUXILIARY SMPS)
 ($V_{IN} = 3.3\text{V}$, $I_{LOAD} = 1.2\text{mA}$, SHDN = HIGH)



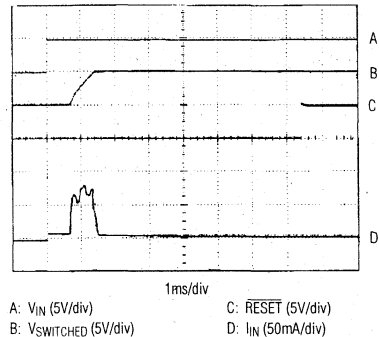
START-UP WAVEFORMS (5V MAIN SMPS)
 ($V_{IN} = 3.3\text{V}$, $I_{LOAD} = 0\text{A}$, ONA = LOW)



START-UP INRUSH CURRENT ($V_{IN} = 3.3\text{V}$)
 ($I_{LOAD} = 5\text{mA}$, SHDN = ONA = LOW)



START-UP INRUSH CURRENT ($V_{IN} = 5\text{V}$)
 ($I_{LOAD} = 5\text{mA}$, SHDN = ONA = LOW)

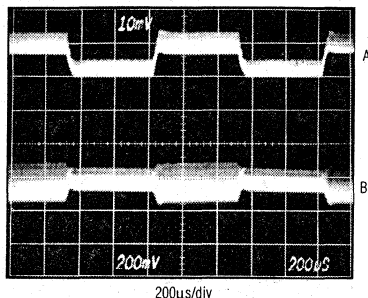


Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Typical Operating Characteristics (continued)

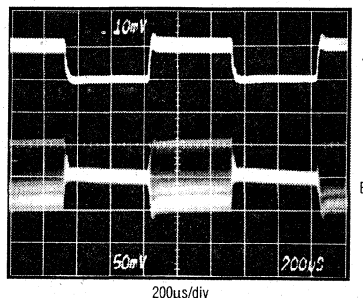
(Circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (12V AUXILIARY SMPS)



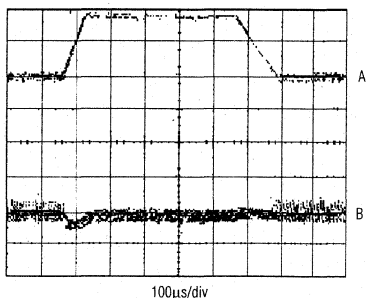
A: $I_{\text{LOAD}} = 0\text{mA to } 80\text{mA}$
B: 12V AUXILIARY SMPS (200mV/div, AC-COUPLED)

LOAD-TRANSIENT RESPONSE (5V MAIN SMPS)



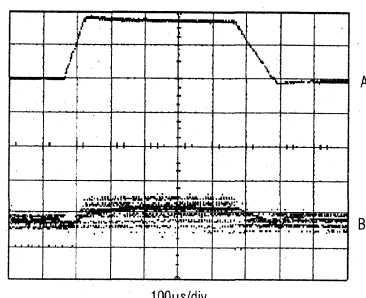
A: $I_{\text{LOAD}} = 0\text{mA to } 200\text{mA}$
B: 5V MAIN SMPS (50mV/div, AC-COUPLED)

**LINE-TRANSIENT RESPONSE
(12V AUXILIARY SMPS)**



$I_{\text{LOAD}} = 20\text{mA}$
A: $V_{\text{IN}} = 3.3\text{V to } 5\text{V}$
B: 12V AUXILIARY OUTPUT (200mV/div, AC-COUPLED)

**LINE-TRANSIENT RESPONSE
(5V MAIN SMPS)**



$I_{\text{LOAD}} = 40\text{mA}$
A: $V_{\text{IN}} = 3.3\text{V to } 5\text{V}$
B: 5V MAIN OUTPUT (50mV/div, AC-COUPLED)

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Pin Description

PIN	NAME	FUNCTION
1	EXT	Gate-Drive Output. Drives inrush surge-current limiting MOSFET. EXT is fed by an internal charge-pump tripler that swings from GND to $V_{IN} \times 3$.
2	RESET	Power-On Reset Output. Low when $V_{IN} < 2.8V$ and for 4ms after $V_{IN} > 2.8V$. EXT is low when RESET is low. Swings from GND to V_{IN} .
3	REF	2V Reference Output. Bypass to GND with 0.1 μ F. No external load current is allowed.
4	GND	Quiet Analog Ground and Low-Side Current-Sense Input for Auxiliary SMPS
5	SHDN	Shutdown. Disables both SMPSs when low. In shutdown, the surge-protection input MOSFET is kept on.
6	ONA	On/Off Control Input for Auxiliary SMPS, low = off
7	SS5	Soft-Start Input for 5V Main SMPS. An external soft-start capacitor varies the 5V start-up time. Ramp time to full current limit is approximately 50 μ s per nF of soft-start capacitance.
8	SSA	Soft-Start Input for Auxiliary SMPS. An external soft-start capacitor varies the auxiliary SMPS start-up time. Ramp time to full current limit is approximately 50 μ s per nF of soft-start capacitance.
9	FBA	Feedback Input for Auxiliary SMPS. Regulates around REF (2V nominal). FBA is a high-impedance CMOS input.
10	VA	Output Voltage Sense Input for Auxiliary SMPS. The only purpose of this pin is to set the SMPS timing algorithm. Internally, VA connects to the top of a 250k Ω $\pm$ 30% resistor that connects to V_{IN} .
11	CSA	Current-Sense Input for Auxiliary SMPS. Current-limit threshold is 200mV nominal with respect to GND.
12	DA	Gate-Drive Output for Auxiliary SMPS. Swings 0V to FB5.
13	FB5	Feedback Input for 5V Main SMPS. FB5 also serves as the supply voltage rail for much of the internal circuitry for both SMPSs (bootstrap supply input).
14	PGND	Power Ground, source connection for the main 5V SMPS power MOSFET
15	LX5	Drain Connection for 5V Main SMPS Power MOSFET
16	VIN	Input Supply Voltage from the External Supply. Normal operating range is 3V to 5.5V.

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Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Standard Application Circuit

In the standard application circuit (Figure 1), the MAX624 generates 5V at 200mA (guaranteed) and 12V at 80mA from a 3.3V or 5V input, and includes soft-start and inrush surge-current limiting features. Successful use of the circuit does not require calculations; use the values given in Figure 1. For more detailed applications information, see the *Design Procedure for Main and Auxiliary SMPS*.

Detailed Description

The MAX624 is a dual-output DC-DC boost converter. The device accepts input voltages from 3V to 5.5V and generates two outputs: a 5V output at 200mA, and an adjustable output (i.e. 12V or 30V). The main 5V output has an internal MOSFET switch and current-sense resistor (0.15 Ω), which senses the output current and triggers the current-limit comparator. The auxiliary SMPS's current-limit resistor and MOSFET switch are external to the device. The current-limit voltage of the auxiliary SMPS is 200mV. Both the main and auxiliary SMPS have a soft-start feature that varies the start-up time of the outputs. The SS output source impedance of the two outputs is 20k Ω to charge the external SS capacitor to 150mV (5V output) or 200mV (auxiliary output). The impedance of the SS pin when the device is in reset (5V) and when ONA = low (auxiliary) is 50 Ω to GND. Full current limit is reached at a 50 μ s/nF rate.

To prevent surge currents when the card is plugged into a live socket, this device is capable of driving an external high-side N-channel MOSFET in series with the main VCC supply to the card. The EXT pin drives the gate of the external MOSFET and is fed by an internal charge-pump tripler that delivers three-times V_{IN} , even in shutdown mode. The output source impedance of EXT is approximately 100k Ω , and has an active pull-down.

The SS capacitor and the external inrush-limiting MOSFET are optional components, not necessary unless inrush current is a concern. However, do not remove C9.

When the MAX624 is in reset, the FB5 and VA outputs are discharged to V_{IN} via two internal switches (Figure 2). Discharging the output capacitors to a low voltage level protects against false programming of flash memory chips.

5V Main SMPS

The main output is powered from the FB5 pin (i.e., bootstrapped) for higher speed and lower on-resistance of the power MOSFET. This SMPS consists of an error comparator, an output undervoltage-lockout comparator (set at 4V output), a timing generator for t_{ON}

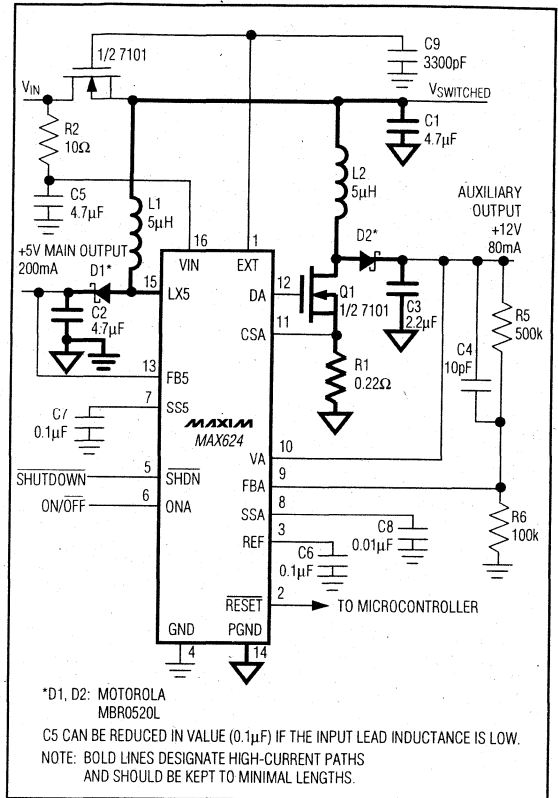


Figure 1. Standard Application Circuit

and t_{OFF} , a current-limit comparator, a MOSFET driver, and the power switch (Figure 2).

The error comparator's noninverting input voltage is internally set to V_{REF} . FB5's voltage is scaled internally, so that when it exceeds 5V the comparator output trips and shuts down the PFM.

Leaving only the error comparator on when the switch is off keeps the quiescent current low. The current comparator is powered up after the switch is turned on. This provides leading-edge blanking on the current comparator, in order to filter noise spikes caused by switch gate capacitance so they don't trip the overcurrent comparator and turn off the switch.

The main PFM has an undervoltage-lockout circuit that trips at 4V (preset internal threshold). Until the 4V threshold is reached, the timing generator is disabled and a 100kHz start-up oscillator is used to generate the output.

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

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Table 1. Recommended Components for 12V/80mA Auxiliary SMPS and 5V Main SMPS

DESIGNATION	QTY	DESCRIPTION	SOURCE/TYPE
Q1	1	Dual, N-channel MOSFET	IRF7101 or Si9956DY
L1, L2	2	5 μ H inductors	Sumida CLS-62B, drawing #94T-217
C1, C2	2	4.7 μ F ceramic capacitors	Marcon THCR40E1E475ZT or THCS40E1E475ZT
C3	1	2.2 μ F ceramic capacitor	Marcon THCR30E1E225ZT or THCS30E1E225ZT
C4	1	10pF capacitor	
C5, C6, C7	3	0.1 μ F capacitors	Murata-Erie GRM42-6X7R104K025V
C8	1	10nF capacitor	
C9	1	3300pF capacitor	
D1, D2	2	I _F = 1A, V _R = 20V Schottky rectifier	Motorola MBR0520L
R1	1	0.22 Ω $\pm$ 10% resistor	Ohmtek 1205LR220LBT or IMS RC-I-1206
R2	1	10 Ω resistor	

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX
IMS	(401) 683-9700	(401) 683-5571
International Rectifier	(310) 241-7876	(310) 640-6515
Motorola	(602) 244-3576	(602) 244-4015
Murata-Erie	(800) 831-9172	(814) 238-0490
Ohmtek	(716) 283-4025	(716) 283-5932
Siliconix	(408) 988-8000	(408) 970-3950
Sumida USA	(708) 956-0666	(708) 956-0702
Sumida Japan	(03) 607-5111	(03) 607-5144
Toshiba Marcon	(708) 913-9980	(708) 913-1150

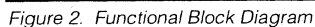
Table 3. Operating States

STATE	V _{IN}	SHDN	ONA	V _{MAIN}	V _{AUX} *	EXT	I (V _{IN})
Reset	<2.8V	X	X	OFF	OFF	OFF	10 μ A
Shutdown	>2.8V	LO	X	OFF	OFF	ON	40 μ A
Main On	>2.8V	HI	LO	5.0V	OFF	ON	0.52mA
Both On	>2.8V	HI	HI	5.0V	12V**	ON	1.2mA

* When off, V_{AUX} = V_{IN}.

** V_{AUX} is set to 12V in this example.

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Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Adjustable Auxiliary SMPS

The auxiliary output is adjustable from 5V to 15V; two external resistors set the output voltage. The auxiliary SMPS is similar to the main SMPS, but it does not have an undervoltage-lockout comparator, and requires an external power MOSFET (see *Typical Operating Circuit* and *Design Procedure for Main and Auxiliary SMPS*).

The 5V SMPS undervoltage-lockout circuit overrides the ONA input until the 5V main SMPS (VMAIN) output reaches about 4V. This feature ensures that the external auxiliary SMPS MOSFET has sufficient gate-drive voltage.

The adjustable output voltage can be increased to 30V or higher (Figure 9). However, such high output voltages cause the inductor current to become discontinuous, consequently reducing the load-current capability.

Voltage Reference

The MAX624's internal 2.00V reference is powered from the VIN input. The reference is kept alive in all modes (needed for reset function) and must be bypassed with a 0.1μF capacitor to GND for low-noise operation. No external load current is allowed.

Pulse-Frequency-Modulation Control Scheme

A unique pulse-frequency-modulation (PFM) control scheme, with adjustable on-time/off-time circuitry and current limit, is a key feature of both the main SMPS regulator and the auxiliary SMPS converter. The PFM scheme combines the advantages of pulse-width modulation (high output power and efficiency) with those of a traditional pulse-skipper (ultra-low quiescent currents). The on-time is calculated from the input voltage, and the off-time is calculated from $V_{OUT} - V_{IN}$. The off-time is divided by two so that the inductor current can ramp into continuous conduction. Switch on-times are adjusted down at high input voltages in order to minimize output ripple.

Use the following formulas to calculate t_{ON} and t_{OFF} :

$$t_{ON} = K / V_{IN}$$

$$t_{OFF} = 0.5 \times K / (V_{OUT} + 0.6V - V_{IN})$$

Nominally, $K = 1.3\mu s \cdot V$ for the main SMPS, and $K = 2.2\mu s \cdot V$ for the auxiliary SMPS. The K (design constant) scale factor that sets the switching frequency also sets the peak inductor current to control no-load output ripple at low input-to-output differentials (e.g., $V_{IN} = 5V$, $V_{OUT} = 5V$).

The PFM's high switching frequency (1MHz) helps reduce external component size. When the peak current limit is reached, the MOSFET switch turns off for at least the off-time set by the one-shot. When the comparator monitoring the output voltage is less than the desired value, it starts another cycle by turning the switch on.

Surge Prevention

Surge prevention is accomplished by slowly high-side driving an N-channel switch. The gate is driven by an on-chip charge pump that triples the input voltage. This charge pump is powered from the input voltage and runs continuously. The reset trip voltage is set to 2.8V to guarantee that the surge-prevention MOSFET can be turned on under worst-case low input voltage conditions. Otherwise, the card would go out of reset even though the supply voltage is unavailable.

Design Procedure for Main and Auxiliary SMPS

Output Filter Capacitor Selection

The output filter capacitor should have the minimum possible ESR for low ripple, and the minimum possible value for smallest physical size (i.e., ceramic). Larger sizes can be used for lower cost (i.e., tantalum). The output ripple is the sum of two components, due to C_F and ESR.

To select the filter capacitor value, follow the steps below:

- 1) Select the maximum ripple you can tolerate (e.g., 80mV).
- 2) Calculate the value of C_F , using the formula below:

$$C_F \text{ (in F)} > \frac{2 \times K \times I_{LOAD}}{V_{RIPPLEC} (V_{OUT} + 0.5V - V_{IN})}$$

where K is a design constant. Use the worst-case value from the *Electrical Characteristics*.

- 3) Calculate the output capacitor's required ESR, using the formula below.

$$ESR \text{ (in } \Omega) < \frac{V_{RIPPLEESR} \times V_{IN}}{4 \times I_{LOAD} (V_{OUT} + 0.5V - V_{IN})}$$

For example: For the 5V main SMPS with $K = 1.7\mu s \cdot V$, $I_{LOAD} = 200mA$, $V_{OUT} = 5V$, $V_{IN} = 3.3V$, and maximum tolerable ripple = 80mVp-p, assume $V_{RIPPLEC} = 60mV$ and $V_{RIPPLEESR} = 20mV$. Calculate $C_F > 5\mu F$ with $ESR < 37m\Omega$.

Inductor Selection

Select the inductor value to optimize one of the following:

- High Load Currents: Higher inductor values give higher load currents, since the inductor operates in deep continuous conduction.
- Small Physical Size: Lower inductor values result in lower energy storage requirements, hence smaller physical size. The filter capacitor can also be smaller, since the inductor current can ramp up faster when the load is suddenly increased.

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

To select the inductor value for the main SMPS, take the following steps:

- 1) Select the input voltage.
- 2) Select I_{LIMIT} and I_{LOAD} .
- 3) Use the specified data sheet values and the following formula:

$$L \text{ (in H)} = \frac{SR5 \times K5 (V_{IN} - A)}{2 \times I_{LIMIT} (V_{IN} + A) - 2 \times I_{LOAD} \times B}$$

$$A = I_{LIMIT} \times R_{ON}$$

$$B = V_{OUT} + V_{DIODE}$$

where: inductor current = $I_{LIMIT}(\min) = 0.7A$, $I_{LOAD}(\min) = 200mA$, $SR5$ (the switch off-time ratio) = 0.8, $K5(\max) = 1.7\mu s-V$, $R_{ON}(\max) = 0.6\Omega$, $V_{OUT} = 5V$, $V_{DIODE} = 0.5V$, $V_{IN}(\min) = 3.0V$, and $L = 5\mu H$ (for best performance, use a Sumida 5 μH (CLS-62B)).

Input Filter Capacitor Selection

The input filter capacitor is required to reduce reflected current ripple to the input source, and to improve efficiency by providing a low-impedance path for the ripple current. For memory card applications, the input filter capacitor is absolutely necessary due to possible contact resistance in the edge connector. To limit surge currents, use smaller values. Ceramic capacitors are the best choice.

Output Voltage and Component Selection for the Auxiliary SMPS

To select the output voltage and component values for the auxiliary SMPS, take the following steps:

- 1) Select the desired output voltage between 5V and 15V (e.g., 12V).
- 2) Select the minimum input voltage (V_{IN}).
- 3) Select $R6$ and $R5$. Choose $R6$ in the $10k\Omega$ to $200k\Omega$ range (e.g., $100k\Omega$). Choose $R5 = R6 (V_{OUT} / V_{REF} - 1)$. For example, if $V_{OUT} = 12V$, then $R6 = 100k\Omega$ and $R5 = 500k\Omega$.
- 4) Select the desired output current (I_{OUT}). Calculate the minimum inductor current (I_{LIMIT}) using the following formula:

$$I_{LIMIT} \text{ (in Amps)} = [(V_{OUT} + 0.5V) / (V_{IN}(\min) - 0.3V)] \times I_{LOAD} \times 2$$

For example: $V_{OUT} = 12V$, $V_{IN}(\min) = 3V$, $I_{LOAD} = 80mA$, and $I_{LIMIT} = 0.7A$.

- 5) To calculate the minimum required inductor value, use the following formula:

$$L \text{ (in H)} = \frac{SRA \times KA (V_{IN} - A)}{2 \times I_{LIMIT} (V_{IN} - A) - 2 \times I_{LOAD} \times B}$$

$$A = I_{LIMIT} \times R_{ON}$$

$$B = V_{OUT} + V_{DIODE}$$

For example: $I_{LOAD} = 80mA$, $I_{LIMIT} = 0.7A$ (calculated using the above formula), SRA (switch off-time ratio) = 0.9, KA (switch on-time) = $3.0\mu s-V$, $R_{ON}(\max) = 0.2\Omega$, $V_{OUT} = 12V$, $V_{DIODE} = 0.5V$, and $L(\min) = 3.8\mu H$.

- 6) $R \text{ (in } \Omega) = 180mV / I_{LIMIT} = 0.25\Omega$ for $I_{LIMIT} = 0.7A$.
- 7) To select the output capacitor value, take the following steps:

A) Select the maximum ripple you can tolerate.

B) Calculate C_F using the formula below.

$$C_F \text{ (in F)} = \frac{2 \times KA \times I_{LOAD}}{V_{RIPPLEC} \times (V_{OUT} + 0.5 - V_{IN})}$$

- C) Calculate the output capacitor's required ESR using the formula below.

$$ESR \text{ (in } \Omega) = \frac{V_{RIPPLE} ESR \times V_{IN}}{4 \times I_{LOAD} \times (V_{OUT} + 0.5V - V_{IN})}$$

PC Board Layout and Grounding

Because of the MAX624's high-frequency operation, careful PC board layout is necessary to minimize ground bounce and noise. PC board layout instructions should be explicit, and the layout artist should work from a pencil sketch that shows the placement of power switching components and high-current routing. Use Figures 3-8 (the component placement guide and PC board layouts for the MAX624 evaluation board) as a rough guide for component placement and ground connections. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the following step-by-step guide.

- 1) Place the high-power components ($C1$, $C2$, $C3$, $D1$, $D2$, $L1$, $L2$, $Q1$, and $R1$) first.

Priority 1: Minimize current-sense resistor trace lengths.

Priority 2: Minimize ground trace lengths in the high-current paths (the bold lines in the application circuits).

Priority 3: Minimize other trace lengths in the high-current paths. Use traces more than 5mm wide.

Ideally, surface-mount power components are butted up against one another with their ground terminals almost touching. These high-current grounds

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

MAX624

(C1, C2, C3, R1, and PGND) are then connected with a wide filled zone of top-layer copper, so they don't go through vias. The resulting top-layer "sub-ground plane" is connected to the normal inner-layer ground plane at the ground output terminals (at the ground of C2). Other high-current paths should also be minimized, but focusing on short ground and current-sense connections eliminates about 90% of all PC board layout problems. See Figures 3–8 for examples.

- 2) Place the IC and signal components. Keep the main switching node traces (LX node) short and away from sensitive analog components (current-sense traces and REF and SS capacitors). Important: the IC must be no farther than 5mm from the current-sense resistor. Keep the gate-drive trace shorter than 10mm and route it away from REF and SS.

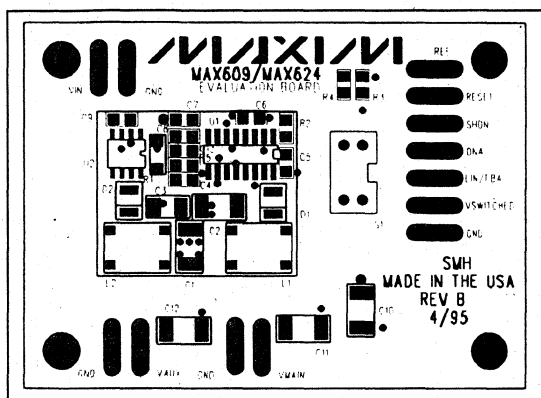


Figure 3. MAX624 PC Board Component Placement Guide

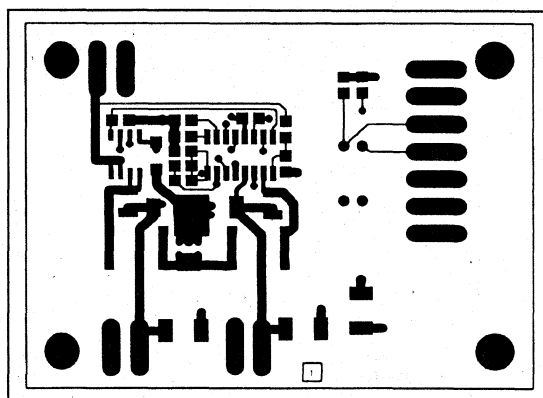


Figure 5. MAX624 PC Board Layout—Component Side

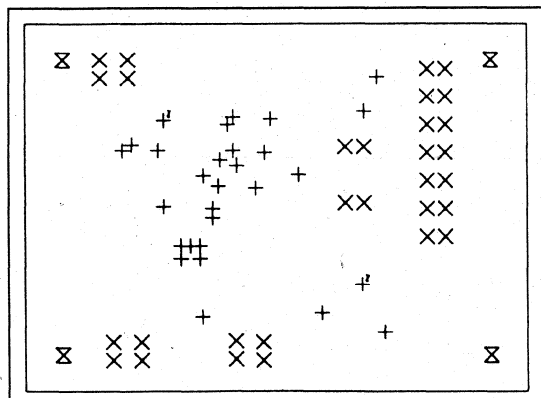


Figure 4. MAX624 PC Board Drill and Mechanical Guide

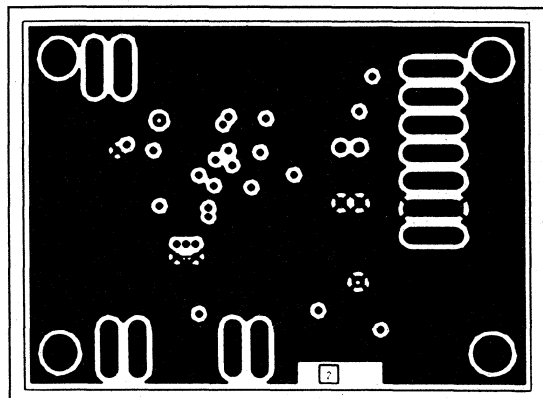


Figure 6. MAX624 PC Board Layout—VSWITCHED Plane

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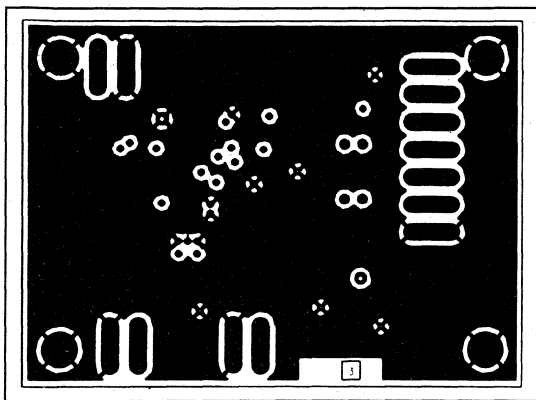


Figure 7. MAX624 PC Board Layout—Ground Plane

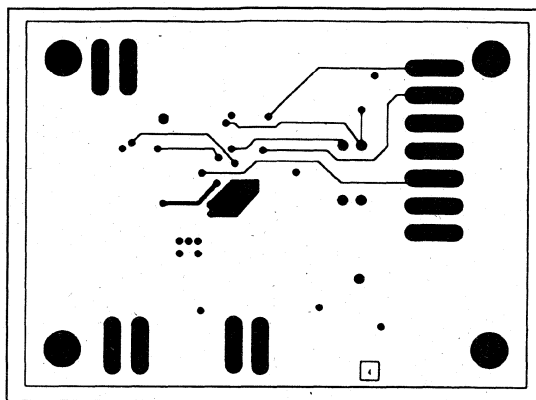


Figure 8. MAX624 PC Board Layout—Solder Side

Application Circuits

Positive 30V Auxiliary Output Circuits

The MAX624 can be used to generate a 30V output at 25mA (Figures 9 and 10). Note that the 12V zener clamp shown in Figure 10 must be used for 5V input applications. A 30V output at 25mA can be generated by tying the VA pin to the main SMPS output, but this circuit does not make optimal use of the inductor (the off-time is about 0.5 μ s). An alternative approach is to clamp the VA output to 12V using a zener. The off-time is optimized (reduced), which in turn makes better use of the inductor and produces a higher output current of about 35mA (Figure 10). Note that the 12V zener clamp shown in Figure 10 must be used for 5V input applications.

Negative Output Application Circuit

The MAX624 can be used to generate a negative 30V output to power-up LCD supplies (Figure 11). This circuit is part switching regulator and part charge pump. The switching regulator boosts the input to a high positive voltage (30V), while the actual negative voltage is generated using a charge-pump tap on the switching node. The negative 30V output has a 5% load-regulation error from 1mA to 20mA. The ratio of R5 and R6 resistors can be used to adjust the LCD contrast.

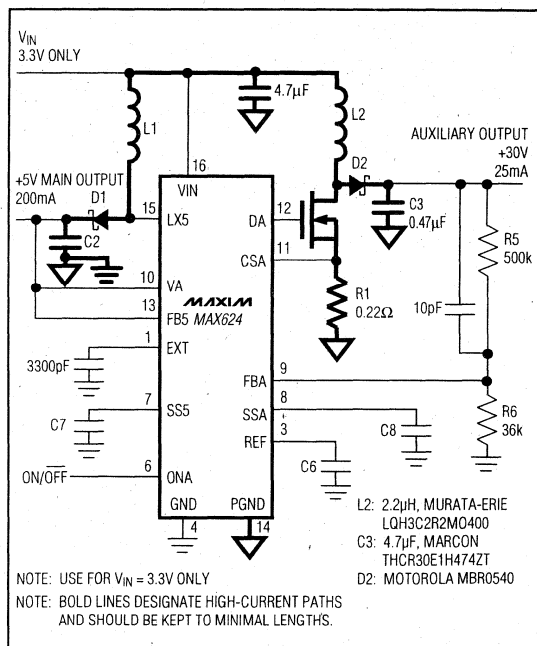


Figure 9. Positive 30V (25mA) Auxiliary Output Application Circuit

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

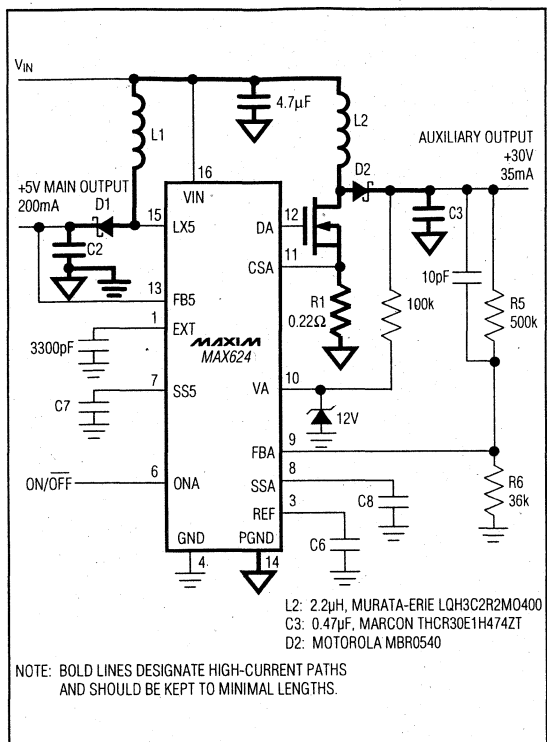


Figure 10. Positive 30V (35mA) Auxiliary Output Application Circuit

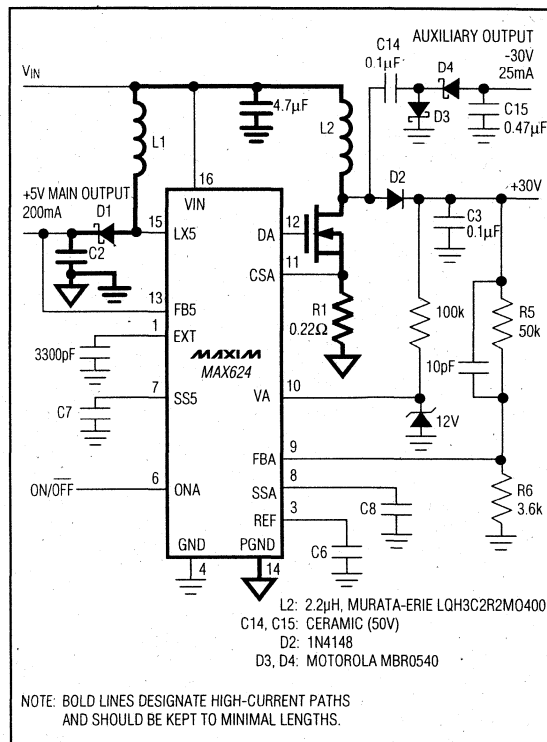


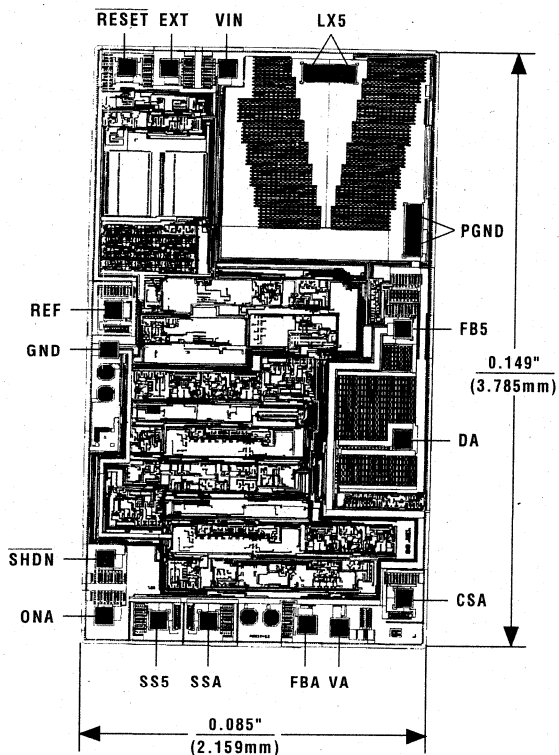
Figure 11. Negative 30V Auxiliary Output Application Circuit

MAX624

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Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Chip Topography



TRANSISTOR COUNT: 926
SUBSTRATE CONNECTED TO GND

EVALUATION KIT
AVAILABLE

MAXIM

High-Accuracy, Low-Dropout Linear Regulators

General Description

The MAX687/MAX688/MAX689 low-dropout linear regulators operate with an input-to-output voltage differential limited only by an external PNP transistor. Outputs are fixed at 3.3V (MAX687/MAX688) or 3.0V (MAX689). The only external components required are a PNP pass transistor and output, compensation, and bypass capacitors. Base drive to the external transistor is at least 10mA, permitting output currents to exceed 1A when using high-gain transistors ($\beta > 100$). Output current limiting is implemented by limiting the external transistor's base current. Output voltage monitoring and shutdown functions are included.

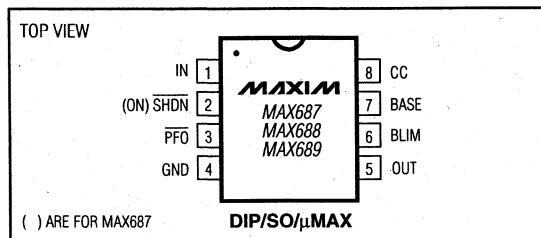
The 3.3V MAX687 automatically shuts down whenever the output voltage drops below 2.96V. An internal power-fail comparator also monitors the output and provides an early warning of low output voltage before the device shuts down. When shut down, the output is latched off until the ON input is pulsed. Turning off the power supply in this way prevents battery damage due to excessive discharge or cell-reversal. Typical applications include portable telephones and other battery-powered equipment where the power supply must be disabled when the battery voltage is low.

The MAX688 and MAX689 do not have an automatic shutdown function, and are identical except for their output voltages. Each device has an active-low shutdown-control input, used to turn its output on or off at any time. As SHDN falls, the device enters a standby mode before fully shutting down. When in standby, the reference and comparators are fully operational, permitting the transition from normal mode to standby mode to occur at a precise voltage level on SHDN.

Applications

High-Efficiency Linear Regulator
Battery-Powered Devices
Portable Instruments
Portable Telephones
Power Supply or Backup Supply for Memory

Pin Configuration



Features

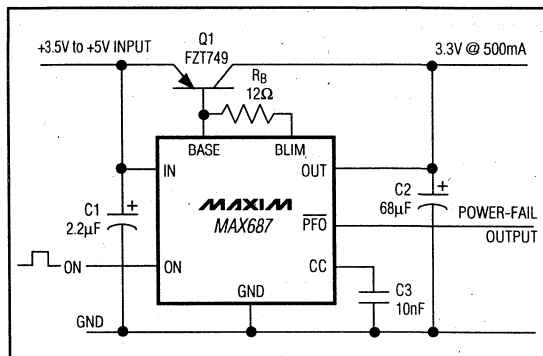
- ♦ Fixed Outputs:
 - 3.3V (MAX687/MAX688)
 - 3.0V (MAX689)
- ♦ Directly Drives External PNP Transistor
- ♦ 10mA Min Base-Current Drive for >1A Output
- ♦ Low Dropout Voltage:
 - 100mV Dropout at 650mA Output (FZT749)
 - 40mV Dropout at 200mA Output (FZT749)
 - 0.8V Dropout at 4A Output
- ♦ Power-Fail Output Monitors the Output Voltage
- ♦ Automatic, Latched Shutdown when Output Falls Out of Regulation (MAX687)
- ♦ Precision Threshold Shutdown Control (MAX688/MAX689)
- ♦ Low Supply Current:
 - 150μA Operating
 - <1μA Shutdown
- ♦ 2.7V to 11.0V Supply Range
- ♦ 8-Pin DIP/SO/μMAX Packages
- ♦ <2mV Line Transient with 3.4V to 3.6V Input
- ♦ Output Accuracy <±2%

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX687CPA	0°C to +70°C	8 Plastic DIP
MAX687CSA	0°C to +70°C	8 SO
MAX687CUA	0°C to +70°C	8 μMAX
MAX687EPA	-40°C to +85°C	8 Plastic DIP
MAX687ESA	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

Typical Operating Circuit



MAXIM

Maxim Integrated Products 4-99

Call toll free 1-800-998-8800 for free samples or literature.

MAX687/MAX688/MAX689

4

High-Accuracy, Low-Dropout Linear Regulators

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage IN to GND	12V
Terminal Voltages to GND	
PFO (MAX687)	-0.3V to $V_{OUT} + 0.3V$
PFO (MAX688/MAX689)	-0.3V to 12V
All Remaining Pins	-0.3V to $V_{IN} + 0.3V$
PFO Sink Current	10mA
PFO Source Current (MAX687)	10mA

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
Plastic DIP (derate 9.09mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	727mW
SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	471mW
μMAX (derate 4.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	330mW
Operating Temperature Ranges	
MAX68_C_A	0°C to $+70^\circ\text{C}$
MAX68_E_A	-40°C to $+85^\circ\text{C}$
Storage Temperature Range	-65°C to $+165^\circ\text{C}$
Lead Temperature (soldering, 10sec)	$+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN} = 3.8V$, $\overline{\text{SHDN}} = V_{IN}$ (MAX688/MAX689), $R_B = 0\Omega$, $C_1 = 2.2\mu\text{F}$, $C_2 = 10\mu\text{F}$, $C_3 = 10\text{nF}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR						
Supply Voltage	V_{IN}	(Note 1)	2.7		11.0	V
Output Voltage	V_{OUT}	MAX687/MAX688	$V_{IN} = 3.8V$, $I_{BASE} = 1\text{mA}$	3.2	3.3	3.4
			$3.8V \leq V_{IN} \leq 11.0V$, $1\mu\text{A} \leq I_{BASE} \leq 10\text{mA}$	3.13	3.3	3.47
		MAX689	$V_{IN} = 3.5V$, $I_{BASE} = 1\text{mA}$	2.9	3.0	3.1
			$3.5V \leq V_{IN} \leq 11.0V$, $1\mu\text{A} \leq I_{BASE} \leq 10\text{mA}$	2.85	3.0	3.15
Dropout Voltage (Note 2)	$V_{IN} - V_{OUT}$	PNP = FZT749, $I_{LOAD} = 200\text{mA}$, $C_2 = 20\mu\text{F}$		40		mV
Line Regulation		MAX687/MAX688	$3.8V \leq V_{IN} \leq 11.0V$, $I_{BASE} = 1\text{mA}$	0.4	1.4	mV/V
		MAX689	$3.5V \leq V_{IN} \leq 11.0V$, $I_{BASE} = 1\text{mA}$	0.4	1.4	
Load Regulation		$1\mu\text{A} \leq I_{BASE} \leq 10\text{mA}$		45	60	mV
Supply Current	I_{GND}	$V_{IN} = 3.8V$, PNP = FZT749, no load	On	150	250	μA
			Standby, MAX688/MAX689	11	25	
			Shutdown	< 0.02	1	
BASE Sink Current	I_{BASE}	$V_{BASE} = V_{IN} - 1V$	10	20	40	mA
Base-Current Limit		R_B is connected from BASE to BLIM (Ω), $R_B = 0\Omega$ to 100Ω	70 $\overline{R_B + 5\Omega}$	100 $\overline{R_B + 5\Omega}$	130 $\overline{R_B + 5\Omega}$	mA
Start-Up Time		(Note 3)		300		μs
Start-Up Overshoot				2		%
Load Capacitance	C_2	PNP = FZT749, $I_{LOAD} = 100\text{mA}$ (Note 4)	10			μF

High-Accuracy, Low-Dropout Linear Regulators

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 3.8V$, $\overline{SHDN} = V_{IN}$ (MAX688/MAX689), $R_B = 0\Omega$, $C_1 = 2.2\mu F$, $C_2 = 10\mu F$, $C_3 = 10nF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MAX687: ON, PFO, SHDN							
PFO Threshold Voltage Below VNOM (Note 5)	VNOM - VPFT	Falling VOUT, comparators monitor VOUT		110	170		mV
PFO Hysteresis					7		mV
Shutdown Threshold Voltage Below VPFT	VPFT - VSD	Falling VOUT, comparators monitor VOUT		20	70		mV
Shutdown Threshold Voltage	VSD	Falling VOUT, comparators monitor VOUT		2.96			V
PFO Output Voltage High	VOH	ISOURCE = 50μA, part on, VIN = 2.7V		VOUT - 0.3			V
PFO Output Voltage Low	VOL	ISINK = 1.2mA, VIN = 2.7V			0.06	0.3	V
ON Threshold Voltage	VIH	Output turns on		1.0			V
	VIL	Output remains off				0.2	
ON Input Leakage Current					0.2	100	nA
MAX688/MAX689: SHDN, PFO							
PFO Threshold Voltage	VPFT	Falling VOUT, comparators monitor VOUT	MAX688	3.07	3.13	3.19	V
			MAX689	2.77	2.85	2.89	
PFO Hysteresis					7		mV
SHDN Threshold Voltages	VSON	On, SHDN falling		1.25			V
	VSSY	Standby		1.0		1.2	
	VSSD	Shutdown				0.2	
SHDN Hysteresis		Rising SHDN, standby→on			70		mV
SHDN Input Current		V SHDN = 1.23V		-25		25	nA
PFO, SHDN Transient Rejection		Glitch immunity			100		μs
PFO Output Voltage Low	VOL	ISINK = 1.2mA, VIN = 2.7V			0.06	0.3	V
PFO Off Leakage Current		V PFO = 11V, V SHDN > 1.25V				1	μA
Output Noise Voltage	en	10Hz ≤ f ≤ 10kHz, ILOAD = 200mA			66		μVRMS
		10Hz ≤ f ≤ 1MHz, ILOAD = 200mA			105		

Note 1: Minimum V_{IN} for regulated V_{OUT} depends on the characteristics of the external PNP transistor, and on the load. The reference and comparators are functional down to the minimum voltage specified, but the output may not be in regulation.

Note 2: Dropout voltage is defined as $V_{IN} - V_{OUT}$ when V_{OUT} is 50mV below its value at $V_{IN} = V_{NOM} + 1V$.

Note 3: The start-up time specification is the time taken from ON or $\overline{SHDN}$ rising to BASE sinking current. V_{OUT} rise time is longer and is a function of load capacitance, C_2 , and load resistance, R_L .

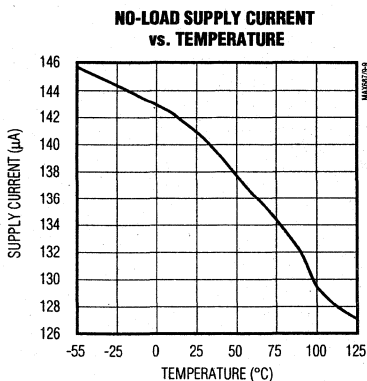
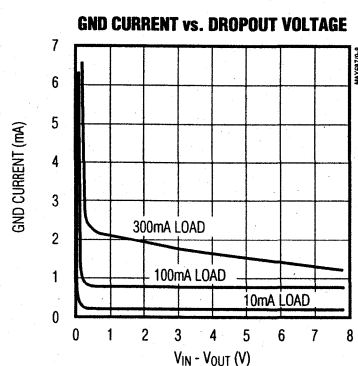
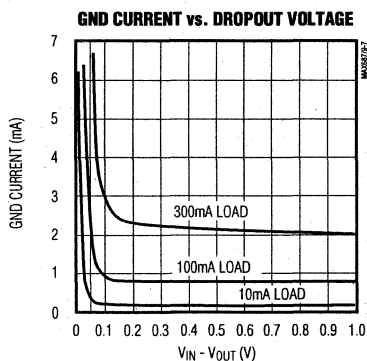
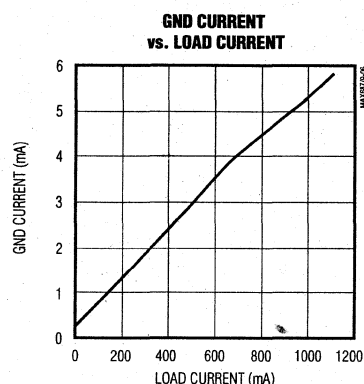
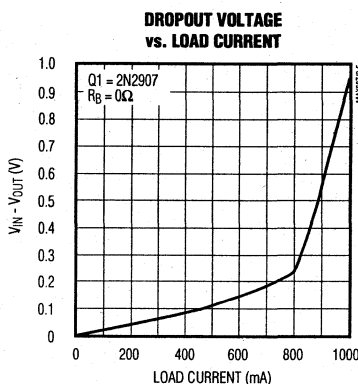
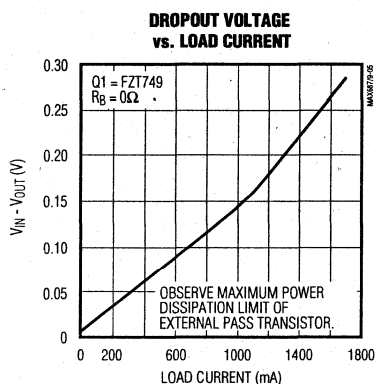
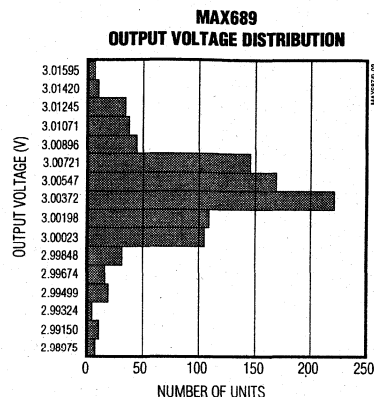
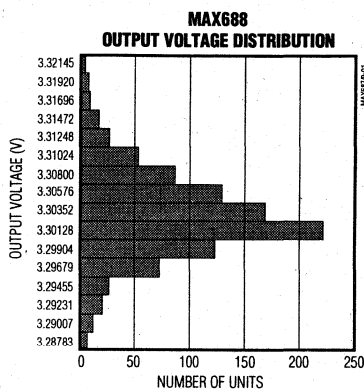
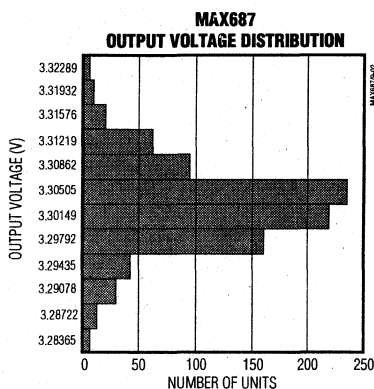
Note 4: Minimum load capacitance is a function of R_L . Minimum $C_2 = 10\mu F$ for loads up to 100mA and $1\mu F/10mA$ for higher loads. ESR of C_2 should be no larger than 1/100 of R_L . Guaranteed by design.

Note 5: The nominal output voltage, V_{NOM} , is defined under the default conditions of testing: $V_{IN} = 3.8V$, $I_{BASE} = 1mA$, $T_A = T_{MIN}$ to T_{MAX} .

High-Accuracy, Low-Dropout Linear Regulators

Typical Operating Characteristics

(Circuits of Figures 1 and 2, $V_{IN} = 5V$, $Q1 = FZT749$, $T_A = +25^\circ C$, unless otherwise noted.)

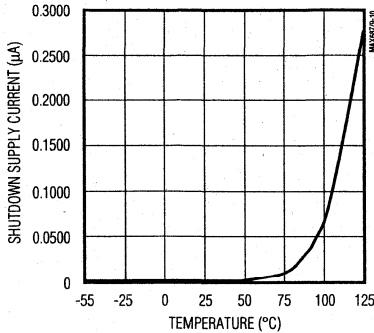


High-Accuracy, Low-Dropout Linear Regulators

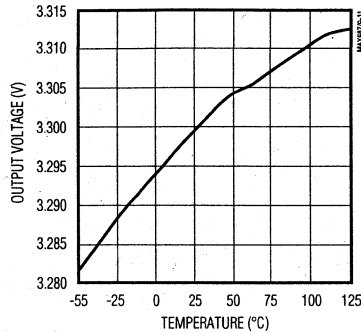
Typical Operating Characteristics (continued)

(Circuits of Figures 1 and 2, $V_{IN} = 5V$, $Q1 = FZT749$, $T_A = +25^\circ C$, unless otherwise noted.)

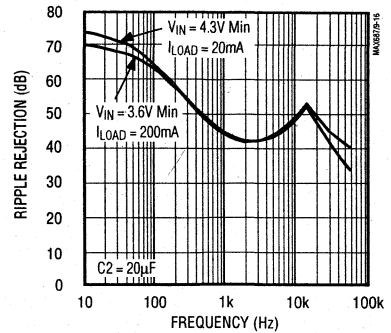
**SHUTDOWN SUPPLY CURRENT
vs. TEMPERATURE**



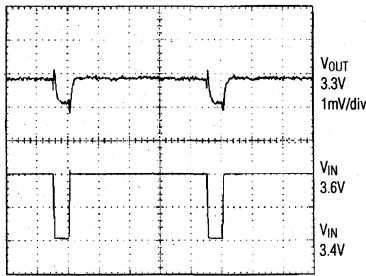
**OUTPUT VOLTAGE
vs. TEMPERATURE**



**MAX687/MAX688
RIPPLE REJECTION vs. FREQUENCY**

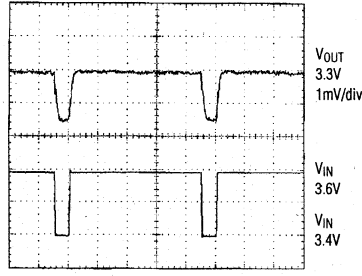


LINE-TRANSIENT RESPONSE



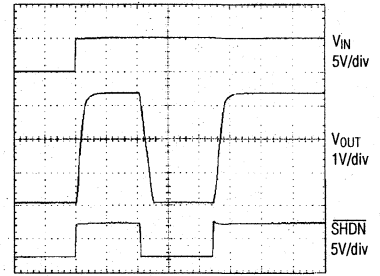
$I_{LOAD} = 70mA$
 $C1 = 2.2\mu F$
 $C2 = 20\mu F$
 $C3 = 10nF$

LINE-TRANSIENT RESPONSE



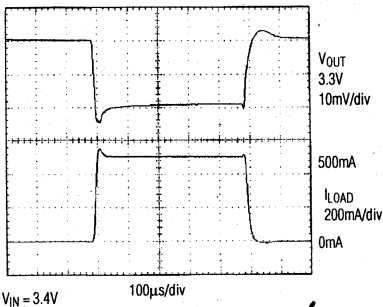
$I_{LOAD} = 200mA$
 $C1 = 2.2\mu F$
 $C2 = 20\mu F$
 $C3 = 10nF$

**MAX687/MAX688
POWER-UP AND EXIT FROM SHUTDOWN**

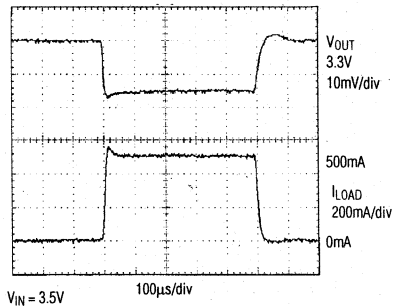


$I_{LOAD} = 500mA$
 $C1 = 2.2\mu F$
 $C2 = 68\mu F$
 $C3 = 10nF$

LOAD-TRANSIENT RESPONSE



LOAD-TRANSIENT RESPONSE



High-Accuracy, Low-Dropout Linear Regulators

Pin Description

PIN	NAME	FUNCTION
1	IN	Positive input voltage, 2.7V to 11.0V
2	ON (MAX687)	ON activates the regulator when pulsed high. In order for the regulator to remain on, ON must remain high until V_{OUT} exceeds the internal shutdown threshold voltage. The MAX687 is shut down when $V_{OUT} < 2.96V$, and remains latched off until ON is pulsed high. When powered up, the MAX687 does not start up until ON is pulsed high. Connect to V_{IN} if not used.
	SHDN (MAX688/ MAX689)	SHDN is a three-level input that controls the mode of operation. The device is on when $V_{SHDN} > 1.25V$. The output is disabled and the supply current is reduced ($I_{IN} < 25\mu A$, standby mode) when $V_{SHDN} < 1.2V$, and is fully off ($I_{IN} < 1\mu A$, shutdown mode) when $V_{SHDN} < 0.2V$. Connect SHDN to IN if the shutdown function is not used. PFO is low when SHDN is low (below 0.2V).
3	PFO	Power-Fail Output. PFO trips when V_{OUT} is 170mV below nominal V_{OUT} at $I_{BASE} = 1mA$. PFO sources and sinks current in the MAX687, but is an open drain in the MAX688/MAX689. When shut down, PFO is always low and sinks current. Leave PFO open if not used.
4	GND	Ground
5	OUT	Regulator Output. MAX687/MAX688, 3.3V; MAX689, 3.0V.
6	BLIM	Base current limit. A resistor (R_B) connected between BASE and BLIM sets the maximum base drive to the PNP transistor: $I_{BASE} \leq 0.1V / (R_B + 5\Omega)$. This limits quiescent current rise during dropout and also provides current limiting without using a current-sense resistor in the collector of the external PNP, thus not impacting dropout. Output current limiting accuracy depends on how well the external PNP beta (h_{FE}) is controlled. Connect to BASE if not used.
7	BASE	Base drive for the external PNP transistor. Current limiting is controlled using a resistor (R_B) connected between BASE and BLIM. For maximum output current, connect BASE to BLIM.
8	CC	Compensation Capacitor. Connect a non-polarized capacitor (10nF to 100nF) from CC to GND.

Detailed Description

The MAX687/MAX688/MAX689 are precision low-dropout linear regulators employing external PNP transistors to achieve a wide range of output currents at voltages of 3.0V or 3.3V. The maximum base current for the PNP can be limited using a resistor. Limiting the base drive keeps high currents from being wasted when the device is in dropout (e.g., at low input voltages), and limits the regulator's output current. The dropout voltage is limited only by the PNP transistor's $V_{CE(SAT)}$. The Power-Fail Output (PFO) goes low when the output voltage drops 170mV below the nominal level.

The three devices differ in their output voltages, in their shutdown-control functions, and in PFO's output drive (see Table 1).

Table 1. Device Functions

FUNCTION	MAX687	MAX688	MAX689
V_{OUT}	3.3V	3.3V	3.0V
Shutdown Control	Automatic at low V_{OUT} . Latched. Use ON to start.	External SHDN	External SHDN
PFO	Sources & Sinks	Open Drain	Open Drain

The MAX687's output voltage is internally monitored; a falling V_{OUT} is signaled by PFO going low. As the output falls further, the MAX687 automatically enters a low-power shutdown mode, where the base drive to the external PNP is cut off. PFO trips at a minimum of 110mV below the nominal V_{OUT} , and shutdown occurs by 2.96V. PFO is guaranteed to trip before the device

High-Accuracy, Low-Dropout Linear Regulators

shuts down. Once the MAX687 is shut down, it can only be turned on again when (a) the ON pin is pulsed high, and (b) the conditions that triggered shutdown have changed (e.g., the load has been reduced or the input voltage has increased). In order for the MAX687 to latch into its on state, the ON pulse must remain high until the output voltage has risen above the shutdown threshold. The internal shutdown can be used to prevent deep discharge of a battery, for example, to provide "self backup" of CMOS RAM or to protect the battery itself.

The RC circuit attached to the ON input in Figure 1 achieves automatic start-up at power-on by delivering a brief pulse whenever the input voltage is suddenly applied. This circuit is not suitable for applications where the input voltage rises slowly. The RC values should be chosen to keep ON high until the output rises above about 3.13V. The values shown in Figure 1 for C4 and R1 (0.1 μ F and 10k Ω) are suitable for most applications. To ensure start-up when the input voltage is very close to the circuit's dropout voltage, when the circuit is used to drive a very large capacitive load, or for high-power circuits (I_{LOAD} > 3A), increase the value of R1 to increase the ON pulse width.

The 3.3V MAX688 and the 3.0V MAX689 incorporate the same PFO warning whenever V_{OUT} droops. However, the MAX688/MAX689 do not automatically shut down when the output voltage drops even further. Instead, the SHDN input controls external shutdown. As SHDN is pulled low, the chip first enters a low-current standby state (<25 μ A). The threshold at which standby mode is entered is precisely controlled ($\pm 2\%$) so the output can be turned off at a well-defined point.

70mV of hysteresis between the standby and on states prevents chatter between the two modes. The voltage applied to the SHDN pin can be derived from a resistive divider from V_{IN}. When V_{SHDN} is less than 1.2V, the output is off. The device is fully shut down (<1 μ A) when SHDN is pulled below 200mV. SHDN is not latched, and as SHDN is raised, the MAX688/MAX689 exit shutdown and enter the standby mode. At the higher SHDN threshold, the output is turned on.

Figure 1 shows a typical circuit for the MAX687, and Figure 2 shows the same circuit configured for the MAX688/MAX689.

The accuracy of the output current limit depends on accurate knowledge of the PNP pass transistor's current gain (h_{FE}). With R_B = 12 Ω , BLIM limits base current to 6mA (I_{BASE} = 0.1V / (R_B + 5 Ω)). See *Base-Current Limiting* section.

The PFO comparators on all three devices, and the internal shutdown comparator on the MAX687, reject high-speed spikes (<100 μ s). This reduces the PFO output's noise sensitivity, and stops the MAX687 from being shut down inadvertently when there is noise on the input supply.

Transistor Selection

Specifications

The PNP pass transistor must meet specifications for

- current gain,
- power dissipation, and
- collector current.

The h_{FE} influences the maximum output current the circuit can deliver. The largest guaranteed output current

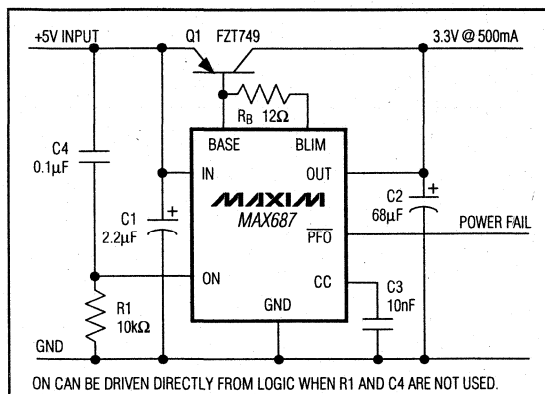


Figure 1. MAX687 Operating Circuit

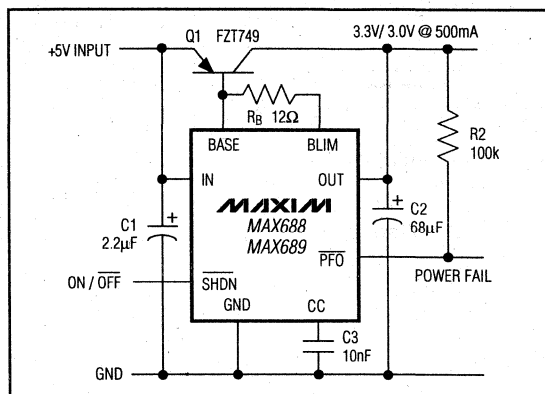


Figure 2. MAX688/MAX689 Operating Circuit

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is given by $I_{LOAD(MAX)} = 10mA \times h_{FE(MIN)}$. The transistor's rated power dissipation must exceed the actual power dissipated in the transistor. The power dissipated (PD) equals the maximum load current ($I_{LOAD(MAX)}$) times the maximum input to output voltage differential: $PD = I_{LOAD(MAX)} \times (V_{IN(MAX)} - V_{OUT})$. The rated transistor collector current must exceed the maximum load current. Suitable transistors include the Zetex FZT749, and the 2N2907A (see Table 2).

Base-Current Limiting

A comparator monitors the voltage across the external base-current-limiting resistor (between BASE and BLIM). This sets the maximum base current. If BASE and BLIM are shorted, base current is limited nominally to 20mA due to an internal 5Ω resistor in series with the external resistance. Choose the base-current-limiting resistor, R_B , so the drop across it at rated load is approximately 50mV.

$$R_B = \frac{(50mV) \times h_{FE(MIN)}}{I_{LOAD(MAX)}} - 5\Omega$$

The base drive is controlled so the voltage on BLIM is limited to 100mV below the voltage on BASE; with a 50mV nominal drop across $R_B + 5\Omega$, base-current drive is limited to twice the nominal. This limits base current when the external PNP is heavily saturated, such as when the regulator is in dropout due to low input voltage. In addition, if the external PNP's h_{FE} is defined within reasonable limits, base-current control effectively limits output current without a dropout voltage penalty.

Capacitor Selection

Bypass Capacitor (C1)

Connect a bypass capacitor from IN to GND. $4.7\mu F$ makes the circuit insensitive to layout, and is sufficient for any load. Smaller values may be used—down to $0.33\mu F$ —with low-ESR capacitors, good board layout, and a low-impedance incoming supply.

Connect the bypass capacitor directly between pins 1 and 4 of the IC, using short leads. Connect the emitter of the PNP transistor directly to the bypass capacitor using a very short trace.

Output Capacitor (C2)

The output filter capacitor must be at least $10\mu F$. For currents above 100mA, use $1\mu F$ of capacitance for every 10mA of load current (e.g., $20\mu F$ for 200mA load, $50\mu F$ for 500mA). Low-ESR capacitors give best stability and transient response. Ensure that the capacitor's ESR is less than 1% of the load resistance. See Table 2 for a list of manufacturers. Sanyo OS-CON capacitors are recommended for applications operating at temperatures below $0^\circ C$.

Compensation Capacitor (C3)

Connect a compensation capacitor from CC to GND. $10nF$ is recommended, although higher values (up to $100nF$) may also be used. Higher C3 values eliminate power-on overshoot, but extend power-up times. Current flowing into or out of CC causes the regulator's reference voltage to change, resulting in shifted output voltage and trip thresholds. Use non-polarized capacitors (e.g., ceramic, polyester, etc.) to keep leakage currents below 25nA. Aluminum and tantalum electrolytic capacitors are unsuitable because of their high leakage currents.

Power-Fail Output

The $\overline{PFO}$ output trips when V_{OUT} is 170mV below nominal V_{OUT} at $I_{BASE} = 1mA$. $\overline{PFO}$ sources and sinks current in the MAX687, but is an open drain in the MAX688/MAX689 and only sinks current. When shut down, $\overline{PFO}$ is always low regardless of the voltage at OUT. Leave $\overline{PFO}$ open if it is not used.

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Applications Information

High-Power Output Circuit

Figure 3 shows a pseudo-Darlington transistor configuration to increase load-current capability and maintain a low dropout voltage with a 4A load. A heatsink must be added when high power is dissipated in the pass transistor.

Figure 4 shows the ($V_{IN} - V_{OUT}$) voltage required to maintain regulation for different load currents. Figure 5 shows an oscilloscope plot of the transient response of a 200mA to 4A load step.

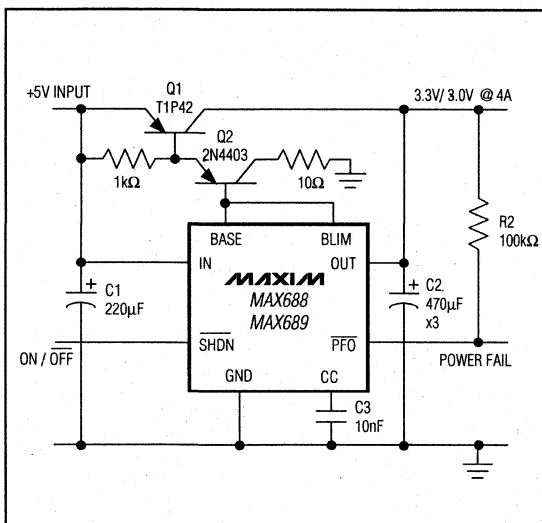


Figure 3. 4A Low-Dropout Circuit

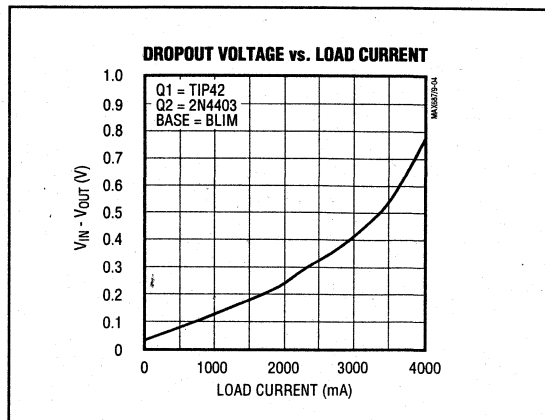


Figure 4. Dropout Voltage vs. Load Current of Figure 3

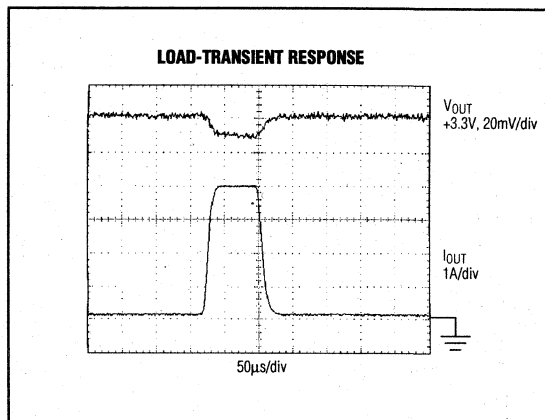


Figure 5. Transient Response for a 200mA to 4A Load Step Using Circuit of Figure 3

High-Accuracy, Low-Dropout Linear Regulators

Table 2a. Component Suppliers

DEVICE	MANUFACTURER	PRODUCTION METHOD
CAPACITORS		
267 series	Matsuo	Surface Mount
F95 Tantalum series	Nichicon	
595 Tantalum series	Sprague	
OS-CON series low-ESR organic semiconductor	Sanyo	Through-Hole
LXF series	United Chemi-Con	
BIPOLAR TRANSISTORS		
ZTX749	Zetex	Through-Hole
T1P42	Motorola	
2N4403	Motorola	
2N2907A	Motorola	
CMPT2907A	Central Semiconductor	Surface Mount
PZT2907AT1	Motorola	
FZT749	Zetex	

Table 2b. Manufacturers' Phone
and Fax Numbers

MANU-FACTURER	COUNTRY	TELEPHONE	FAX
Central Semiconductor	USA	(516) 435-1110	(516) 435-1824
Matsuo	USA	(714) 969-2491	(714) 960-6492
Motorola	USA	(602) 244-3370	(602) 244-4015
Nichicon	USA	(708) 843-7500	(708) 843-2798
	Japan	+81-7-5231-8461	+81-7-5256-4158
Sanyo	USA	(619) 661-6835	(619) 661-1055
	Japan	+81-7-2070-6306	+81-7-2070-1174
Sprague	USA	(603) 224-1961	(603) 224-1430
United Chemi-Con	USA	(714) 255-9500	(714) 255-9400
Zetex	USA	(516) 543-7100	(516) 864-7630
	UK	+44-61-627-5105	+44-61-627-5467

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX688 CPA	0°C to +70°C	8 Plastic DIP
MAX688CSA	0°C to +70°C	8 SO
MAX688CUA	0°C to +70°C	8 μ MAX
MAX688EPA	-40°C to +85°C	8 Plastic DIP
MAX688ESA	-40°C to +85°C	8 SO
MAX689 CPA	0°C to +70°C	8 Plastic DIP
MAX689CSA	0°C to +70°C	8 SO
MAX689CUA	0°C to +70°C	8 μ MAX
MAX689EPA	-40°C to +85°C	8 Plastic DIP
MAX689ESA	-40°C to +85°C	8 SO

EVALUATION KITS
AVAILABLE

MAXIM

Step-Down Controllers with Synchronous Rectifier for CPU Power

General Description

The MAX796/MAX797/MAX799 high-performance, step-down DC-DC converters with single or dual outputs provide main CPU power in battery-powered systems. These buck controllers achieve 96% efficiency by using synchronous rectification and Maxim's proprietary Idle Mode™ control scheme to extend battery life at full-load (up to 10A) and no-load outputs. Excellent dynamic response corrects output transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Unique bootstrap circuitry drives inexpensive N-channel MOSFETs, reducing system cost and eliminating the crowbar switching currents found in some PMOS/NMOS switch designs.

The MAX796/MAX799 are specially equipped with a secondary feedback input (SECFB) for transformer-based dual-output applications. This secondary feedback path improves cross-regulation of positive (MAX796) or negative (MAX799) auxiliary outputs.

The MAX797 has a logic-controlled and synchronizable fixed-frequency pulse-width-modulating (PWM) operating mode, which reduces noise and RF interference in sensitive mobile-communications and pen-entry applications. The SKIP override input allows automatic switchover to idle-mode operation (for high-efficiency pulse skipping) at light loads, or forces fixed-frequency mode for lowest noise at all loads.

The MAX796/MAX797/MAX799 are all available in 16-pin DIP and narrow SO packages. See the table below to compare these three converters.

PART	MAIN OUTPUT	SPECIAL FEATURE
MAX796	3.3V/5V or adj.	Regulates positive secondary voltage (such as +12V)
MAX797	3.3V/5V or adj.	Logic-controlled low-noise mode
MAX799	3.3V/5V or adj.	Regulates negative secondary voltage (such as -5V)

Applications

Notebook and Subnotebook Computers
PDAs and Mobile Communicators
Cellular Phones

Features

- ♦ 96% Efficiency
- ♦ 4.5V to 30V Input Range
- ♦ 2.5V to 6V Adjustable Output
- ♦ Preset 3.3V and 5V Outputs (at up to 10A)
- ♦ Multiple Regulated Outputs
- ♦ +5V Linear-Regulator Output
- ♦ Precision 2.505V Reference Output
- ♦ Automatic Bootstrap Circuit
- ♦ 150kHz/300kHz Fixed-Frequency PWM Operation
- ♦ Programmable Soft-Start
- ♦ 375µA Typ Quiescent Current ($V_{IN} = 12V$, $V_{OUT} = 5V$)
- ♦ 1µA Typ Shutdown Current

Ordering Information

EV KIT	V _{OUT}	BOARD TYPE
MAX796EVKIT-SO	+5V/+15V (dual)	Surface Mount
MAX797EVKIT-SO	+3.3V or Adj.	Surface Mount

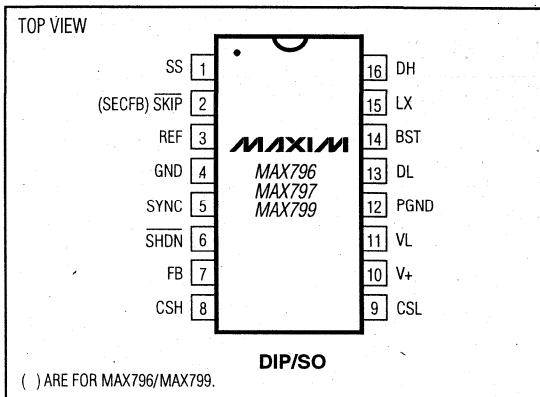
PART	TEMP. RANGE	PIN-PACKAGE
MAX796CPE	0°C to +70°C	16 Plastic DIP
MAX796CSE	0°C to +70°C	16 Narrow SO
MAX796C/D	0°C to +70°C	Dice*
MAX796EPE	-40°C to +85°C	16 Plastic DIP
MAX796ESE	-40°C to +85°C	16 Narrow SO
MAX796MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

*Contact factory for dice specifications.

U.S. and foreign patents pending.

Pin Configuration



™ Idle Mode is a trademark of Maxim Integrated Products.

MAXIM

Maxim Integrated Products 4-109

Call toll free 1-800-998-8800 for free samples or literature.

MAX796/MAX797/MAX799

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Step-Down Controllers with Synchronous Rectifier for CPU Power

ABSOLUTE MAXIMUM RATINGS

V+ to GND	-0.3V, +36V
GND to PGND	±2V
VL to GND	-0.3V, +7V
BST to GND	-0.3V, +36V
DH to LX	-0.3V, BST + 0.3V
LX to BST	-7V, +0.3V
SHDN to GND	-0.3V, +36V
SYNC, SS, REF, SECFB, SKIP, DL to GND	-0.3V, VL + 0.3V
CSH, CSL to GND	-0.3V, +7V
VL Short Circuit to GND	Momentary
REF Short Circuit to GND	Continuous

VL Output Current	50mA
Continuous Power Dissipation (TA = +70°C)	
SO (derate 8.70mW/°C above +70°C)	696mW
Plastic DIP (derate 10.53mW/°C above +70°C)	842mW
CERDIP (derate 10.00mW/°C above +70°C)	800mW
Operating Temperature Ranges	
MAX79_C	0°C to +70°C
MAX79_E	-40°C to +85°C
MAX79_MJE	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0A, TA = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	
+3.3V AND +5V STEP-DOWN CONTROLLERS							
Input Supply Range		MAX79_C	4.5		30	V	
		MAX79_E/M	5.0		30		
5V Output Voltage (CSL)	0mV < (CSH-CSL) < 80mV, FB = VL, 6V < V+ < 30V, includes line and load regulation		4.85	5.10	5.25	V	
3.3V Output Voltage (CSL)	0mV < (CSH-CSL) < 80mV, FB = 0V, 4.5V < V+ < 30V, includes line and load regulation		3.20	3.35	3.46	V	
Nominal Adjustable Output Voltage Range	External resistor divider		REF		6	V	
Feedback Voltage	(CSH-CSL) = 0V		2.43	2.505	2.57	V	
Load Regulation	0mV < (CSH-CSL) < 80mV		2.5			%	
	25mV < (CSH-CSL) < 80mV		1.5				
Line Regulation	6V < V+ < 30V		0.04			0.06	%/V
Current-Limit Voltage	CSH-CSL, positive		80	100	120	mV	
	CSH-CSL, negative		-50	-100	-160		
SS Source Current			2.5	4.0	6.5	μA	
SS Fault Sink Current			2.0			mA	
FLYBACK/PWM CONTROLLER							
SECFB Regulation Setpoint	Falling edge, hysteresis = 15mV (MAX796)		2.45	2.505	2.55	V	
	Falling edge, hysteresis = 20mV (MAX799)		-0.05	0	0.05		
INTERNAL REGULATOR AND REFERENCE							
VL Output Voltage	SHDN = 2V, 0mA < I _{VL} < 25mA, 5.5V < V+ < 30V		4.7		5.3	V	
VL Fault Lockout Voltage	Rising edge, hysteresis = 15mV		3.8		4.0	V	
VL/CSL Switchover Voltage	Rising edge, hysteresis = 25mV		4.2		4.7	V	

Step-Down Controllers with Synchronous Rectifier for CPU Power

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0A, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

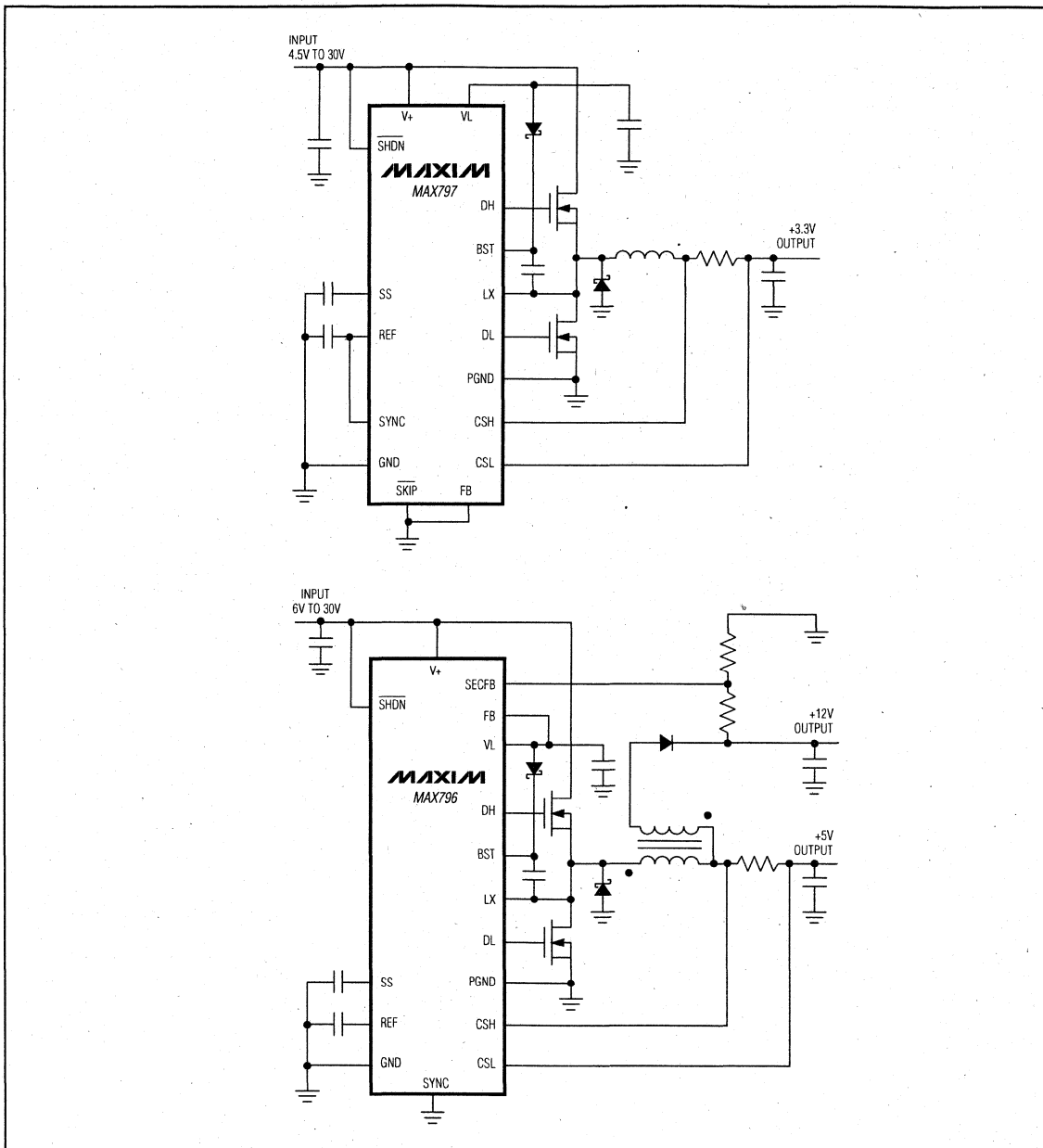
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Output Voltage	No external load (Note 1)	MAX79_C	2.46	2.505	2.54	V
		MAX79_E/M	2.45		2.55	
Reference Fault Lockout Voltage	Falling edge		1.8		2.3	V
Reference Load Regulation	0μA < IREF < 100μA				50	mV
CSL Shutdown Leakage Current	SHDN = 0V, CSL = 6V, V+ = 0V or 30V, VL = 0V			0.1	1	μA
V+ Shutdown Current	SHDN = 0V, V+ = 30V, CSL = 0V or 6V	MAX79_C		1	3	μA
		MAX79_E/M		1	5	
V+ Off-State Leakage Current	FB = CSH = CSL = 6V, VL switched over to CSL	MAX79_C		1	3	μA
		MAX79_E/M		1	5	
Dropout Power Consumption	V+ = 4V, CSL = 0V (Note 2)			4	8	mW
Quiescent Power Consumption	CSH = CSL = 6V			4.8	6.6	mW
OSCILLATOR AND INPUTS/OUTPUTS						
Oscillator Frequency	SYNC = REF		270	300	330	kHz
	SYNC = 0V or 5V		125	150	175	
SYNC High Pulse Width			200			ns
SYNC Low Pulse Width			200			ns
SYNC Rise/Fall Time	Guaranteed by design				200	ns
Oscillator Sync Range			190		340	kHz
Maximum Duty Cycle	SYNC = REF		89	91		%
	SYNC = 0V or 5V		93	96		
Input High Voltage	SYNC		VL - 0.5			V
	SHDN, SKIP		2.0			
Input Low Voltage	SYNC				0.8	V
	SHDN, SKIP				0.5	
Input Current	SHDN, 0V or 30V				2.0	μA
	SECFB, 0V or 4V				0.1	
	SYNC, SKIP				1.0	
	CSH, CSL, CSH = CSL = 6V, device not shut down				50	
	FB, FB = REF				±100	nA
DL Sink/Source Current	DL forced to 2V			1		A
DH Sink/Source Current	DH forced to 2V, BST-LX = 4.5V			1		A
DL On-Resistance	High or low				7	Ω
DH On-Resistance	High or low, BST-LX = 4.5V				7	Ω

Note 1: Since the reference uses VL as its supply, V+ line-regulation error is insignificant.

Note 2: At very low input voltages, quiescent supply current may increase due to excess PNP base current in the VL linear regulator. This occurs only if V+ falls below the preset VL regulation point (5V nominal). See the Quiescent Supply Current vs. Supply Voltage graph in the *Typical Operating Characteristics*.

Step-Down Controllers with Synchronous Rectifier for CPU Power

Typical Operating Circuits

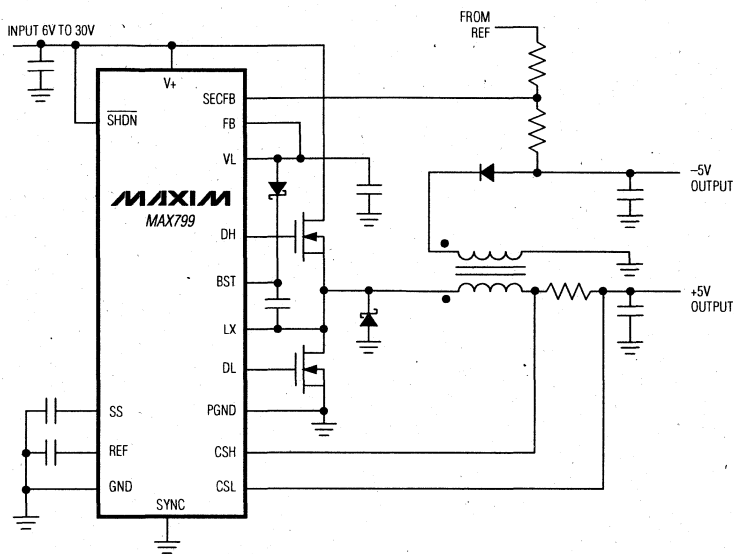


Step-Down Controllers with Synchronous Rectifier for CPU Power

Typical Operating Circuits (continued)

MAX796/MAX797/MAX799

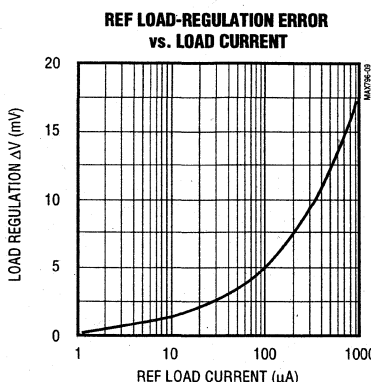
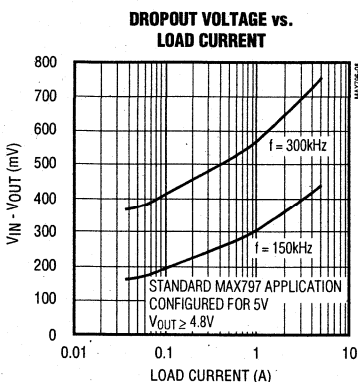
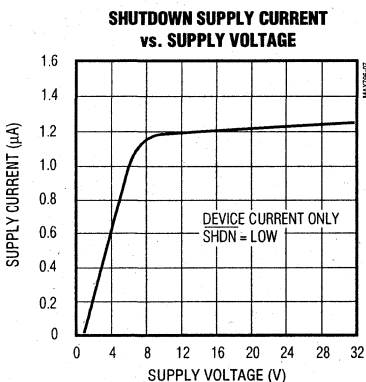
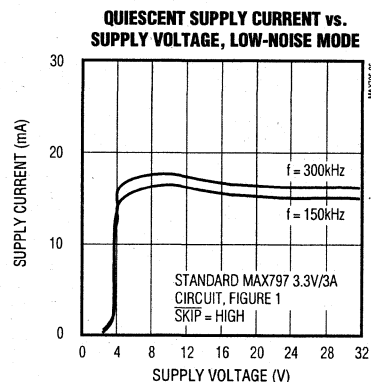
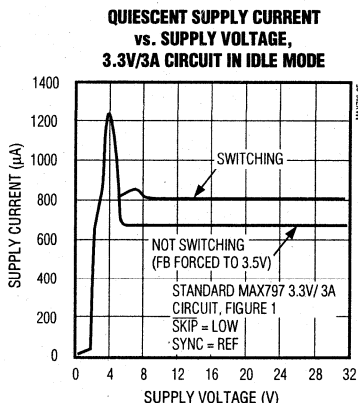
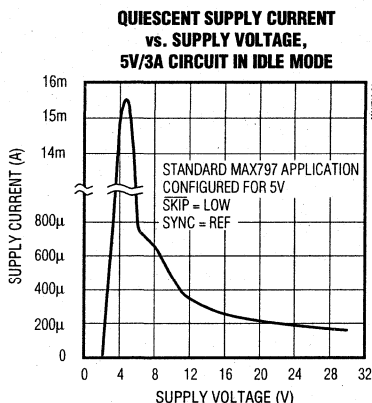
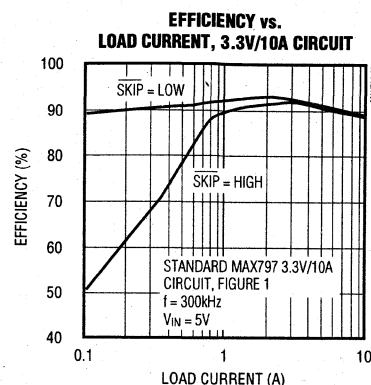
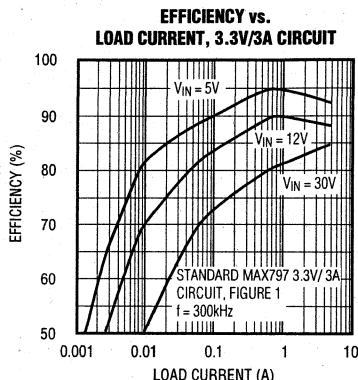
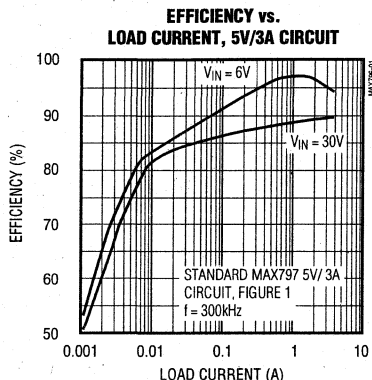
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Step-Down Controllers with Synchronous Rectifier for CPU Power

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

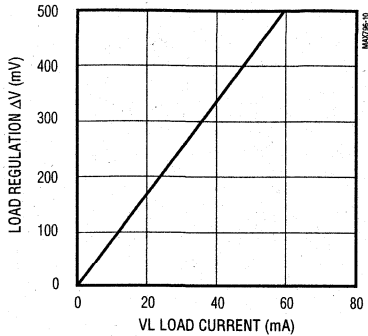


Step-Down Controllers with Synchronous Rectifier for CPU Power

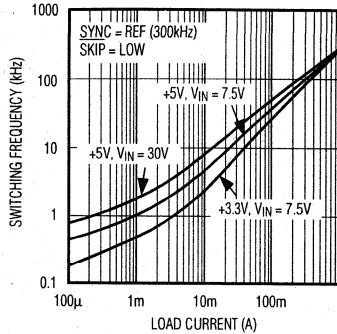
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

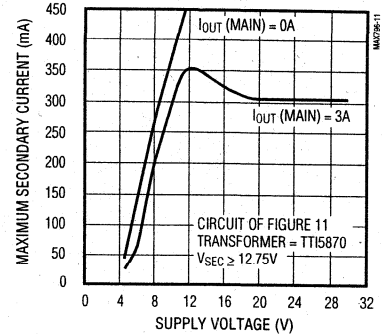
VL LOAD-REGULATION ERROR vs. LOAD CURRENT



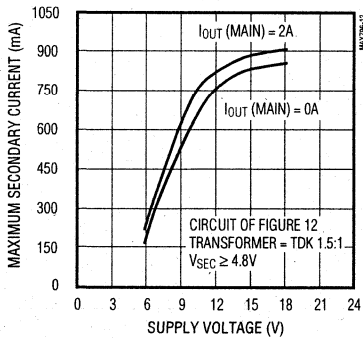
SWITCHING FREQUENCY vs. LOAD CURRENT



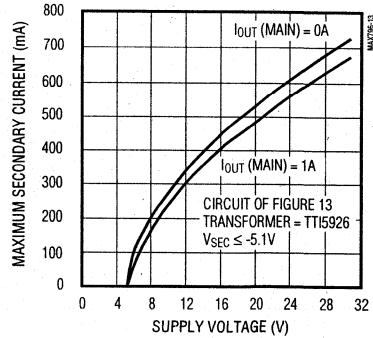
**MAX796
MAXIMUM SECONDARY CURRENT vs. SUPPLY VOLTAGE, 5V/15V CIRCUIT**



**MAX796
MAXIMUM SECONDARY CURRENT vs. SUPPLY VOLTAGE, 3.3V/5V CIRCUIT**



**MAX799
MAXIMUM SECONDARY CURRENT vs. SUPPLY VOLTAGE, ±5V CIRCUIT**

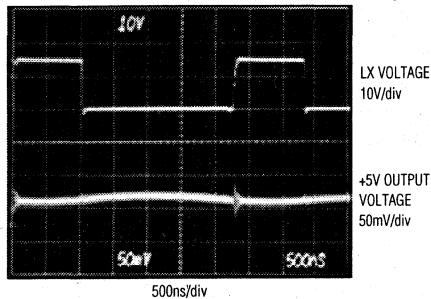


Step-Down Controllers with Synchronous Rectifier for CPU Power

Typical Operating Characteristics (continued)

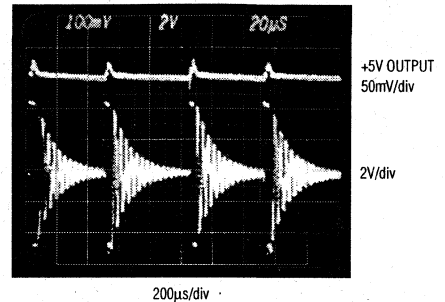
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

PULSE-WIDTH-MODULATION MODE WAVEFORMS



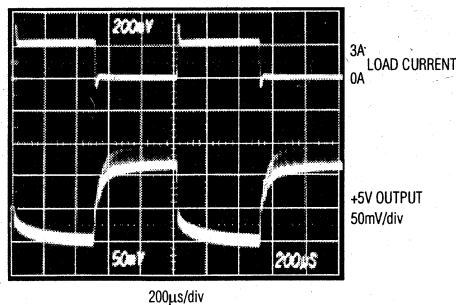
$I_{\text{LOAD}} = 1\text{A}$, $V_{\text{IN}} = 16\text{V}$,
CIRCUIT OF FIGURE 1

IDLE-MODE WAVEFORMS



$I_{\text{LOAD}} = 100\text{mA}$, $V_{\text{IN}} = 10\text{V}$,
CIRCUIT OF FIGURE 1

+5V LOAD-TRANSIENT RESPONSE



$V_{\text{IN}} = 15\text{V}$, CIRCUIT OF FIGURE 1

Step-Down Controllers with Synchronous Rectifier for CPU Power

Pin Description

PIN	NAME	FUNCTION
1	SS	Soft-Start timing capacitor connection. Ramp time to full current limit is approximately 1ms/nF.
2	SECFB (MAX796/ MAX799)	Secondary winding Feedback input. Normally connected to a resistor divider from an auxiliary output. Don't leave SECFB unconnected. - MAX796: SECFB regulates at VSECFB = 2.505V. Tie to VL if not used. - MAX799: SECFB regulates at VSECFB = 0V. Tie to a negative voltage through a high-value current-limiting resistor (I_{MAX} = 100μA) if not used.
	SKIP (MAX797)	Disables pulse-skipping mode when high. Connect to GND for normal use. Don't leave SKIP unconnected. With SKIP grounded, the device will <i>automatically</i> change from pulse-skipping operation to full PWM operation when the load current exceeds approximately 30% of maximum. (See Table 3.)
3	REF	Reference voltage output. Bypass to GND with 0.33μF minimum.
4	GND	Low-noise analog Ground and feedback reference point.
5	SYNC	Oscillator Synchronization and frequency select. Tie to GND or VL for 150kHz operation; tie to REF for 300kHz operation. A high-to-low transition begins a new cycle. Drive SYNC with 0V to 5V logic levels (see the <i>Electrical Characteristics</i> table for V _{IH} and V _{IL} specifications). SYNC capture range is 190kHz to 340kHz guaranteed.
6	SHDN	Shutdown control input, active low. Logic threshold is set at approximately 1V (V _{TH} of an internal N-channel MOSFET). Tie SHDN to V+ for automatic start-up.
7	FB	Feedback input. Regulates at FB = REF (approximately 2.505V) in adjustable mode. FB is a Dual-Mode™ input that also selects the fixed output voltage settings as follows: - Connect to GND for 3.3V operation. - Connect to VL for 5V operation. - Connect FB to a resistor divider for adjustable mode. FB can be driven with +5V rail-to-rail logic in order to change the output voltage under system control.
8	CSH	Current-Sense input, High side. Current-limit level is 100mV referred to CSL.
9	CSL	Current-Sense input, Low side. Also serves as the feedback input in fixed-output modes.
10	V+	Battery voltage input (4.5V to 30V). Bypass V+ to PGND close to the IC with a 0.1μF capacitor. Connects to a linear regulator that powers VL.
11	VL	5V Internal linear-regulator output. VL is also the supply voltage rail for the chip. VL is switched to the output voltage via CSL (V _{CSL} > 4.5V) for automatic bootstrapping. Bypass to GND with 4.7μF. VL can supply up to 5mA for external loads.
12	PGND	Power Ground.
13	DL	Low-side gate-drive output. Normally drives the synchronous-rectifier MOSFET. Swings 0V to VL.
14	BST	Boost capacitor connection for high-side gate drive (0.1μF).
15	LX	Switching node (inductor) connection. Can swing 2V below ground without hazard.
16	DH	High-side gate-drive output. Normally drives the main buck switch. DH is a floating driver output that swings from LX to BST, riding on the LX switching-node voltage.

™ Dual Mode is a trademark of Maxim Integrated Products.

Step-Down Controllers with Synchronous Rectifier for CPU Power

Standard Application Circuit

It is easy to adapt the basic MAX797 single-output 3.3V buck converter (Figure 1) to meet a wide range of applications with inputs up to 28V (limited by choice of external MOSFET). Simply substitute the appropriate components from Table 1. These circuits represent a good set of tradeoffs between cost, size, and efficiency while staying within the worst-case specification limits for stress-related parameters such as capacitor ripple current. Each of these circuits is rated for a continuous load current at $T_A = +85^\circ\text{C}$, as shown. The 1A, 2A and 10A applications can withstand a continuous output short-circuit to ground. The 3A and 5A applications can

withstand a short circuit of many seconds duration, but the synchronous-rectifier MOSFET overheats, exceeding the manufacturer's ratings for junction temperature by 50°C or more.

If the 3A or 5A circuit must be guaranteed to withstand a continuous output short circuit indefinitely, see the section *MOSFET Switches* under *Selecting Other Components*. Don't change the frequency of these circuits without first recalculating component values (particularly inductance value at maximum battery voltage).

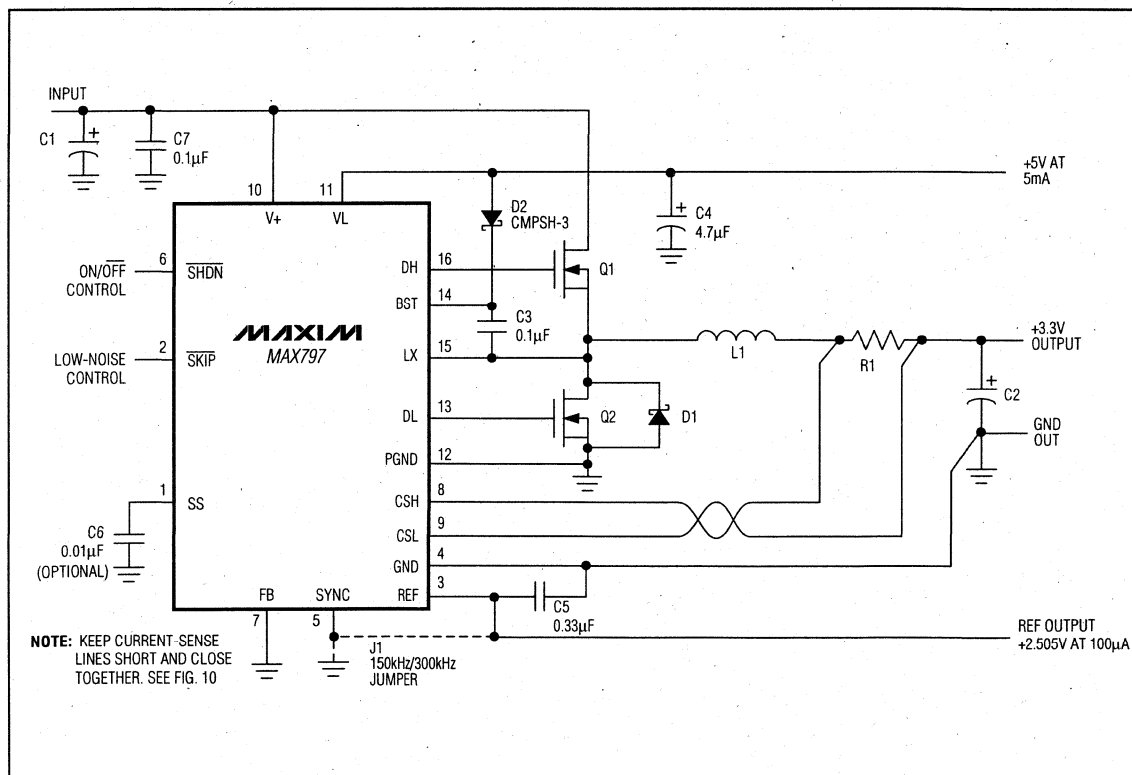


Figure 1. Standard 3.3V Application Circuit

Step-Down Controllers with Synchronous Rectifier for CPU Power

Table 1. Component Selection for Standard 3.3V Applications

COMPONENT	LOAD CURRENT				
	1A	2A	3A	4A	10A
Input Range	4.75V to 18V	4.75V to 18V	4.75V to 28V	4.75V to 24V	4.5V to 6V
Application	PDA	Sub-Notebook	Notebook	High-End Notebook	Desktop 5V-to-3V
Frequency	150kHz	300kHz	300kHz	300kHz	300kHz
Q1 High-Side MOSFET	International Rectifier 1/2 IRF7101	Motorola 1/2 MMDF3N03HD or 1/2 Si9936	Motorola MMSF5N03HD or Si9410	Motorola MTD20N03HDL DPAK	Motorola MTD75N03HDL D ² PAK
Q2 Low-Side MOSFET	International Rectifier 1/2 IRF7101	Motorola 1/2 MMDF3N03HD or 1/2 Si9936	Motorola MMSF5N03HD or Si9410	Motorola MTD20N03HDL DPAK	Motorola MTD75N03HDL D ² PAK
C1 Input Capacitor	22μF, 35V AVX TPS or Sprague 595D	2 x 22μF, 35V AVX TPS or Sprague 595D	2 x 22μF, 35V AVX TPS or Sprague 595D	4 x 22μF, 35V AVX TPS or Sprague 595D	2 x 220μF, 10V Sanyo OS-CON 10SA220M
C2 Output Capacitor	150μF, 10V AVX TPS or Sprague 595D	150μF, 10V AVX TPS or Sprague 595D	220μF, 10V AVX TPS or Sprague 595D	3 x 220μF, 10V AVX TPS or Sprague 595D	4 x 220μF, 10V Sanyo OS-CON 10SA220M
D1 Rectifier	1N5817 Motorola MBR0502L SOD-89	1N5817 NIEC EC10QS02L or Motorola MBRS130T3	1N5819 NIEC EC10QS03 or Motorola MBRS130T3	1N5821 NIEC NSQ03A04 or Motorola MBRS340T3	1N5820 NIEC NSQ03A02, or Motorola MBRS340T3
R1 Resistor	0.062Ω IRC LR2010-01-R062	0.039Ω IRC LR2010-01-R039	0.025Ω IRC LR2010-01-R025	0.015Ω IRC LR2010-01-015	3 x 0.02Ω IRC LR2010-01-R020 (3 in parallel)
L1 Inductor	47μH, 1.2A Ferrite or Kool-Mu Sumida CD75-470	33μH, 2.2A Ferrite Dale LPE6562-330MB	10μH, 3A Ferrite Sumida CDRH125	4.7μH, 5.5A Ferrite Coilcraft DO3316-472	1.5μH, 11A, 3.5mΩ Coiltronics CTX03-12357-1

Table 2. Component Suppliers

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
AVX	(803) 946-0238	[1] 803-626-3123
Central Semiconductor	(516) 435-1110	[1] 516-435-1824
Coilcraft	(708) 639-2361	[1] 708-639-1469
Coiltronics	(407) 241-7876	[1] 407-241-9339
Dale	(605) 665-9301	[1] 605-665-1627
International Rectifier	(310) 241-7876	[1] 310-640-6515
IRC	(213) 772-2000	[1] 213-772-9028
Matsuo	(714) 969-2491	[81] 6-331-1386
Motorola	(602) 244-3576	[1] 602-244-4015
Murata-Erie	(404) 736-1300	[1] 404-736-3030
NIEC	(805) 867-2555*	[81] 3-3494-7414
Sanyo	(619) 661-6835	[1] 0952-82-3074
Siliconix	(408) 988-8000	[1] 408-970-3950
Sprague	(508) 339-8900	[1] 508-339-5063
Sumida	(708) 956-0666	[81] 3-3607-5428
TDK	(708) 803-6100	[81] 3-3278-5358
Transpower Technologies	(702) 831-0140	[1] 702-831-3521

* Distributor

Detailed Description

The MAX796 is a BiCMOS, switch-mode power-supply controller designed primarily for buck-topology regulators in battery-powered applications where high efficiency and low quiescent supply current are critical. The MAX796 also works well in other topologies such as boost, inverting, and Cuk due to the flexibility of its floating high-speed gate driver. Light-load efficiency is enhanced by automatic idle-mode operation—a variable-frequency pulse-skipping mode that reduces losses due to MOSFET gate charge. The step-down power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average of the AC voltage at the switching node, which is adjusted and regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET must exceed the battery voltage and is provided by a flying capacitor boost circuit that uses a 100nF capacitor connected to BST.

The MAX796 contains nine major circuit blocks, which are shown in Figure 2.

Step-Down Controllers with Synchronous Rectifier for CPU Power

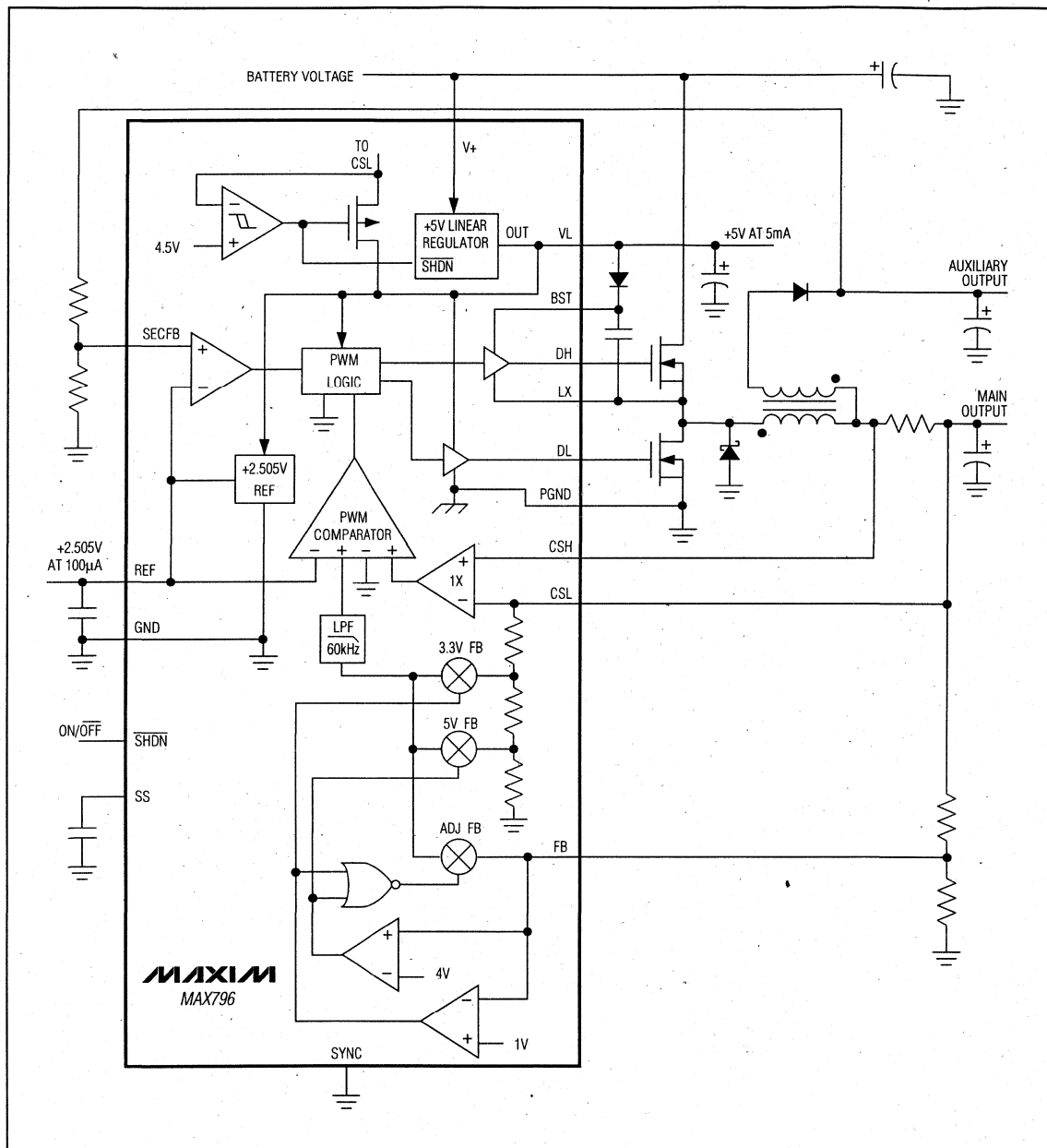


Figure 2. MAX796 Block Diagram

Step-Down Controllers with Synchronous Rectifier for CPU Power

PWM Controller Blocks:

- Multi-Input PWM Comparator
- Current-Sense Circuit
- PWM Logic Block
- Dual-Mode Internal Feedback Mux
- Gate-Driver Outputs
- Secondary Feedback Comparator

Bias Generator Blocks:

- +5V Linear Regulator
- Automatic Bootstrap Switchover Circuit
- +2.505V Reference

These internal IC blocks aren't powered directly from the battery. Instead, a +5V linear regulator steps down the battery voltage to supply both the IC internal rail (VL pin) as well as the gate drivers. The synchronous-switch gate driver is directly powered from +5V VL, while the high-side-switch gate driver is indirectly powered from VL via an external diode-capacitor boost circuit. An automatic bootstrap circuit turns off the +5V linear regulator and powers the IC from its output voltage if the output is above 4.5V.

PWM Controller Block

The heart of the current-mode PWM controller is a multi-input open-loop comparator that sums three signals: output voltage error signal with respect to the reference voltage, current-sense signal, and slope compensation ramp (Figure 3). The PWM controller is a direct summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches the ideal of cycle-by-cycle control over the output voltage.

Under heavy loads, the controller operates in full PWM mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT}/V_{IN}). As the high-switch turns off, the synchronous rectifier latch is set. 60ns later the low-side switch turns on, and stays on until the beginning of the next clock cycle (in continuous mode) or until the inductor current crosses zero (in discontinuous mode). Under fault conditions where the inductor current exceeds the 100mV current-limit threshold, the high-side latch resets and the high-side switch turns off.

At light loads ($SKIP = low$), the inductor current fails to exceed the 30mV threshold set by the minimum-current comparator. When this occurs, the controller goes into idle mode, skipping most of the oscillator pulses in order to reduce the switching frequency and cut back gate-charge losses. The oscillator is effectively gated off at light loads because the minimum-current comparator immediately resets the high-side latch at the

Table 3. Operating-Mode Truth Table

SHDN	SKIP	LOAD CURRENT	MODE NAME	DESCRIPTION
Low	X	X	Shutdown	All circuit blocks turned off; supply current = 1 μ A typ
High	Low	Low, <10%	Idle	Pulse-skipping; supply current = 700 μ A typ at $V_{IN} = 10V$; discontinuous inductor current
High	Low	Medium, <30%	Idle	Pulse-skipping; continuous inductor current
High	Low	High, >30%	PWM	Constant-frequency PWM; continuous inductor current
High	High	X	Low Noise* (PWM)	Constant-frequency PWM regardless of load; continuous inductor current even at no load

* MAX796/MAX799 have no $SKIP$ pin and therefore can't go into low-noise mode.

X = Don't Care

beginning of each cycle, unless the feedback signal falls below the reference voltage level.

When in PWM mode, the controller operates as a fixed-frequency current-mode controller where the duty ratio is set by the input/output voltage ratio. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak current, the circuit acts as a switch-mode transconductance amplifier and pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current "staircasing," a slope-compensation ramp is summed into the main PWM comparator to reduce the apparent duty factor to less than 50%.

The relative gains of the voltage- and current-sense inputs are weighted by the values of current sources that bias three differential input stages in the main PWM comparator (Figure 4). The relative gain of the voltage comparator to the current comparator is internally fixed at $K = 2:1$. The resulting loop gain (which is relatively low) determines the 2.5% typical load regulation error. The low loop-gain value helps reduce output filter capacitor size and cost by shifting the unity-gain crossover to a lower frequency.

Step-Down Controllers with Synchronous Rectifier for CPU Power

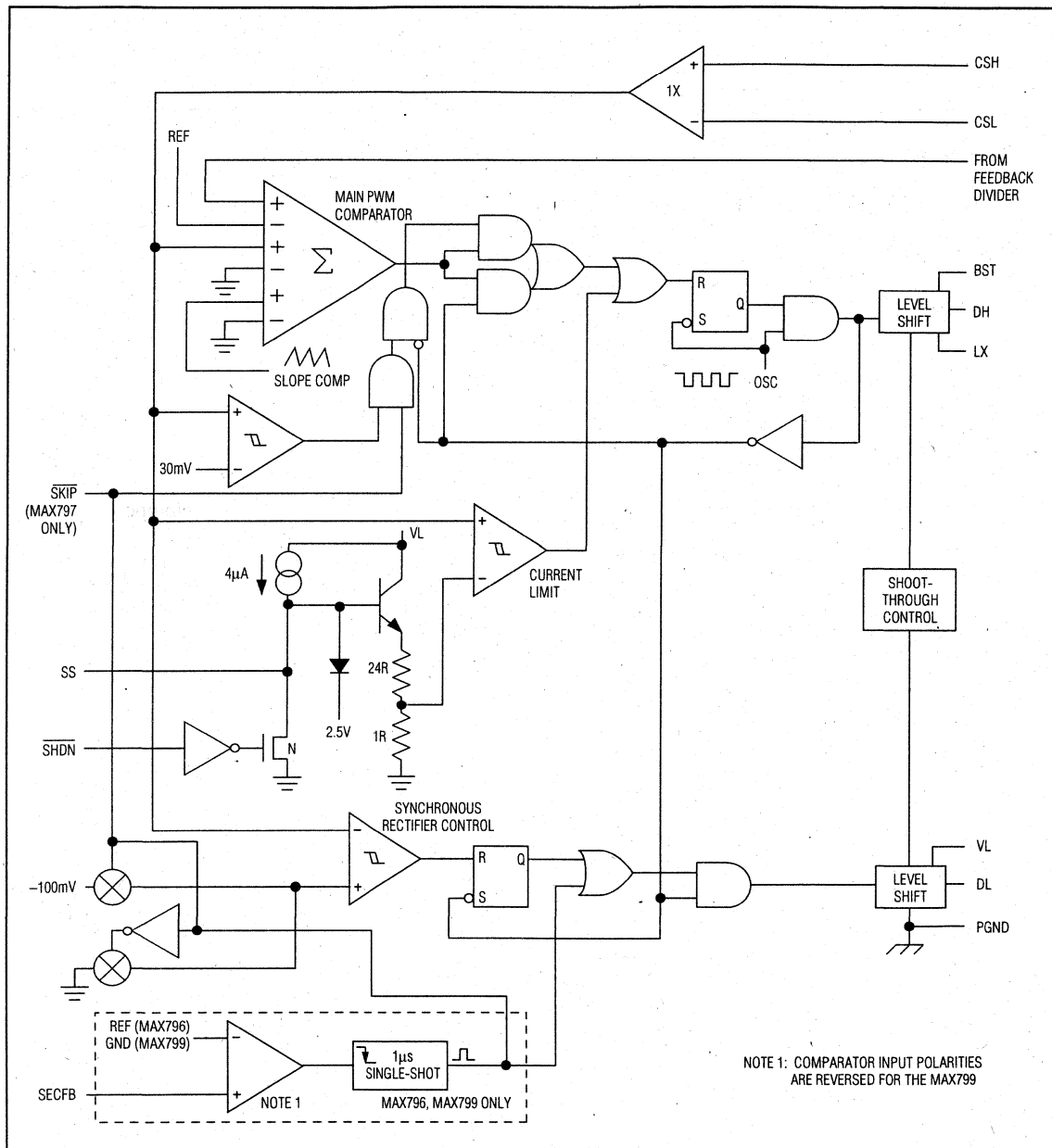


Figure 3. PWM Controller Detailed Block Diagram

Step-Down Controllers with Synchronous Rectifier for CPU Power

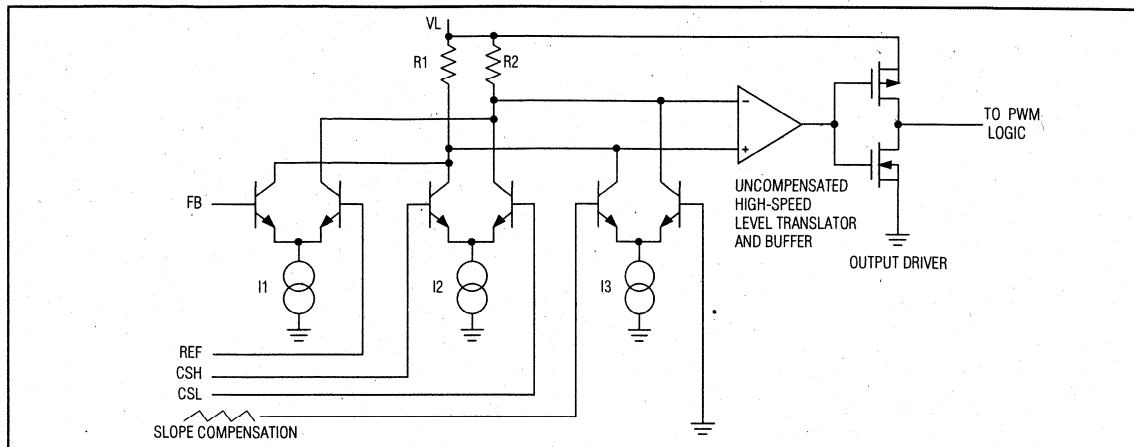


Figure 4. Main PWM Comparator Block Diagram

The output filter capacitor C2 sets a dominant pole in the feedback loop. This pole must roll off the loop gain to unity before the zero introduced by the output capacitor's parasitic resistance (ESR) is encountered (see *Design Procedure* section). A 60kHz pole-zero cancellation filter provides additional rolloff above the unity-gain crossover. This internal 60kHz lowpass compensation filter cancels the zero due to the filter capacitor's ESR. The 60kHz filter is included in the loop in both fixed- and adjustable-output modes.

Synchronous-Rectifier Driver (DL Pin)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode with a low-resistance MOSFET switch. The synchronous rectifier also ensures proper start-up of the boost-gate driver circuit. If you must omit the synchronous power MOSFET for cost or other reasons, replace it with a small-signal MOSFET such as a 2N7002.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through"). In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero. The synchronous rectifier works under all operating conditions, including idle mode. The synchronous-switch timing is further controlled by the secondary feedback (SECFB) signal in order to improve multiple-output cross-regulation (see *Secondary Feedback-Regulation Loop* section).

Internal VL and REF Supplies

An internal regulator produces the 5V supply (VL) that powers the PWM controller, logic, reference, and other blocks within the MAX796. This +5V low-dropout linear regulator can supply up to 5mA for external loads, with a reserve of 20mA for gate-drive power. Bypass VL to GND with 4.7μF. **Important:** VL must not be allowed to exceed 6V. Measure VL with the main output fully loaded. If VL is being pumped up above 5.5V, the probable cause is either excessive boost-diode capacitance or excessive ripple at V+. Use only small-signal diodes for D2 (1N4148 preferred) and bypass V+ to PGND with 0.1μF directly at the package pins.

The 2.505V reference (REF) is accurate to ±1.6% over temperature, making REF useful as a precision system reference. Bypass REF to GND with 0.33μF minimum. REF can supply up to 1mA for external loads. However, if tight-accuracy specs for either VOUT or REF are essential, avoid loading REF with more than 100μA. Loading REF reduces the main output voltage slightly, according to the reference-voltage load regulation error. In MAX799 applications, ensure that the SECFB divider doesn't load REF heavily.

When the main output voltage is above 4.5V, an internal P-channel MOSFET switch connects CSL to VL while simultaneously shutting down the VL linear regulator. This action bootstraps the IC, powering the internal circuitry from the output voltage, rather than through a linear regulator from the battery. Bootstrapping reduces power dissipation caused by gate-charge and quiescent losses by providing that power from a 90%-efficient switch-mode source, rather than from a 50%-efficient linear regulator.

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It's often possible to achieve a bootstrap-like effect, even for circuits that are set to $V_{OUT} < 4.5V$, by powering VL from an external-system +5V supply. To achieve this pseudo-bootstrap, add a Schottky diode between the external +5V source and VL, with the cathode to the VL side. This circuit provides a 1% to 2% efficiency boost and also extends the minimum battery input to less than 4V. The external source must be in the range of 4.8V to 6V. Another way to achieve a pseudo-bootstrap is to add an extra flyback winding to the main inductor to generate the +5V bootstrap source, as shown in the +3.3V/+5V Dual-Output Application (Figure 12).

Boost High-Side Gate-Driver Supply (BST Pin)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit as shown in Figure 5. The capacitor is alternately charged from the VL supply and placed in parallel with the high-side MOSFET's gate-source terminals.

On start-up, the synchronous rectifier (low-side MOSFET) forces LX to 0V and charges the BST capacitor to 5V. On the second half-cycle, the PWM turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary enhancement voltage to turn on the high-side switch, an action that "boosts" the 5V gate-drive signal above the battery voltage.

Ringing seen at the high-side MOSFET gate (DH) in discontinuous-conduction mode (light loads) is a natural operating condition, and is caused by the residual energy in the tank circuit formed by the inductor and stray capacitance at the switching node LX. The gate-driver negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at $\pm 100mV$. The tolerance on the positive current limit is $\pm 20\%$, so the external low-value sense resistor must be sized for $80mV/R1$ to guarantee enough load capability, while components must be designed to withstand continuous current stresses of $120mV/R1$.

For breadboarding purposes or very high-current applications, it may be useful to wire the current-sense inputs with a twisted pair rather than PC traces. This twisted pair needn't be anything special, perhaps two pieces of wire-wrap wire twisted together.

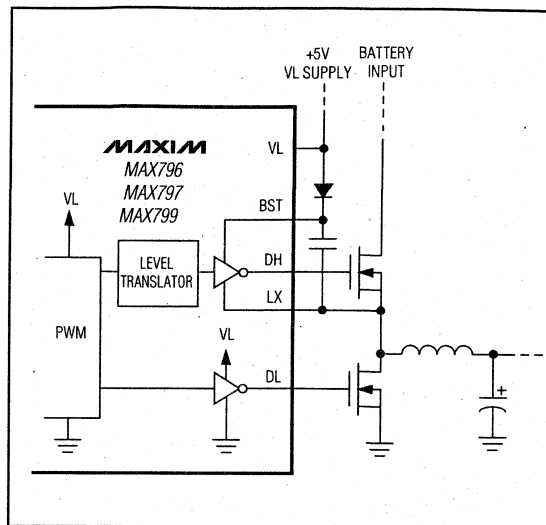


Figure 5. Boost Supply for Gate Drivers

Oscillator Frequency and Synchronization (SYNC Pin)

The SYNC input controls the oscillator frequency. Connecting SYNC to GND or to VL selects 150kHz operation; connecting SYNC to REF selects 300kHz. SYNC can also be used to synchronize with an external 5V CMOS or TTL clock generator. SYNC has a guaranteed 190kHz to 340kHz capture range.

300kHz operation optimizes the application circuit for component size and cost. 150kHz operation provides increased efficiency and improved load-transient response at low input-output voltage differences (see Low-Voltage Operation section).

Low-Noise Mode (SKIP Pin)

The low-noise mode (SKIP = high) is useful for minimizing RF and audio interference in noise-sensitive applications such as Soundblaster™ hi-fi audio-equipped systems, cellular phones, RF communicating computers, and electromagnetic pen-entry systems. See the summary of operating modes in Table 3. SKIP can be driven from an external logic signal.

The MAX797 can reduce interference due to switching noise by ensuring a constant switching frequency regardless of load and line conditions, thus concentrating the emissions at a known frequency outside the system audio or IF bands. Choose an oscillator fre-

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quency where harmonics of the switching frequency don't overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator.

The low-noise mode ($\overline{\text{SKIP}} = \text{high}$) forces two changes upon the PWM controller. First, it ensures fixed-frequency operation by disabling the minimum-current comparator and ensuring that the PWM latch is set at the beginning of each cycle, even if the output is in regulation. Second, it ensures continuous inductor current flow, and thereby suppresses discontinuous-mode inductor ringing by changing the reverse current-limit detection threshold from zero to -100mV, allowing the inductor current to reverse at very light loads.

In most applications, $\overline{\text{SKIP}}$ should be tied to GND in order to minimize quiescent supply current. Supply current with $\overline{\text{SKIP}}$ high is typically 10mA to 20mA, depending on external MOSFET gate capacitance and switching losses.

Forced continuous conduction via $\overline{\text{SKIP}}$ can improve cross regulation of transformer-coupled multiple-output supplies. This second function of the $\overline{\text{SKIP}}$ pin produces a result that is similar to the method of adding secondary regulation via the SECFB feedback pin, but with much higher quiescent supply current. Still, improving cross regulation by enabling $\overline{\text{SKIP}}$ instead of building in SECFB feedback can be useful in noise-sensitive applications, since SECFB and $\overline{\text{SKIP}}$ are mutually exclusive pins/functions in the MAX796 family.

Adjustable-Output Feedback (Dual-Mode FB Pin)

Adjusting the main output voltage with external resistors is easy for any of the devices in the MAX796 family, via the circuit of Figure 6. The nominal output voltage (given by the formula in Figure 6) should be set approximately 2% high in order to make up for the MAX796's -2.5% typical load-regulation error. For example, if designing for a 3.0V output, use a resistor ratio that results in a nominal output voltage of 3.06V. This slight offsetting gives the best possible accuracy. Recommended normal values for R_5 range from 5k Ω to 100k Ω . To achieve a 2.505V nominal output, simply connect FB to CSL directly. To achieve output voltages lower than 2.5V, use an external reference-voltage source higher than V_{REF} , as shown in Figure 7. For best accuracy, this second reference voltage should be much higher than V_{REF} . Alternatively, an external op amp could be used to gain-up REF in order to create the second reference source. This scheme requires a minimum load on the output in order to sink the R_3/R_4 divider current.

Remote sensing of the output voltage, while not possible in fixed-output mode due to the combined nature of the voltage- and current-sense input (CSL), is easy to achieve in adjustable mode by using the top of the external resistor divider as the remote sense point. Fixed-output accuracy is guaranteed to be $\pm 4\%$ over all conditions. In special circumstances, it may be necessary to improve upon this output accuracy. The High-Accuracy Adjustable-Output Application (Figure 18) provides $\pm 2.5\%$ accuracy by adding an integrator-type error amplifier.

The breakdown voltage rating of the current-sense inputs (7V absolute maximum) determines the 6V maximum output adjustment range. To extend this output range, add two matched resistor dividers and speed-up capacitors to form a level translator, as shown in Figure 8. Be sure to set these resistor ratios accurately (using 0.1% resistors), to avoid adding excessive error to the 100mV current-limit threshold.

Secondary Feedback-Regulation Loop (SECFB Pin)

A flyback winding control loop regulates a secondary winding output (MAX796/MAX799 only), improving cross-regulation when the primary is lightly loaded or when there is a low input-output differential voltage. If SECFB crosses its regulation threshold (V_{REF} for the

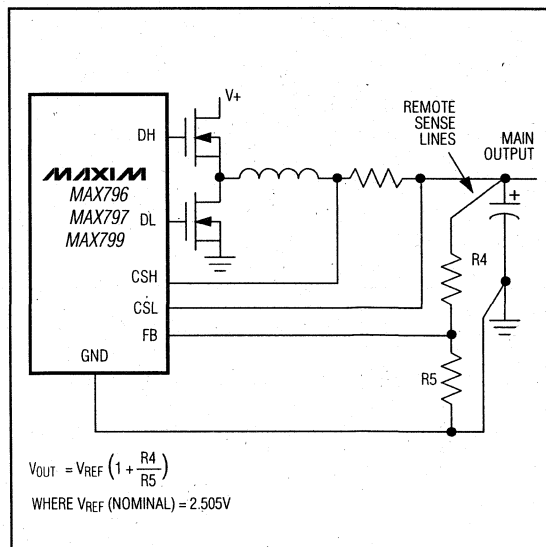


Figure 6. Adjusting the Main Output Voltage

Step-Down Controllers with Synchronous Rectifier for CPU Power

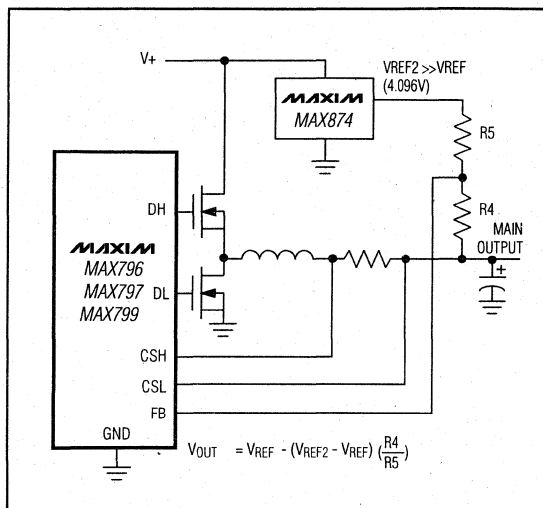


Figure 7. Output Voltage Less than 2.5V

MAX796), a 1 μ s one-shot is triggered that extends the low-side switch's on-time beyond the point where the inductor current crosses zero (in discontinuous mode). This causes the inductor (primary) current to reverse, which in turn pulls current out of the output filter capacitor and causes the flyback transformer to operate in the forward mode. The low impedance presented by the transformer secondary in the forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing SECFB back into regulation. The SECFB feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this mode, secondary output accuracy is determined, as usual, by the secondary rectifier drop, turns ratio, and accuracy of the main output voltage. So, a linear post-regulator may still be needed in order to meet tight output accuracy specifications.

The secondary output voltage-regulation point is determined by an external resistor divider at SECFB. For negative output voltages, the SECFB comparator is referenced to GND (MAX799); for positive output voltages, SECFB regulates at the 2.505V reference (MAX796). As a result, output resistor divider connections and design equations for the two device types differ slightly (Figure 9). Ordinarily, the secondary regulation point is set 5% to 10% below the voltage normally produced by the flyback effect. For example, if the output voltage as determined by the turns ratio is

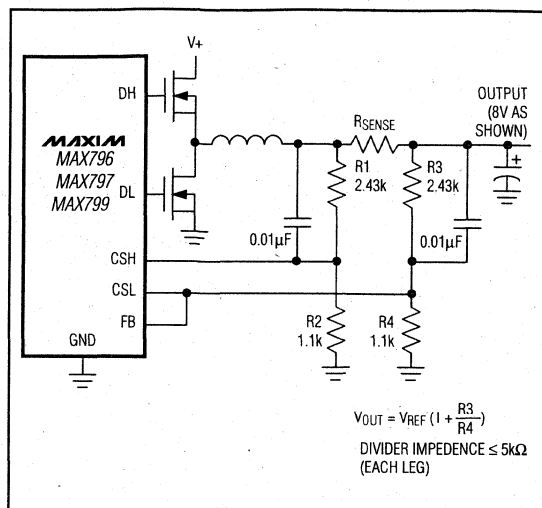


Figure 8. Adjusting the Output Voltage to Greater than 6V

+15V, the feedback resistor ratio should be set to produce about +13.5V; otherwise, the SECFB one-shot might be triggered unintentionally, causing an unnecessary increase in supply current and output noise. In negative-output (MAX799) applications, the resistor divider acts as a load on the internal reference, which in turn can cause errors at the main output. Avoid overloading REF (see the Reference Load-Regulation Error vs. Load Current graph in the *Typical Operating Characteristics*). 100k Ω is a good value for R3 in MAX799 circuits.

Soft-Start Circuit (SS)

Soft-start allows a gradual increase of the internal current-limit level at start-up for the purpose of reducing input surge currents, and perhaps for power-supply sequencing. In shutdown mode, the soft-start circuit holds the SS capacitor discharged to ground. When SHDN goes high, a 4 μ A current source charges the SS capacitor up to 3.2V. The resulting linear ramp waveform causes the internal current-limit level to increase proportionally from 20mV to 100mV. The main output capacitor thus charges up relatively slowly, depending on the SS capacitor value. The exact time of the output rise depends on output capacitance and load current and is typically 1ms per nanofarad of soft-start capacitance. With no SS capacitor connected, maximum current limit is reached within 10 μ s.

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Design Procedure

The five pre-designed standard application circuits (Figure 1 and Table 1) contain ready-to-use solutions for common applications. Use the following design procedure to optimize the basic schematic for different voltage or current requirements. Before beginning a design, firmly establish the following:

VIN(MAX), the maximum input (battery) voltage. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is connected but no battery is installed. VIN(MAX) must not exceed 30V. This 30V upper limit is determined by the breakdown voltage of the BST floating gate driver to GND (36V absolute maximum).

VIN(MIN), the minimum input (battery) voltage. This should be taken at full-load under the lowest battery conditions. If VIN(MIN) is less than 4.5V, a special circuit must be used to externally hold up VL above 4.8V. If the minimum input-output difference is less than 1.5V, the filter capacitance required to maintain good AC load regulation increases.

Inductor Value

The exact inductor value isn't critical and can be adjusted freely in order to make tradeoffs among size, cost, and efficiency. Although lower inductor values will minimize size and cost, they will also reduce efficiency due to higher peak currents. To permit use of the physically smallest inductor, lower the inductance until the circuit is operating at the border between continuous and discontinuous modes. Reducing the inductor value even further, below this crossover point, results in discontinuous-conduction operation even at full load. This helps reduce output filter capacitance requirements but causes the core energy storage requirements to increase again. On the other hand, higher inductor values will increase efficiency, but at some point resistive losses due to extra turns of wire will exceed the benefit gained from lower AC current levels. Also, high inductor values can affect load-transient response; see the VSAG equation in the *Low-Voltage Operation* section.

The following equations are given for continuous-conduction operation since the MAX796 is mainly intended for high-efficiency battery-powered applications. See Appendix A in Maxim's *Battery Management and DC-DC Converter Circuit Collection* for crossover point and discontinuous-mode equations. Discontinuous conduction doesn't affect normal idle-mode operation.

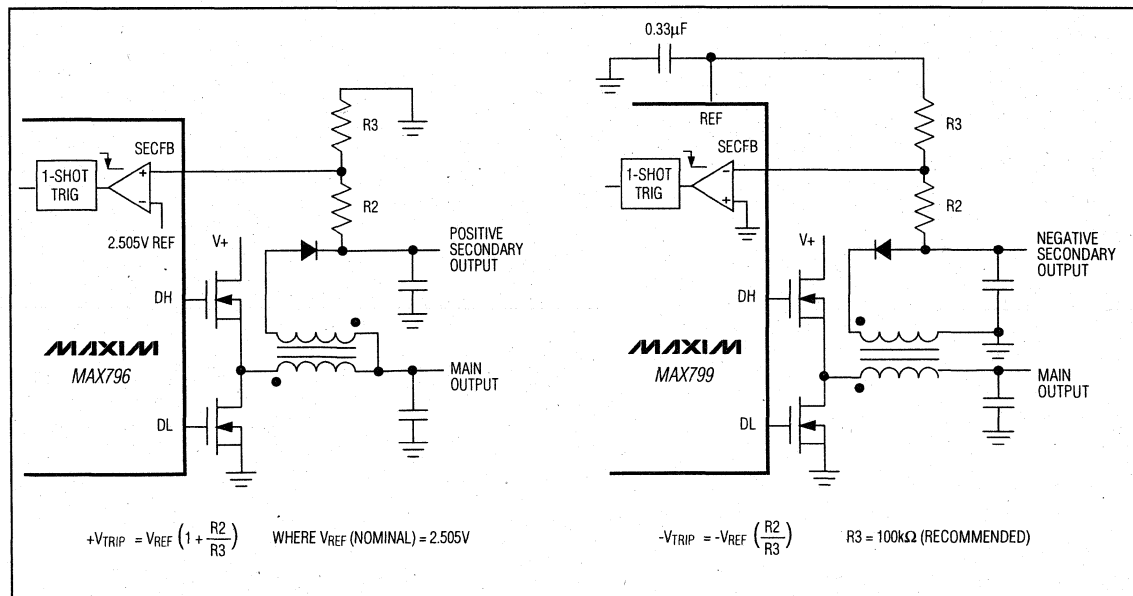


Figure 9. Secondary-Output Feedback Dividers, MAX796 vs. MAX799

Step-Down Controllers with Synchronous Rectifier for CPU Power

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher value of LIR allows smaller inductance, but results in higher losses and ripple. A good compromise between size and losses is found at a 30% ripple current to load current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

$$L = \frac{V_{OUT} (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{OUT} \times LIR}$$

where: f = switching frequency, normally 150kHz or 300kHz

I_{OUT} = maximum DC load current

LIR = ratio of AC to DC inductor current, typically 0.3

The peak inductor current at full load is 1.15 x I_{OUT} if the above equation is used; otherwise, the peak current can be calculated by:

$$I_{PEAK} = I_{LOAD} + \frac{V_{OUT} (V_{IN(MAX)} - V_{OUT})}{2 \times f \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance is a key parameter for efficiency performance and must be ruthlessly minimized, preferably to less than 25mΩ at I_{OUT} = 3A. If a standard off-the-shelf inductor is not available, choose a core with an LI² rating greater than L x I_{PEAK}² and wind it with the largest diameter wire that fits the winding area. For 300kHz applications, ferrite core material is strongly preferred; for 150kHz applications, Kool-mu (aluminum alloy) and even powdered iron can be acceptable. If light-load efficiency is unimportant (in desktop 5V-to-3V applications, for example) then low-permeability iron-powder cores, such as the Micrometals type found in Pulse Engineering's 2.1μH PE-53680, may be acceptable even at 300kHz. For high-current applications, shielded core geometries (such as toroidal or pot core) help keep noise, EMI, and switching-waveform jitter low.

Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case-low current-limit threshold voltage (from the *Electrical Characteristics* table) and the peak inductor current. The continuous-mode peak inductor-current calculations that follow are also useful for sizing the switches and specifying the inductor-current saturation ratings. In order to simplify the calculation, I_{LOAD}

may be used in place of I_{PEAK} if the inductor value has been set for LIR = 0.3 or less (high inductor values) and 300kHz operation is selected. Low-inductance resistors, such as surface-mount metal-film resistors, are preferred.

$$R_{SENSE} = \frac{80mV}{I_{PEAK}}$$

Input Capacitor Value

Place a small ceramic capacitor (0.1μF) between V+ and GND, close to the device. Also, connect a low-ESR bulk capacitor directly to the drain of the high-side MOSFET. Select the bulk input filter capacitor according to input ripple-current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors that have low enough ESR to meet the ripple-current requirement invariably have more than adequate capacitance values. Aluminum-electrolytic capacitors such as Sanyo OS-CON or Nichicon PL are preferred over tantalum types, which could cause power-up surge-current failure, especially when connecting to robust AC adaptors or low-impedance batteries. RMS input ripple current is determined by the input voltage and load current, with the worst possible case occurring at V_{IN} = 2 x V_{OUT}:

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT} (V_{IN} - V_{OUT})}}{V_{IN}}$$

$$I_{RMS} = I_{LOAD} / 2 \text{ when } V_{IN} \text{ is } 2 \times V_{OUT}$$

Output Filter Capacitor Value

The output filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements for loop stability. In other words, the low-ESR electrolytic capacitor that meets the ESR requirement usually has more output capacitance than is required for AC stability. Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the capacitor must meet *both* minimum capacitance and maximum ESR values as given in the following equations:

$$C_F > \frac{V_{REF} (1 + V_{OUT} / V_{IN(MIN)})}{V_{OUT} \times R_{SENSE} \times f}$$

$$RESR < \frac{R_{SENSE} \times V_{OUT}}{V_{REF}}$$

(can be multiplied by 1.5, see note below)

Step-Down Controllers with Synchronous Rectifier for CPU Power

These equations are "worst-case" with 45 degrees of phase margin to ensure jitter-free fixed-frequency operation and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules by using less expensive (lower quality) capacitors, particularly if the load lacks large step changes. This practice is tolerable, provided that some bench testing over temperature is done to verify acceptable noise and transient response.

There is no well-defined boundary between stable and unstable operation. As phase margin is reduced, the first symptom is a bit of timing jitter, which shows up as blurred edges in the switching waveforms where the scope won't quite sync up. Technically speaking, this (usually) harmless jitter is unstable operation, since the switching frequency is now non-constant. As the capacitor quality is reduced, the jitter becomes more pronounced and the load-transient output voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output voltage tolerance. Note that even with zero phase margin and gross instability present, the output voltage noise never gets much worse than $I_{PEAK} \times R_{ESR}$ (under constant loads, at least).

Designers of RF communicators or other noise-sensitive analog equipment should be conservative and stick to the guidelines. Designers of notebook computers and similar commercial-temperature-range digital systems can multiply the R_{ESR} value by a factor of 1.5 without hurting stability or transient response.

The output voltage ripple is usually dominated by the ESR of the filter capacitor and can be approximated as $I_{RIPPLE} \times R_{ESR}$. There is also a capacitive term, so the full equation for ripple in the continuous mode is $V_{NOISE(p-p)} = I_{RIPPLE} \times (R_{ESR} + 1 / (2 \times \pi \times f \times C_f))$. In idle mode, the inductor current becomes discontinuous with high peaks and widely spaced pulses, so the noise can actually be higher at light load compared to full load. In idle mode, the output ripple can be calculated as:

$$V_{NOISE(p-p)} = \frac{0.02 \times R_{ESR}}{R_{SENSE}} + \frac{0.0003 \times L \times [1 / V_{OUT} + 1 / (V_{IN} - V_{OUT})]}{(R_{SENSE})^2 \times C_f}$$

Transformer Design (MAX796/MAX799 Only)

Buck-plus-flyback applications, sometimes called "coupled-inductor" topologies, need a transformer in order to generate multiple output voltages. The basic electrical design is a simple task of calculating turns ratios and adding the power delivered to the secondary in order to calculate the current-sense resistor and primary inductance. However, extremes of low input-output differentials, widely different output loading levels, and high turns ratios can complicate the design due to parasitic transformer parameters such as inter-winding capacitance, secondary resistance, and leakage inductance. For examples of what is possible with real-world transformers, see the graphs of Maximum Secondary Current vs. Input Voltage in the *Typical Operating Characteristics*.

Power from the main and secondary outputs is lumped together to obtain an equivalent current referred to the main output voltage (see Inductor L1 for definitions of parameters). Set the value of the current-sense resistor at $80mV / I_{TOTAL}$.

P_{TOTAL} = the sum of the output power from all outputs

$I_{TOTAL} = P_{TOTAL} / V_{OUT}$ = the equivalent output current referred to V_{OUT}

$$L(\text{primary}) = \frac{V_{OUT} (V_{IN}(\text{MAX}) - V_{OUT})}{V_{IN}(\text{MAX}) \times f \times I_{TOTAL} \times LIR}$$

$$\text{Turns Ratio } N = \frac{V_{SEC} + V_{FWD}}{V_{OUT}(\text{MIN}) + V_{RECT} + V_{SENSE}}$$

where: V_{SEC} is the minimum required rectified secondary-output voltage

V_{FWD} is the forward drop across the secondary rectifier

$V_{OUT}(\text{MIN})$ is the *minimum* value of the main output voltage (from the *Electrical Characteristics*)

V_{RECT} is the on-state voltage drop across the synchronous-rectifier MOSFET

V_{SENSE} is the voltage drop across the sense resistor

In positive-output (MAX796) applications, the transformer secondary return is often referred to the main output voltage rather than to ground in order to reduce the needed turns ratio. In this case, the main output voltage must first be subtracted from the secondary voltage to obtain V_{SEC} .

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Selecting Other Components

MOSFET Switches

The two high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at $V_{GS} = 4.5V$. Lower gate threshold specs are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% derating factor. The best MOSFETs will have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)} \times Q_G$ provides a meaningful figure by which to compare various MOSFETs. Newer MOSFET process technologies with dense cell structures generally give the best performance. The internal gate drivers can tolerate $>100nC$ total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high- and low-side MOSFETs. I^2R losses are distributed between Q1 and Q2 according to duty factor (see the equations below). Switching losses affect the upper MOSFET only, since the Schottky rectifier clamps the switching node before the synchronous rectifier turns on. Gate-charge losses are dissipated by the driver and don't heat the MOSFET. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. The worst-case dissipation for the high-side MOSFET occurs at the minimum battery voltage, and the worst-case for the low-side MOSFET occurs at the maximum battery voltage.

$$PD(\text{upper FET}) = I_{LOAD}^2 \times R_{DS(ON)} \times DUTY$$

$$+ V_{IN} \times I_{LOAD} \times f \times \left(\frac{V_{IN} \times C_{RSS}}{I_{GATE}} + 20ns \right)$$

$$PD(\text{lower FET}) = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - DUTY)$$

$$DUTY = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1})$$

where: On-state voltage drop $V_{Q1} = I_{LOAD} \times R_{DS(ON)}$
 C_{RSS} = MOSFET reverse transfer capacitance
 I_{GATE} = DH driver peak output current capability (1A typically)

$$20ns = \text{DH driver inherent rise/fall time}$$

Under output short circuit, the synchronous-rectifier MOSFET suffers extra stress and may need to be oversized if a continuous DC short circuit must be tolerated.

During short circuit, Q2's duty factor can increase to greater than 0.9 according to:

$$Q2 \text{ DUTY (short circuit)} = 1 - [V_{Q2} / (V_{IN(MAX)} - V_{Q1})]$$

where the on-state voltage drop $V_Q = (I_{200mA} / R_{SENSE}) \times R_{DS(ON)}$.

Rectifier Diode D1

Rectifier D1 is a clamp that catches the negative inductor swing during the 110ns dead time between turning off the high-side MOSFET and turning on the low-side. D1 must be a Schottky type in order to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit D1 and let the body diode clamp the negative inductor swing, but efficiency will drop one or two percent as a result. Use an MBR0530 (500mA rated) type for loads up to 1.5A, a 1N5819 type for loads up to 3A, or a 1N5822 type for loads up to 10A. D1's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

Boost-Supply Diode D2

A signal diode such as a 1N4148 works well for D2 in most applications. If the input voltage can go below 6V, use a small (20mA) Schottky diode for slightly improved efficiency and dropout characteristics. Don't use large power diodes such as 1N5817 or 1N4001, since high junction capacitance can cause V_L to be pumped up to excessive voltages.

Rectifier Diode D3 (Transformer Secondary Diode)

The secondary diode in coupled-inductor applications must withstand high flyback voltages greater than 60V, which usually rules out most Schottky rectifiers. Common silicon rectifiers such as the 1N4001 are also prohibited, as they are far too slow. This often makes fast silicon rectifiers such as the MURS120 the only choice. The flyback voltage across the rectifier is related to the V_{IN} - V_{OUT} difference according to the transformer turns ratio:

$$V_{FLYBACK} = V_{SEC} + (V_{IN} - V_{OUT}) \times N$$

where: N is the transformer turns ratio SEC/PRI
 V_{SEC} is the maximum secondary DC output voltage
 V_{OUT} is the primary (main) output voltage

Subtract the main output voltage (V_{OUT}) from $V_{FLYBACK}$ in this equation if the secondary winding is returned to V_{OUT} and not to ground. The diode reverse breakdown rating must also accommodate any ringing due to leakage inductance. D3's current rating should be at least twice the DC load current on the secondary output.

Step-Down Controllers with Synchronous Rectifier for CPU Power

Low-Voltage Operation

Low input voltages and low input-output differential voltages each require some extra care in the design. Low absolute input voltages can cause the VL linear regulator to enter dropout, and eventually shut itself off. Low input voltages relative to the output (low V_{IN} - V_{OUT} differential) can cause bad load regulation in multi-output flyback applications. See the design equations in the *Transformer Design* section. Finally, low V_{IN} - V_{OUT} differentials can also cause the output voltage to sag when the load current changes abruptly. The amplitude of the sag is a function of inductor value and maximum duty factor (an *Electrical Characteristics* parameter, 93% guaranteed over temperature at $f = 150\text{kHz}$) as follows:

$$V_{SAG} = \frac{(I_{STEP})^2 \times L}{2 \times C_F \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The cure for low-voltage sag is to increase the value of the output capacitor. For example, at $V_{IN} = 5.5\text{V}$, $V_{OUT} = 5\text{V}$, $L = 10\mu\text{H}$, $f = 150\text{kHz}$, a total capacitance of $660\mu\text{F}$ will prevent excessive sag. Note that only the capacitance requirement is increased and the ESR requirements don't change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor.

Applications Information

Heavy-Load Efficiency Considerations

The major efficiency loss mechanisms under loads are, in the usual order of importance:

- $P(I^2R)$, I^2R losses
- $P(\text{gate})$, gate-charge losses
- $P(\text{diode})$, diode-conduction losses
- $P(\text{tran})$, transition losses
- $P(\text{cap})$, capacitor ESR losses
- $P(\text{IC})$, losses due to the operating supply current of the IC

Inductor-core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, they aren't accounted for in this analysis. Ferrite cores are preferred, especially at 300kHz , but powdered cores such as Kool-mu can work well.

$$\begin{aligned} \text{Efficiency} &= P_{OUT} / P_{IN} \times 100\% \\ &= P_{OUT} / (P_{OUT} + P_{TOTAL}) \times 100\% \end{aligned}$$

$$P_{TOTAL} = P(I^2R) + P(\text{gate}) + P(\text{diode}) + P(\text{tran}) + P(\text{cap}) + P(\text{IC})$$

$$P(I^2R) = (I_{LOAD})^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

where R_{DC} is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and R_{SENSE} is the current-

Table 4. Low-Voltage Troubleshooting

SYMPTOM	CONDITION	ROOT CAUSE	SOLUTION
Sag or droop in V_{OUT} under step load change	Low V_{IN} - V_{OUT} differential, $<1.5\text{V}$	Limited inductor-current slew rate per cycle.	Increase bulk output capacitance per formula above. Reduce inductor value.
Dropout voltage is too high (V_{OUT} follows V_{IN} as V_{IN} decreases)	Low V_{IN} - V_{OUT} differential, $<1\text{V}$	Maximum duty-cycle limits exceeded.	Reduce f to 150kHz . Reduce MOSFET on-resistance and coil DCR.
Unstable—jitters between two distinct duty factors	Low V_{IN} - V_{OUT} differential, $<1\text{V}$	Inherent limitation of fixed-frequency current-mode SMPS slope compensation.	Reduce L value. Tolerate the remaining jitter (extra output capacitance helps somewhat).
Secondary output won't support a load	Low V_{IN} - V_{OUT} differential, $V_{IN} < 1.3 \times V_{OUT(\text{main})}$ (MAX796/MAX799 only)	Not enough duty cycle left to initiate forward-mode operation. Small AC current in primary can't store energy for flyback operation.	Reduce f to 150kHz . Reduce secondary impedances—use Schottky if possible. Stack secondary winding on main output.
High supply current, poor efficiency	Low input voltage, $<5\text{V}$	VL linear regulator is going into dropout and isn't providing good gate-drive levels.	Use a small 20mA Schottky diode for boost diode D2. Supply VL from an external source.
Won't start under load or quits before battery is completely dead	Low input voltage, $<4.5\text{V}$	VL output is so low that it hits the VL UVLO threshold at 4.2V max.	Supply VL from an external source other than V_{BATT} , such as the system 5V supply.

Step-Down Controllers with Synchronous Rectifier for CPU Power

sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high- and low-side switches because they time-share the inductor current. If the MOSFETs aren't identical, their losses can be estimated by averaging the losses according to duty factor.

$$P(\text{gate}) = \text{gate-driver loss} = qG \times f \times V_L$$

where V_L is the MAX796 internal logic supply voltage (5V), and qG is the sum of the gate-charge values for low- and high-side switches. For matched MOSFETs, qG is twice the data sheet value of an individual MOSFET. If V_{OUT} is set to less than 4.5V, replace V_L in this equation with V_{BATT} . In this case, efficiency can be improved by connecting V_L to an efficient 5V source, such as the system +5V supply.

$$P(\text{diode}) = \text{diode conduction losses} \\ = I_{LOAD} \times V_{FWD} \times t_D \times f$$

where t_D is the diode conduction time (110ns typ) and V_{FWD} is the forward voltage of the Schottky.

$$P_D(\text{tran}) = \text{transition loss} =$$

$$V_{BATT} \times I_{LOAD} \times f \times \left(\frac{V_{BATT} \times C_{RSS}}{I_{GATE}} + 20\text{ns} \right)$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data sheet parameter), I_{GATE} is the DH gate-driver peak output current (1A typ), and 20ns is the rise/fall time of the DH driver (20ns typ).

$$P(\text{cap}) = \text{input capacitor ESR loss} = (I_{RMS})^2 \times R_{ESR}$$

where I_{RMS} is the input ripple current as calculated in the *Input Capacitor Value* section of the *Design Procedure*.

Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode, where the inductor current discharges to zero at some point during the switching cycle. This causes the AC component of the inductor current to be high compared to the load current, which increases core losses and I^2R losses in the output filter capacitors. Obtain best light-load efficiency by using MOSFETs with moderate gate-charge levels and by using ferrite, MPP, or other low-loss core material. Avoid powdered iron cores; even Kool-mu (aluminum alloy) is not as good as ferrite.

PC Board Layout Considerations

Good PC board layout is *required* to achieve specified noise, efficiency, and stability performance. The PC board layout artist must be provided with explicit instructions, preferably a pencil sketch of the placement of power switching components and high-current routing. See the evaluation kit PC board layouts in the MAX796 and MAX797 EV kit manuals for examples. A

ground plane is essential for optimum performance. In most applications, the circuit will be located on a multi-layer board and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections (REF, SS, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide.

- 1) Place the high-power components (C1, C2, Q1, Q2, D1, L1, and R1) first, with their grounds adjacent.

Priority 1: **Minimize current-sense resistor trace lengths** (see Figure 10).

Priority 2: **Minimize ground trace lengths** in the high-current paths (discussed below).

Priority 3: Minimize other trace lengths in the high-current paths. Use >5mm wide traces. C1 to Q1: 10mm max length. D1 cathode to Q2: 5mm max length. LX node (Q1 source, Q2 drain, D1 cathode, inductor): 15mm max length

Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds (C1-, C2-, source of Q2, anode of D1, and PGND) are then connected to each other with a wide filled zone of top-layer copper, so that they don't go through vias. The resulting top-layer "sub-ground-plane" is connected to the normal inner-layer ground plane at the output ground terminals. This ensures that the analog GND of the IC is sensing at the output terminals of the supply, without interference from IR drops and ground noise. Other high-current paths should also be minimized, **but focusing ruthlessly on short ground and current-sense connections eliminates about 90% of all PC layout headaches.** See the evaluation kit PC board layouts for examples.

- 2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and REF and SS capacitors). Placing the IC and analog components on the opposite side of the board from the power-switching node is desirable. Important: the IC must be no farther than 10mm from the current-sense resistor. Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm and route them away from CSH, CSL, REF, and SS.
- 3) Employ a single-point star ground where the input ground trace, power ground (sub-ground-plane), and normal ground plane all meet at the output ground terminal of the supply.

Step-Down Controllers with Synchronous Rectifier for CPU Power

MAX796/MAX797/MAX799

4

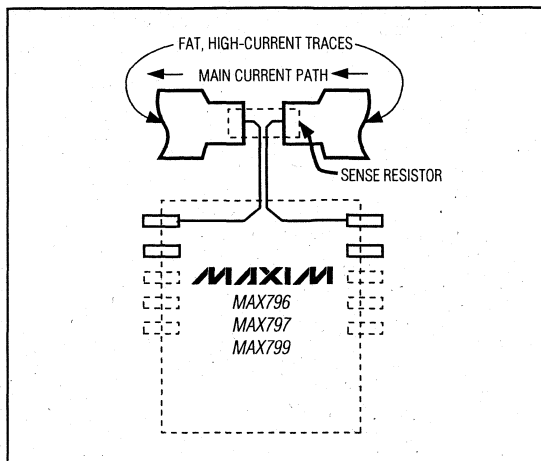


Figure 10. Kelvin Connections for the Current-Sense Resistor

Application Circuits

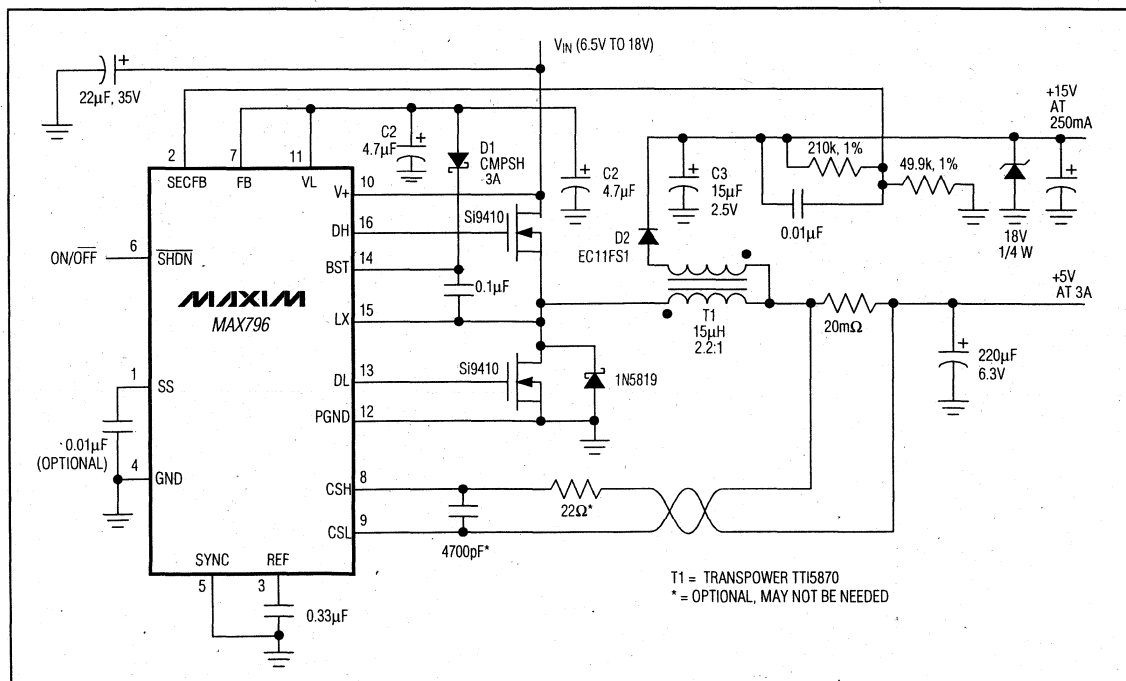


Figure 11. +5V/+15V Dual-Output Application (MAX796)

Step-Down Controllers with Synchronous Rectifier for CPU Power

Application Circuits (continued)

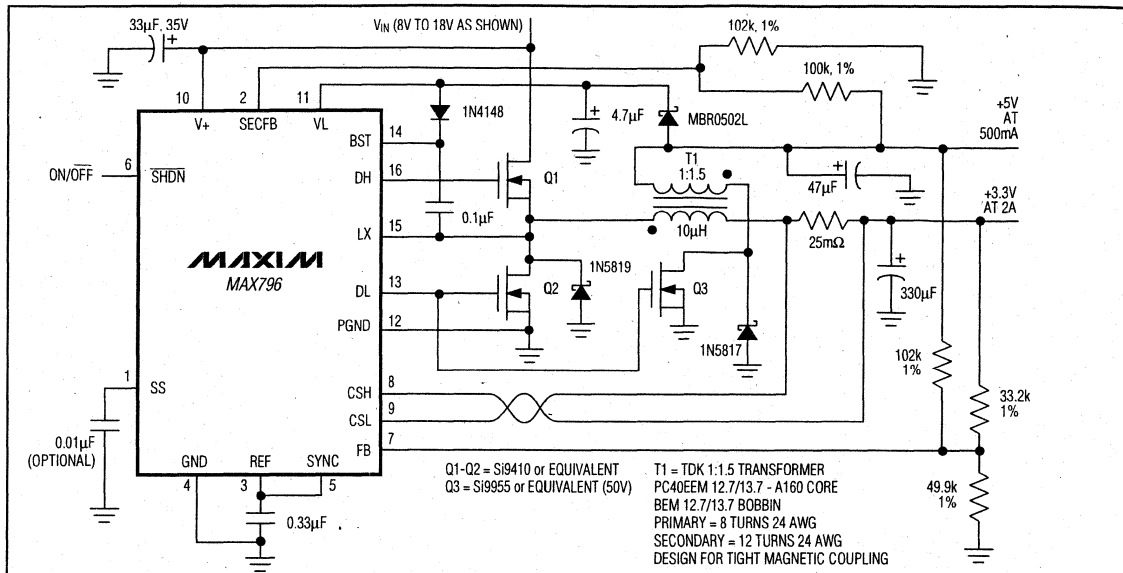


Figure 12. +3.3V/+5V Dual-Output Application (MAX796)

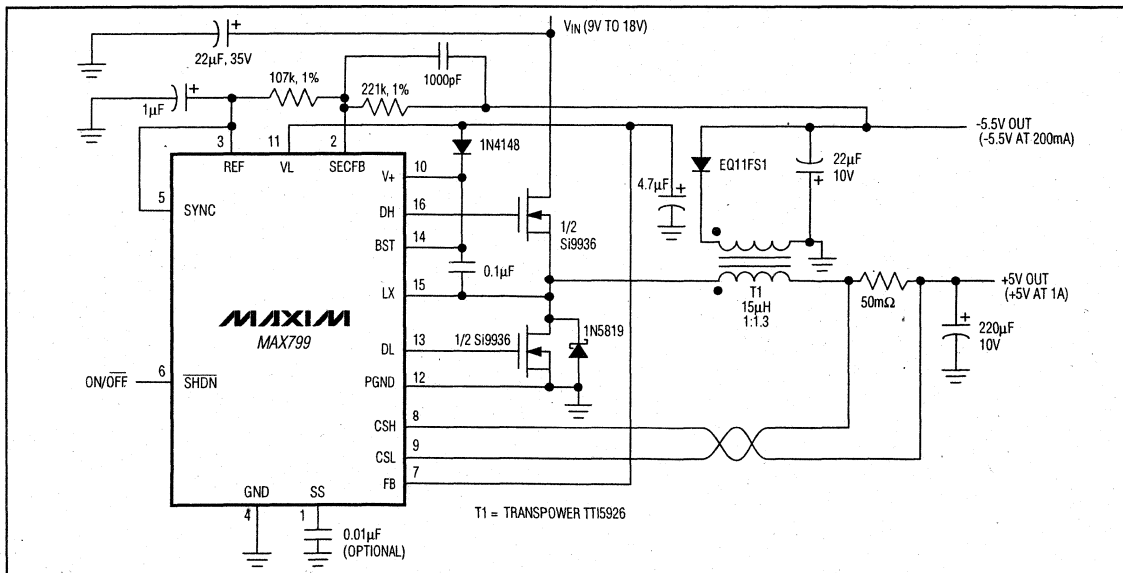


Figure 13. ±5V Dual-Output Application (MAX799)

Step-Down Controllers with Synchronous Rectifier for CPU Power

Application Circuits (continued)

MAX796/MAX797/MAX799

4

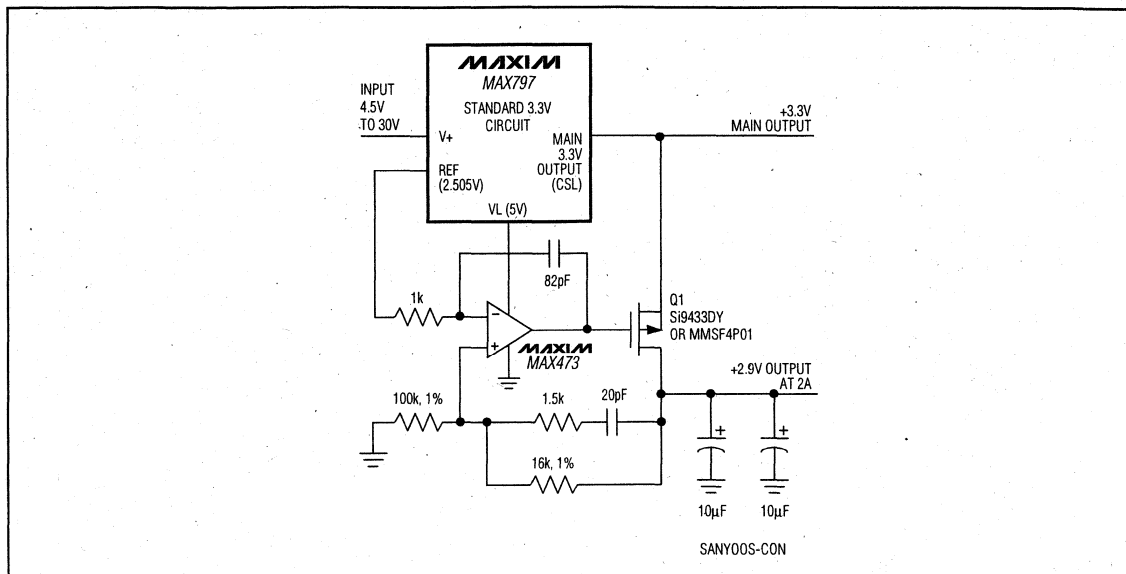


Figure 14. 2.9V Low-Dropout Linear Regulator with Fast Transient Response

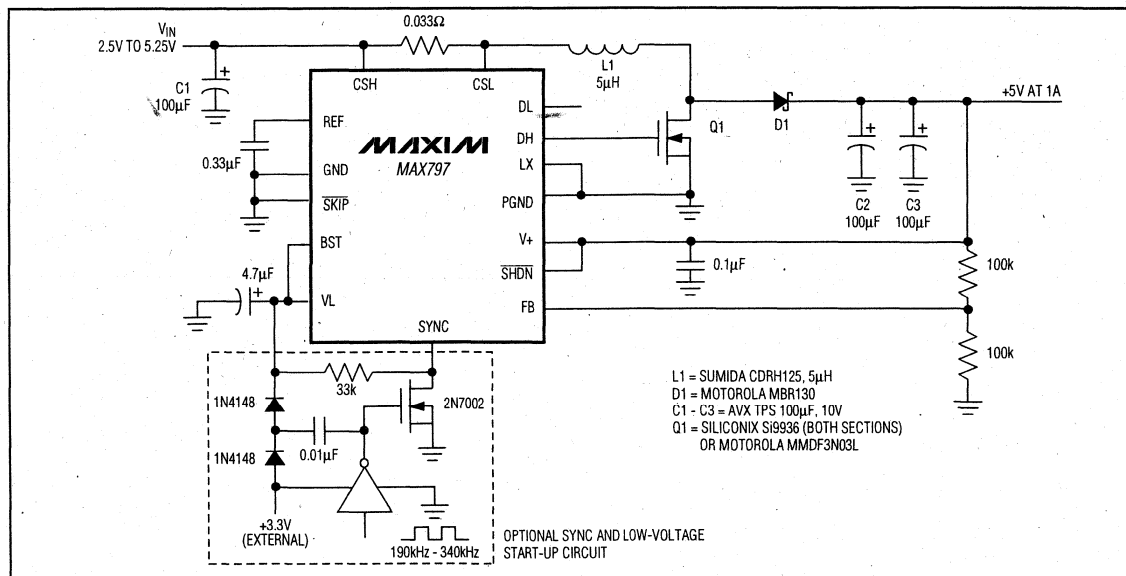


Figure 15. Low-Noise Boost Converter for Cellular Phones

Step-Down Controllers with Synchronous Rectifier for CPU Power

Application Circuits (continued)

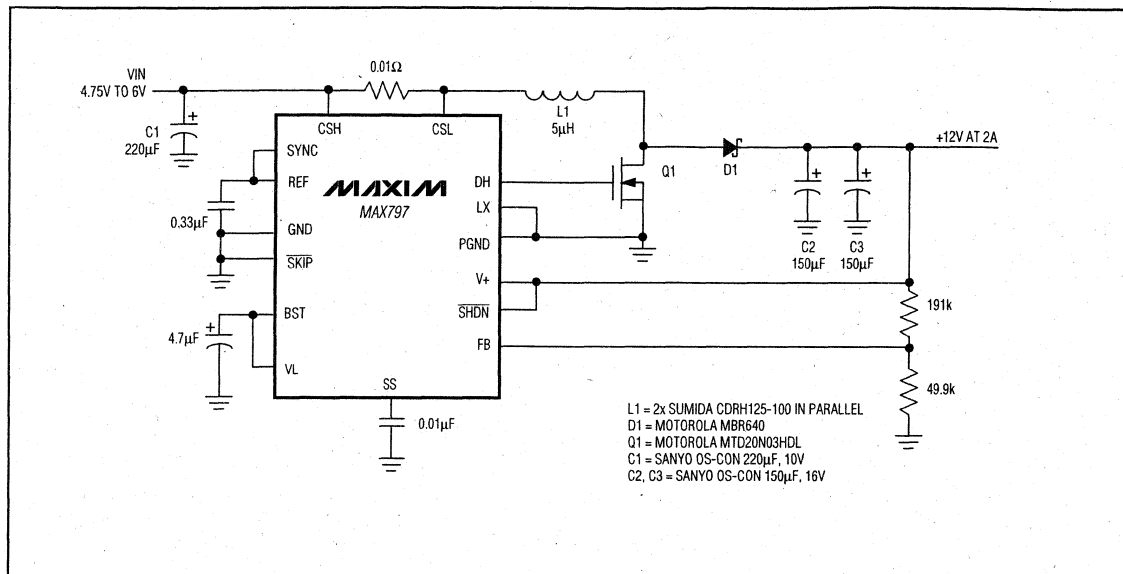


Figure 16. 5V-to-12V PWM Boost Converter

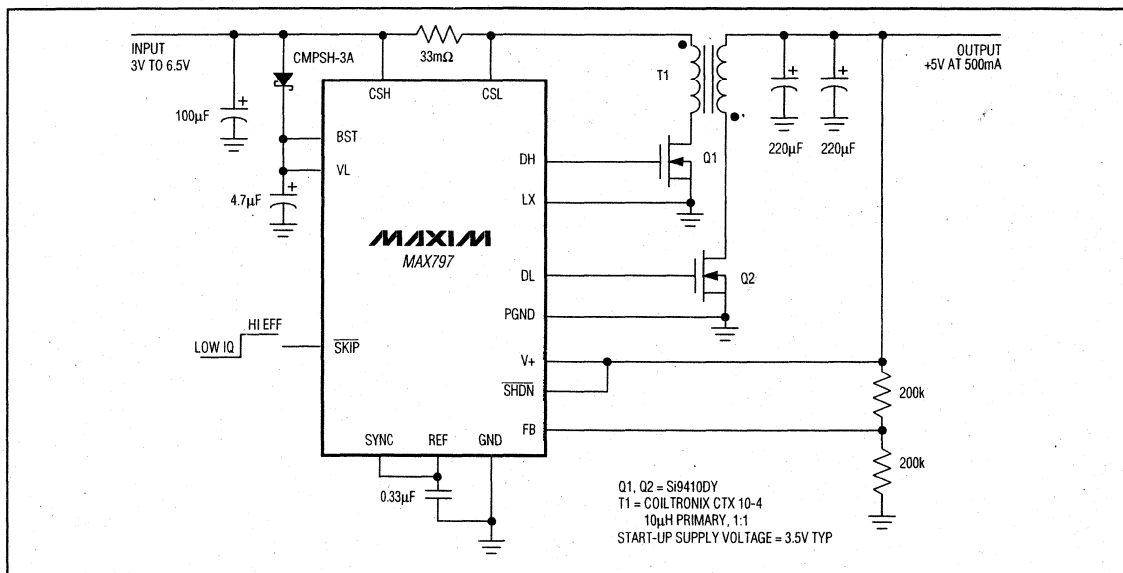
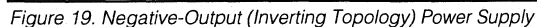
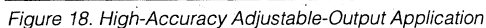


Figure 17. 90% Efficient, Low-Voltage PWM Flyback Converter (4 Cells to 5V)

Application Circuits (continued)

MAX796/MAX797/MAX799

4



Step-Down Controllers with Synchronous Rectifier for CPU Power

Application Circuits (continued)

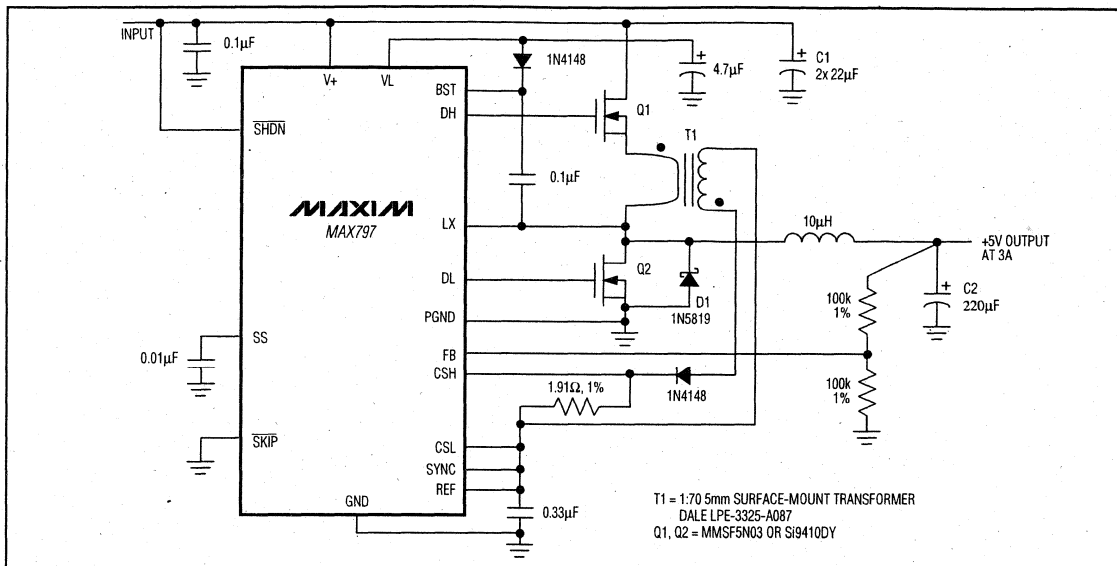


Figure 20. Buck Converter with Low-Loss SMT Current-Sense Transformer

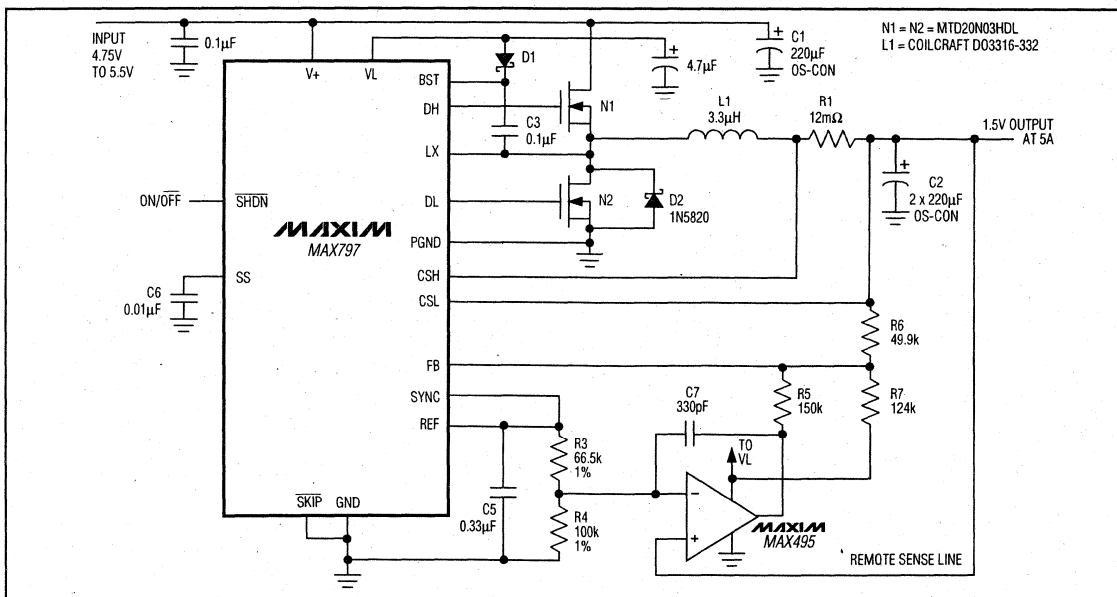


Figure 21. 1.5V GTL Bus Termination Supply

Step-Down Controllers with Synchronous Rectifier for CPU Power

Application Circuits (continued)

MAX796/MAX797/MAX799

4

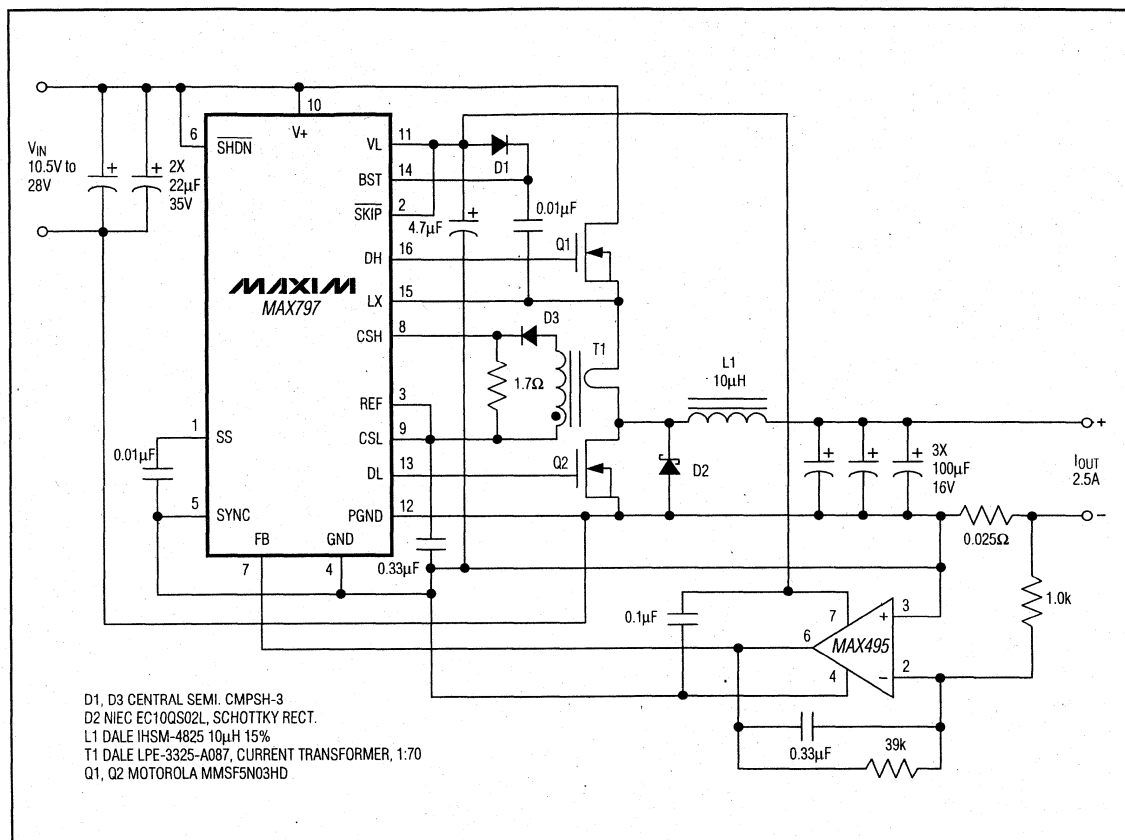


Figure 22. Battery-Charger Current Source

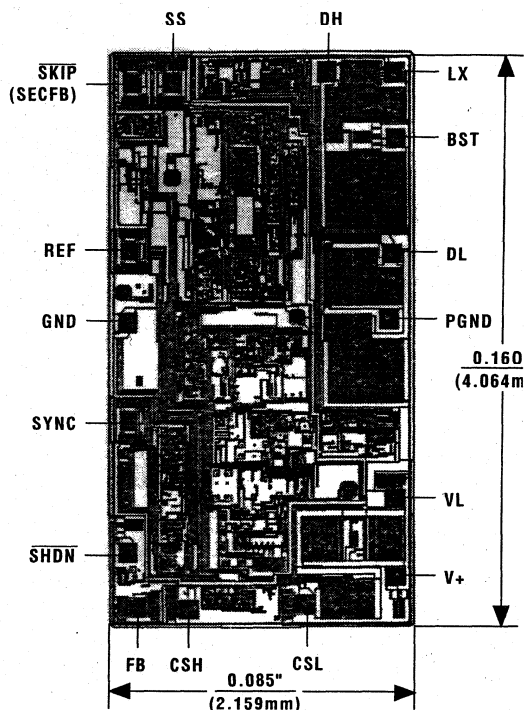
Step-Down Controllers with Synchronous Rectifier for CPU Power

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX797CPE	0°C to +70°C	16 Plastic DIP
MAX797CSE	0°C to +70°C	16 Narrow SO
MAX797C/D	0°C to +70°C	Dice*
MAX797EPE	-40°C to +85°C	16 Plastic DIP
MAX797ESE	-40°C to +85°C	16 Narrow SO
MAX797MJE	-55°C to +125°C	16 Cerdip
MAX799CPE	0°C to +70°C	16 Plastic DIP
MAX799CSE	0°C to +70°C	16 Narrow SO
MAX799C/D	0°C to +70°C	Dice*
MAX799EPE	-40°C to +85°C	16 Plastic DIP
MAX799ESE	-40°C to +85°C	16 Narrow SO
MAX799MJE	-55°C to +125°C	16 Cerdip

*Contact factory for dice specifications

Chip Topography



() ARE FOR MAX796/MAX799 ONLY.

TRANSISTOR COUNT: 913

SUBSTRATE CONNECTED TO GND

EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V/3V/Adjustable-Output, 1A, Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

The MAX830/MAX831/MAX832/MAX833 are monolithic, bipolar, pulse-width-modulation (PWM), switch-mode, step-down DC-DC regulators. Each is rated at 1A. Very few external components are needed for standard operation because the power switch, oscillator, feedback, and control circuitry are all on-chip. Employing a classic buck topology, these regulators perform high-current step-down functions.

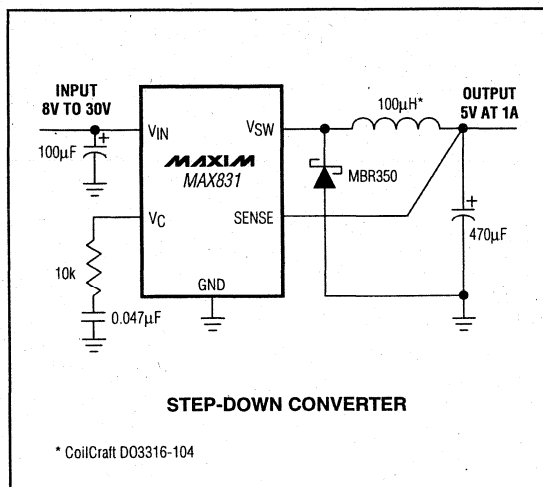
These regulators have excellent dynamic and transient response characteristics, while featuring cycle-by-cycle current limiting to protect against overcurrent faults and short-circuit output faults. They have a wide 8V to 30V input range. Outputs for the MAX831/MAX832/MAX833 are fixed at 5V/3.3V/3V, respectively. The MAX830 output is adjustable.

Available in 16-pin SO packages, the MAX830-MAX833 have a preset 100kHz oscillator frequency. In addition, the preset current limit and micropower shutdown can be externally controlled. See the MAX724/MAX726 data sheet for more applications information.

Applications

- Distributed Power from High-Voltage Buses
- High-Current, High-Voltage Step-Down Applications
- Multiple-Output Buck Converter

Typical Operating Circuit



Features

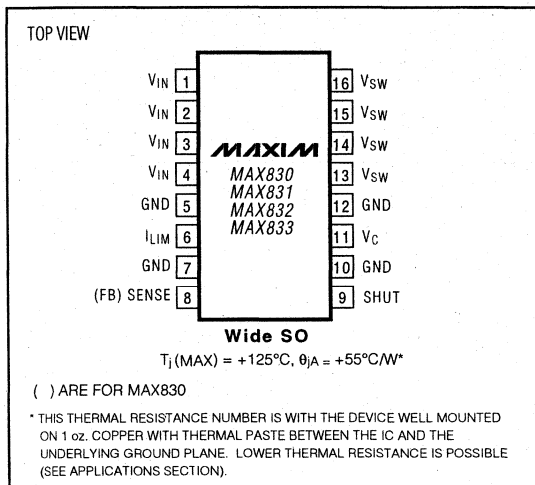
- ◆ Input Range: Up to 30V
- ◆ 1A On-Chip Power Switch
- ◆ Adjustable Output (MAX830)
Fixed Outputs: 5V (MAX831)
3.3V (MAX832)
3V (MAX833)
- ◆ 100kHz Switching Frequency
- ◆ Excellent Dynamic Characteristics
- ◆ Few External Components
- ◆ 8mA Quiescent Current
- ◆ 16-Pin SO Package
- ◆ Evaluation Kit Available

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX830CWE	0°C to +70°C	16 Wide SO
MAX831CWE	0°C to +70°C	16 Wide SO
MAX832CWE	0°C to +70°C	16 Wide SO
MAX833CWE	0°C to +70°C	16 Wide SO

4

Pin Configuration

**MAXIM**

Maxim Integrated Products 4-141

Call toll free 1-800-998-8800 for free samples or literature.

5V/3.3V/3V/Adjustable-Output, 1A, Step-Down, PWM, Switch-Mode DC-DC Regulators

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Switch Voltage with Respect to Input Voltage	50V
Switch Voltage with Respect to GND (V_{SW} negative) (Note 1)	20V
FB/SENSE Voltage	-0.3V, +10V
SHUT Voltage (not to exceed V_{IN})	30V

I_{LIM} Voltage (forced)	5.5V
Operating Temperature Range	0°C to +70°C
Junction Temperature Range	0°C to +125°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: Do not exceed switch-to-input voltage limitation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN} = 25V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Voltage Range			8		30	V
Switch-On Voltage (Note 2)	ISW = 0.2A				1.1	V
	ISW = 1A				1.4	
Switch-Off Leakage	VIN = 25V, VSW = 0V	TA = +25°C			150	µA
	VIN = 30V, VSW = 0V				250	
Supply Current (Note 3)	VIN ≤ 30V, VSENSE = 5.5V (MAX831/MAX832/MAX833) or VFB = 2.5V (MAX830)		8	11		mA
	VSHUT = 0.1V (Note 4)		140	500		µA
Minimum Supply Voltage (Note 5)	Normal mode		7.3	8.0		V
	Startup mode		3.5	4.8		
Switch-Current Limit (Note 6)	ILIM open		1.2	1.7	2.2	A
	RLIM = 10kΩ (Note 7)	TA = +25°C	1.2			
	RLIM = 7kΩ (Note 7)		0.8			
Maximum Duty Cycle			85	90		%
Switching Frequency	TA = +25°C		90	100	110	kHz
			85		120	
	VFB or VSENSE = 0V (Note 6) TA = +25°C		20			
Switching-Frequency Line Regulation	8V ≤ VIN ≤ 30V			0.03	0.10	%/V
Error-Amplifier Voltage Gain	1V ≤ VC ≤ 4V	TA = +25°C	2000			V/V
Error-Amplifier Transconductance	TA = +25°C		3000	5000	9000	µmho
Error-Amplifier Source Current	VFB = 2.0V (MAX830) or VSENSE = 2.0V (MAX831/832/833)	TA = +25°C	100	140	225	µA
Error-Amplifier Sink Current	VFB = 2.5V (MAX830) or VSENSE = 5.5V (MAX831/832/833)	TA = +25°C	0.6	1.0	1.7	mA

5V/3.3V/3V/Adjustable-Output, 1A, Step-Down, PWM, Switch-Mode DC-DC Regulators

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 25V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
SENSE Voltage	V _C = 2V	MAX831	4.85	5.00	5.15	V
		MAX832	3.20	3.30	3.40	
		MAX833	2.90	3.00	3.10	
SENSE Divider Resistance	T _A = +25°C	MAX831	3.0	5.0	8.0	kΩ
		MAX832	2.5	4.2	7.0	
		MAX833	2.2	3.8	6.5	
SENSE Voltage Tolerance (Note 8)	V _{OUT} (nominal) = 5V (MAX831), 3.3V (MAX832), or 3V (MAX833)	T _A = +25°C		±0.5	±2.0	%
				±0.5	±3.0	
FB Bias Current	V _{FB} = V _{REF} (MAX830)			0.5	2.0	μA
Reference Voltage	V _C = 2V (MAX830) (Note 9)		2.155	2.21	2.265	V
Reference Voltage Tolerance (Notes 8, 9)	V _{REF} (nominal = 2.21V) (MAX830)	T _A = +25°C		±0.5	±1.5	%
				±1.0	±2.5	
Output Voltage Line Regulation	8V ≤ V _{IN} ≤ 30V			0.005	0.020	%/V
V _C Voltage	0% duty cycle	T _A = +25°C		1.5		V
V _C Voltage Temperature Coefficient	0% duty cycle			-4		mV/°C
SHUT Current	V _{SHUT} = 5V			10	20	μA
	V _{SHUT} = 0.1V (shutdown)				50	
SHUT Threshold	(shutdown)		0.10	0.20	0.50	V

Note 2: For switch currents between 0.2A and 1A, maximum switch-on voltage can be calculated via linear interpolation.

Note 3: By setting the SENSE pin to 5.5V (or the FB pin to 2.5V), the V_C pin is forced to its low clamp level and the switch duty cycle is forced to zero, approximating the zero load condition.

Note 4: Device shut down. Switch leakage current not included.

Note 5: For proper regulation, total voltage from V_{IN} to GND must be $\geq 8V$ after start-up. During start-up mode, device is switching but not regulating.

Note 6: To avoid extremely short switch-on times, the switch frequency is internally scaled down when V_{FB} or V_{SENSE} is less than 1.3V. Switch current limit is tested with V_{SENSE} or V_{FB} adjusted to give a 1 μs minimum switch-on time.

Note 7: $R_{LIM} = \left[\frac{I_{LIM}}{1A} \times 7.6k\Omega \right] + 1k\Omega$. Typical value only. Minimum to maximum deviation in current limit will be $\pm 30\%$, comparable to that with I_{LIM} pin open.

Note 8: All conditions of input voltage, output voltage, temperature, and load current.

Note 9: FB is at the reference voltage when the MAX830 output voltage is in regulation.

MAX830-MAX833

4

5V/3.3V/3V/Adjustable-Output, 1A, Step-Down, PWM, Switch-Mode DC-DC Regulators

Pin Description

PIN	NAME	FUNCTION
8	SENSE (MAX831/2/3)	For the MAX831/MAX832/MAX833, SENSE input is the internal error amplifier's input, and should be directly connected to V _{OUT} . SENSE also aids current-limiting by reducing oscillator frequency when V _{OUT} is low.
	FB (MAX830)	For the MAX830, the FB input is the internal error amplifier's input, and should be connected to the mid-point of a potential divider between V _{OUT} and GND (Figure 1). The output voltage, during regulation, will be that value that forces 2.21V (V _{REF}) at the FB pin.
11	V _C	Error-amplifier output. A series RC network connected to this pin compensates the device. Output swing is limited to about 5.8V in the positive direction and -0.7V in the negative direction. V _C can also synchronize the device to an external TTL clock in the 115kHz to 170kHz range.
5, 7, 10, 12	GND	Ground requires a short, low-noise connection to ensure good load regulation. The internal reference is referred to GND, so errors at this pin are multiplied by the error amplifier. Use thick copper for low thermal resistance.
13, 14, 15, 16	V _{SW}	Internal power switch output (rated for 1A load current)
1, 2, 3, 4	V _{IN}	V _{IN} supplies power to the internal circuitry and also connects to the collector of the internal power switch. V _{IN} must be bypassed with a low-ESR capacitor, typically 100μF.
6	I _{LIM}	Switch-current limit can be reduced by connecting an external resistor (R _{LIM}) from I _{LIM} to GND (See Note 7 in <i>Electrical Characteristics</i>). Leave I _{LIM} floating for maximum current limit.
9	SHUT	Shutdown is achieved by pulling SHUT low. Leave SHUT floating for normal operation.

Applications Information

Although the MAX830-MAX833 are high-efficiency step-down voltage converters, certain precautions are required to avoid excessive chip temperature (the absolute maximum rating for this parameter, T_j, is +125°C). The 16-pin SO package has thermal resistance of +55°C/W when mounted properly; this limits continuous chip power dissipation to the 1W range.

When installing these chips:

- 1) Use wide and, if possible, thick copper traces to connect the leads (especially the GND pins) to reduce thermal resistance.
- 2) Bond the package firmly to the board or use a clip-style heatsink. A very small drop of thermal paste between the chip package and the copper ground plane is also helpful.
- 3) Confirm that the range of device operation is such that the chip temperature does not exceed the allowed maximum of T_j = +125°C. This can be determined from Tables 1 and 2.

Tables 1 and 2 show numbers for maximum allowed load current based on not exceeding the T_j = +125°C limit. If the input voltage range, ambient temperature, and/or output voltage setting allow for an unsafe level of load current, limit the load current to a safe value by connecting the appropriate resistor from the I_{LIM} pin to GND. With no external resistor, the preset switch cur-

rent limit (typically 1.7A) will limit the load current to about 1.3A. Table 1 shows safe operating load currents for the MAX830 for various values of input and output voltage and at three different ambient temperatures of T_A = +25°C, +45°C, and +70°C, respectively. Table 2 shows the same information, but for the fixed output voltage MAX831, MAX832, and MAX833.

When consulting these tables, note that power surges of less than 30sec need not be considered from a thermal standpoint. It is important for proper regulation, however, that a power surge not require a peak switch current exceeding the 1.2A (min) switch current limit. Also, the inductor's current rating should exceed I_{PEAK}. For highest efficiency, the inductor series resistance should be 0.4Ω or less. I_{PEAK} and I_{LOAD} are related by the following formula:

$$I_{PEAK} = I_{LOAD} + \frac{[V_{OUT} \times (V_{IN} - V_{OUT})]}{V_{IN} \times L \times 200,000}$$

Example: MAX830 with V_{IN} = 30V, V_{OUT} = 15V, I_{LOAD} = 0.5A continuous, L = 100μH and T_A = +70°C:
 I_{PEAK} = 0.86A (which is below 1.2A (min) preset switch current limit);
 and from Table 1:
 maximum I_{LOAD} allowed = 0.8A continuous (i.e., operation is safe).

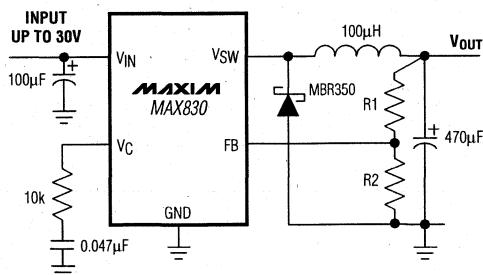
5V/3.3V/3V/Adjustable-Output, 1A, Step-Down, PWM, Switch-Mode DC-DC Regulators

Table 1. MAX830 Maximum Load Current (continuous with $\theta_{jA} = +55^{\circ}\text{C/W}$) vs. Output Voltage and Ambient Temperature

OUTPUT VOLTAGE	CONTINUOUS LOAD CURRENT		
	$T_A = +25^{\circ}\text{C}$	$T_A = +45^{\circ}\text{C}$	$T_A = +70^{\circ}\text{C}$
Up to 10V	1A	1A	1A
10V to 15V	1A	1A	0.8A
15V to 20V	1A	0.8A	0.7A
20V to 25V	0.8A	0.7A	0.6A

Table 2. MAX831/MAX832/MAX833 Maximum Load Current (continuous with $\theta_{jA} = +55^{\circ}\text{C/W}$) vs. Ambient Temperature

OUTPUT VOLTAGE	CONTINUOUS LOAD CURRENT		
	$T_A = +25^{\circ}\text{C}$	$T_A = +45^{\circ}\text{C}$	$T_A = +70^{\circ}\text{C}$
Fixed: 5V, 3.3V or 3V	1A	1A	1A



$$V_{OUT} = \left[1 + \frac{R1}{R2} \right] \times 2.21V$$

STEP-DOWN CONVERTER

Figure 1. MAX830 Typical Operating Circuit

EVALUATION KIT
AVAILABLE**MAXIM**

Low-Noise, Regulated, -2V GaAsFET Bias

General Description

The MAX840/MAX843/MAX844 low-noise, inverting charge-pump power supplies are ideal for biasing GaAsFETs in cellular telephone transmitter amplifiers. They operate with inputs down to 2.5V.

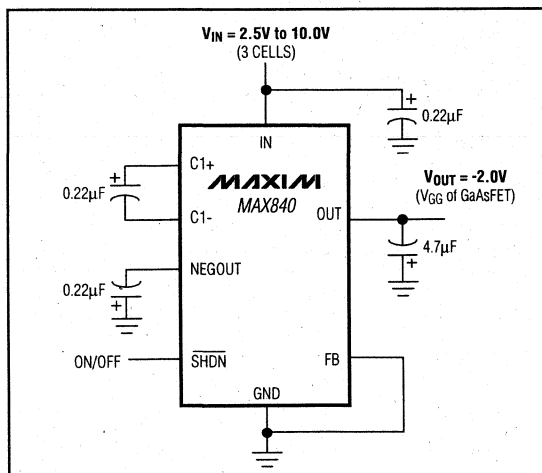
The MAX840 offers both a -2V preset output and a -0.5V to -9.4V adjustable output. The MAX843/MAX844 use an external positive control voltage to set the negative output voltage. Input voltage range for all the devices is 2.5V to 10V, and output current is 4mA with $V_{IN} > 2.7V$. These circuits can operate with small capacitors, as low as 0.22 μ F.

An internal linear regulator reduces the MAX840's output voltage ripple to 1mVp-p. With a well-filtered control voltage (V_{CTRL}), the MAX843/MAX844 also achieve less than 1mVp-p typical output ripple. Supply current is 750 μ A, and reduces to less than 1 μ A in shutdown (MAX840/MAX843). The MAX844's unregulated output is active in shutdown, with the charge pump switching at 20kHz. It provides a low-power LCD supply.

Applications

Cellular Phones
GaAsFET Power Amplifier Modules
Personal Communicators, PDAs
Wireless Data Loggers
Continuously Adjustable GaAsFET Bias
LCD-Bias Contrast Control
Regulated Negative Power Supplies

Typical Operating Circuit



Features

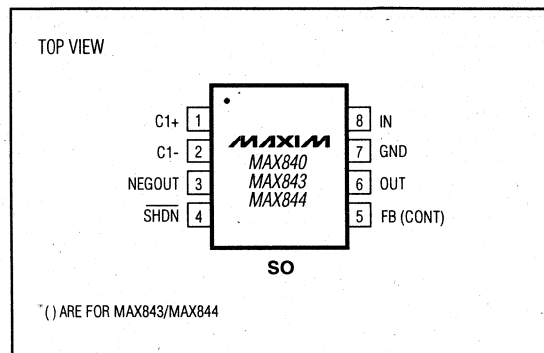
- ♦ Fixed -2V or Adjustable -0.5V to -9.4V Output at 4mA (MAX840)
- ♦ 2.5V to 10V Input Voltage Range
- ♦ Operate with Small Capacitors (as low as 0.22 μ F)
- ♦ 1mVp-p Output Voltage Ripple
- ♦ Charge-Pump Switching Frequency:
100kHz in Normal Operation
20kHz in Shutdown Mode (MAX844)
- ♦ 1 μ A Max Logic-Level Shutdown Over Temp. (MAX840/MAX843)
- ♦ Small 8-Pin SO Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX840C/D	0°C to +70°C	Dice*
MAX840ISA	-25°C to +85°C	8 SO
MAX840ESA	-40°C to +85°C	8 SO
MAX843C/D	0°C to +70°C	Dice*
MAX843ISA	-25°C to +85°C	8 SO
MAX843ESA	-40°C to +85°C	8 SO
MAX844C/D	0°C to +70°C	Dice*
MAX844ISA	-25°C to +85°C	8 SO
MAX844ESA	-40°C to +85°C	8 SO

* Dice are specified at $T_A = +25^\circ\text{C}$ only.

Pin Configuration



MAX840/MAX843/MAX844

4

MAXIM

Maxim Integrated Products 4-147

Call toll free 1-800-998-8800 for free samples or literature.

Low-Noise, Regulated, -2V GaAsFET Bias

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} to GND-0.3V to 10.5V
 V_{NEGOUT} to GND-10.5V to 0.3V
 V_{IN} to V_{NEGOUT} -0.3V to 21V
 V_{OUT} to GND (Note 1) V_{NEGOUT} to 0.3V
 V_{SHDN} to GND-0.3V to ($V_{IN} + 0.3V$)
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 SO (derate 10.00mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)800mW

Operating Temperature Ranges

MAX84_I-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
 MAX84_E-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
 Storage Temperature Range-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
 Lead Temperature (soldering, 10sec)+300 $^\circ\text{C}$

Note 1: The output may be shorted to $NEGOUT$ or GND if the package power dissipation is not exceeded. Typical short-circuit current from 4V to GND is 40mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Figures 2a and 2c, $2.5V \leq V_{IN} \leq 10V$, $V_{OUT} = -2V$, GND = 0V, $R_L = \infty$, $SHDN = V_{IN}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are measured at $V_{IN} = 3.6V$ and $T_A = +25^\circ\text{C}$.)

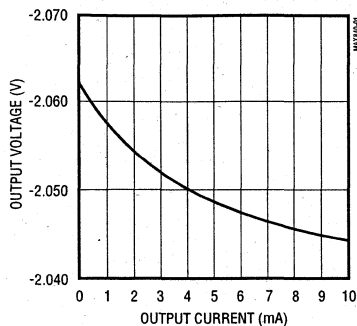
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}		2.5		10	V
Output Voltage	V_{OUT}	MAX840, $V_{FB} = 0V$				V
		$V_{IN} \geq 2.5V$, $I_{OUT} = 0mA$ to 3mA	-2.1	-2.0	-1.9	
		$V_{IN} \geq 2.7V$, $I_{OUT} = 0mA$ to 4mA	-2.1	-2.0	-1.9	
		MAX843/MAX844, $V_{CTRL} = 2V$				
Output Voltage Adjust Range	V_{OUT}	$V_{IN} \geq 2.5V$, $I_{OUT} = 0mA$ to 3mA	-2.05	-2.0	-1.95	V
		$V_{IN} \geq 2.7V$, $I_{OUT} = 0mA$ to 4mA	-2.05	-2.0	-1.95	
Output Voltage Adjust Range	V_{OUT}			-0.5 to ($V_{IN} - 0.6$)		V
FB Voltage	V_{FB}	MAX840, no load	-0.516	-0.5	-0.484	V
FB Leakage Current	I_{FB}	MAX840, $V_{FB} = -0.5V$		± 1	± 100	nA
CONT Leakage Current	I_{CONT}	MAX843/MAX844, $V_{CONT} = 0V$		± 1	± 100	nA
Supply Current	I_Q	No load, $V_{IN} \leq 3.6V$		750	1100	μA
Shutdown Supply Current	I_{SHUT}	MAX840/MAX843, $V_{IN} = 10V$, $SHDN = 0V$			1	μA
		MAX844, $V_{IN} = 10V$, $SHDN = 0V$		940		
		MAX844, $V_{IN} \leq 3.6V$, $SHDN = 0V$		175	300	
V_{OUT} Load Regulation		$V_{IN} = 3.6V$, $R_L = \infty$ or 500 Ω				mV/mA
		MAX840, $V_{FB} = 0V$		3	8	
V_{OUT} Load Regulation		MAX843/MAX844, $V_{CTRL} = 2V$		2	8	mV/mA
V_{OUT} Ripple		$C_4 = 10\mu F$		1		mVp-p
Oscillator Frequency	F_{OSC}	$V_{IN} = 3.6V$, $T_A = +25^\circ\text{C}$	80	100	120	kHz
		MAX844, $SHDN = 0V$	14	20	26	
Input High Voltage	V_{IH}	$SHDN$	2.2			V
Input Low Voltage	V_{IL}	$SHDN$			0.5	V
Input Current	I_{IN}	$SHDN$	-1		1	μA
Input Capacitance	C_{IN}	$SHDN$		10		pF

Low-Noise, Regulated, -2V GaAsFET Bias

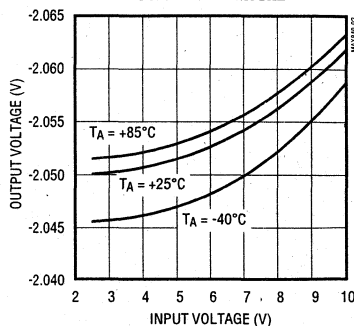
Typical Operating Characteristics

(Circuit of Figure 2a, $V_{IN} = 3.6V$, $T_A = +25^\circ C$, unless otherwise noted.)

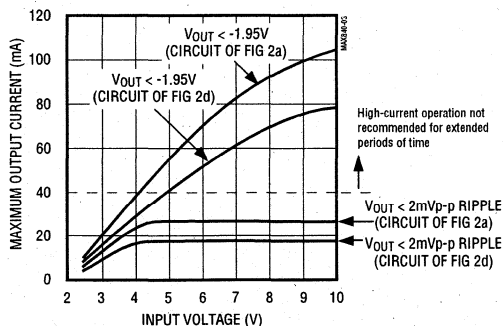
OUTPUT VOLTAGE vs. OUTPUT CURRENT



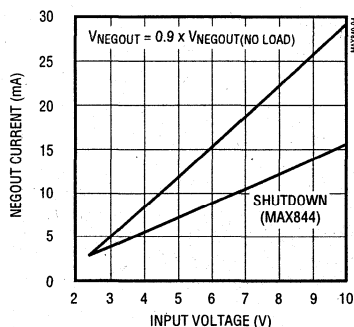
OUTPUT VOLTAGE vs. INPUT VOLTAGE OVER TEMPERATURE



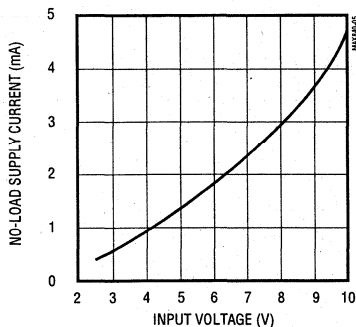
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



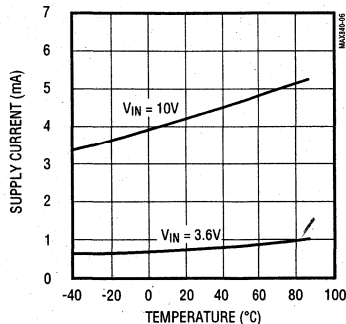
NEGOUT CURRENT vs. INPUT VOLTAGE



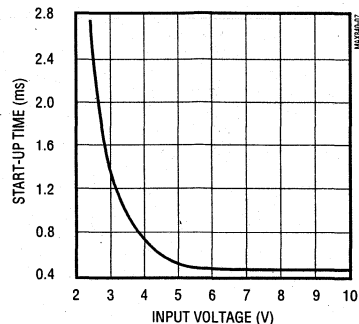
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



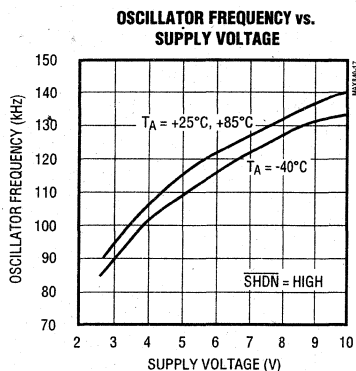
START-UP TIME vs. INPUT VOLTAGE



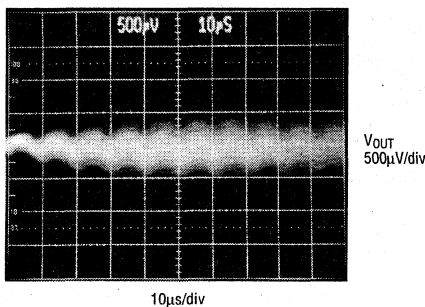
Low-Noise, Regulated, -2V GaAsFET Bias

Typical Operating Characteristics (continued)

(Circuit of Figure 2a, $V_{IN} = 3.6V$, $T_A = +25^\circ C$, unless otherwise noted.)

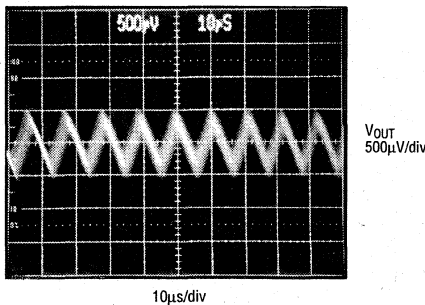


MAX840 OUTPUT NOISE AND RIPPLE
($C_1 = C_2 = C_3 = 1\mu F$, $C_4 = 10\mu F$)

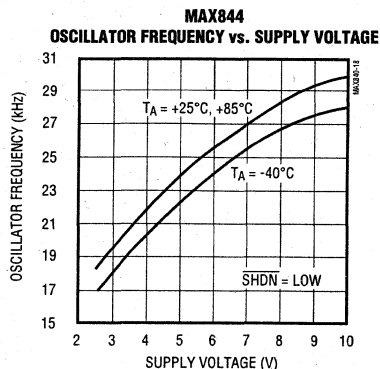


$V_{IN} = 3.6V$, $V_{OUT} = -2V$, $I_{OUT} = 4mA$, AC COUPLED

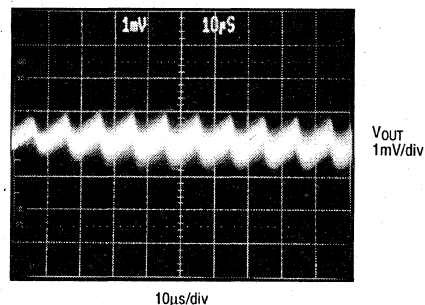
MAX843/MAX844 OUTPUT NOISE AND RIPPLE
($C_1 = C_2 = C_3 = 1\mu F$, $C_4 = 10\mu F$)



$V_{IN} = 3.6V$, $V_{OUT} = -2V$, $I_{OUT} = 4mA$, AC COUPLED

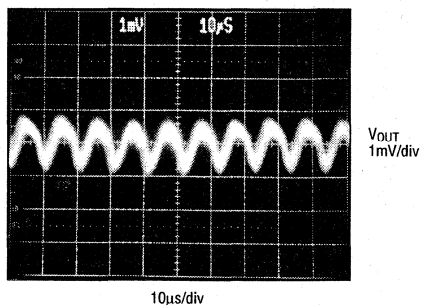


MAX840 OUTPUT NOISE AND RIPPLE
($C_1 = C_2 = C_3 = 0.22\mu F$, $C_4 = 4.7\mu F$)



$V_{IN} = 3.6V$, $V_{OUT} = -2V$, $I_{OUT} = 4mA$, AC COUPLED

MAX843/MAX844 OUTPUT NOISE AND RIPPLE
($C_1 = C_2 = C_3 = 0.22\mu F$, $C_4 = 4.7\mu F$)



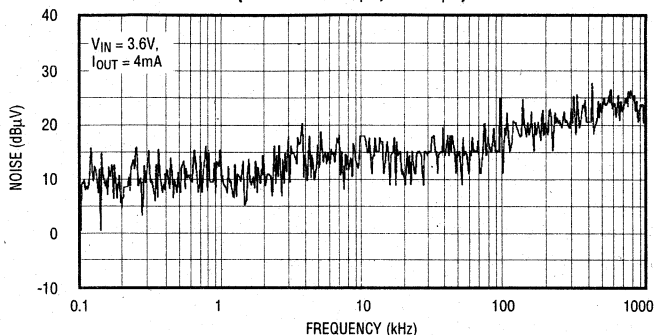
$V_{IN} = 3.6V$, $V_{OUT} = -2V$, $I_{OUT} = 4mA$, AC COUPLED

Low-Noise, Regulated, -2V GaAsFET Bias

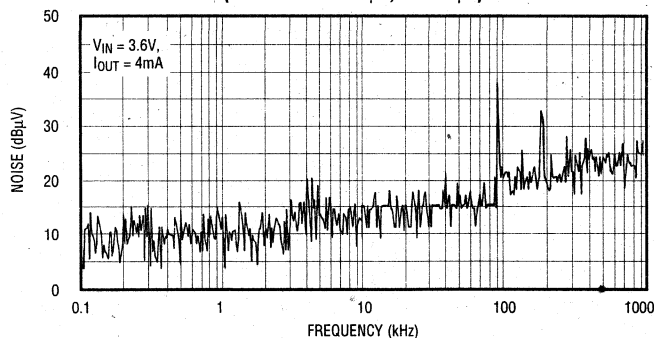
Typical Operating Characteristics (continued)

(Circuit of Figure 2a, $V_{IN} = 3.6V$, $T_A = +25^\circ C$, unless otherwise noted.)

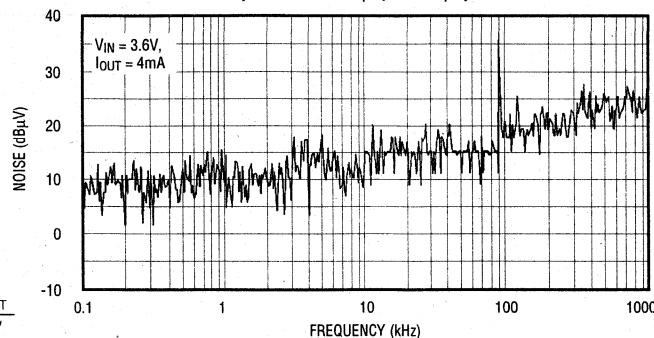
MAX840 NOISE SPECTRUM
($C_1 = C_2 = C_3 = 1\mu F$, $C_4 = 10\mu F$)



MAX840 NOISE SPECTRUM
($C_1 = C_2 = C_3 = 0.22\mu F$, $C_4 = 4.7\mu F$)



MAX843/MAX844 NOISE SPECTRUM
($C_1 = C_2 = C_3 = 1\mu F$, $C_4 = 10\mu F$)



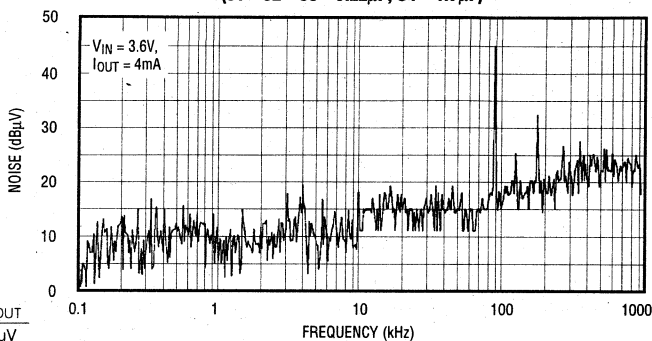
NOTE: $dB\mu V = 20 \text{ LOG } \frac{V_{OUT}}{1\mu V}$

Low-Noise, Regulated, -2V GaAsFET Bias

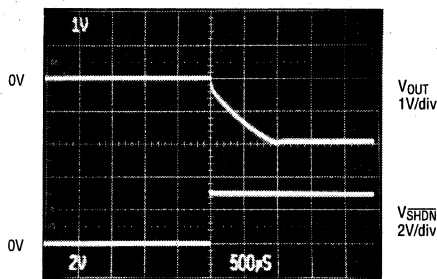
Typical Operating Characteristics (continued)

(Circuit of Figure 2a, $V_{IN} = 3.6V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX843/MAX844 NOISE SPECTRUM
($C_1 = C_2 = C_3 = 0.22\mu F$, $C_4 = 4.7\mu F$)

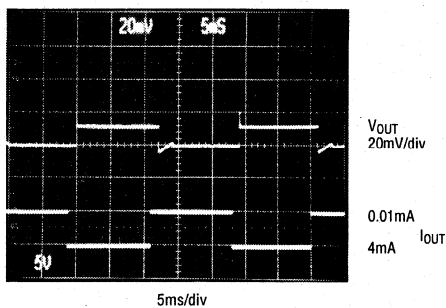


START-UP FROM SHUTDOWN



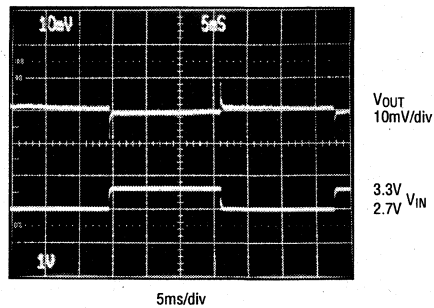
$V_{IN} = 3.6V$, $V_{OUT} = -2V$, $I_{OUT} = 4mA$

LOAD-TRANSIENT RESPONSE



$V_{IN} = 3.6V$, $V_{OUT} = -2V$

LINE-TRANSIENT RESPONSE



$V_{OUT} = -2V$, $I_{OUT} = 4mA$, AC COUPLED

Low-Noise, Regulated, -2V GaAsFET Bias

Pin Description

PIN		NAME	FUNCTION
MAX840	MAX843 MAX844		
1	1	C1+	Positive Terminal for C1
2	2	C1-	Negative Terminal for C1
3	3	NEGOUT	Negative Output Voltage (unregulated)
4	4	SHDN	Active-Low, TTL Logic-Level Shutdown Input
5	—	FB	Dual-Mode™ Feedback Input. When FB is grounded, the output is preset to -2V. To select other output voltages, connect FB to an external resistor divider (Figure 2b).
—	5	CONT	Control Voltage Input. To set V_{OUT} , connect a resistor divider between OUT and a positive control voltage between 0V and 10V (Figure 2c).
6	6	OUT	Regulated Negative Output Voltage
7	7	GND	Ground
8	8	IN	Positive Power-Supply Input

™Dual-Mode is a trademark of Maxim Integrated Products.

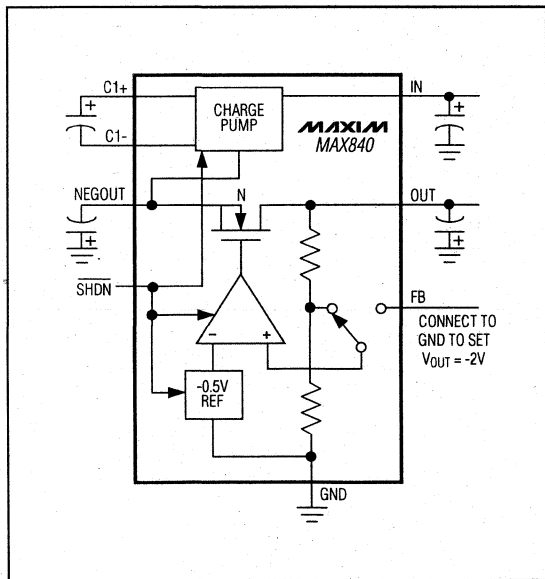


Figure 1a. MAX840 Block Diagram

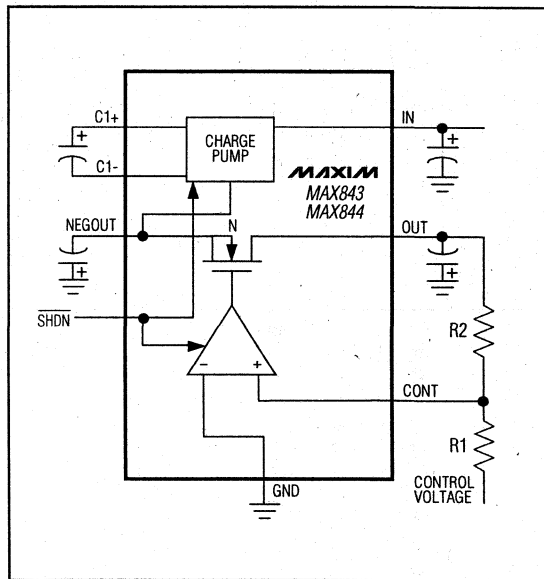


Figure 1b. MAX843/MAX844 Block Diagram

Low-Noise, Regulated, -2V GaAsFET Bias

Detailed Description

The MAX840/MAX843/MAX844 are low-noise, inverting, regulated charge-pump power supplies designed for biasing GaAsFET devices, such as power-amplifier modules in cellular handsets.

The applied input voltage (V_{IN}) is first inverted to a negative voltage at NEGOUT by a capacitive charge pump. This voltage is then regulated by an internal low-noise linear regulator, and appears at OUT (Figure 1). The minimum (most negative) output voltage achievable is the inverted positive voltage, plus the 0.6V required by the post-regulator. For the MAX840, the linear regulator reduces ripple noise induced by the charge-pump inverter to 1mVp-p at VOUT. In addition, the linear regulator's excellent AC rejection attenuates noise from the incoming supply.

Applications Information

Setting the Output Voltage

For the MAX840, select either a fixed or adjustable output voltage. Connect FB directly to GND for a fixed -2V output (Figure 2a). Select an alternate output voltage by connecting FB to the midpoint of a resistor voltage divider from OUT to GND (Figure 2b). V_{IN} must be 0.6V above the absolute value of VOUT to allow proper regulation. The output voltage is calculated from the formula below. Choose R2 to be between 100k Ω and 400k Ω .

$$V_{OUT} = (-0.5V)(1 + R2 / R1)$$

For the MAX843/MAX844, set the output voltage by connecting a resistor voltage divider between OUT and a positive control voltage (VCTRL) (Figure 2c).

$$V_{OUT} = -V_{CTRL} (R2 / R1)$$

Shutdown Mode

The MAX840/MAX843/MAX844 feature a shutdown mode that reduces the supply current to 1 μ A max over temperature (300 μ A max for the MAX844). When the MAX840/MAX843 are in shutdown, the outputs (OUT, NEGOUT) and the charge-pump oscillator are disabled. When the MAX844 is in shutdown, only the linear regulator is disabled and the NEGOUT output remains enabled. However, the charge-pump oscillation frequency is reduced to 20kHz, reducing the available power at NEGOUT. The output voltage at NEGOUT can be used to bias an LCD while in shutdown.

Capacitors

Use capacitors with low effective series resistance (ESR) to maintain a low dropout voltage ($V_{IN} - |V_{OUT}|$). The overall dropout voltage is a function of the charge pump's output resistance and the voltage drop across the linear regulator (N-channel pass transistor). At the 100kHz switching frequency, the charge-pump output resistance is a function of C1 and C2's ESR. Therefore, minimizing the ESR of the charge-pump capacitors minimizes the dropout voltage.

The output resistance of the entire circuit is approximately:

$$R_{OUT} = R_O + 4 \times ESR_{C1} + ESR_{C4} + 1 / (f_S \times C1) + R(\text{linear regulator})$$

where [$R_O + R(\text{linear regulator})$], the effective resistance of the internal switches and the resistance across the linear regulator, is approximately 71 Ω at $V_{IN} = 2.5V$, 48 Ω at $V_{IN} = 5V$, and 40 Ω at $V_{IN} = 10V$.

C1, C2, and C3 should be 1 μ F capacitors with less than 0.8 Ω ESR. C4 should be a 10 μ F capacitor with less than 0.2 Ω ESR. Smaller capacitor values can be used ($C1 = C2 = C3 = 0.22\mu F$, $C4 = 4.7\mu F$) with a small increase in output noise and ripple (Figure 2d). All capacitors should be either surface-mount chip tantalum or ceramic types. External capacitor values can be adjusted to optimize size and cost.

Layout and Grounding

Good layout is important, primarily for good noise performance. Take the following steps to ensure good layout:

- 1) Mount all components as close together as possible.
- 2) Keep traces short to minimize parasitic inductance and capacitance. This includes connections to FB.
- 3) Use a ground plane.

Noise and Ripple Measurement

Accurately measuring the output noise and ripple is a challenge. Slight momentary differences in ground potential between the MAX840/MAX843/MAX844 circuit and the oscilloscope (which results from the charge pump's switching action) cause ground currents in the probe's wires, inducing sharp voltage spikes. For best results, measure directly across the output capacitor (C4). Do not use the ground lead of the oscilloscope probe; instead, remove the probe's tip cover and touch the ground ring on the probe directly to C4's ground terminal. You can also use a Tektronix chassis-mount test jack (part no. 131-0258) to connect your scope probe directly. This direct connection gives the most accurate noise and ripple measurement.

Low-Noise, Regulated, -2V GaAsFET Bias

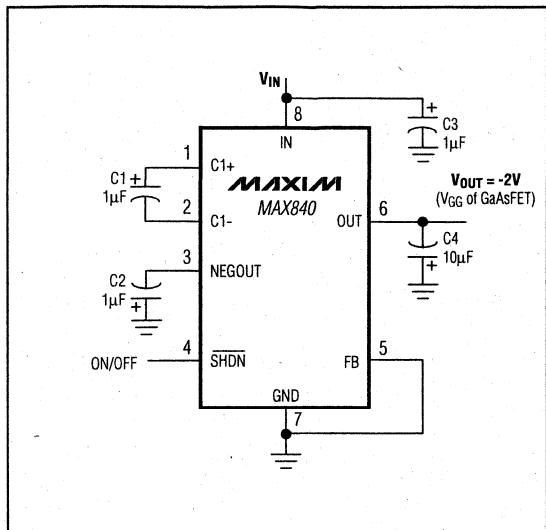


Figure 2a. MAX840 Standard Application Circuit

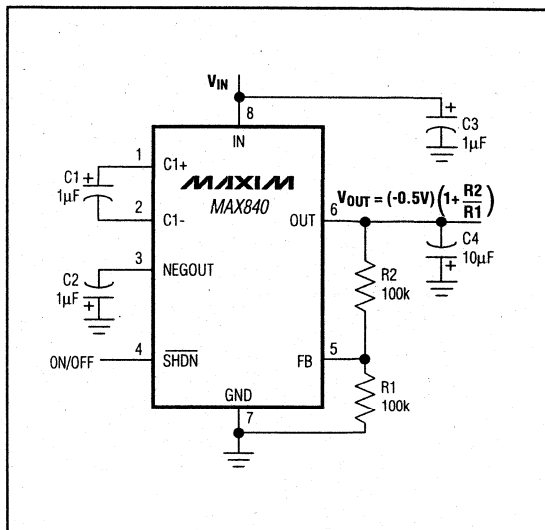


Figure 2b. MAX840 Adjustable Configuration

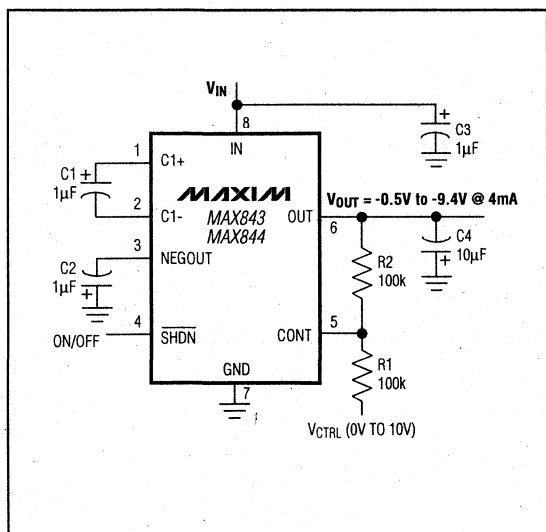


Figure 2c. MAX843/MAX844 Standard Application Circuit

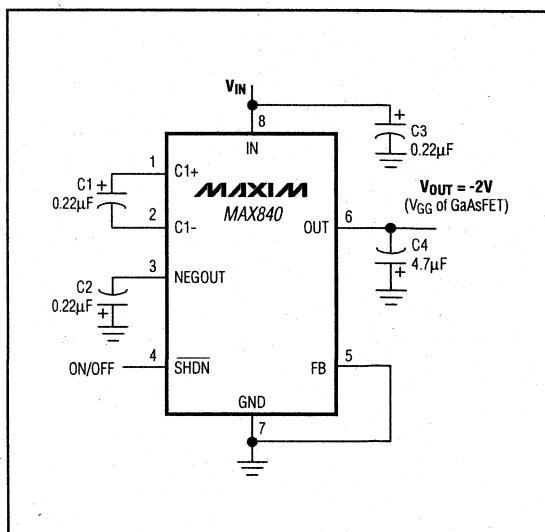
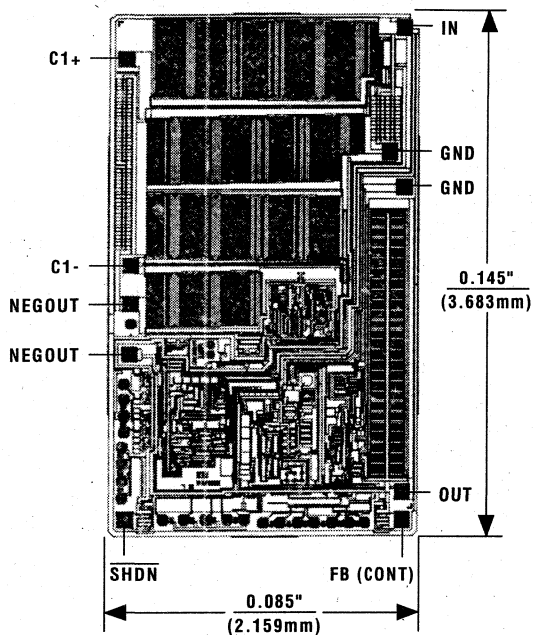


Figure 2d. MAX840 Application Circuit Using Smaller Capacitors

Low-Noise, Regulated, -2V GaAsFET Bias

Chip Topography



() ARE FOR MAX843/MAX844

TRANSISTOR COUNT: 148

SUBSTRATE CONNECTED TO IN

EVALUATION KIT
AVAILABLE**MAXIM**

Isolated Transformer Driver for PCMCIA Applications

MAX845

General Description

The MAX845 provides an isolated power supply small enough to fit in thin PCMCIA cards and space-sensitive applications. It drives a low-profile center-tapped transformer primary from a 5V or 3.3V DC power supply. The secondary can be wound to provide any isolated positive or negative voltage at powers up to 750mW.

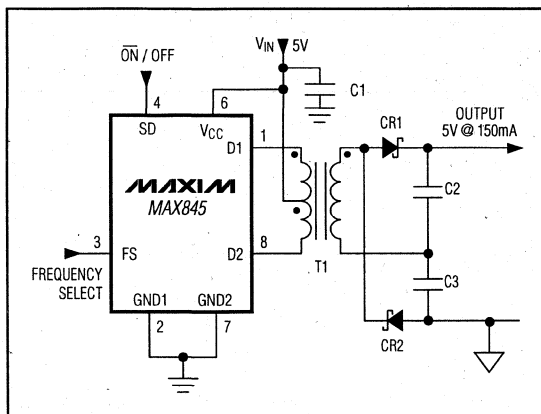
The MAX845 consists of an oscillator followed by a toggle flip-flop. The flip-flop generates two 50% duty-cycle square waves, which are complementary at half the oscillator frequency (450kHz, min). These two signals drive the ground-referenced N-channel power switches. Internal circuitry ensures break-before-make action between the two switches.

A low-power shutdown disables both the switches and the oscillator, reducing power consumption. An evaluation kit (MAX845EVKIT-MM) is available to evaluate low-profile 5V 40mA and 5V 100mA applications.

Applications

PCMCIA Modem Cards
Isolated Data Acquisition
Isolated Interface Power Supply
Noise-Immunity Communications Interface
Bridging Ground Differences
Medical Equipment
Process Control
Low-Power LAN Networks

Typical Operating Circuit



Features

- ♦ Transformer Driver for Ultra-Thin 5V- μ s Transformers
- ♦ Isolated DC-to-DC Power Supply for PCMCIA Applications
- ♦ 450kHz Minimum Switching Frequency
- ♦ Ultra-Low Input Supply Current Ripple
- ♦ Single +5V or +3.3V Supply
- ♦ 5 μ W Low-Power Shutdown Mode
- ♦ 8-Pin SO and μ MAX Packages
- ♦ Low Output Ripple Permits Miniature Output Capacitors

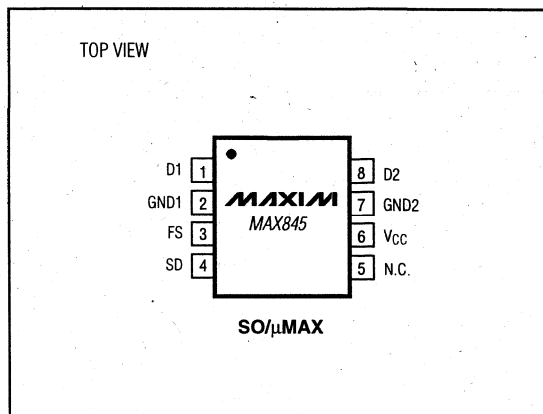
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX845ESA	-40°C to +85°C	8 SO
MAX845EUA	-40°C to +85°C	8 μ MAX
MAX845C/D	0°C to +70°C	Dice*

*Contact factory for dice specifications.

4

Pin Configuration

**MAXIM**

Maxim Integrated Products 4-157

Call toll free 1-800-998-8800 for free samples or literature.

Isolated Transformer Driver for PCMCIA Applications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})-0.3V to +7V
 Control Input Voltages (SD, FS)-0.3V to (V_{CC} + 0.3V)
 Peak Output Switch Current (D1, D2)1A
 Output Switch Voltage (D1, D2)12V
 Average Output Switch Current (D1, D2)200mA
 Continuous Power Dissipation (T_A = +70°C)
 SO (derate 5.88mW/°C above +70°C)471mW
 μMAX (derate 4.10mW/°C above +70°C)330mW

Operating Temperature Range-40°C to +85°C
 Storage Temperature Range-65°C to +160°C
 Junction Temperature+150°C
 Lead Temperature (soldering, 10sec)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switch On-Resistance	D1, D2; 100mA		1.5	4.0	Ω
Switch Frequency	FS = V _{CC} = 4.5V	450	675	900	kHz
	FS = V _{CC} = 5.5V	550	860	1100	
	FS = 0V, V _{CC} = 4.5V		500		
	FS = 0V, V _{CC} = 5.5V		575		
Operating Supply Current (Note 1)	No load, SD = 0V, FS = V _{CC}		1.1	5.0	mA
Shutdown Supply Current (Note 2)	SD = V _{CC}		0.4		μA
Shutdown Input Threshold	High	2.4			V
	Low			0.8	
Shutdown Input Leakage Current			10		pA
FS Input Threshold	High	2.4			V
	Low			0.8	
FS Input Current	FS = 0V			50	μA
	FS = V _{CC}		10		
Minimum Start-Up Voltage		2.5	2.2		V

Note 1: Operating supply current is the current used by the MAX845 only. Load current is not included.

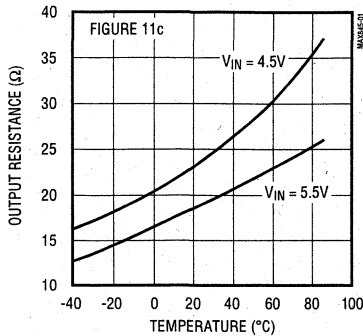
Note 2: Shutdown supply current includes output switch leakage currents.

Isolated Transformer Driver for PCMCIA Applications

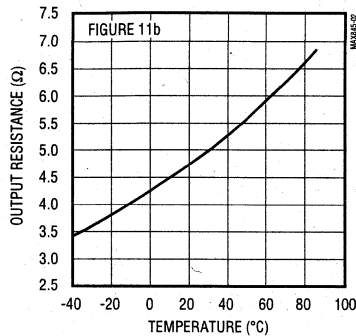
Typical Operating Characteristics

(Typical Operating Circuit, $V_{IN} = 5V$, $C_1 = 0.1\mu F$, $C_2 = C_3 = 0.33\mu F$, $T_1 = \text{Halo TGM-010P3}$, $CR_1 = CR_2 = \text{MBR0520}$, $FS = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

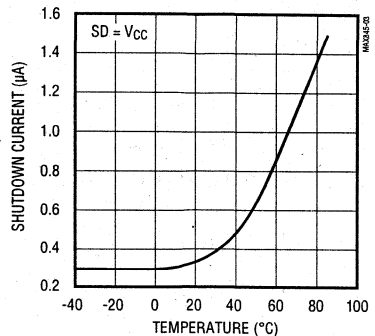
OUTPUT RESISTANCE vs. TEMPERATURE



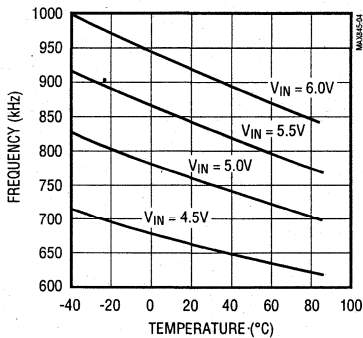
OUTPUT RESISTANCE vs. TEMPERATURE



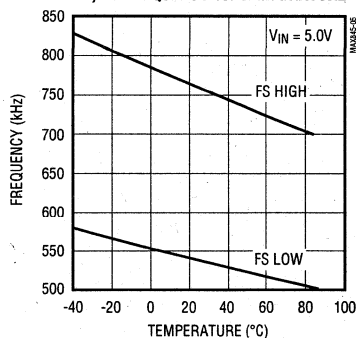
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



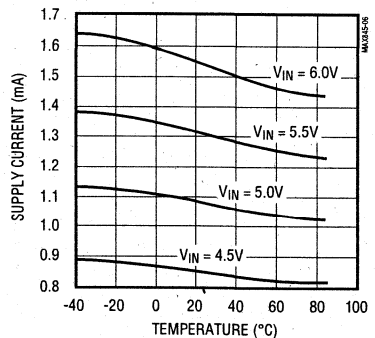
D1, D2 FREQUENCY vs. TEMPERATURE



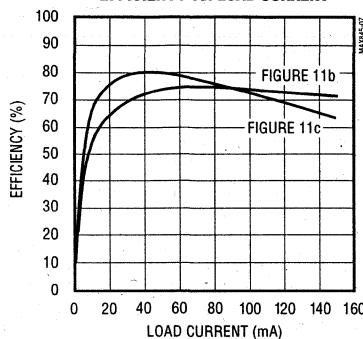
D1, D2 FREQUENCY vs. TEMPERATURE



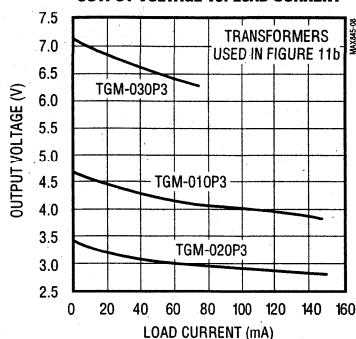
SUPPLY CURRENT vs. TEMPERATURE



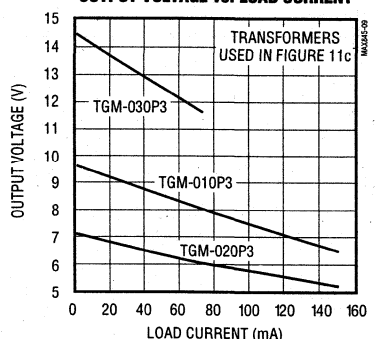
EFFICIENCY vs. LOAD CURRENT



OUTPUT VOLTAGE vs. LOAD CURRENT



OUTPUT VOLTAGE vs. LOAD CURRENT

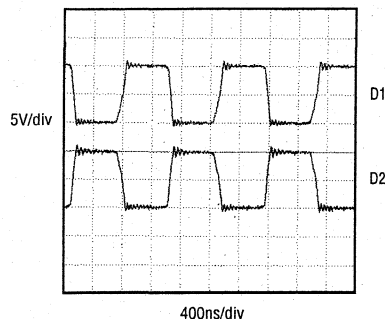


Isolated Transformer Driver for PCMCIA Applications

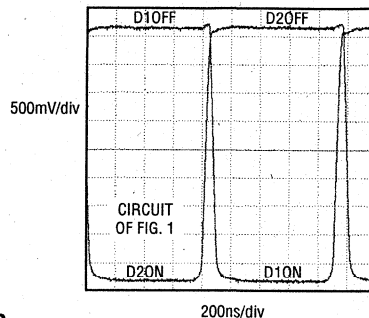
Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{IN} = 5V$, $C1 = 0.1\mu F$, $C2 = C3 = 0.33\mu F$, $T1 = \text{Halo TGM-010P3}$, $CR1 = CR2 = \text{MBR0520}$, $FS = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

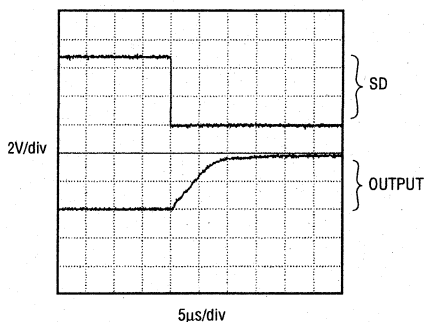
**SWITCHING WAVEFORMS
(TWO CYCLES)**



**SWITCHING WAVEFORM
(BREAK-BEFORE-MAKE)**



TIME FROM SHUTDOWN TO POWER-UP



Pin Description

PIN	NAME	FUNCTION
1	D1	Open drain of N-channel transformer drive 1.
2	GND1	Ground. Connect both GND1 and GND2 to ground.
3	FS	Frequency Select (internal pull-up). If $FS = V_{CC}$ or open, switch frequency = 725kHz; if $FS = 0V$, switch frequency = 535kHz.
4	SD	Shutdown. Ground for normal operation, connect to V_{CC} for shutdown.
5	N.C.	Not internally connected.
6	VCC	+5V supply voltage.
7	GND2	Ground. Connect both GND1 and GND2 to ground.
8	D2	Open drain of N-channel transformer drive 2.

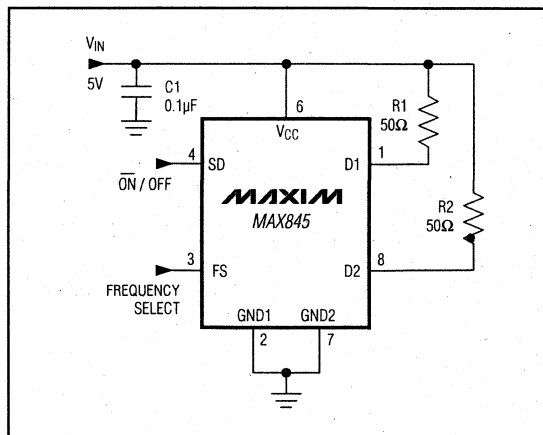


Figure 1. Test Circuit

Isolated Transformer Driver for PCMCIA Applications

MAX845

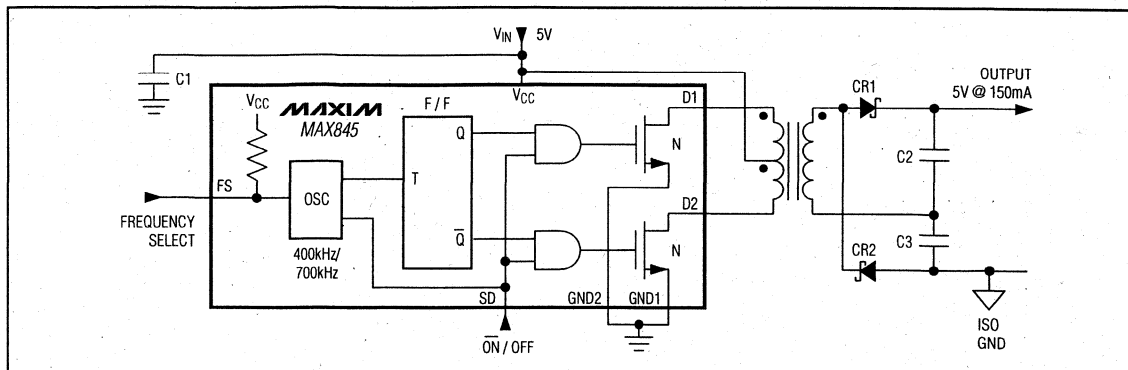


Figure 2. Detailed Block Diagram

Detailed Description

The MAX845 is a transformer driver specifically designed to provide isolated power for PCMCIA and other height- and/or space-sensitive applications. It drives a center-tapped transformer primary from a 5V or 3.3V DC power supply. The secondary can be wound to provide any isolated DC voltage needed at power levels up to 750mW.

The 450kHz minimum switching frequency allows the use of very thin transformers, making the MAX845 ideal for PCMCIA and other space-limited applications. The MAX845 is designed to drive a single transformer less than 0.09 inches (2.3mm) in height, including package. Further reduction down to 0.050 inches (1.27mm), can be achieved using a transformer without a package.

The MAX845 consists of an RC oscillator driving a pair of N-channel power switches. The oscillator runs at double the output frequency, driving a toggle flip-flop to ensure 50% duty cycle to each of the switches. Internal circuitry ensures break-before-make action between the two switches.

A low-current shutdown mode disables all internal circuitry, including the oscillator and both power switches. Drive the shutdown pin (SD) high to shut down the part; drive SD low for normal operation. The SD pin has no internal default condition and must not be allowed to float.

Most MAX845 applications will operate at high frequencies. The frequency-select pin (FS) is pulled high or left open (FS is internally pulled up to VCC) to operate at a minimum of 450kHz. Pulling FS low selects the low-frequency state.

Theory of Operation

Figure 2 shows the MAX845 driving both a TGM-010P3 transformer with a center-tapped primary, and a secondary with a voltage-doubler rectifier topology. All of the transformers driven by the MAX845 must have a center tap with VIN applied. Whenever one of the MAX845 outputs (D1 or D2) goes low, the other goes to approximately double the supply voltage. A voltage is induced in the secondary and the rectifier diodes steer the currents into the appropriate output capacitor. On alternate half cycles, each capacitor is charged. The output voltage is the sum of the voltages from each output capacitor. This topology yields the simplest and smallest transformer because the least number of secondary turns is required for a given voltage.

Applications Information

With the MAX845 transformer driver, designers have the advantages of push/pull converter topology in space-sensitive applications. The push/pull DC-DC converter topology allows isolated multiple outputs, step-up/step-down or inverted outputs, easier filtering on the input and the output, and lower overall noise.

Isolated Power for PCMCIA Applications

Medical instrumentation, modems, and LAN-interface cards often require isolated power supplies. One of the best switching-regulator topologies for this application is the push/pull forward-converting DC-DC power supply shown in Figures 3 and 4. Because the transformer works in the forward mode (rather than the flyback mode), its core does not store energy and, therefore, can be small. Input and output capacitors can be small because of the high-frequency and continuous-current waveforms.

Isolated Transformer Driver for PCMCIA Applications

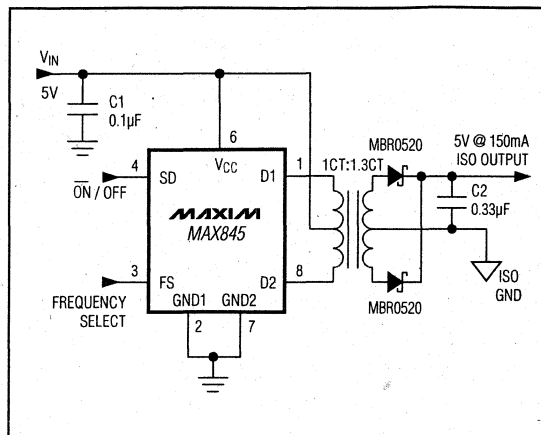


Figure 3. 5V to Isolated 5V Application Circuit

The MAX845 is a versatile transformer driver, capable of driving a center-tapped transformer primary from a 5V or 3.3V DC power supply (Figures 3 and 4). The secondary can be wound to provide any isolated voltage needed at power levels up to 750mW with a 5V supply or up to 500mW with a 3.3V supply. Figure 3 shows a typical 5V to isolated 5V application circuit that delivers up to 150mA of isolated 5V power.

3.3V Supply

Any of the application circuits shown may be converted to 3.3V operation by changing the turns ratio of the transformer and operating the MAX845 from a boost supply, as shown in Figure 4. In normal operation, whenever one of the MAX845 outputs goes low, the other goes to approximately double the supply voltage. Since the circuit is symmetrical, the two outputs can be combined with diodes, lightly filtered, then used to power the MAX845, and possibly other light loads as well.

The diodes on the primary side may be any fast-switching small-signal diodes, such as the 1N914, 1N4148, or CMPD2838. The value of the primary filter capacitor is not critical and can be very small, since it only needs to supply current to the MAX845 during the break-before-make interval.

The transformer could be any of the same ones used for 5V operation, but for optimum performance it should have fewer primary turns, as the ET product required is now only 3.3V-µs. For a given power level, the currents

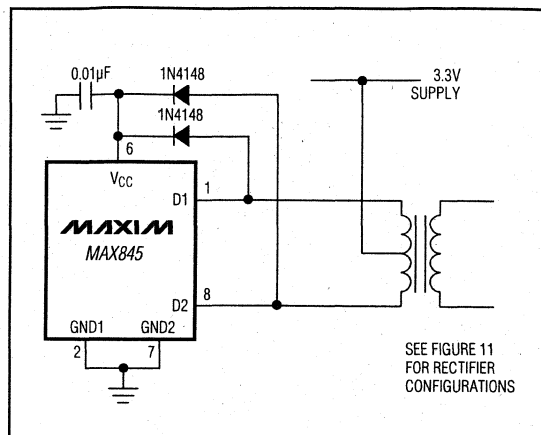


Figure 4. 3.3V Input to Isolated Output Application Circuit

will be higher at 3.3V, so transformer winding resistance will be more critical and efficiencies will be lower. The MAX845 output current must still be limited to 200mA (see *Absolute Maximum Ratings*), so the available output power will be less than with a 5V power source.

Low-Noise Power Supply

The MAX845 topology is inherently low noise, in that either one or the other of the two power devices is on at any given time. By alternating between two identical states with one side on and the other off, the input current is nearly constant and secondary output power is available at all times. There is an intentional break-before-make action to prevent any possibility of both power switches conducting at the same time. During this 100ns non-overlap interval, the input current goes to zero. This adds a small high-frequency component to the input current waveform. This ripple current can easily be absorbed by a small input bypass capacitor (0.33µF) from VCC to ground. Figure 5 shows a low-noise bias supply using the MAX845 transformer driver.

When using the two-diode push-pull (Figure 11a) rectifier or the four-diode bridge (Figure 11b), the output voltage tends to be more constant than in most alternative topologies. As described above, the circuit alternates between two identical states that both provide power to the load. The only part of the cycle that produces output ripple is the 100ns non-overlap interval, which can easily be filtered by a small ceramic output capacitor (0.33µF).

Isolated Transformer Driver for PCMCIA Applications

MAX845

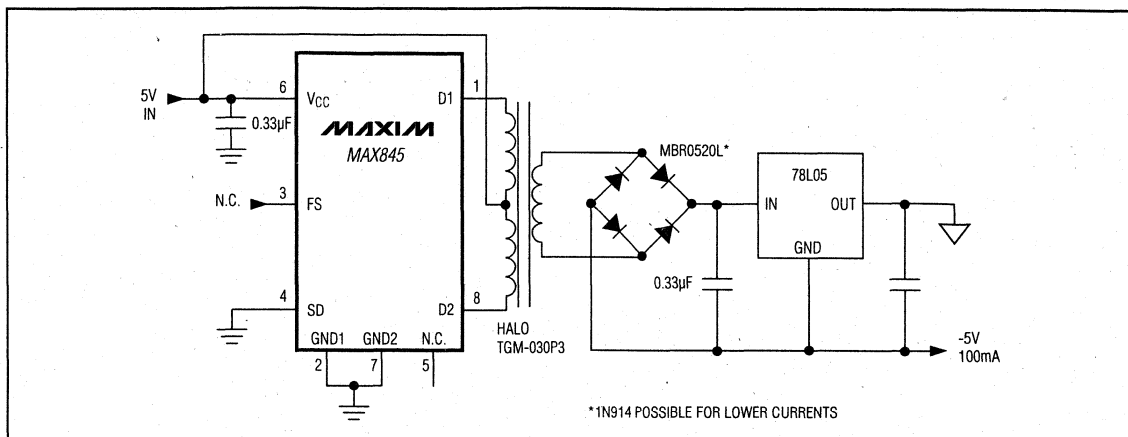


Figure 5. Low-Noise Supply

Isolated Data Conversion

Almost any serial-interface device is a candidate for operation across an isolation barrier; Figure 6 illustrates one example. The MAX176 analog-to-digital converter (ADC) operates from +5V and -12V supplies, provided by the multiple-tapped secondary and linear regulators. This circuit easily supplies several hundred milliwatts of additional isolated power for signal conditioning, multiplexing, or sensors. A +12V supply can be generated by adding two more diodes from the ends of the secondary, and a -5V supply can be generated by connecting additional diodes to the $\frac{1}{4}$ and $\frac{3}{4}$ tap points on the secondary. The MAX845 supplies sufficient power for almost any Maxim ADC.

Telephone-Subscriber-Line Power Supply

The standard telephone system is placed in the "off hook" state by placing a load on the line to signal the central office that service is requested. Normally, most of this power is wasted in a load resistor, but some systems can benefit from utilizing this free power. Figure 7 shows one way to transform the wasted telephone power to an isolated, regulated 5V at currents up to 50mA.

Because the telephone line is a high-impedance source, there can be a start-up problem with any DC-to-DC converter; when the line voltage is low during start-up, the frequency can be too low for the transformer, causing it to saturate. This excess saturation current can keep the voltage from climbing to normal operating levels. Thus the purpose of Q1, Q2, and the associated resistors is to ensure that the MAX845

remains in the shutdown mode until the voltage is high enough to allow proper operation.

Isolated 4mA to 20mA Analog Interface

The 4mA to 20mA current loop is widely used in the process-control industry for transducer and actuator control signals. These signals are commonly referred to a distant ground that may be at a considerably higher voltage with respect to the local ground. The circuit in Figure 8 generates an isolated 4mA to 20mA current from a 5V supply.

Isolated RS-485 Data Interface

The MAX845 power-supply transformer driver also provides isolated power for RS-485 data-interface applications. The application circuit of Figure 9 combines the MAX845 with a low-dropout linear regulator, a transformer, several high-speed optocouplers, and a Maxim RS-485 interface device.

Isolated RS-232 Data Interface

The MAX845 is ideal for isolated RS-232 data-interface applications requiring more than four transceivers. Its 750mW output power capability enables it to drive 10 transceivers simultaneously. Figure 10 shows the typical application circuit for a complete 120kbps isolated RS-232 data interface. This figure also shows how the Sharp PC417 optocouplers can be replaced by the lower-cost Quality Technologies 4N25 devices to achieve data transfer rates up to 19.2kbps.

4

Isolated Transformer Driver for PCMCIA Applications

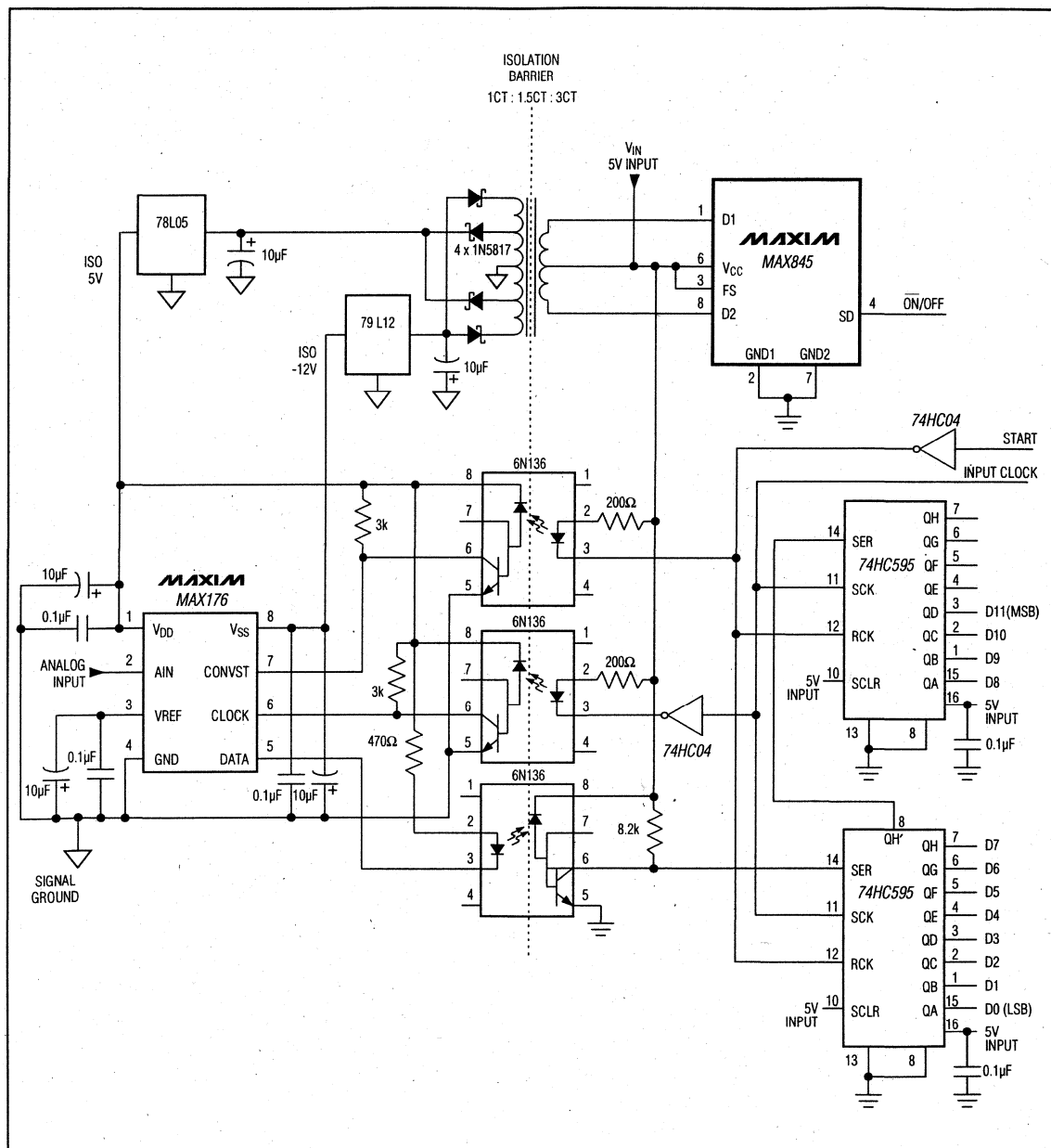


Figure 6. Typical Isolated Data-Conversion Application

Isolated Transformer Driver for PCMCIA Applications

MAX845

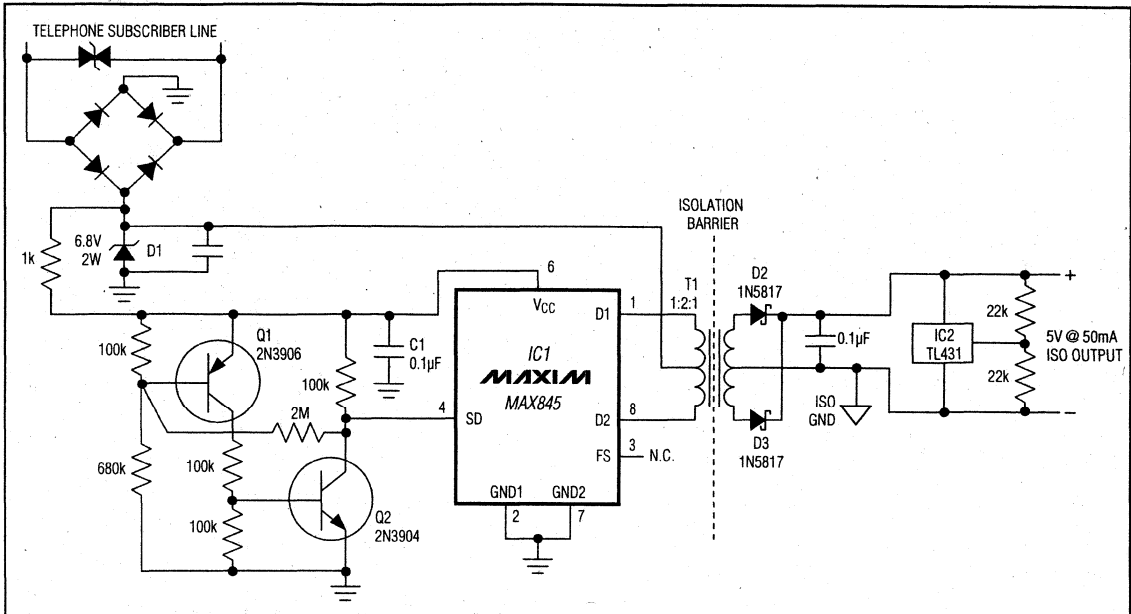


Figure 7. 5V from Telephone-Subscriber Line

4

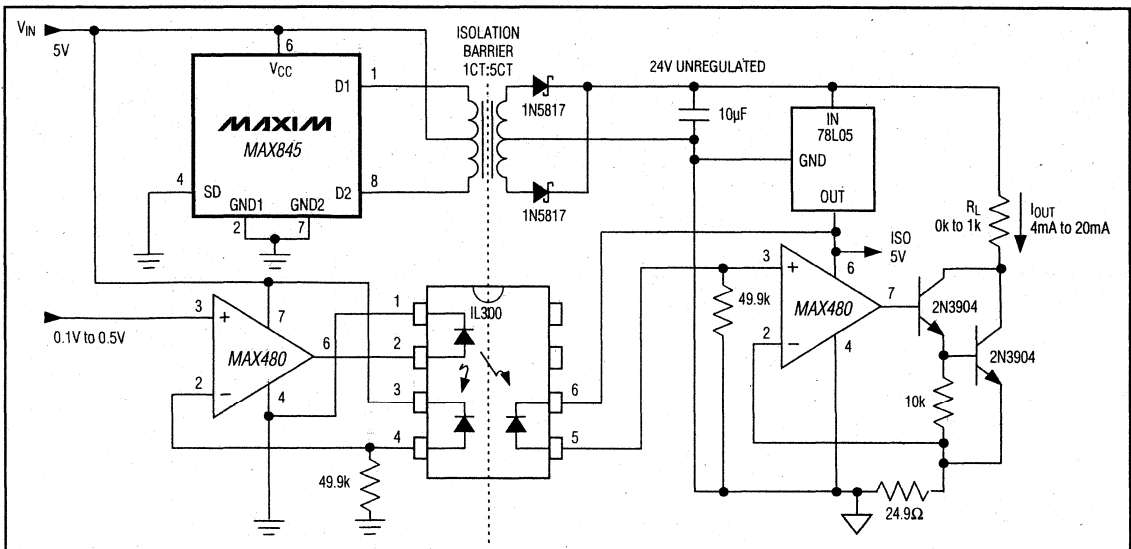


Figure 8. Typical 4mA/20mA Application Circuit

Isolated Transformer Driver for PCMCIA Applications

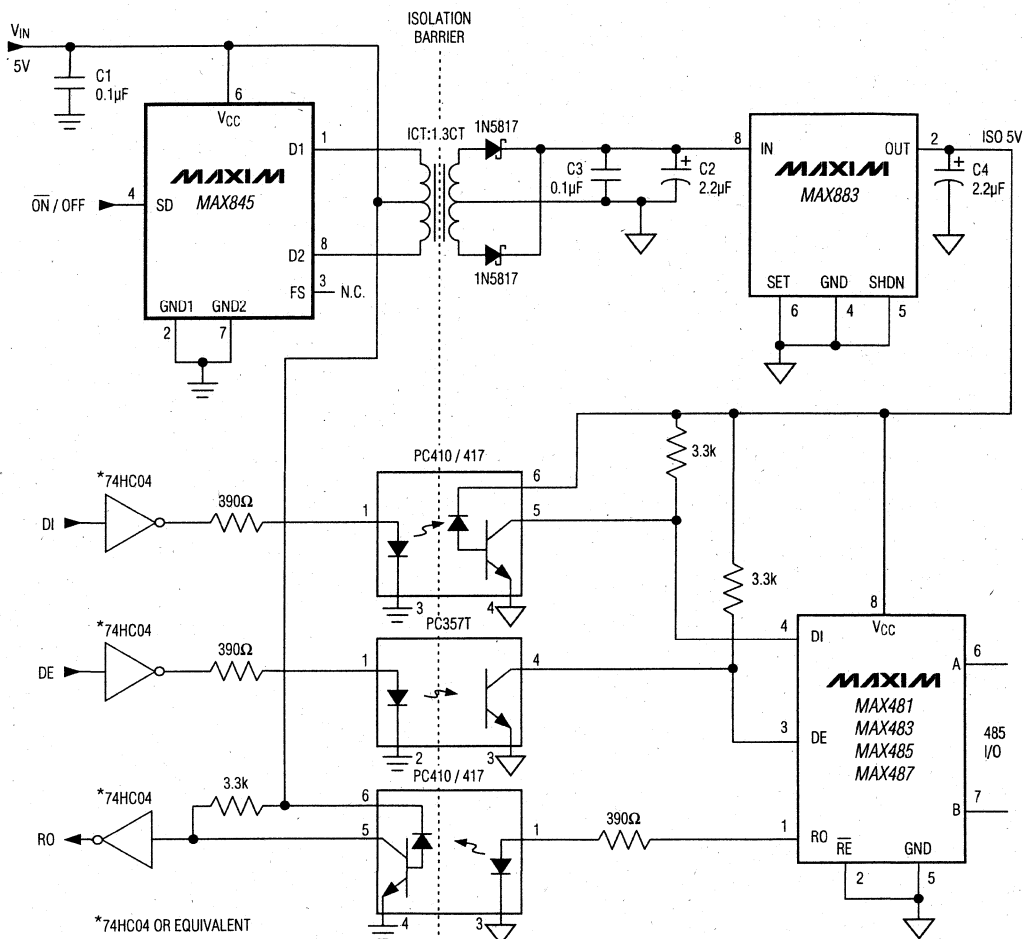


Figure 9. Typical RS-485 Application Circuit

Isolated Transformer Driver for PCMCIA Applications

MAX845

4

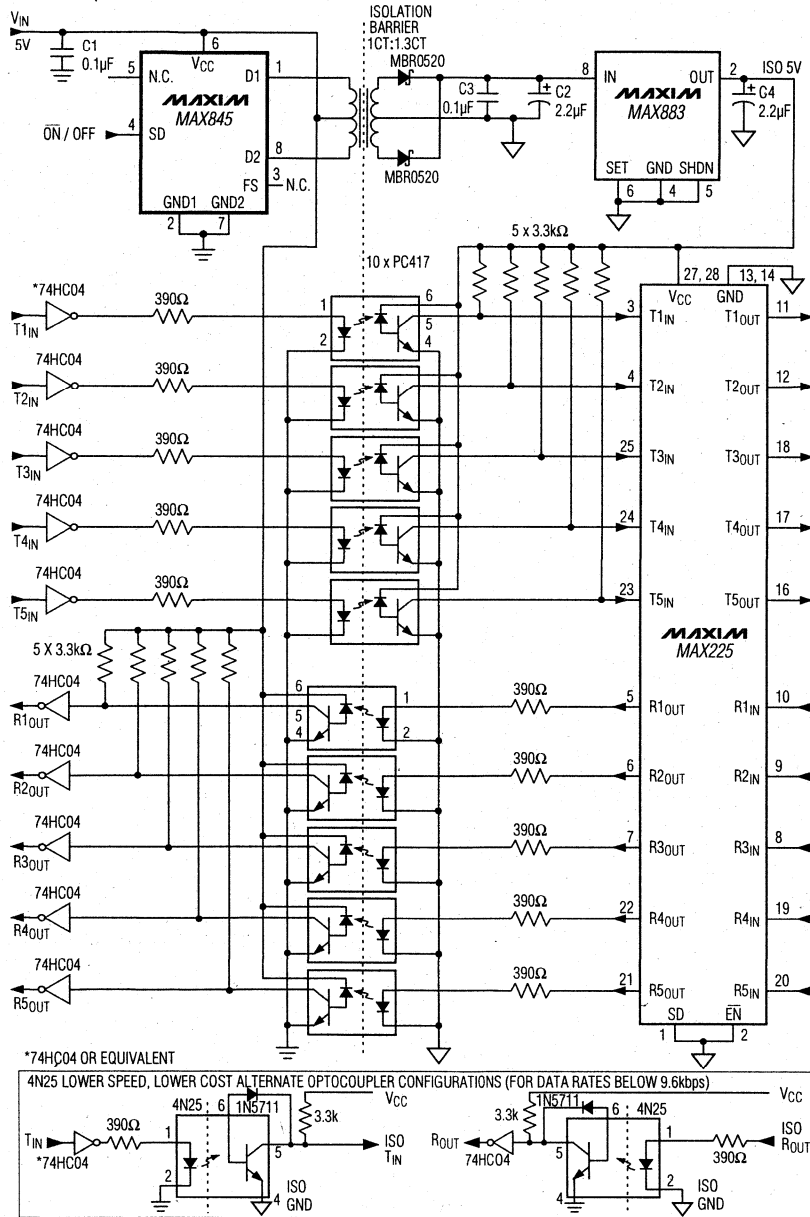


Figure 10. Typical RS-232 Application Circuit

Isolated Transformer Driver for PCMCIA Applications

Component Selection

Transformer

The MAX845 drives any transformer that has a center-tapped primary and a saturation rating of at least 5V- μ s (ET product) per side. The oscillator frequency varies linearly with V_{CC}. The transformer is most vulnerable to saturation at the minimum frequency, because the switches are on for the longest period. At V_{CC} = 4.5V, the transformer must withstand at least:

$$4.5V \times \frac{1}{450\text{kHz min}} \times \frac{1}{2} = 5V\text{-}\mu\text{s}$$

And at V_{CC} = 5.5V, the transformer must withstand at least:

$$5.5V \times \frac{1}{550\text{kHz min}} \times \frac{1}{2} = 5V\text{-}\mu\text{s}$$

Thus, the required ET product is constant over the entire 5V $\pm$ 10% range.

Select either a toroid or a gapped core. Although some applications will require custom transformers, many can make use of standard transformer designs such as those available from Halo Electronics and BH (see Table 1 for contact information). It is a good idea to approach the magnetics supplier early in the design cycle because, given a set of requirements, they can determine whether they have any suitable standard products, or they can help design a feasible custom product.

Table 1. Transformer and Transformer-Core Suppliers

TRANSFORMERS	TRANSFORMER CORES
CoilCraft Phone: (708) 639-6400 FAX: (708) 639-1469	Magnetics Inc. Phone: (412) 282-8282 FAX: (412) 282-6955
Halo Electronics Phone: (415) 969-7313 FAX: (415) 367-7158	Fair-Rite Products Phone: (914) 895-2055 FAX: (914) 895-2629
TDK Corporation Phone: (408) 437-9585 FAX: (408) 437-9591	Philips Components Phone: (401) 762-3800 FAX: (401) 762-3805, ext. 324
BH Electronics Phone: (507) 532-3211 FAX: (507) 532-3705	MMG (Magnetic Materials Group) Phone: (201) 345-8900 FAX: (201) 345-1172
Sumida USA Phone: (708) 956-0666 FAX: (708) 956-0702	Amidon Associates Phone: (714) 850-4660 FAX: (714) 850-1163

An ungapped toroid core must never be allowed to saturate. An empirical way to measure a toroid's ET product is to wind 20 turns on the bare core and observe the current waveform on an oscilloscope while driving the winding with a function generator. Generate a 50% duty-cycle square wave at a test frequency of 500kHz, with no DC offset. Gradually increase the driving voltage until the waveform suddenly begins to draw more current. At this point, the core is saturating, so reduce the driving voltage until the core just barely stops saturating. The ET product indicated is simply the maximum voltage that can be applied without saturation, multiplied by 1 μ s (the time of half of the period of the input signal). Because the ET product varies linearly with the number of turns, this test winding can be scaled up or down to act as a suitable primary for that particular core.

A gapped core, such as a bobbin or drum core, is not limited by ET product, but rather by inductance and winding resistance. The primary inductance must be high enough to prevent excessive current flow under light-load conditions, yet low enough that it can be wound on the core. Good results can be achieved by using a primary inductance between 50 μ H and 200 μ H. Calculate the number of turns required by using the manufacturer's A_L (inductance per turn squared) value, or measure a test winding with an inductance meter. Inductance varies with the square of the number of turns.

While most MAX845 applications will use a toroid transformer for highest efficiency and lowest EMI, there may be applications that can utilize less expensive transformers, such as E, I, or U-shaped cores, magnetic bobbins, or etched windings on a printed circuit board. Table 1 lists some transformer and core suppliers who can assist with your magnetics design.

The secondary or secondaries can be scaled to produce whatever output is required for the application at hand, taking into account the rectifier topology to be used and the forward voltage loss of the diodes selected.

Step-by-Step Transformer Design Procedure

Before starting the design, determine the minimum and maximum output voltage requirement, the minimum and maximum load current, the physical size constraints, and the cost budget.

- 1) Select an appropriate core shape and material from core vendors' data sheets; trade-off EMI vs. space and cost. Since the MAX845's output waveform is a square wave, it is rich in harmonics, so choose a material with low losses at up to several MHz.

Isolated Transformer Driver for PCMCIA Applications

MAX845

- 2) Use a test winding to measure ET product (if using an ungapped toroid) and/or A_L value for the core.
- 3) Determine the number of turns required for the primary winding. For an ungapped toroid, ET product from center-tap to D1 must be at least 5V- μ s. Other core types must have sufficient inductance to limit D1 and D2 output current under minimum load conditions, and must not be allowed to saturate.
- 4) Select a rectifier topology based on performance requirements (ripple vs. loss, and space required for secondary winding). Refer to Table 2, Rectifier Topology Trade-Offs.
- 5) Work backwards from V_{OUT} requirements to determine the secondary to primary turns ratio. Include losses in the rectifier diodes, and estimate resistive losses in the windings. For load currents exceeding 150mA, use a voltage step-down transformer to step up the output current from the MAX845. Do not exceed the MAX845's absolute maximum output current rating (200mA).
- 6) Wind the transformer with the largest diameter wire that will fit the winding area. Select a wire gauge to fill the winding aperture as much as possible. Larger diameter wire has lower resistance per unit length. Doubling the wire diameter reduces resistive losses by a factor of four.

Bobbin or drum cores suffer from low coupling between windings. This usually requires bifilar winding for the two halves of the primary.

Due to the inherent complexity of magnetic circuit design, it will be necessary to build a prototype and re-iterate the design. If necessary, adjust the design by altering the number of primary or secondary turns, or the wire gauge. If using a different core material or geometry, evaluate its ET product or A_L as described above.

Rectifier Topology

Figure 11 shows various rectifier topologies. Refer to Table 2 for selection criteria. The turns ratio of the transformer must be set to provide the minimum required output voltage at the maximum anticipated load, with the minimum expected input voltage. In addition, the calculations should allow for worst-case losses in the rectifiers. Since the turns ratio determined in this manner will ordinarily produce a much higher voltage at the secondary under conditions of high input voltage and/or light loading, be careful to prevent an overvoltage condition from occurring (see the Output Voltage vs. Load Current graph in the *Typical Operating Characteristics*).

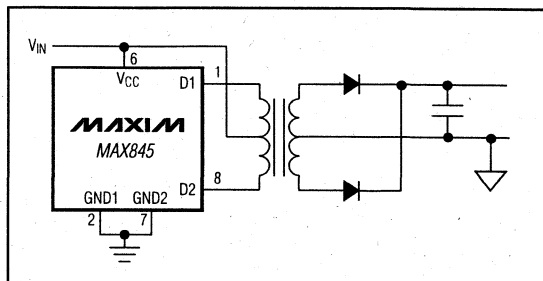


Figure 11a. 2-Diode Push-Pull

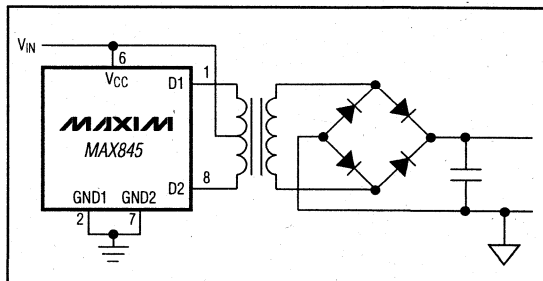


Figure 11b. 4-Diode Bridge

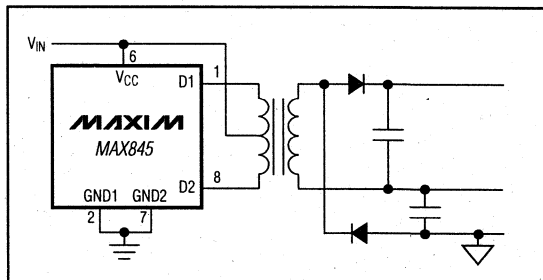


Figure 11c. Voltage Doubler

Diodes

Use fast-switching diode rectifiers. Ordinary silicon signal diodes like the 1N914 or 1N4148 may be used for low output current levels (less than 50mA), but Schottky diodes have a lower forward voltage drop and should be used for higher-current applications. Central Semiconductor has low-current Schottky diodes as duals in SOT-23 packages (CMPSH-3 series). The Nihon SB05W05C is a common-cathode dual in a SOT-23; it works well in the two-diode full-wave configuration. The Motorola MBR0520 is an excellent choice for all configurations.

Isolated Transformer Driver for PCMCIA Applications

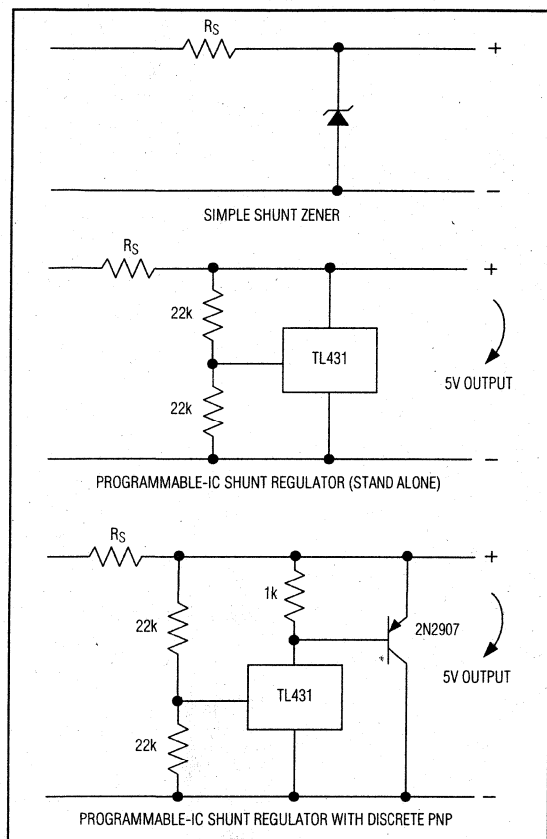


Figure 12. Shunt-Regulator Circuits

Output Regulator

Since the output voltage is not regulated against changes in the input voltage or load current, an output voltage regulator may be needed. A series linear regulator gives good performance and reasonably good efficiency at low cost. A shunt regulator costs less, occupies less space, and gives adequate performance for some applications.

Series regulators such as the MAX666, MAX667, MAX882/MAX883/MAX884, or MAX603/MAX604 simplify designs. Just select one with the desired output voltage and current capability, and connect it.

The simplest voltage regulator is the shunt zener shown in Figure 12. The series resistor (R_S) value should be as high as possible to still deliver the maximum expected load current with minimum input voltage. Be sure that no ratings are exceeded at maximum input voltage and minimum load current conditions; under such conditions, the zener diode may have to dissipate much more power than the load. Alternatively, start with the maximum allowable zener dissipation and select the series resistor under light-load, high-line conditions. Then verify that there is sufficient output current available with worst-case low input voltage.

For better regulation than the simple shunt zener, consider a shunt regulator IC such as the TL431. This device behaves like a zener diode whose voltage can be programmed by a resistor ratio. It can be used as a stand-alone device or can be boosted above its 150mA maximum rating without compromising its accuracy by adding a discrete PNP transistor, as shown in Figure 12.

The input power of a shunt regulator is nearly independent of load, so efficiency at light loads tends to be worse than it would be with a series regulator.

Output Filter Capacitor

Ceramic capacitors can be used as output capacitors because of the lower level of output ripple current. In applications where output ripple is not critical, a 0.33 μ F chip or ceramic capacitor is normally sufficient. Refer to Table 3 for suggested capacitor suppliers.

In applications sensitive to output-ripple noise, the output filter capacitor (C_2) should have a low equivalent series resistance (ESR) and a low equivalent series inductance (ESL), and its capacitance should remain fairly constant over temperature.

Sprague 595D surface-mount solid tantalum capacitors and Sanyo OS-CON through-hole capacitors are recommended, if space allows, due to their extremely low ESR. Capacitor ESR usually rises at low temperatures, but OS-CON capacitors provide very low ESR below 0°C.

Input Bypass Capacitor

The input bypass capacitor (C_1) is not critical. Unlike switching regulators, the MAX845's supply current is fairly constant, and is therefore less dependent on the input bypass capacitor. A low-cost 0.33 μ F chip or ceramic capacitor is normally sufficient for input bypassing.

Isolated Transformer Driver for PCMCIA Applications

Table 2. Rectifier Topology Trade-Offs

TOPOLOGY	ADVANTAGE	DISADVANTAGE
2-Diode Push/Pull (Figure 11a)	• Only 3 external components • Low output ripple • Single diode drop	• More turns on transformer
4-Diode Bridge (Figure 11b)	• Simpler transformer winding requirements • Low output ripple	• 5 external components • Higher cost • 2 diode drops
Voltage Doubler (Figure 11c)	• Fewest turns on transformer	• 4 external components • Higher output ripple • 2 diode drops

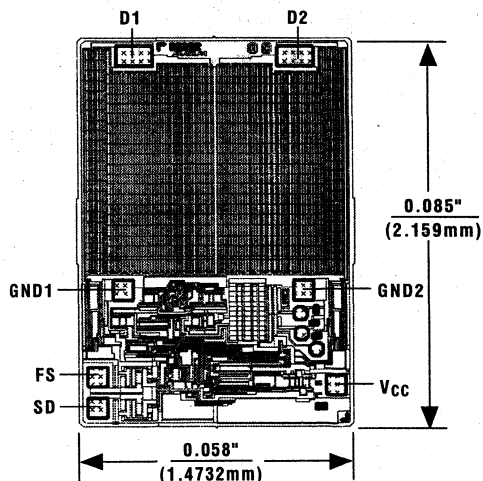
Table 3. Suggested Capacitor Suppliers

CAPACITOR	SUPPLIER
Low-ESR 267 Series	Matsuo USA Phone: (714) 969-2491 FAX: (714) 960-6492
Ceramic	Murata Erie USA Phone: (800) 831-9172 FAX: (404) 436-3030
Very Low-ESR 595D/293D Series	Sprague Electric Co. USA Phone: (603) 224-1961 FAX: (603) 224-1430

MAX845

Chip Topography

4



SUBSTRATE CONNECTED TO V_{CC}
TRANSISTOR COUNT: 31

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/95

MAXIM

1 to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

General Description

The MAX848/MAX849 boost converters set a new standard of high efficiency and high integration for noise-sensitive power-supply applications, such as portable phones and small systems with RF data links. The heart of these devices is a synchronous boost-topology regulator that generates a fixed 3.3V output (or 2.7V to 5V adjustable output) from one to three NiCd/NiMH cells or one lithium-ion cell.

Synchronous rectification provides a 5% efficiency improvement over similar non-synchronous boost regulators. In standby mode, pulse-skipping PFM operation keeps the output voltage alive with only 150 μ W quiescent power consumption. Fixed-frequency PWM operation ensures that the switching noise spectrum is confined to the 300kHz fundamental and its harmonics, allowing easy post-filtering noise reduction. Synchronizing to a 200kHz to 400kHz external clock will achieve even tighter noise-spectrum control.

Battery monitoring is provided by a 2-channel voltage-to-frequency type A/D converter. One channel is internally connected to the battery input, while the other channel is brought out for monitoring external voltages (AIN pin).

A latch is included for push-on/push-off control via a momentary pushbutton switch; otherwise, start-up can be automatic with battery installation. Upon power-up, an internal comparator monitors the output voltage to generate a power-good output (PWROK).

These two devices are identical, except for their low-side, N-channel MOSFET power switches: 0.5A for the MAX848, 1A for the MAX849.

Applications

Digital Cordless Phones
PCS Phones
Hand-Held Instruments
Palmtop Computers
Personal Communicators
Local 3.3V to 5V Supplies

Features

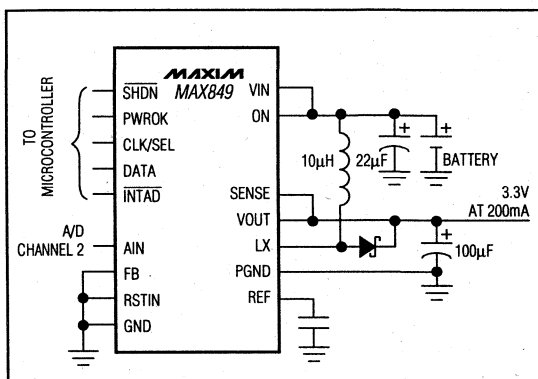
- ♦ 90% Efficiency from 1.1V Input
- ♦ Guaranteed 200mA Output from 1.1V Input (MAX849), (100mA for MAX848)
- ♦ Regulated 3.3V or Adjustable Output (2.7V to 5V)
- ♦ 0.8V to 5V Input Range
- ♦ Low-Power (0.15mW) Standby Mode
- ♦ Low-Noise Constant-Frequency Mode (300kHz)
- ♦ Synchronizable Switching Frequency (200kHz to 400kHz)
- ♦ 2-Channel A/D Converter with Serial Output
- ♦ Power-Good Function
- ♦ Integrated On/Off Functions

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX848CSE	0°C to +70°C	16 Narrow SO
MAX848C/D	0°C to +70°C	Dice*
MAX848ESE	-40°C to +85°C	16 Narrow SO
MAX849CSE	0°C to +70°C	16 Narrow SO
MAX849C/D	0°C to +70°C	Dice*
MAX849ESE	-40°C to +85°C	16 Narrow SO

*Contact factory for dice specifications.

Typical Operating Circuit



MAXIM

Maxim Integrated Products 4-173

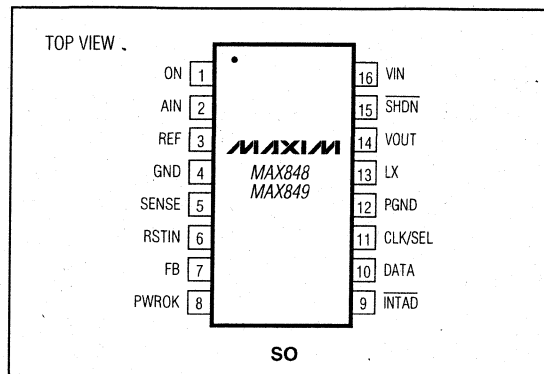
Call toll free 1-800-998-8800 for free samples or literature.

MAX848/MAX849

4

1 to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

EVALUATION KIT WILL BE AVAILABLE

MAXIM Dual, PFM, Step-Up DC-DC Controller

MAX863

General Description

The MAX863 dual-output DC-DC converter contains two independent, high-efficiency, current-limited PFM (pulse-frequency-modulated) boost controllers integrated on one space-saving circuit. It accepts inputs down to 1.5V and is intended for use in small, hand-held equipment powered from two or three battery cells or one lithium ion cell. The MAX863 comes in a miniature 16-pin QSOP that fits in the same area as a standard 8-pin SO.

Each output can be set to any boosted voltage using two external resistors. One of the outputs also uses the Dual-Mode™ feature, which allows a 3.3V or 5V output. Both controllers drive inexpensive, external N-channel MOSFETs at up to 300kHz, permitting small external components.

The MAX863 extends battery life with 82% efficiency over a 20mA to 1A output range. It also saves battery life with a low 65µA (max) quiescent supply current, even when both supplies are on. A separate logic-controlled shutdown for each converter allows power-management flexibility and decreases supply current to just 1µA (max).

Other features include soft-start to prevent surge currents when powering up, and a built-in LBI/LBO low-battery detector. The MAX863 evaluation kit (MAX863 EVKIT-SO) is available to assist with designs. For a single-output controller, refer to the MAX1771 data sheet.

Applications

2 or 3 Cell Portable Equipment
Organizers, PDAs, and Palmtops
Dual 3.3V/5V Logic and Positive LCD Supply
Flash Memory Programmers
Split 3.3V Logic and 5V Memory Systems

Features

- ◆ Smallest Dual Boost Controller
- ◆ 16-Pin QSOP Fits in 8-Pin SO Area
- ◆ High Efficiency (>80% from 20mA to 1A)
- ◆ 65µA (max) Quiescent Supply Current
- ◆ 1µA (max) Shutdown Current
- ◆ LBI/LBO Low-Battery Detector
- ◆ Drives Surface-Mount, Dual N-Channel FET
- ◆ 2 or 3 NiCd/NiMH Cell or 1 Lithium Cell Operation
- ◆ Also Configurable as Step-Up/Down Controller

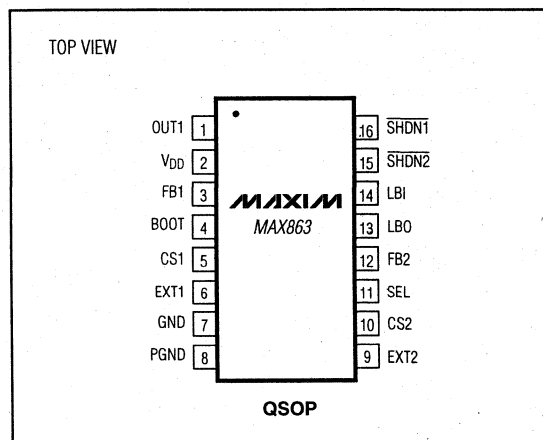
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX863C/D	0°C to +70°C	Dice*
MAX863IKE	-25°C to +85°C	16 QSOP
MAX863EKE	-40°C to +85°C	16 QSOP

*Dice are tested at $T_A = +25^\circ\text{C}$.

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Pin Configuration



Dual Mode is a trademark of Maxim Integrated Products.

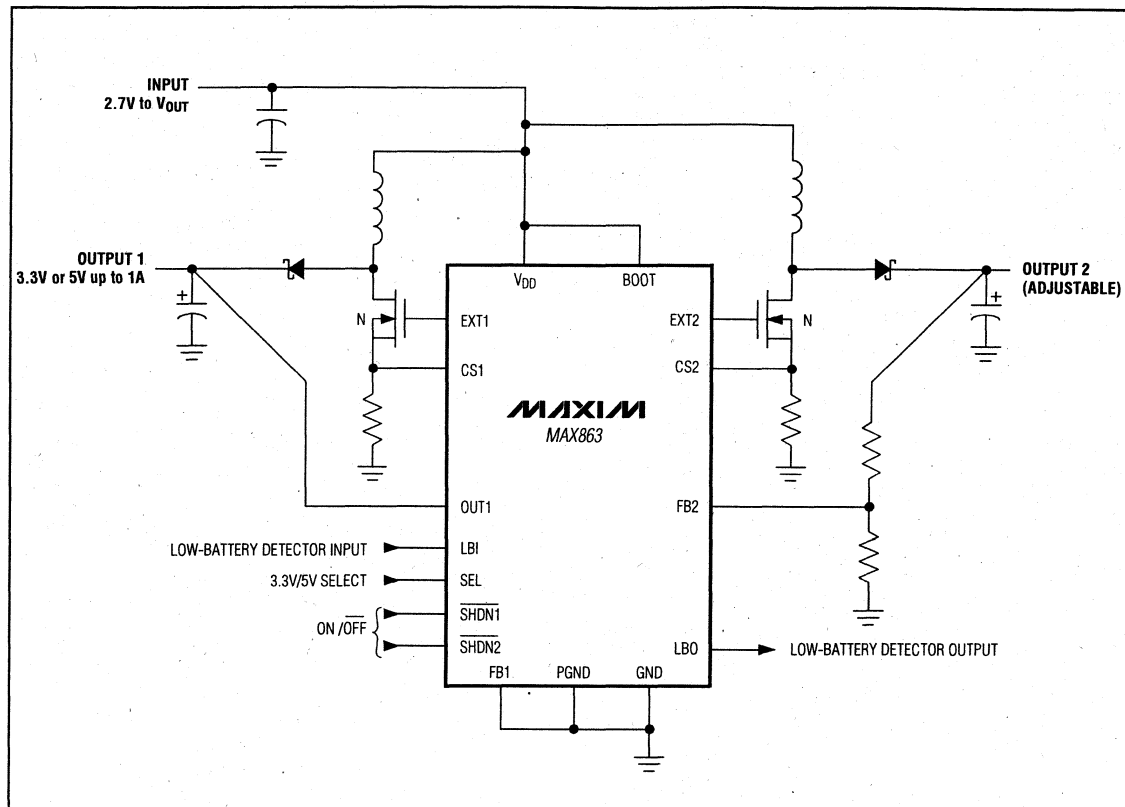
MAXIM

Maxim Integrated Products 4-175

Call toll free 1-800-998-8800 for free samples or literature.

Dual, PFM, Step-Up DC-DC Controller

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter with Shutdown

General Description

The MAX864 is a dual-output charge-pump voltage converter that doubles and inverts the input voltage to provide split-supply outputs. It can be used when a single positive supply is available and both positive and negative voltages are required. Common applications include the generation of $\pm 6V$ from a 3V battery, and the generation of $\pm 10V$ from the standard +5V logic supply used with analog circuits.

Switching frequency is pin selectable from 5kHz to 200kHz, allowing a trade-off between quiescent supply current (200 μA at 5kHz) and capacitor size (1 μF at 200kHz). The output source impedance is typically 75 Ω from the positive output and 38 Ω from the negative output, providing over 10mA of output current.

Other features include a logic-controlled shutdown pin that reduces supply current to less than 1 μA , and a space-saving 16-pin QSOP package that fits in the same area as a standard 8-pin SO.

For a similar product in a smaller μMAX package, refer to the MAX865 data sheet.

Applications

- Small LCD Panels
- Handy-Terminals
- Serial-Interface Circuits
- Negative Voltage Generator in 2V and 3V Systems
- Dual Supply for Cellular Phones: Negative GaAsFET and Positive LCD Bias
- Split-Supply Op-Amp Power for Low-Voltage, Single-Supply Systems
- PDA's
- Organizers

Ordering Information

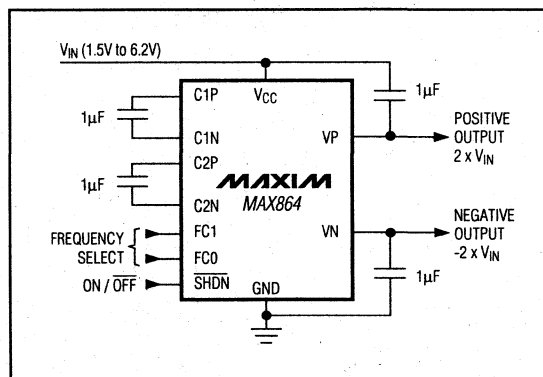
PART	TEMP. RANGE	PIN-PACKAGE
MAX864C/D	0°C to +70°C	Dice*
MAX864EKE	-40°C to +85°C	16 QSOP

* Dice are specified at $T_A = +25^\circ C$.

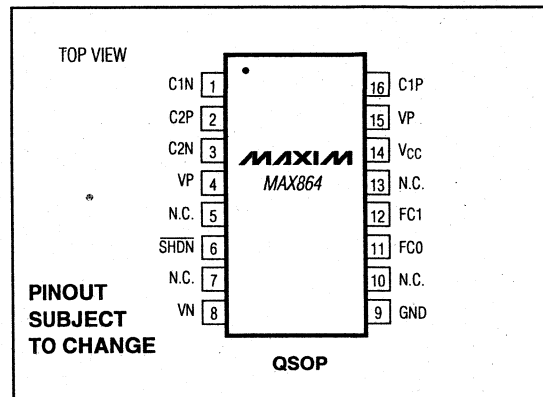
Features

- ◆ Requires Only Four 1 μF Capacitors
- ◆ $\pm 6V$ from +3V Input (dual outputs)
- ◆ 1.5V to 6.2V Input Voltage Range
- ◆ 5kHz, 30kHz, 100kHz, or 200kHz Pin-Selectable Switching Frequency
- ◆ Shutdown Pin ($I_Q = 1\mu A$ max)
- ◆ 16-Pin QSOP Package (same size as 8-pin SO)
- ◆ 10mA Output Current

Typical Operating Circuit



Pin Configuration



MAX864

4

MAXIM

Maxim Integrated Products 4-177

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter

General Description

The MAX865 is a dual-output charge-pump voltage converter that doubles and inverts the input voltage to provide split-supply outputs. It can be used when a single positive supply is available and both positive and negative voltages are required. Common applications include generating $\pm 6V$ from a 3V battery, and generating $\pm 10V$ from the standard +5V logic supply used with analog circuits.

The MAX865 comes in a space-saving μ MAX package that is only 1.1mm high. Its 30kHz switching frequency allows for small external capacitors. The output impedance is typically 150Ω from the positive output and 75Ω from the negative output, providing up to 10mA of output current.

For a similar product with an adjustable switching frequency and shutdown capability, refer to the MAX864 data sheet.

Applications

Negative Voltage Generator in 2V and 3V Systems
Small LCD Panels
Dual Supply for Cellular Phones: Negative GaAsFET and Positive LCD Bias
Split-Supply Op-Amp Power for Low-Voltage, Single-Supply Systems
Handy-Terminals
PDAs
Organizers
Serial-Interface Circuits

Features

- ◆ Requires Only Four 3.3 μ F Capacitors
- ◆ 1.1mm High μ MAX Package
- ◆ $\pm 6V$ from +3V Input (dual outputs)
- ◆ 1.5V to 6.2V Input Voltage Range
- ◆ 30kHz Switching Frequency
- ◆ 10mA Output Current

MAX865

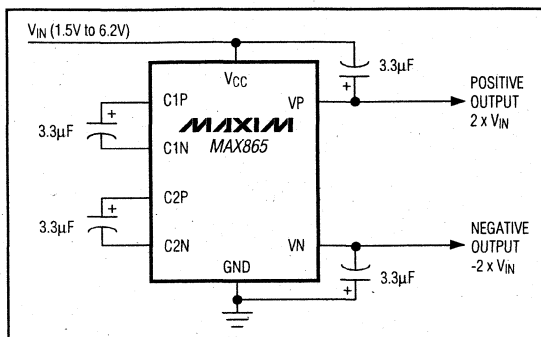
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX865C/D	0°C to +70°C	Dice*
MAX865EUA	-40°C to +85°C	8 μ MAX

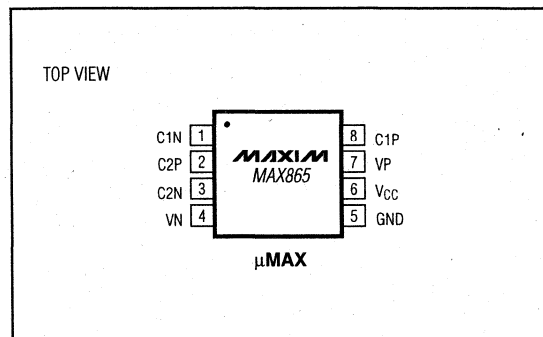
* Dice are tested at $T_A = +25^\circ C$.

4

Typical Operating Circuit



Pin Configuration



MAXIM

Maxim Integrated Products 4-179

Call toll free 1-800-998-8800 for free samples or literature.



3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

General Description

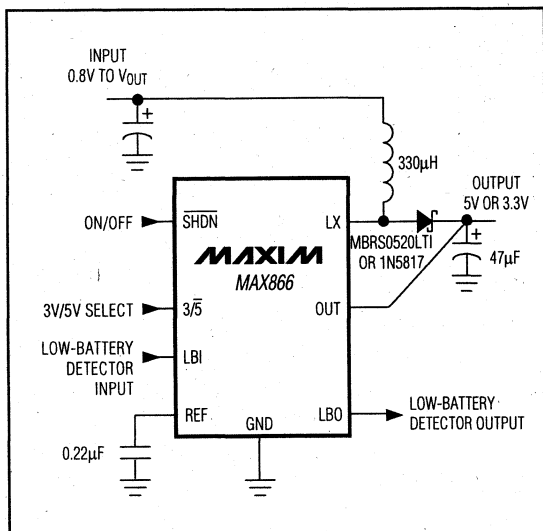
The MAX866 and MAX867 are ultra-small, high-efficiency, CMOS, step-up, DC-DC switching regulators for 1-cell battery-powered systems. The MAX866 accepts a positive input voltage between 0.8V and V_{OUT} and converts it to a higher, pin-selectable output voltage of 3.3V or 5V. The MAX867 adjustable version accepts 0.8V to 6.0V input voltages and generates a higher adjustable output voltage in the 2.7V to 6.0V range. Typical efficiencies are greater than 80%. Typical no-load supply current is 100 μ A (1 μ A in shutdown).

The MAX866/MAX867 combine ultra-low quiescent supply current and high efficiency to give maximum battery life. Its high switching frequency permits the use of small, low-cost inductors and capacitors. Additionally, internal peak-current limiting protects the IC.

Applications

Pagers
Remote Controls
Detectors
1-Cell Battery-Operated Equipment
Backup Supplies

Typical Operating Circuit



Features

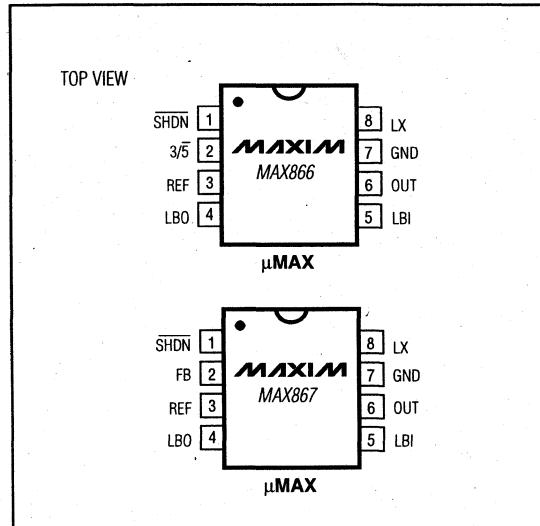
- ◆ 0.8V to 6.0V Input Supply Voltage
- ◆ 0.9V Guaranteed Start-Up Supply Voltage
- ◆ >80% Efficiency Over Wide Load Range
- ◆ 100 μ A No-Load Battery Current ($V_{OUT} = 3.3V$)
- ◆ 1 μ A Shutdown Mode
- ◆ Up to 250kHz Switching Frequency
- ◆ $\pm 1.5\%$ Reference Tolerance
- ◆ Low-Battery Detector (LBI/LBO)
- ◆ Ultra-Small 8-Pin μ MAX Package (1.11mm high)
- ◆ Circuit Fits in 0.2in²

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX866C/D	0°C to +70°C	Dice*
MAX866EUA	-40°C to +85°C	8 μ MAX
MAX867C/D	0°C to +70°C	Dice*
MAX867EUA	-40°C to +85°C	8 μ MAX

* Dice are tested at $T_A = +25^\circ\text{C}$ only.

Pin Configurations



3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (OUT to GND)	-0.3V, +7V
Switch Voltage (LX to GND)	-0.3V, +7V
SHDN, LBO to GND	-0.3V, +7V
LBI, REF, 3/5, FB to GND	-0.3V, (VOUT + 0.3V)
Reference Current (I _{REF})	2.5mA
Continuous Power Dissipation (T _A = +70°C)	
μMAX (derate 4.1mW/°C above +70°C)	330mW

Reverse Battery Current (T _A ≤ +45°C) (Note 1)	750mA
Operating Temperature Ranges	
MAX86_C/D	0°C to +70°C
MAX86_EUA	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: Reverse battery current is measured from the *Typical Operating Circuit*'s battery input terminal to GND when the battery is connected backwards. A reverse current of 750mA will not exceed the package dissipation limits but, if left for an extended time (more than ten minutes), may degrade performance.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 1.2V, I_{LOAD} = 0mA, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Supply Voltage				0.8	0.9	V
Output Voltage (Note 2)	0.9V ≤ V _{IN} ≤ 3V	MAX866, 3/5 = 0V, 0mA ≤ I _{LOAD} ≤ 6mA	4.80	5.0	5.20	V
		MAX866, 3/5 = 3V, 0mA ≤ I _{LOAD} ≤ 8mA	3.17	3.3	3.43	
		MAX867, V _{OUT} = 5V, 0mA ≤ I _{LOAD} ≤ 6mA	4.80	5.0	5.20	
	0.9V ≤ V _{IN} ≤ 3V, T _A = T _{MIN} TO T _{MAX} (Note 3)	MAX866, 3/5 = 0V, 0mA ≤ I _{LOAD} ≤ 6mA	4.75	5.0	5.25	
		MAX866, 3/5 = 3V, 0mA ≤ I _{LOAD} ≤ 8mA	3.13	3.3	3.47	
		MAX867, V _{OUT} = 5V, 0mA ≤ I _{LOAD} ≤ 6mA	4.75	5.0	5.25	
	1.2V ≤ V _{IN} ≤ 3V	MAX866, 3/5 = 0V, 0mA ≤ I _{LOAD} ≤ 10mA	4.80	5.0	5.20	
		MAX866, 3/5 = 3V, 0mA ≤ I _{LOAD} ≤ 15mA	3.17	3.3	3.43	
		MAX867, V _{OUT} = 5V, 0mA ≤ I _{LOAD} ≤ 10mA	4.80	5.0	5.20	
Maximum Load Current (Note 2)	0.9V ≤ V _{IN} ≤ 3V	MAX866, 3/5 = 0V, 4.8V ≤ V _{LOAD} ≤ 5.2V	6	9		mA
		MAX866, 3/5 = 3V, 3.17V ≤ V _{LOAD} ≤ 3.43V	8	13		
		MAX867, V _{OUT} = 5V, 4.8V ≤ V _{LOAD} ≤ 5.2V	6	9		
	1.2V ≤ V _{IN} ≤ 3V	MAX866, 3/5 = 0V, 4.8V ≤ V _{LOAD} ≤ 5.2V	10	15		
		MAX866, 3/5 = 3V, 3.17V ≤ V _{LOAD} ≤ 3.43V	15	23		
		MAX867, V _{OUT} = 5V, 4.8V ≤ V _{LOAD} ≤ 5.2V	10	15		
Quiescent Supply Current in 3.3V mode (Note 4)	I _{LOAD} = 0mA, 3/5 = 3V, LBI = 1.5V, V _{OUT} = 3.47V, FB = 1.5V			27	60	μA
No-Load Battery Current	Output set for 3.3V, measured at V _{IN} in Figure 2, V _{IN} = 1.5V			100		μA
Shutdown Quiescent Current (Note 4)	SHDN = 0V, 3/5 = 3V, LBI = 1.5V, V _{OUT} = 3.47V, FB = 1.5V				1	μA
Peak Inductor Current Limit				500		mA
Reference Voltage	No REF load		1.22	1.25	1.28	V
Reference Load Regulation	3/5 = 3V, -20μA ≤ REF load ≤ 250μA, C _{REF} = 0.22μF			0.8	2.0	%
LBI Input Threshold	With falling edge		1.22	1.25	1.28	V

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, $V_{IN} = 1.2V$, $I_{LOAD} = 0mA$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LBI Input Hysteresis			25		mV
LBO Output Voltage Low	$I_{SINK} = 2mA$, open-drain output			0.4	V
LBO Output Leakage Current	LBO = 5V			1	μA
SHDN, 3/5 Input Voltage Low				$0.08 \times V_{OUT}$	V
SHDN, 3/5 Input Voltage High				$0.32 \times V_{OUT}$	V
SHDN, 3/5, FB, LBI Input Current	LBI = 1.5V, FB = 1.5V, SHDN = 0V or 3V, 3/5 = 0V or 3V	± 40	± 100		nA
FB Voltage	MAX867, output in regulation	1.22	1.25	1.28	V
Output Voltage Range	MAX867	2.7		6.0	V

Note 2: Output current specified with circuit of Figure 2 and CoilCraft D01608-334 inductor for test purposes only. More (or less) output current can be supplied with other coil types depending on inductance value and coil resistance. See *Typical Operating Characteristics* for other coil types. Output voltage and output current are guaranteed over this V_{IN} operating range once the device has started up. Actual V_{IN} start-up voltage depends on load current.

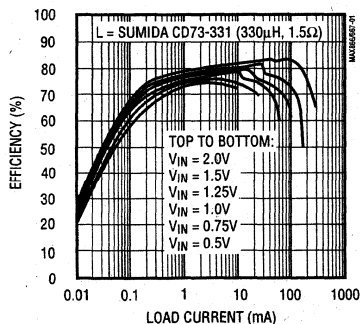
Note 3: Output voltage specifications over temperature are guaranteed by design to limits that are 6 sigma from either side of the mean.

Note 4: Current measured into OUT. V_{OUT} is forced to 3.47V to maintain LX off when measuring device current.

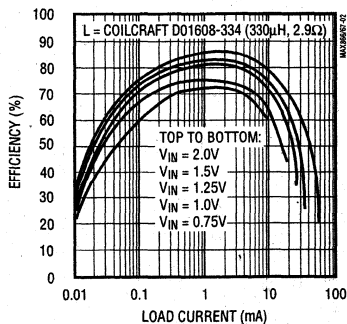
Typical Operating Characteristics

(Circuits of Figure 2, $T_A = +25^\circ C$, unless otherwise noted.)

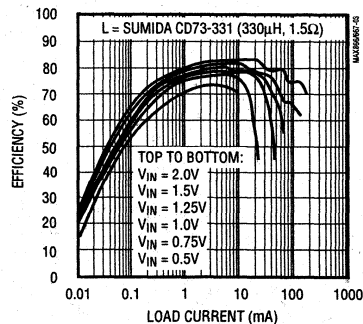
EFFICIENCY vs. LOAD CURRENT ($V_{OUT} = 3.3V$)



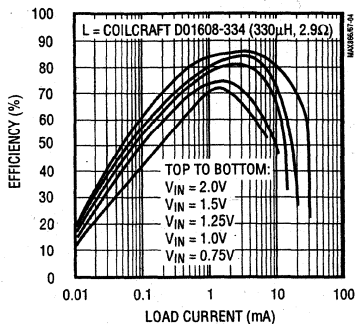
EFFICIENCY vs. LOAD CURRENT ($V_{OUT} = 3.3V$)



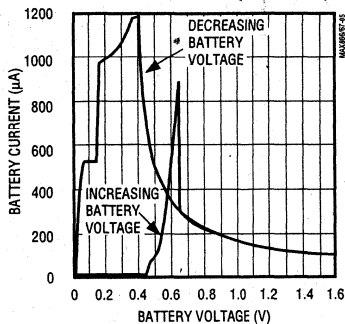
EFFICIENCY vs. LOAD CURRENT ($V_{OUT} = 5.0V$)



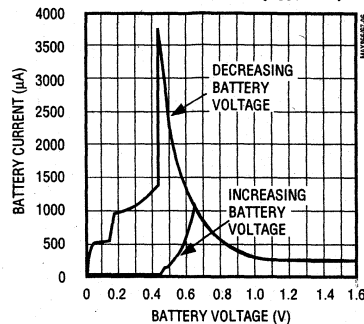
EFFICIENCY vs. LOAD CURRENT ($V_{OUT} = 5.0V$)



NO-LOAD BATTERY CURRENT vs. BATTERY VOLTAGE ($V_{OUT} = 3.3V$)



NO-LOAD BATTERY CURRENT vs. BATTERY VOLTAGE ($V_{OUT} = 5V$)

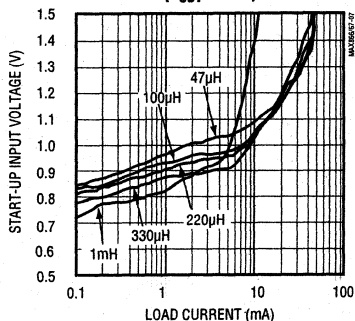


3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

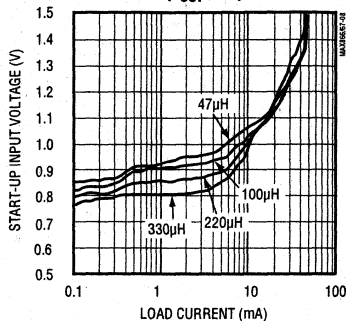
Typical Operating Characteristics (continued)

(Circuits of Figure 2, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

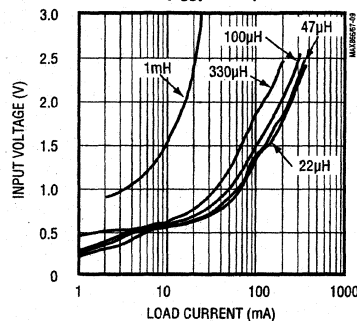
START-UP INPUT VOLTAGE vs. LOAD CURRENT
($V_{OUT} = 3.3\text{V}$)



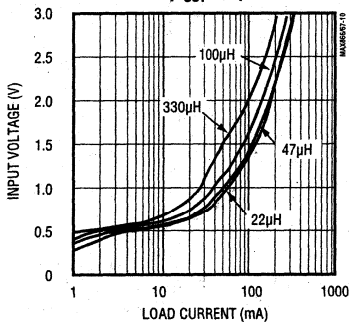
START-UP INPUT VOLTAGE vs. LOAD CURRENT
($V_{OUT} = 5\text{V}$)



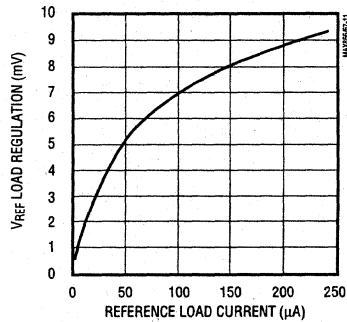
INPUT VOLTAGE vs. LOAD CURRENT
($V_{OUT} = 3.3\text{V}$)



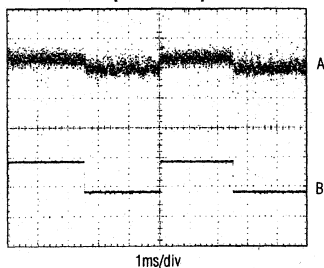
INPUT VOLTAGE vs. LOAD CURRENT
($V_{OUT} = 5\text{V}$)



REFERENCE VOLTAGE
vs. REFERENCE CURRENT

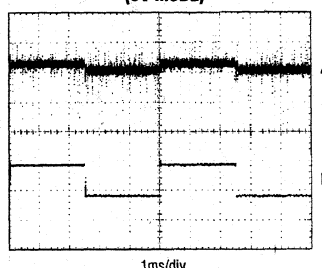


MAX866 LINE-TRANSIENT RESPONSE
(3.3V MODE)



A: 3.3V OUTPUT VOLTAGE, AC COUPLED 20mV/div
B: INPUT VOLTAGE (0.9V AND 1.4V) 500mV/div
 $I_{LOAD} = 10\text{mA}$, $C_{OUT} = 47\mu\text{F}$

MAX866 LINE-TRANSIENT RESPONSE
(5V MODE)



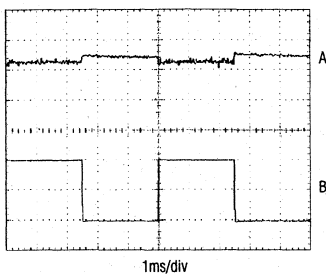
A: 5.0V OUTPUT VOLTAGE, AC COUPLED 20mV/div
B: INPUT VOLTAGE (0.9V AND 1.4V) 500mV/div
 $I_{LOAD} = 10\text{mA}$, $C_{OUT} = 47\mu\text{F}$

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

Typical Operating Characteristics (continued)

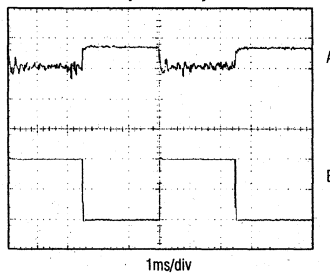
(Circuits of Figure 2, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX866 LOAD-TRANSIENT RESPONSE (3.3V MODE)



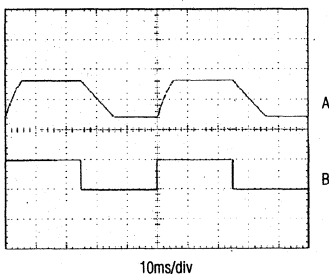
A: 3.3V OUTPUT VOLTAGE, AC COUPLED 20mV/div
B: OUTPUT CURRENT (0mA AND 10mA) 5mV/div
(TEKTRONIX P6042 CURRENT PROBE)
 $I_{LOAD} = 5\text{mA}$, $C_{OUT} = 47\mu\text{F}$, $V_{IN} = 1.25\text{V}$

MAX866 LOAD-TRANSIENT RESPONSE (5V MODE)



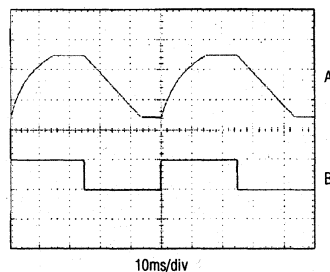
A: 5.0V OUTPUT VOLTAGE, AC COUPLED 20mV/div
B: OUTPUT CURRENT (0mA AND 10mA) 5mV/div
(TEKTRONIX P6042 CURRENT PROBE)
 $I_{LOAD} = 5\text{mA}$, $C_{OUT} = 47\mu\text{F}$, $V_{IN} = 1.25\text{V}$

MAX866 SHUTDOWN RESPONSE (3.3V MODE)



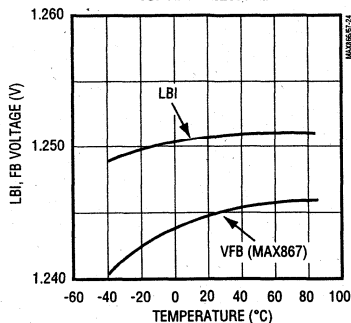
A: 3.3V OUTPUT VOLTAGE, 2V/div
B: SHDN INPUT VOLTAGE (0V AND 5V) 2V/div
 $I_{LOAD} = 10\text{mA}$

MAX866 SHUTDOWN RESPONSE (5V MODE)

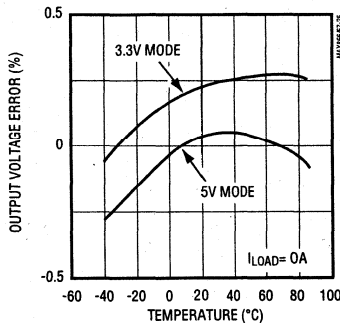


A: 5.0V OUTPUT VOLTAGE, 2V/div
B: SHDN INPUT VOLTAGE (0V AND 5V) 5V/div
 $I_{LOAD} = 10\text{mA}$

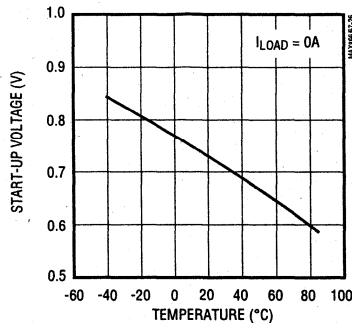
MAX867 LBI AND FB THRESHOLD vs. TEMPERATURE



MAX866 OUTPUT VOLTAGE ERROR vs. TEMPERATURE



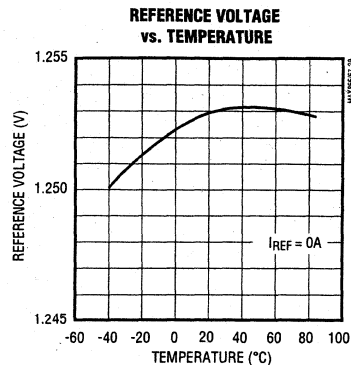
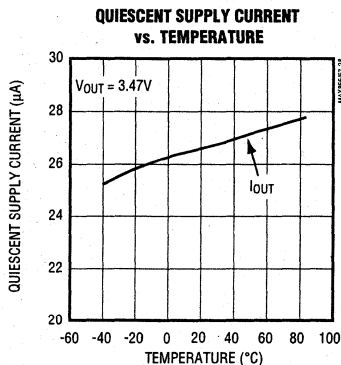
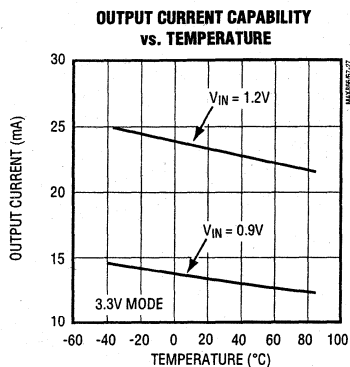
START-UP VOLTAGE vs. TEMPERATURE



3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

Typical Operating Characteristics (continued)

(Circuits of Figure 2, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
MAX866	MAX867		
1	1	SHDN	Shutdown Input. When low, the entire circuit is off and $V_{OUT} = V_{IN} - V_D$, where V_D is the forward voltage drop of the external Schottky rectifier.
2	—	3/5	Selects the output voltage; connect to GND for 5V output, and to OUT for 3.3V output.
—	2	FB	Feedback Input for adjustable-output operation. Connect to an external resistor voltage divider between OUT and GND.
3	3	REF	1.25V Reference Voltage Output. Bypass with 0.22µF to GND (0.1µF if there is no external reference load). Maximum load capability is 250µA source, 20µA sink.
4	4	LBO	Low-Battery Output. An open-drain N-channel MOSFET sinks current when the voltage at LBI drops below 1.25V.
5	5	LBI	Low-Battery Input. When the voltage on LBI drops below 1.25V, LBO sinks current. If not used, connect to V_{IN} .
6	6	OUT	Connect OUT to the regulator output. OUT provides bootstrap power to the IC.
7	7	GND	Power Ground. Must be low impedance; solder directly to ground plane.
8	8	LX	N-Channel Power-MOSFET Drain

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

MAX866/MAX867

4

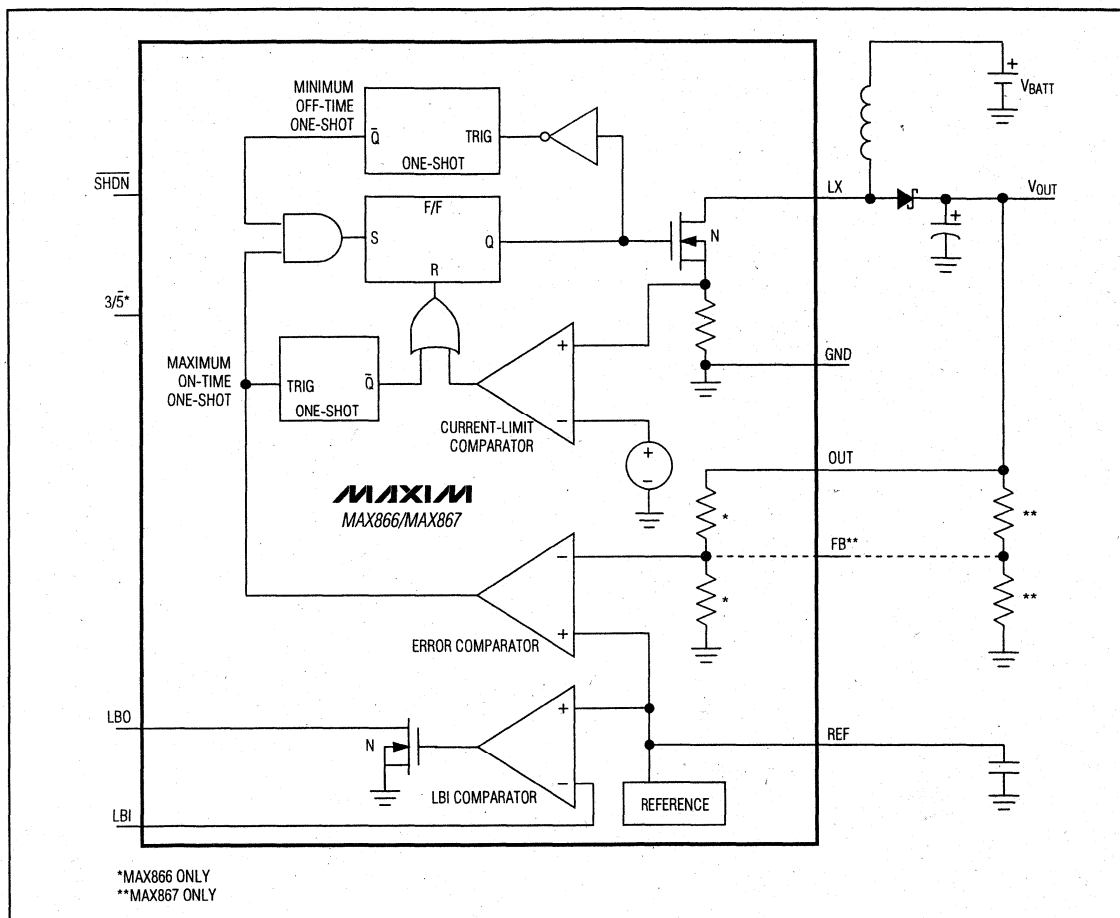


Figure 1. Block Diagram

Detailed Description

Operating Principle

The MAX866/MAX867 combine a switch-mode regulator, N-channel power MOSFET, precision voltage reference, and power-fail detector in a single monolithic device. The MOSFET is a "sense-FET" type for best efficiency, and has a very low gate threshold voltage to ensure start-up with low battery voltages (0.8V typ).

PFM Control Scheme

The MAX866/MAX867 control scheme (Figure 1) combines low-voltage efficiency (80% typ) with low battery

drain (100 μ A typ). There is no oscillator; switching is accomplished by a pair of one shots that set a maximum LX on-time (4.5 μ s typ) and a minimum LX off-time (1 μ s). LX on-time will be terminated early if the inductor current reaches 0.5A before 4.5 μ s elapses. With the standard application circuit (Figure 2a), LX current is typically less than 50mA, so LX on-time is normally not terminated by the 0.5A limit and lasts the complete 4.5 μ s. The LX on-resistance is typically 1 Ω to minimize switch losses. The MAX866/MAX867 switching frequency depends on load, input voltage, and inductor value, and it can range up to 250kHz with typical component values.

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

Voltage Reference

The precision voltage reference is suitable for driving external loads, such as an analog-to-digital converter. The voltage-reference output changes less than $\pm 2\%$ when sourcing up to $250\mu\text{A}$ and sinking up to $20\mu\text{A}$. If the reference drives an external load, bypass it with $0.22\mu\text{F}$ to GND. If the reference is unloaded, bypass it with at least $0.1\mu\text{F}$.

Logic Inputs and Outputs

The $3/\bar{5}$ input is internally diode clamped to GND and OUT, and should not be connected to signals outside this range. The SHDN input and LBO output (open-drain) are not clamped to $V+$ and can be pulled as high as $7V$ regardless of the voltage at OUT. **Do not leave control inputs ($3/\bar{5}$, LBI, or SHDN) floating.**

Design Procedure

Output Voltage Selection

For the MAX866, you can select a 3.3V or 5V output voltage under logic control, or by tying $3/\bar{5}$ to GND or OUT. The MAX867's output voltage is set by two resistors, $R1$ and $R2$ (Figure 2b), which form a voltage divider between the output and FB. Use the following equation to determine the output voltage:

$$V_{OUT} = V_{REF} \left(\frac{R1 + R2}{R2} \right)$$

where $V_{REF} = 1.25V$.

To simplify resistor selection:

$$R1 = R2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

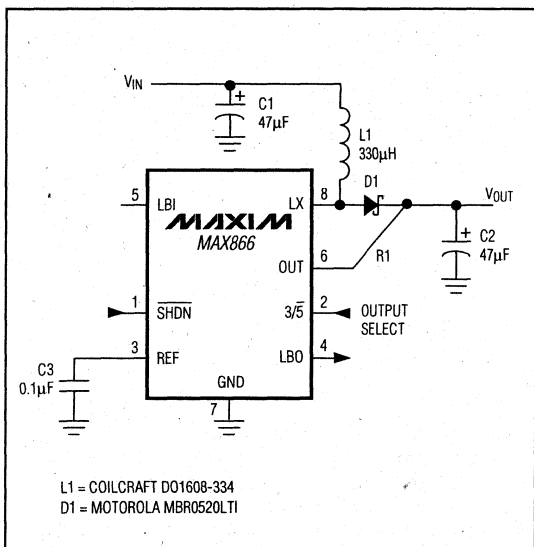


Figure 2a. Standard Application Circuit—Preset Output Voltage

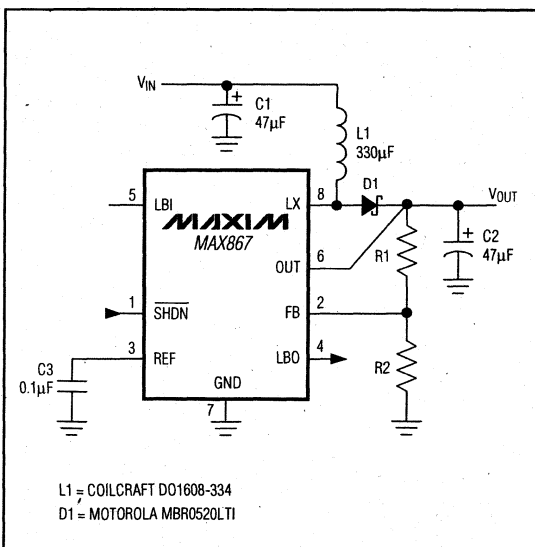


Figure 2b. Standard Application Circuit—Adjustable Output Voltage

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

MAX866/MAX867

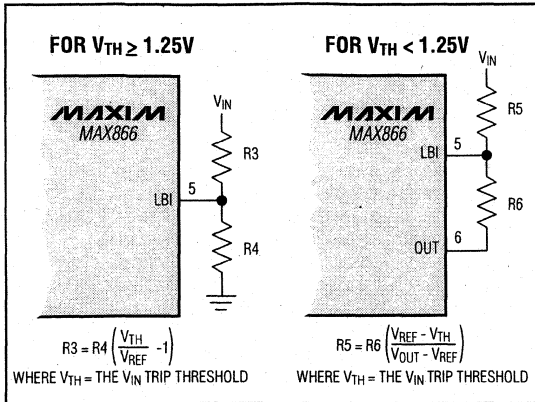


Figure 3. Low-Battery Detector Circuits

Since the input bias current at FB has a maximum value of 100nA, large values (10kΩ to 300kΩ) can be used for R1 and R2 with no significant accuracy loss. For 1% error, the current through R1 should be at least 100 times FB's bias current.

Low-Battery Detection, $V_{TH} \geq 1.25V$

The MAX866 series contains an on-chip comparator for low-battery detection. If the voltage at LBI falls below the regulator's internal reference voltage (1.25V), LBO (an open-drain output) sinks current to GND. The low-battery monitor's threshold is set by two resistors, R3 and R4 (Figure 3). Set the threshold voltage using the following equation:

$$R3 = R4 \left(\frac{V_{TH}}{V_{REF}} - 1 \right)$$

where V_{TH} is the desired threshold of the low-battery detector and V_{REF} is the internal 1.25V reference.

Since the LBI current is less than 100nA, large resistor values (typically 10kΩ to 300kΩ) can be used for R3 and R4 to minimize loading of the input supply.

When the voltage at LBI is below the internal threshold, LBO sinks current to GND. Connect a pull-up resistor of 100kΩ or more from LBO to OUT when driving CMOS circuits. When LBI is above the threshold, the LBO output is off. If the low-battery comparator is not used, connect LBI to V_{IN} and leave LBO open.

Low-Battery Detection, $V_{TH} < 1.25V$

When the low-battery detection threshold voltage is below 1.25V, use the circuit shown on the right in

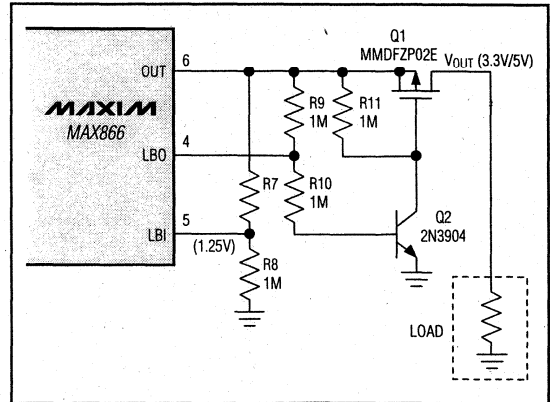


Figure 4. Low-Voltage Start-Up Circuit

Figure 3. This circuit uses V_{OUT} (3.3V or 5.0V in the MAX866, adjustable in MAX867) as a reference. The voltage divider formed by R5 and R6 allows the effective trip point of V_{IN} to be set below 1.25V. R6 is usually set to approximately 100kΩ, and R5 is given by the formula:

$$R5 = [R6 \times (V_{REF} - V_{TH})] / (V_{OUT} - V_{REF})$$

Note that LBI drops below the 1.25V LBI threshold trip point when either V_{IN} or V_{OUT} is low.

Since V_{OUT} regulation and the LBI threshold are derived from the same internal voltage reference, they track together over temperature.

Low-Battery Start-Up

The MAX866/MAX867 are bootstrapped circuits; they can start under no-load conditions at much lower battery voltages than under full load. Once started, the output can maintain a moderate load as the battery voltage decreases below the start-up voltage (see *Typical Operating Characteristics*). The circuit shown in Figure 4 allows the circuit to start with no load, then uses the LBI circuit and an external low-threshold P-channel MOSFET switch to apply the load after the output has started.

Resistors R7 and R8 are selected to trip the LBI detector at about 90% of the output voltage. On start-up, LBI and LBO are low, Q2 is off, and transistor Q1's gate is held high by R11. This disconnects the load, allowing the MAX866 to bootstrap itself at the lowest possible voltage. When the output reaches its final output voltage, LBI and LBO go high, turning on Q2, Q1, and the load.

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS	RECTIFIERS
Surface Mount	See Table 2	Matsuo 267 series Sprague 595D series AVX TPS series	Motorola MBR 0530 Nihon EC15QS02L
Miniature Through Hole	Sumida RCH654-220	Sanyo OS-CON series low-ESR organic semiconductor	Motorola 1N5017

COMPANY	PHONE	FAX
AVX	USA: (207) 282-5111	(207) 283-1941
CoilCraft	USA: (708) 639-6400	(708) 639-1469
Matsuo	USA: (714) 969-2491	(714) 960-6492
Motorola	USA: (602) 244-5303	(602) 244-4015
Murata-Erie	USA: (800) 831-9172	(814) 238-0490
Nihon	USA: (805) 867-2555 Japan: 81-3-3494-7411	(805) 867-2556 81-3-3494-7414
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sumida	USA: (708) 956-0666 Japan: 81-3-3607-5111	(708) 956-0702 81-3-3607-5144
TDK	USA: (708) 803-6100 Japan: 03-3278-5111	(708) 803-6294 03-3278-5358
J.W. Miller	USA: (310) 515-1720	(310) 515-1962

Inductor Selection

An inductor value of 330 μ H works well in most applications, supplying loads over 10mA and allowing typical start-up voltages of 0.8V. The inductor value is not critical, and the MAX866/MAX867 can operate with values from 22 μ H to 1mH. In general, smaller inductor values supply more output current while larger values start with lower input voltage. Several inductor suppliers and part numbers are listed in Tables 1 and 2.

The peak inductor current should not exceed the inductor's current rating. Since the MAX866/MAX867 current limit of 0.5A will not be reached in most applications, the peak coil current (I_{PK}) is:

$$I_{PK} = (V_{IN(max)} \times 4.5\mu s) / L$$

For a typical 1-cell alkaline design, $V_{IN(max)}$ is 1.55V, so:

$$I_{PK} = (1.55V \times 4.5\mu s) / 330\mu H = 21.14mA$$

which is well within the ratings of most surface-mount coils. Higher efficiency and output current are achieved with lower inductor resistance, but unfortunately this is inversely related to physical size. Table 2 indicates resistance and height for each coil. Some of the smallest coils have resistances over 10 Ω , and will not provide the same output power or efficiency of a 1 Ω coil. At light loads however (below 5mA), the efficiency differences between low- and high-resistance coils may be only a percent or two. The *Typical Operating Characteristics* graphs show efficiency and output current plots for 1.5 Ω and 2.9 Ω , 330 μ H coils.

Capacitor Selection

A 47 μ F, 6V, 0.85 Ω , surface-mount tantalum (SMT) output filter capacitor typically provides 15mV output ripple when stepping up from 0.9V to 1.4V at 10mA. Smaller capacitors (down to 10 μ F with higher ESRs) are acceptable for light loads or in applications that can

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

MAX866/MAX867

Table 2. Surface-Mount Inductor Information

MANUFACTURER PART	INDUCTANCE (μ H)	RESISTANCE (Ω)	RATED CURRENT (A)	HEIGHT (mm)
Sumida CD73-331	330	1.5	0.28	3.5
Sumida CD104-331	330	1.1	0.42	4
Murata-Erie LQH4N331K04M00**	330	8.2	0.095	2.6
TDK NLC565050T-331K**	330	4.9	0.14	5
CoilCraft D01608-334	330	2.9	0.16	3.2
CoilCraft DT1608-334	330*	2.9	0.16	3.2
CoilCraft D03316-334	330	0.7	0.6	5.4
CoilCraft DT3316-334	330*	0.7	0.6	5.4
J.W. Miller PM105-331K	330	1.1	0.52	5.4

* Shielded

** Low cost

tolerate higher output ripple. Values in the 10 μ F to 47 μ F range are recommended.

The equivalent series resistance (ESR) of both bypass and filter capacitors affects efficiency and output ripple. Use low-ESR capacitors for best performance, or connect two or more filter capacitors in parallel. Low-ESR, SMT tantalum capacitors are currently available from Sprague (595D series) and AVX (TPS series). See Table 1 for a list of suggested capacitor suppliers.

Rectifier Diode

For optimum performance, a switching Schottky diode (such as the 1N5817 or MBR0520LT1) is recommended. Refer to Table 1 for a list of component suppliers. For low output power applications, a PN-junction switching diode (such as the 1N4148) will also work well, although its greater forward voltage drop will reduce efficiency and raise the start-up voltage.

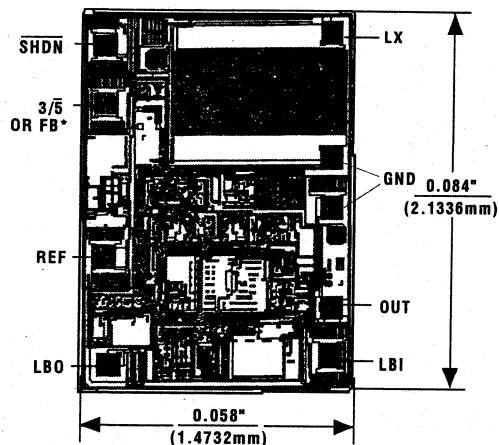
PC Layout and Grounding

The circuit's high-frequency operation makes PC layout important for minimizing ground bounce and noise. Keep the IC's GND pin and the ground leads of C1 and C2 (Figure 2) less than 0.2in (5mm) apart. Also keep all connections to the FB and LX pins as short as possible. To maximize output power and efficiency and minimize output ripple voltage, use a ground plane and solder the IC's GND (pin 7) directly to the ground plane.

4

3.3V/5V or Adjustable-Output, Single-Cell DC-DC Converters

Chip Topography



*3/5 FOR MAX866; FB FOR MAX867.

TRANSISTOR COUNT: 357;
SUBSTRATE IS CONNECTED TO OUT.

MAXIM

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

General Description

The MAX882/MAX883/MAX884 linear regulators maximize battery life by combining ultra-low supply currents and low dropout voltages. They feature 200mA output current capability at up to +125°C junction temperature and come in a 1.5W SOIC package. The 1.5W package (compared to 0.47W for standard SOIC packages) allows a wider operating range for the input voltage and output current. The MAX882/MAX883/MAX884 use a P-channel MOSFET pass transistor to maintain a low 11µA (15µA max) supply current from no-load to the full 200mA output. Unlike earlier bipolar regulators, there are no PNP base current losses that increase with output current. And, in dropout, the MOSFET does not suffer from excessive base currents that occur when PNP transistors go into saturation. Typical dropout voltages are 220mV at 5V and 200mA, or 320mV at 3.3V and 200mA.

The MAX882 features a 7µA standby mode that disables the output but keeps the reference, low-battery comparator, and biasing circuitry alive. The MAX883/MAX884 feature a shutdown (OFF) mode that turns off all circuitry, reducing supply current to less than 1µA. All three devices include a low-battery-detection comparator, foldback current limiting, reverse-current protection, and thermal overload protection.

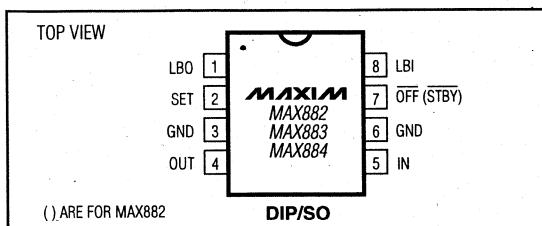
The output is preset at 3.3V for the MAX882/MAX884 and 5V for the MAX883. In addition, all devices employ Dual Mode™ operation, allowing user-adjustable outputs from 1.25V to 11V using external resistors. The input voltage supply range is 2.7V to 11.5V.

For low-dropout linear regulators with output currents up to 500mA, refer to the MAX603/MAX604 data sheet.

Applications

Pagers and Cellular Phones
3.3V and 5V Regulators
1.25V to 11V Adjustable Regulators
High-Efficiency Linear Regulators
Battery-Powered Devices
Portable Instruments
Solar-Powered Instruments

Pin Configuration



™Dual-Mode is a trademark of Maxim Integrated Products.

Features

- ♦ Guaranteed 200mA Output Current at $T_J = +125^\circ\text{C}$, with Foldback Current Limiting
- ♦ High-Power (1.5W) 8-Pin SO Package
- ♦ Dual Mode™ Operation: Fixed or Adjustable Output from 1.25V to 11V
- ♦ Large Input Range (2.7V to 11.5V)
- ♦ Internal 1.1Ω P-Channel Pass Transistor Draws No Base Current
- ♦ Low 220mV Dropout Voltage at 200mA Output Current
- ♦ 11µA Typical Quiescent Current
- ♦ 1µA (max) Shutdown Mode or 7µA (typ) Standby Mode
- ♦ Low-Battery Detection Comparator
- ♦ Reverse-Current Protection
- ♦ Thermal Overload Protection

Ordering Information

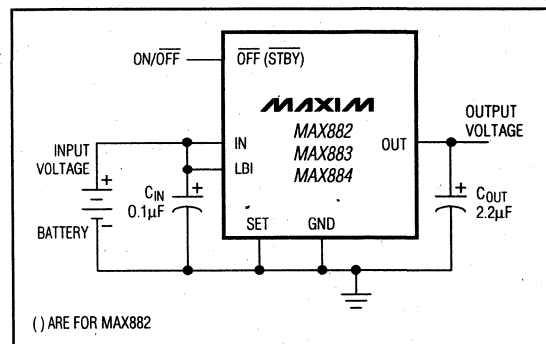
PART	TEMP. RANGE	PIN-PACKAGE
MAX882CPA	0°C to +70°C	8 Plastic DIP
MAX882CSA	0°C to +70°C	8 SO
MAX882C/D	0°C to +70°C	Dice*
MAX882EPA	-40°C to +85°C	8 Plastic DIP
MAX882ESA	-40°C to +85°C	8 SO
MAX882MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued at end of data sheet.

* Dice are tested at $T_J = +25^\circ\text{C}$, DC parameters only.

** Contact factory for availability.

Typical Operating Circuit


MAX882/MAX883/MAX884
4
MAXIM

Maxim Integrated Products 4-193

Call toll free 1-800-998-8800 for free samples or literature.

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IN or OUT to GND).....-0.3V to +12V
 Output Short-Circuit Duration1 minute
 Continuous Output Current.....300mA
 LBO Output Current.....50mA
 LBO Output Voltage and LBI,
 SET, STBY, OFF Input Voltages-0.3V to the greater of
 (IN + 0.3V) or (OUT + 0.3V)
 Continuous Power Dissipation (T_J = +70°C)
 Plastic DIP (derate 9.09mW/°C above +70°C)727mW

High-Power SO (derate 18.75mW/°C above +70°C)1.5W
 CERDIP (derate 8.00mW/°C above +70°C)640mW
 Operating Temperature Ranges
 MAX88_C_A0°C to +70°C
 MAX88_E_A-40°C to +85°C
 MAX88_MJA-55°C to +125°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10sec)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 6V (MAX883) or V_{IN} = 4.3V (MAX882/MAX884), C_{OUT} = 2.2μF, STBY or OFF = V_{IN}, SET = GND, LBI = V_{IN}, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V _{IN}	SET = OUT, R _L = 1kΩ	MAX88_C_A	2.7		11.5	V
			MAX88_E_A	2.9		11.5	
			MAX88_MJA	3.0		11.5	
Output Voltage (Note 2)	V _{OUT}	MAX883, 6.0V ≤ V _{IN} ≤ 11.5V	I _{OUT} = 10μA–200mA, T _J ≤ +125°C	4.75	5.00	5.25	mV
			I _{OUT} = 10μA–250mA, T _J ≤ +85°C				
			I _{OUT} = 10μA–250mA, T _J ≤ +70°C				
		MAX882/MAX884, 4.3V ≤ V _{IN} ≤ 11.5V	I _{OUT} = 10μA–150mA, T _J ≤ +125°C	3.15	3.30	3.45	
			I _{OUT} = 10μA–200mA, T _J ≤ +85°C				
			I _{OUT} = 10μA–200mA, T _J ≤ +70°C				
Load Regulation	ΔV _{LDR}	I _{OUT} = 1mA to 200mA	MAX883C_A/E_A	60	100	mV	
			MAX883MJA		150		
		I _{OUT} = 1mA to 150mA	MAX882, MAX884	30	100		
Line Regulation	ΔV _{LNR}	(V _{OUT} + 0.5V) ≤ V _{IN} ≤ 11.5V, I _{OUT} = 10mA			10	40	mV
Dropout Voltage (Note 3)	ΔV _{DO}	MAX883	I _{OUT} = 100mA	110	220	mV	
			I _{OUT} = 200mA	220	440		
		MAX882/MAX884	I _{OUT} = 100mA	160	320		
			I _{OUT} = 200mA	320	640		
			Quiescent Current	I _Q	SET = OUT, V _{IN} = 6V		MAX88_C_A/E_A
MAX88_MJA		30					
V _{IN} = 11.5V	MAX88_C_A/E_A	15			25		
	MAX88_MJA				40		

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 6V$ (MAX883) or $V_{IN} = 4.3V$ (MAX882/MAX884), $C_{OUT} = 2.2\mu F$, $\overline{STBY}$ or $\overline{OFF} = V_{IN}$, $SET = GND$, $LBI = V_{IN}$, $T_J = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_J = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{STBY}$ Quiescent Current (Note 4)	$I_{Q \overline{STBY}}$	$\overline{STBY} = 0V$, $V_{IN} = 6V$, $SET = OUT$		7	15	μA
		MAX882C_A/E_A			30	
		MAX882MJA			30	
		$\overline{STBY} = 0V$, $V_{IN} = 11.5V$, $SET = OUT$		10	25	
$\overline{OFF}$ Quiescent Current	$I_{Q \overline{OFF}}$	$\overline{OFF} = 0V$, $R_L = 1k\Omega$, $V_{IN} = 11.5V$ (MAX883/MAX884)		0.01	1	μA
		MAX88_C_A			5	
		MAX88_E_A			10	
		MAX88_MJA			10	
Minimum Load Current	$I_{OUT(MIN)}$	$V_{IN} = 11.5V$, $SET = OUT$			1	μA
		MAX88_C_A			3	
		MAX88_E_A			10	
		MAX88_MJA			10	
Foldback Current Limit (Note 5)	I_{LIM}	$V_{OUT} < 0.8V$		170		mA
		$V_{OUT} > 0.8V$ and $V_{IN} - V_{OUT} > 0.7V$		430		
Thermal Shutdown Temperature	T_{SD}			160		$^\circ C$
Thermal Shutdown Hysteresis	ΔT_{SD}			10		$^\circ C$
Reverse-Current-Protection Threshold (Note 6)	ΔV_{RTH}	$V_{OUT} = 4.5V$	MAX883_A	6	20	mV
		$V_{OUT} = 3.0V$	MAX882_A, MAX884_A	6	20	
Reverse Leakage Current	I_{RVL}	MAX882: $V_{IN} = 0V$, $\overline{STBY} = 0V$, $V_{OUT} = 3.0V$		7		μA
		MAX883/MAX884: $V_{IN} = 0V$, $\overline{OFF} = 0V$, $V_{OUT} = 3.0V$		0.01		
Startup Overshoot	V_{OSH}	$R_L = 1k\Omega$, $C_{OUT} = 2.2\mu F$		1		% of V_{OUT}
Time Required to Exit $\overline{OFF}$ or $\overline{STBY}$ Modes	T_{START}	$V_{IN} = 9V$, $R_L = 33\Omega$, $\overline{OFF}$ from $0V$ to V_{IN} , 0% to 95% of V_{OUT}		200		μs
Dual Mode™ SET Threshold	$V_{SET TH}$	For internal feedback		65	30	mV
		For external feedback	150	65		
SET Reference Voltage	V_{SET}	$SET = OUT$, $R_L = 1k\Omega$	1.16	1.20	1.24	V
SET Input Leakage Current	I_{SET}	$V_{SET} = 1.5V$ or $0V$	± 0.01	± 50		nA
LBI Threshold Voltage	V_{LBI}	LBI signal falling	1.15	1.20	1.25	V
LBI Hysteresis	ΔV_{LBI}			7		mV
LBI Input Leakage Current	I_{LBI}	$V_{LBI} = 1.5V$	± 0.01	± 50		nA
LBO Output Low Voltage	V_{LBOL}	$I_{LBO SINK} = 1.2mA$, $V_{LBI} = 1V$, $3V \leq V_{IN} \leq 11.5V$, $SET = OUT$		90	250	mV
LBO Output Leakage Current	$I_{LBO LKG}$	$V_{LBI} = V_{IN}$, $V_{LBO} = V_{IN}$		0.01	0.1	μA
OUT Leakage Current	$I_{OUT LKG}$	$V_{IN} = 11.5V$, $V_{OUT} = 2V$, $SET = OUT$	MAX88_C_A	0.01	1	μA
			MAX88_E_A		3	
			MAX88_MJA		10	

MAX882/MAX883/MAX884

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5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 6V$ (MAX883) or $V_{IN} = 4.3V$ (MAX882/MAX884), $C_{OUT} = 2.2\mu F$, $\overline{STBY}$ or $\overline{OFF} = V_{IN}$, $SET = GND$, $LBI = V_{IN}$, $T_J = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_J = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{STBY}$ Threshold Voltage	$V_{\overline{STBY}}$	$\overline{STBY}$ signal falling	MAX882_A	1.15	1.20	1.25	V
$\overline{STBY}$ Hysteresis	$\Delta V_{\overline{STBY}}$		MAX882_A		7		mV
$\overline{STBY}$ Input Leakage Current	$I_{\overline{STBY}}$	$V_{\overline{STBY}} = V_{IN}$ or 0V	MAX882_A		± 0.01	± 50	nA
$\overline{OFF}$ Threshold Voltage	$V_{IL \overline{OFF}}$	In off mode	MAX883_A, MAX884_A			0.4	V
	$V_{IH \overline{OFF}}$	In on mode, SET = OUT, $V_{IN} \leq 6V$	MAX883_A, MAX884_A	2.0			
		In on mode, SET = OUT, $6V < V_{IN} \leq 11.5V$	MAX883_A, MAX884_A	3.0			
$\overline{OFF}$ Input Leakage Current	$I_{\overline{OFF}}$	$V_{\overline{OFF}} = V_{IN}$ or 0V			± 0.01	± 50	nA
Output Noise (Note 7)	e_n	10Hz to 10kHz, SET = OUT, $R_L = 1k\Omega$, $C_{OUT} = 2.2\mu F$			250		μV_{RMS}

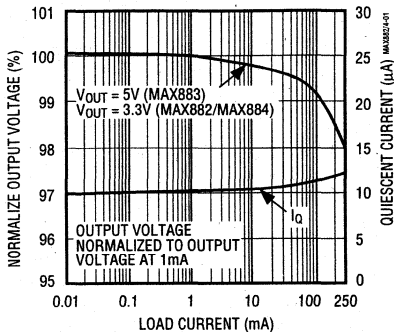
- Note 1:** Electrical specifications are measured by pulse testing and are guaranteed for a junction temperature (T_J) within the operating temperature range, unless otherwise noted. When operating C and E grade parts up to a T_J of $+125^\circ C$, expect performance similar to M grade specifications. For T_J between $+125^\circ C$ and $+150^\circ C$, the output voltage may drift more.
- Note 2:** ($V_{IN} - V_{OUT}$) is limited to keep the product ($I_{OUT} \times (V_{IN} - V_{OUT})$) from exceeding the package power dissipation limits. See Figure 5. Therefore, the combination of high output current and high supply voltage is not tested. Output current at $T_J = +125^\circ C$ is guaranteed by guard banding tests at $T_J = +85^\circ C$ and $+70^\circ C$.
- Note 3:** Dropout Voltage is ($V_{IN} - V_{OUT}$) when V_{OUT} falls to 100mV below its nominal value at $V_{IN} = (V_{OUT} + 2V)$. For example, the MAX883 is tested by measuring the V_{OUT} at $V_{IN} = 7V$, then V_{IN} is lowered until V_{OUT} falls 100mV below the measured value. The difference ($V_{IN} - V_{OUT}$) is then measured and defined as ΔV_{DO} .
- Note 4:** Since standby mode inhibits the output but keeps all biasing circuitry alive, the Standby Quiescent Current is similar to the normal operating quiescent current.
- Note 5:** Foldback Current Limit was characterized by pulse testing to remain below the maximum junction temperature (not production tested).
- Note 6:** The Reverse-Current Protection Threshold is the output/input differential voltage ($V_{OUT} - V_{IN}$) at which reverse-current protection switchover occurs and the pass transistor is turned off. See the section *Reverse Current Protection* in the *Detailed Description*.
- Note 7:** Noise is tested using a bandpass amplifier with two poles at 10Hz and two poles at 10kHz.

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 200mA Linear Regulators

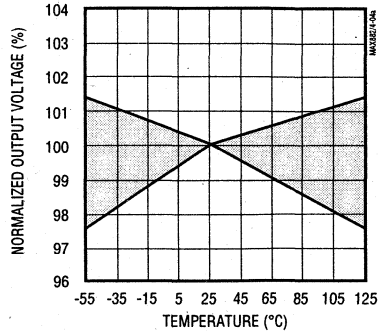
Typical Operating Characteristics

(V_{IN} = 7V for MAX883, V_{IN} = 5.3V for MAX882/MAX884, OFF or STBY = V_{IN}, SET = GND, LBI = V_{IN}, LBO = OPEN, C_{IN} = C_{OUT} = 2.2μF, R_L = 1kΩ, T_A = +25°C, unless otherwise noted.)

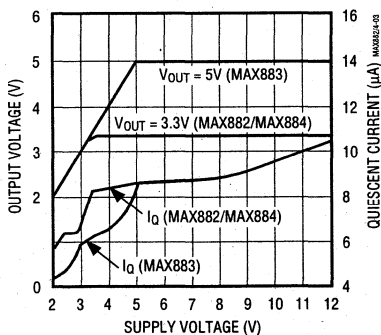
OUTPUT VOLTAGE AND QUIESCENT CURRENT vs. LOAD CURRENT



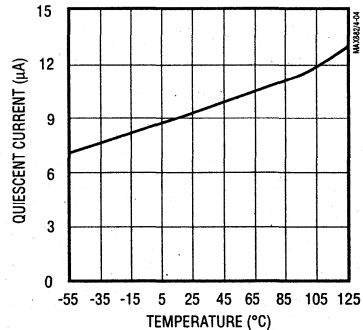
OUTPUT VOLTAGE vs. TEMPERATURE



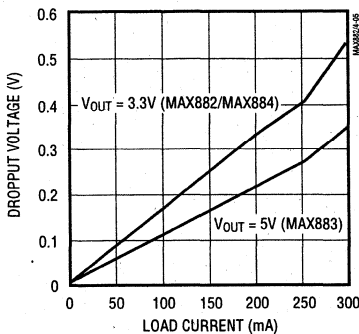
OUTPUT VOLTAGE AND QUIESCENT CURRENT vs. SUPPLY VOLTAGE



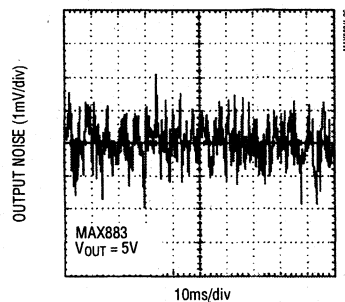
QUIESCENT CURRENT vs. TEMPERATURE



DROPOUT VOLTAGE vs. LOAD CURRENT



10Hz to 10kHz OUTPUT NOISE

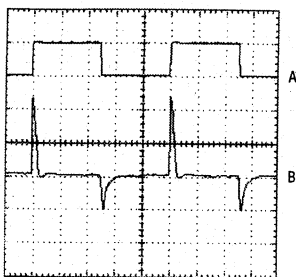


5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

Typical Operating Characteristics (continued)

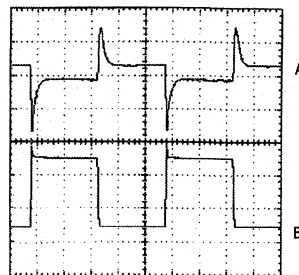
($V_{IN} = 7V$ for MAX883, $V_{IN} = 5.3V$ for MAX882/MAX884, $\overline{OFF}$ or $\overline{STBY} = V_{IN}$, $SET = GND$, $LBI = V_{IN}$, $LBO = OPEN$, $C_{IN} = C_{OUT} = 2.2\mu F$, $R_L = 1k\Omega$, $T_A = +25^\circ C$, unless otherwise noted.)

LINE-TRANSIENT RESPONSE



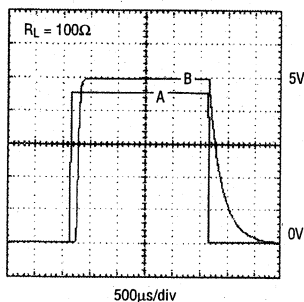
MAX883: $V_{OUT} = 5V$, $C_{IN} = 0\mu F$, $t_R = 15\mu s$, $t_F = 13\mu s$
A: $V_{IN} = 8V$ (HIGH) / $V_{IN} = 7V$ (LOW)
B: OUTPUT VOLTAGE (100mV/div)

LOAD-TRANSIENT RESPONSE



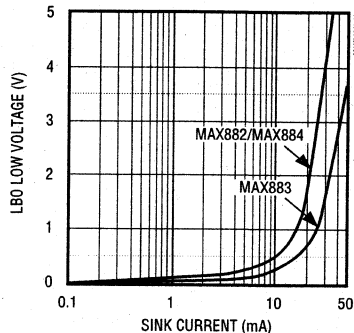
MAX883: $V_{OUT} = 5V$, $t_R = 24\mu s$, $t_F = 44\mu s$
A: OUTPUT VOLTAGE (100mV/div)
B: $I_{OUT} = 250mA$ (HIGH) / $I_{OUT} = 50mA$ (LOW)

OVERSHOOT AND TIME
EXITING SHUTDOWN MODE



$R_L = 100\Omega$
A: $\overline{OFF}$ PIN VOLTAGE (1V/div):
RISE TIME = $9\mu s$
B: MAX883 OUTPUT VOLTAGE (1V/div):
DELAY = $135\mu s$, RISE TIME = $67\mu s$,
OVERSHOOT = 0%

LBO LOW VOLTAGE
vs. SINK CURRENT



5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

Pin Description

PIN		NAME	FUNCTION
MAX882	MAX883/ MAX884		
1	1	LBO	Low-Battery Output is an open-drain output that goes low when LBI is less than 1.2V. Connect to IN or OUT through a pull-up resistor. LBO is undefined during shutdown mode (MAX883/MAX884).
2	2	SET	Feedback for setting the output voltage. Connect to GND to set the output voltage to the preselected 3.3V or 5V. Connect to an external resistor network for adjustable-output operation.
3, 6	3, 6	GND	Ground pins—also function as heatsinks in the SO package. All GND pins must be soldered to the circuit board for proper power dissipation. Connect to large copper pads or planes to channel heat from the IC.
4	4	OUT	Regulator Output. Fixed or adjustable from 1.25V to 11.0V. Sources up to 200mA. Bypass with a 2.2μF capacitor.
5	5	IN	Regulator Input. Supply voltage can range from 2.7V to 11.5V.
7	—	STBY	Standby. Active-low comparator input. Connect to GND to disable the output or to IN for normal operation. A resistor network (from IN) can be used to set a standby mode threshold.
—	7	OFF	Shutdown. Active-low logic input. In OFF mode, supply current is reduced below 1μA and V _{OUT} = 0V
8	8	LBI	Low-Battery comparator Input. Tie to IN when not used.

Detailed Description

The MAX882/MAX883/MAX884 are micropower, low-dropout linear regulators designed primarily for battery-powered applications. They feature Dual-Mode™ operation, allowing a fixed output of 5V for the MAX883 and 3.3V for the MAX882/MAX884, or an adjustable output from 1.25V to 11V. These devices supply up to 200mA while requiring less than 15μA quiescent current. As illustrated in Figure 1, they consist of a 1.20V reference, error amplifier, MOSFET driver, P-channel pass transistor, dual-mode comparator and feedback voltage divider.

The 1.20V reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback voltage is lower than the reference, the pass transistor's gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage divider connected to the OUT pin, or an external resistor network connected to the SET pin. The dual-mode comparator examines the SET pin voltage and selects the feedback path used. If the SET pin is below 65mV, internal feedback is used and the output voltage is regulated to 5V for the MAX883 or

3.3V for the MAX882/MAX884. Additional blocks include a foldback current limiter, reverse-current protection, a thermal sensor, shutdown or standby logic, and a low-battery-detection comparator.

Internal P-Channel Pass Transistor

The MAX882/MAX883/MAX884 feature a 200mA P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The P-channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste large amounts of current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The MAX882/MAX883/MAX884 do not suffer from these problems and consume only 11μA of quiescent current during light loads, heavy loads, and dropout.

Output Voltage Selection

The MAX882/MAX883/MAX884 feature Dual Mode™ operation. In preset voltage mode, the MAX883's output is set to 5V and the MAX882/MAX884's output is set to 3.3V, using internal trimmed feedback resistors. Select this mode by connecting SET to ground.

In preset voltage mode, impedances between SET and ground should be less than 100kΩ. Otherwise, spurious conditions could cause the voltage at SET to exceed the 65mV dual-mode threshold.

MAX882/MAX883/MAX884

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5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

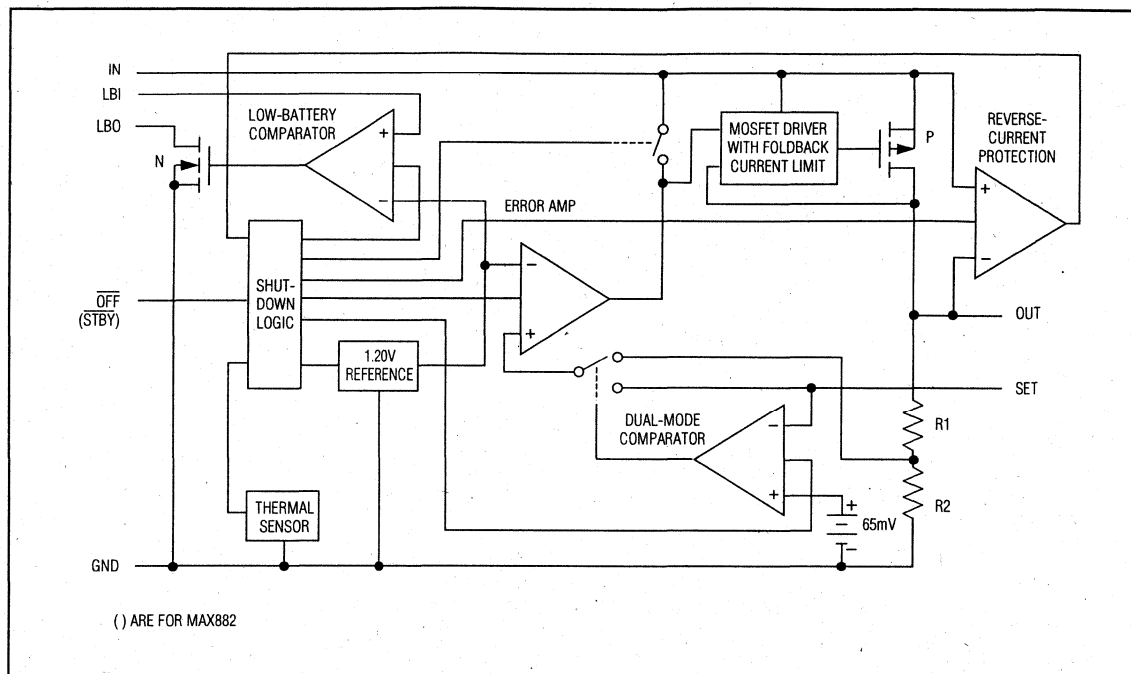


Figure 1. MAX882/MAX883/MAX884 Functional Diagram

In adjustable mode, the user selects an output voltage in the 1.25V to 11V range by connecting two external resistors, used as a voltage divider, to the SET pin (Figure 2).

The output voltage is set by the following equation:

$$V_{OUT} = V_{SET} \left(1 + \frac{R1}{R2} \right)$$

where $V_{SET} = 1.20V$.

To simplify resistor selection:

$$R1 = R2 \left(\frac{V_{OUT}}{V_{SET}} - 1 \right)$$

Since the input bias current at SET is nominally zero, large resistance values can be used for R1 and R2 to minimize power consumption without losing accuracy. Up to $1.5M\Omega$ is acceptable for R2. Since the V_{SET} tolerance is less than $\pm 40mV$, the output can be set using fixed resistors instead of trim pots.

Standby Mode (MAX882)

The MAX882 has a standby feature that disconnects the input from the output when STBY is brought low, but keeps all other circuitry awake. In this mode, V_{OUT} drops to 0V, and the internal biasing circuitry (including the low-battery comparator) remains on. The maximum quiescent current during standby is $15\mu A$. STBY is a comparator input with the other input internally tied to the reference voltage. Use a resistor network as shown in Figure 3 to set a standby-mode threshold voltage for undervoltage lockout. Connect STBY to IN for normal operation.

OFF Mode (MAX883/MAX884)

A low-logic input on the OFF pin shuts down the MAX883/MAX884. In this mode, the pass transistor, control circuit, reference, and all biases are turned off, and the supply current is reduced to less than $1\mu A$. LBO is undefined in OFF mode. Connect OFF to IN for normal operation.

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

MAX882/MAX883/MAX884

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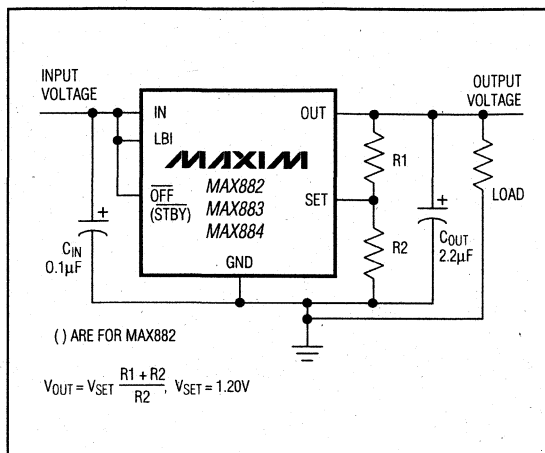


Figure 2. Adjustable Output Using External Feedback Resistors

Foldback Current Limiting

The MAX882/MAX883/MAX884 also include a foldback current limiter. It monitors and controls the pass transistor's gate voltage, estimating the output current and limiting it to 430mA for output voltages above 0.8V and $(V_{IN} - V_{OUT}) > 0.7V$. If the output voltage drops below 0.8V, implying a short-circuit condition, the output current is limited to 170mA. The output can be shorted to ground for 1 minute without damaging the device if the package can dissipate $(V_{IN} \times 170mA)$ without exceeding $T_J = +150^\circ C$. When the output is greater than 0.8V and $(V_{IN} - V_{OUT}) < 0.7V$ (dropout operation), no current limiting is allowed, to provide maximum load drive.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX882/MAX883/MAX884. When the junction temperature exceeds $T_J = +160^\circ C$, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature cools by $10^\circ C$, resulting in a pulsed output during thermal overload conditions.

Thermal overload protection is designed to protect the MAX882/MAX883/MAX884 if fault conditions occur. It is not intended to be used as an operating mode. Prolonged operation in thermal shutdown mode may reduce the IC's reliability. For continual operation, do not exceed the absolute maximum junction temperature rating of $T_J = +150^\circ C$.

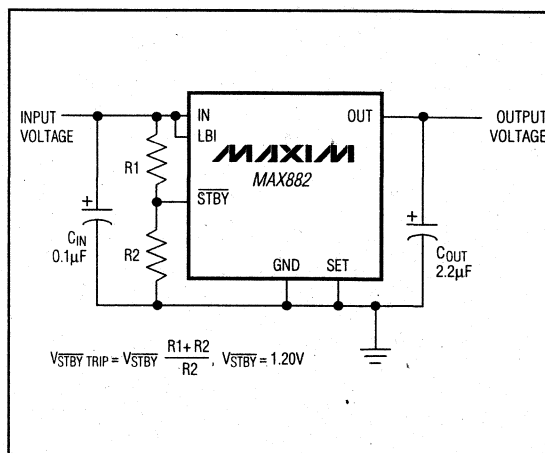


Figure 3. Setting an Undervoltage Lockout Threshold Using STBY

Power Dissipation and Operating Region

Maximum power dissipation of the MAX882/MAX883/MAX884 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. The resulting power dissipation is as follows:

$$P = \frac{(T_J - T_A)}{(\theta_{JB} + \theta_{BA})}$$

where $(T_J - T_A)$ is the temperature difference between the MAX882/MAX883/MAX884 die junction and the surrounding air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package chosen, and θ_{BA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air.

The 8-pin small-outline package for the MAX882/MAX883/MAX884 features a special lead frame with a lower thermal resistance and higher allowable power dissipation. This package's thermal resistance package is $\theta_{JB} = 53^\circ C/W$, compared with $\theta_{JB} = 110^\circ C/W$ for an 8-pin plastic DIP package and $\theta_{JB} = 125^\circ C/W$ for an 8-pin ceramic DIP package.

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

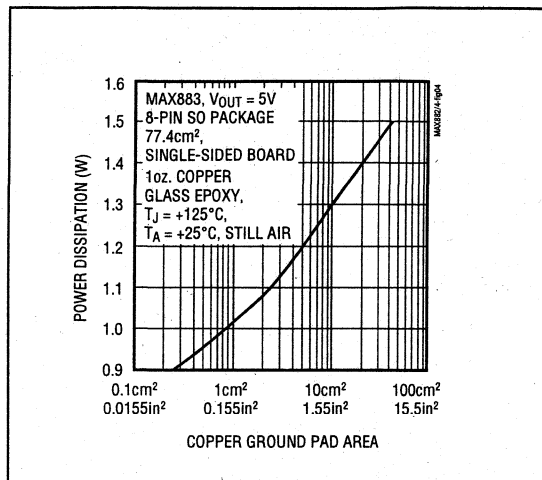


Figure 4. Typical Maximum Power Dissipation vs. Ground Pad Area

The GND pins of the MAX882/MAX883/MAX884 SOIC package perform the dual function of providing an electrical connection to ground and channeling heat away. Connect all GND pins to ground using a large pad or ground plane. Where this is impossible, place a copper plane on an adjacent layer. For a given power dissipation, the pad should exceed the associated dimensions in Figure 4.

Figure 4 assumes the IC is in an 8-pin small-outline package that has a maximum junction temperature of +125°C and is soldered directly to the pad; it also has a +25°C ambient air temperature and no other heat sources. Use larger pad sizes for other packages, lower junction temperatures, higher ambient temperatures, or conditions where the IC is not soldered directly to the heat-sinking ground pad. When operating C and E grade parts up to a T_J of +125°C, expect performance similar to M grade specifications. For T_J between +125°C and +150°C, the output voltage may drift more.

The MAX882/MAX883/MAX884 can regulate currents up to 250mA and operate with input voltages up to 11.5V, but not simultaneously. High output currents can only be sustained when input-output differential voltages are small, as shown in Figure 5. Maximum power dissipation depends on packaging, temperature, and air flow. The maximum output current is as follows:

$$I_{OUT(MAX)} = \frac{P(T_J - T_A)}{(V_{IN} - V_{OUT})100^\circ\text{C}}$$

where P is derived from Figure 4.

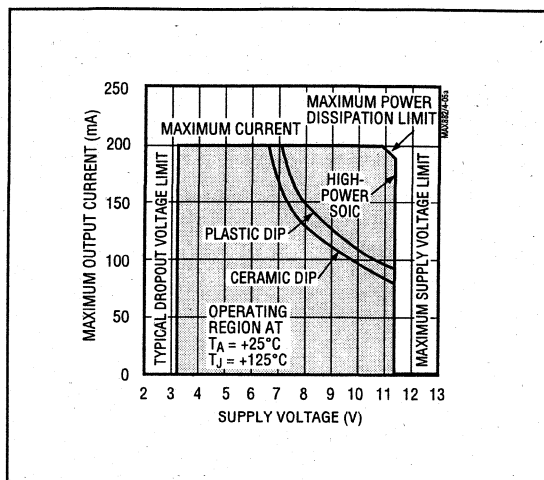


Figure 5a. Safe Operating Regions: MAX882/MAX884 Maximum Output Current vs. Supply Voltage

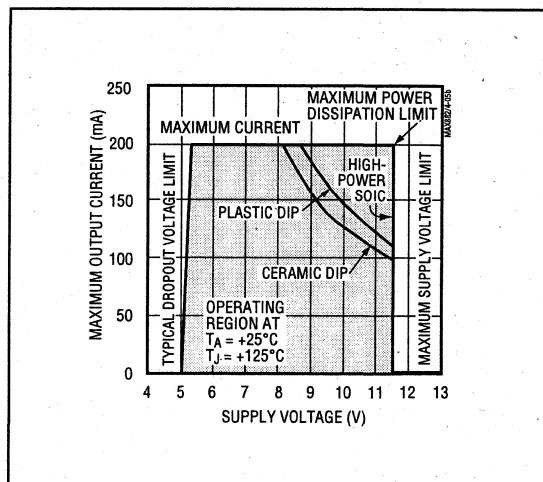


Figure 5b. Safe Operating Regions: MAX883 Maximum Output Current vs. Supply Voltage

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

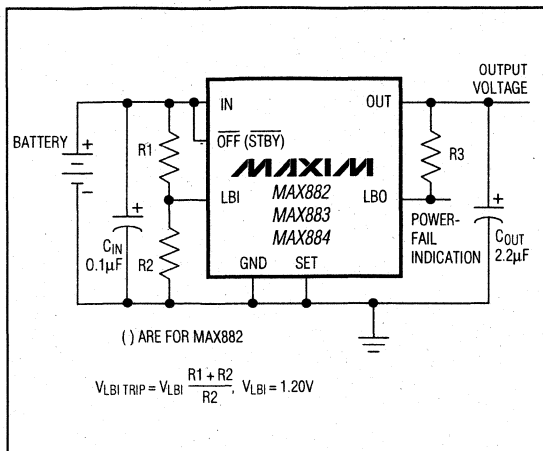


Figure 6. Using the Low-Battery Comparator to Monitor Battery Voltage

Reverse-Current Protection

The MAX882/MAX883/MAX884 have a unique protection scheme that limits reverse currents when the input voltage falls below the output. It monitors the voltages on IN and OUT and switches the IC's substrate and power bus to the more positive of the two. The control circuitry is then able to remain functioning and turn the pass transistor off, limiting reverse currents back through to the input of the device. In this mode, typical current into OUT to GND is 15µA at $V_{OUT} = 3.3V$ and 50µA at $V_{OUT} = 5V$.

Reverse-current protection activates when the voltage on IN falls 6mV (or 20mV maximum) below the voltage on OUT. Before this happens, currents as high as several milliamperes can flow back through the device.

Low-Battery-Detection Comparator

The MAX882/MAX883/MAX884 provide a low-battery comparator that compares the voltage on the LBI pin to the 1.20V internal reference. LBO, an open-drain output, goes low when LBI is below 1.20V. Hysteresis of 7mV has been added to the low-battery comparator to provide noise immunity during switching. LBO remains functional in standby mode for the MAX882, but is undefined in OFF mode for the MAX883 and MAX884. Tie LBI to IN when not used.

Use a resistor-divider network as shown in Figure 6 to set the low-battery trip voltage. Current into the LBI input is $\pm 50nA$ maximum, so R2 can be as large as 1MΩ. Add extra noise immunity by connecting a small capacitor from LBI to GND. Additional hysteresis can be added by connecting a high-value resistor from LBI to LBO.

* Tie LBI to IN when not used.

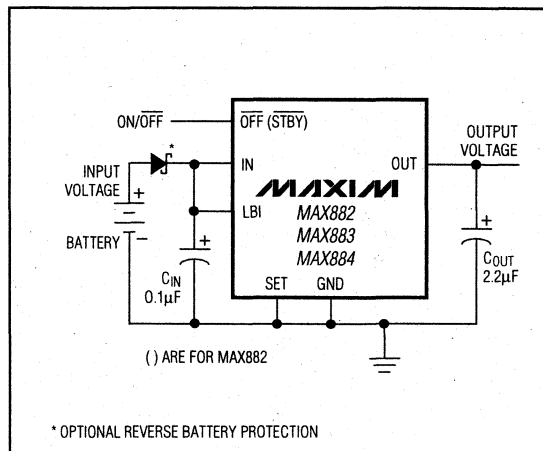


Figure 7. Typical 3.3V or 5V Linear Regulator Circuit

Applications Information

The MAX882/MAX883/MAX884 are series linear regulators designed primarily for battery-powered systems. Figure 7 shows a typical application.

Standby Mode vs. OFF Mode

STBY is a comparator input that allows the user to set the standby-mode threshold voltage, while OFF is a logic-level input. When in standby mode, the output is disconnected from the input, but the biasing circuitry (including the low-battery comparator) is kept alive, causing the device to draw around 7µA. Standby mode is useful in applications where a low-battery comparator function is still needed in shutdown.

A logic low at the OFF pin turns off all biasing circuitry, including the LBI/LBO comparator, and reduces supply current to less than 1µA. OFF mode is useful for maximizing battery life. There is little difference in the time it takes to exit standby mode or OFF mode.

Output Capacitor Selection and Regulator Stability

An output filter capacitor is required at the MAX882/MAX883/MAX884 OUT pin. The minimum output capacitance required for stability is 2.2µF.

5V/3.3V or Adjustable, Low-Dropout, Low IQ, 200mA Linear Regulators

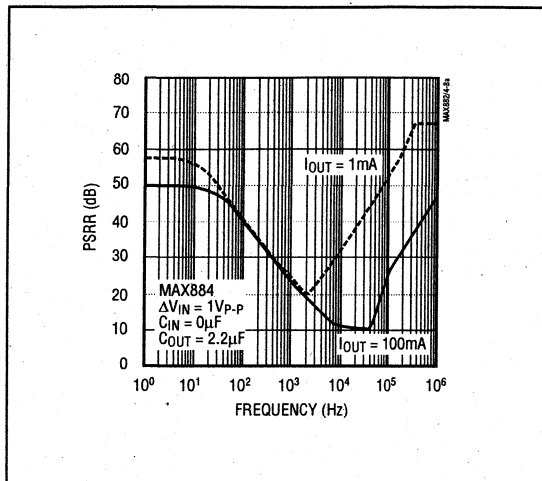


Figure 8a. Power-Supply Rejection Ratio vs. Ripple Frequency for Light and Heavy Loads

The filter capacitor's size depends primarily on the desired power-up time and load-transient responses. Load-transient response is improved by using larger output capacitors.

The output capacitor's equivalent series resistance (ESR) will not affect stability as long as you observe the minimum capacitance requirement. The type of capacitor selected is not critical, but it must remain above the minimum value over the full operating temperature range.

Input Bypass Capacitor

Normally, use 0.1μF to 10μF capacitors on the MAX882/MAX883/MAX884 input. The best value depends primarily on the power-up slew rate of V_{IN} , and on load and line transients. Larger input capacitor values provide better supply-noise rejection and line-transient response, as well as improved performance, when the supply has a high AC impedance. The type of input bypass capacitor used is not critical.

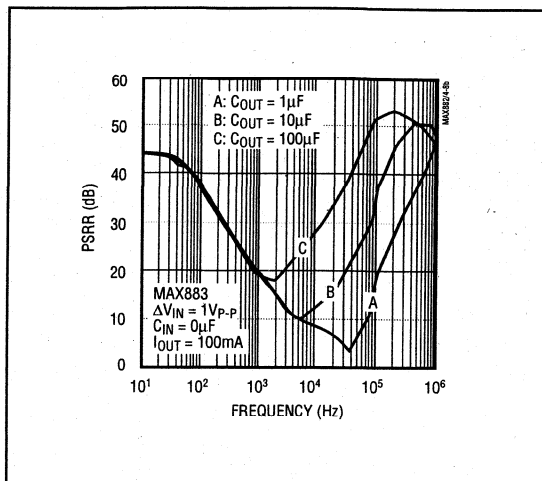


Figure 8b. Power-Supply Rejection Ratio vs. Ripple Frequency for Various Output Capacitances

Noise

The MAX882/MAX883/MAX884 exhibit up to 4mV_{p-p} of noise during normal operation. This is negligible in most applications. When using the MAX882/MAX883/MAX884 for applications that include analog-to-digital converters (ADCs) with resolutions greater than 12 bits, consider the ADC's power-supply rejection specifications. Refer to the output noise plot in the *Typical Operating Characteristics* section.

PSRR and Operation from Sources Other than Batteries

The MAX882/MAX883/MAX884 are designed to achieve low dropout voltages and low quiescent currents in battery-powered systems. However, to gain these benefits, the devices must trade away power-supply noise rejection, as well as swift response to supply variations and load transients. For a 1mA load current, power-supply rejection ranges from 60dB down to 20dB at 2kHz. At higher frequencies, the circuit depends primarily on the characteristics of the output capacitor, and the PSRR increases (Figure 8).

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

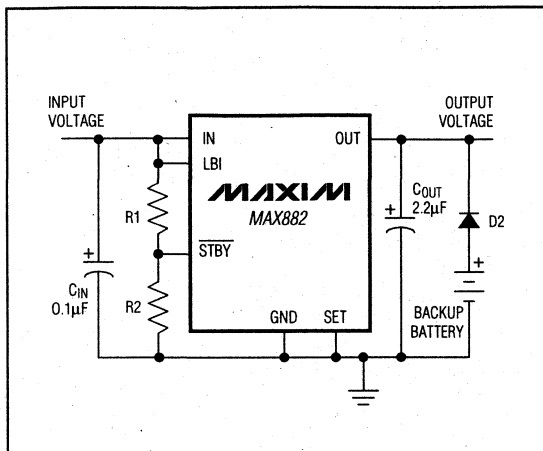


Figure 9. Short-Term Battery Backup Using the MAX882

When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the values of the input and output capacitors and employing passive filtering techniques. Do not use power supplies with ripple voltage exceeding 200mV at 100kHz.

Overshoot and Transient Considerations

The *Typical Operating Characteristics* section shows power-up, supply, and load-transient response graphs. On the load-transient graphs, two components of the output response can be observed: a DC shift from the output impedance due to the different load currents, and the transient response. Typical transients for step changes in the load current from 50mA to 250mA are 200mV. Increasing the output capacitor's value attenuates transient spikes.

During recovery from shutdown, overshoot is negligible if the output voltage has been given time to decay adequately. During power-up from $V_{IN} = 0V$, overshoot is typically less than 1% of V_{OUT} .

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX882/MAX883/MAX884 use a P-channel MOSFET pass transistor, their dropout voltage is a function of $R_{DS(ON)}$ multiplied by the load current (see *Electrical Characteristics*). Quickly stepping up the input voltage from the dropout voltage can result in overshoot.

Short-Term Battery Backup Using the MAX882

Figure 9 illustrates a scheme for implementing battery backup for 3.3V circuits using the MAX882. When the supply voltage drops below some user-specified value based on resistors R1 and R2, the standby function activates, turning off the MAX882's output. Under these conditions, the backup battery supplies power to the load. Reverse current protection prevents the battery from draining back through the regulator to the input.

This application is limited to short-term battery backup for 3.3V circuits. The current drawn by the MAX882's OUT pin at 3.3V during reverse current protection is typically 8µA. It should not be used with the MAX883 and MAX884, since the OFF pin is a logic input, and indeterminate inputs can cause the regulator to turn on intermittently, draining the battery.

Reverse Battery Protection

Reverse battery protection can be added by including an inexpensive Schottky diode between the battery input and the regulator circuit, as shown in Figure 7. However, the dropout voltage of the regulator will be increased by the forward voltage drop of the diode. For example, the forward voltage of a standard 1N5817 Schottky diode is typically 0.29V at 200mA.

5V/3.3V or Adjustable, Low-Dropout, Low Iq, 200mA Linear Regulators

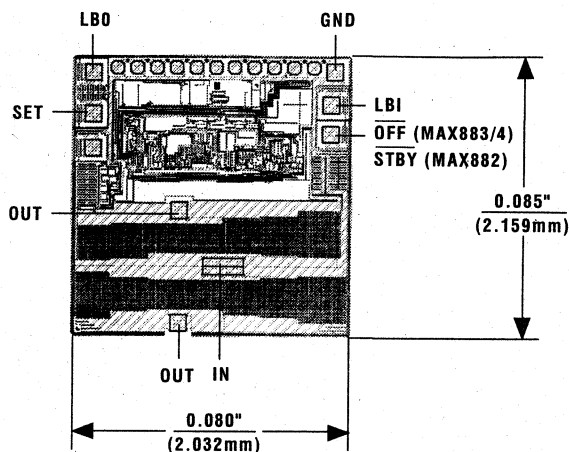
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX883 CPA	0°C to +70°C	8 Plastic DIP
MAX883CSA	0°C to +70°C	8 SO
MAX883C/D	0°C to +70°C	Dice*
MAX883EPA	-40°C to +85°C	8 Plastic DIP
MAX883ESA	-40°C to +85°C	8 SO
MAX883MJA	-55°C to +125°C	8 CERDIP**
MAX884 CPA	0°C to +70°C	8 Plastic DIP
MAX884CSA	0°C to +70°C	8 SO
MAX884C/D	0°C to +70°C	Dice*
MAX884EPA	-40°C to +85°C	8 Plastic DIP
MAX884ESA	-40°C to +85°C	8 SO
MAX884MJA	-55°C to +125°C	8 CERDIP**

* Dice are tested at $T_J = +25^\circ\text{C}$, DC parameters only.

** Contact factory for availability.

Chip Topography



TRANSISTOR COUNT: 151

NO DIRECT SUBSTRATE CONNECTION. THE N-SUBSTRATE IS INTERNALLY SWITCHED BETWEEN THE MORE POSITIVE OF IN OR OUT.



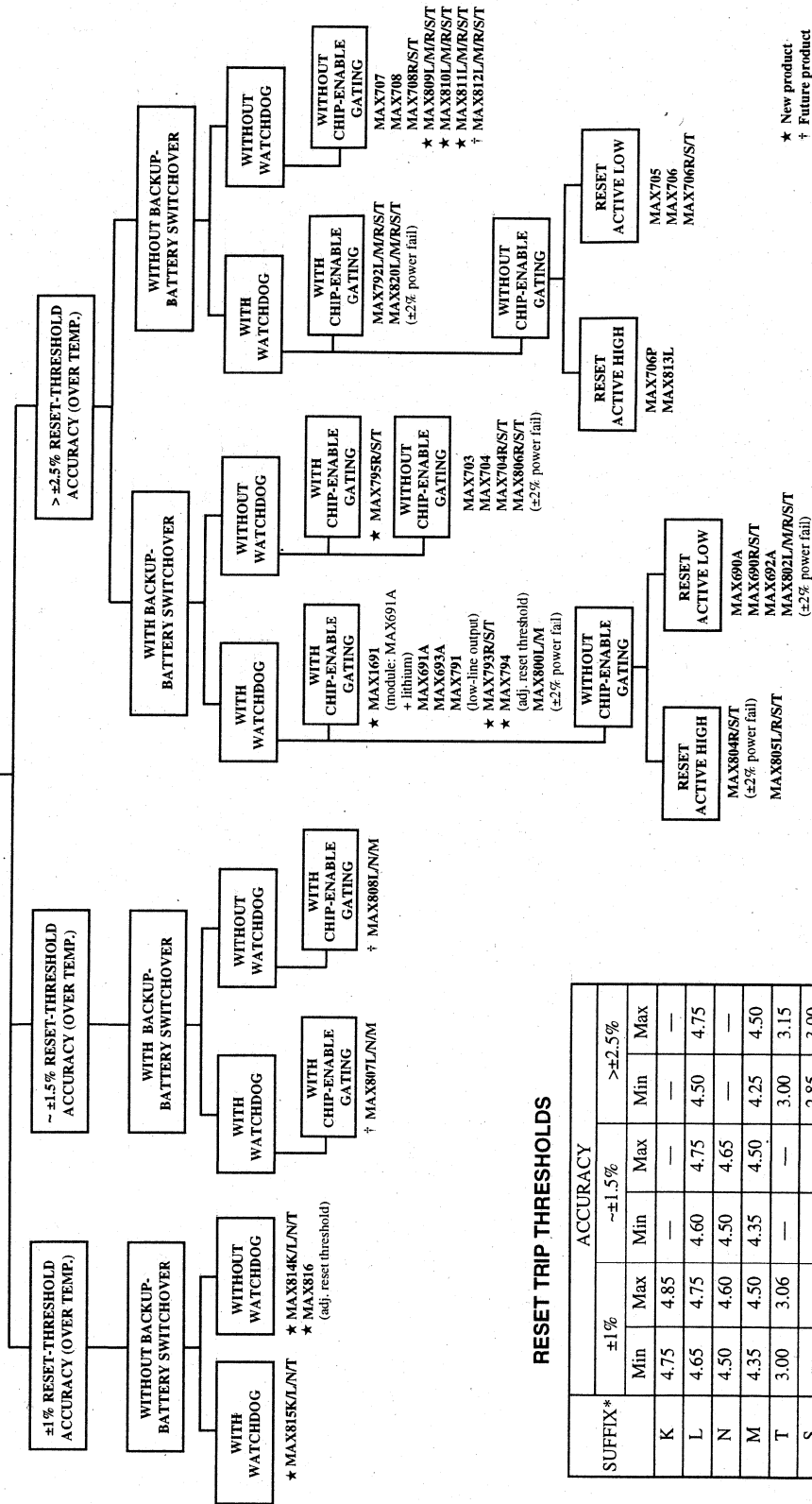
μP Supervisory Circuits

μP Supervisory Circuits, Product Tables and Trees	5-2
MAX1691 Integrated μP Supervisory Module w/ Lithium Backup Battery	5-5
MAX793 3V/3.3V Adjustable μP Supervisory Circuit w/ Battery OK Output	5-21
MAX794 3V/3.3V Adjustable μP Supervisory Circuit w/ Programmable Reset Threshold	5-21
MAX795 3V/3.3V Adjustable μP Supervisory Circuit in 8-Pin DIP/SO	5-21
MAX807L/ M/N μP Supervisory Circuit w/ ±1.5% Reset Accuracy*	5-41
MAX809L/ M/R/S/T 3-Pin μP Reset Circuit w/ $\overline{\text{RESET}}$ Output	5-43
MAX810L/ M/R/S/T 3-Pin μP Reset Circuit w/ RESET Output	5-43
MAX811L/ M/R/S/T 4-Pin μP Voltage Monitor w/ Manual $\overline{\text{RESET}}$ Output	5-49
MAX812L/ M/R/S/T 4-Pin μP Voltage Monitor w/ Manual RESET Output**	5-49
MAX814 High-Accuracy (±1%), Low-Power, 3V & 5V μP Supervisory Circuit w/ Low-Line Detector	5-57
MAX815 High-Accuracy (±1%), Low-Power, 3V & 5V μP Supervisory Circuit w/ Watchdog Input	5-57
MAX816 High-Accuracy (±1%), Low-Power, 3V & 5V μP Supervisory Circuit w/ Adjustable Reset Threshold	5-57

*Advance Information—first page of data sheet in preparation.

**Future Product.

µP SUPERVISORY CIRCUITS



★ New product
† Future product

RESET TRIP THRESHOLDS

SUFFIX*	ACCURACY					
	±1%		~±1.5%		>±2.5%	
	Min	Max	Min	Max	Min	Max
K	4.75	4.85	—	—	—	—
L	4.65	4.75	4.60	4.75	4.50	4.75
N	4.50	4.60	4.50	4.65	—	—
M	4.35	4.50	4.35	4.50	4.25	4.50
T	3.00	3.06	—	—	3.00	3.15
S	—	—	—	—	2.85	3.00
R	—	—	—	—	2.55	2.70

* Not all parts have suffix indicator for trip thresholds.
See µP Supervisory Circuits table for specific information.

µP Supervisory Circuits

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	RESET Valid to VCC = 1V	Nominal Watchdog Timeout Period (sec), if Available	Separate Watchdog Output	Backup-Battery Switch	V _{CC} -to-V _{OUT} On-Resistance Max (Ω)	V _{BATT} -to-V _{OUT} On-Resistance Max (Ω)	CE Write Protect	Power-Fail Comparator	Manual-Reset Input	Low-Line Output	Battery-On Output	ISUPPLY Operating Mode mA (typ)	ISUPPLY Backup Mode mA (typ)	Pins	Price 1000-up (\$)
MAX1232	4.37/4.62	250	✓	✓	✓	0.150/0.12	✓	✓	10	400	✓	✓	✓	✓	✓	0.2(0.05)	5(0.05)	8	1.71
MAX690A/692A	4.65/4.40	140	✓	✓	✓	1.6	✓	✓	6	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8	3.26
MAX690R/ST	2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓	6	400	✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	8	3.23
MAX691A/693A	4.65/4.40	140/adj.	✓	✓	✓	1.6/adj.	✓	✓	1.2	25	✓	✓	✓	✓	✓	0.1(0.035)	5(0.04)	16	3.61
MAX1691	The MAX1691 is a module with the MAX691A and a 125mAh lithium battery																		
MAX696	Adj.	35/adj.	✓	✓	✓	1.6/adj.	✓	✓			✓	✓	✓	✓	✓			16	7.32
MAX697	Adj.	35/adj.	✓	✓	✓	1.6/adj.	✓	✓			✓	✓	✓	✓	✓			16	3.55
MAX700	4.65/adj.	200	✓	✓	✓		✓	✓			✓	✓	✓	✓	✓			16	3.58
MAX703/704	4.65/4.40	140	✓	✓	✓		✓	✓	10	400	✓	✓	✓	✓	✓	0.2(0.1)		8	2.17
MAX704R/ST	2.63/2.93/3.08	140	✓	✓	✓		✓	✓	6	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8	1.38*
MAX705/706	4.65/4.40	140	✓	✓	✓	1.6	✓	✓			✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	8	2.93
MAX706P	2.63	140	✓	✓	✓	1.6	✓	✓			✓	✓	✓	✓	✓	0.35(0.2)		8	1.02*
MAX706R/ST	2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓			✓	✓	✓	✓	✓	0.35(0.2)		8	1.71
MAX707/708	4.65/4.40	140	✓	✓	✓	1.6	✓	✓			✓	✓	✓	✓	✓	0.35(0.2)		8	1.71
MAX708R/ST	2.63/2.93/3.08	140	✓	✓	✓		✓	✓			✓	✓	✓	✓	✓	0.35(0.2)		8	0.88*
MAX791	4.65	140	✓	✓	✓	1	✓	✓	1.2	25	✓	✓	✓	✓	✓	0.15(0.06)	5(0.04)	16	3.90
MAX792L/M/R/ST	4.65/4.40/ 2.63/2.93/3.08	140	✓	✓	✓	1	✓	✓			✓	✓	✓	✓	✓	0.15(0.07)		16	3.42
MAX793R/ST	2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓	0.4	400	✓	✓	✓	✓	✓	6(0.46)	1	16	3.48
MAX794	Adj.	140	✓	✓	✓	1.6	✓	✓	0.4	400	✓	✓	✓	✓	✓	6(0.46)	1	16	3.48
MAX795R/ST	2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓	0.4	400	✓	✓	✓	✓	✓	6(0.46)	1	8	3.41
MAX800L/M	4.60/4.40	140	✓	✓	✓	1.6/adj.	✓	✓	1.2	25	✓	✓	✓	✓	✓	0.1(0.035)	5(0.04)	16	3.88
MAX802L/M/R/ST	4.60/4.40/ 2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓	10	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8	3.59
MAX804R/ST	2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓	6	400	✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	8	3.66
MAX805L/R/ST	4.65/2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓	10	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8	3.26
MAX806R/ST	2.63/2.93/3.08	140	✓	✓	✓	1.6	✓	✓	6	400	✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	8	3.90
MAX807L/N/M	4.68/4.58/4.43	140	✓	✓	✓	1.6	✓	✓	TBD	TBD	✓	✓	✓	✓	✓	TBD	TBD	8	††
MAX808L/N/M	4.68/4.58/4.43	140	✓	✓	✓	1.6	✓	✓	TBD	TBD	✓	✓	✓	✓	✓	TBD	TBD	16	††
MAX809L/M/R/ST	4.65/4.40/ 2.63/2.93/3.08	140	✓	✓	✓		✓	✓			✓	✓	✓	✓	✓	0.06(0.024)		3	0.80**
MAX810L/M/R/ST	4.65/4.40	140	✓	✓	✓		✓	✓								0.06(0.024)		3 (SOT-23)	
MAX811L/M/R/ST	4.65/4.40/ 2.63/2.93/3.08	140	✓	✓	✓		✓	✓				✓	✓					4 (SOT-23)	0.80**
MAX812L/M/R/ST	4.65/4.40/ 2.63/2.93/3.08	140	✓	✓	✓		✓	✓				✓	✓					4 (SOT-143)	0.94**
MAX813L	4.65	140	✓	✓	✓	1.6	✓	✓					✓					4 (SOT-143)	††
MAX814K/L/N/T	4.80/4.70/4.55/3.03	140	✓	✓	✓		✓	✓			✓	✓	✓			0.35(0.2)		8	1.02*
MAX815K/L/N/T	4.80/4.70/4.55/3.03	140	✓	✓	✓	1.6	✓	✓			✓	✓	✓	✓	✓	TBD	TBD	8	4.39
MAX816	Adj. ±1%	140	✓	✓	✓		✓	✓			✓	✓	✓	✓	✓	TBD	TBD	8	4.74
MAX820L/M/R/ST	4.65/4.40/ 2.63/2.93/3.08	140	✓	✓	✓	1	✓	✓			✓	✓	✓	✓	✓	0.15(0.07)		16	4.39
MXD1210	4.37/4.62							✓	2.5	667	✓	✓	✓	✓	✓	0.5(0.23)	0.1(0.002)	8	2.44

† Prices provided are for design guidance and are FOB USA (unless otherwise noted). International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

* 25,000 pc. price, factory direct ** 2500 pc. price, factory direct. Only factory-direct orders in multiples of 2500 pieces accepted.



Integrated μ P Supervisor Module with Lithium Backup Battery

General Description

The MAX1691 reduces the complexity and number of components required for power-supply monitoring and battery control functions in microprocessor (μ P) systems. The MAX1691 features switchover to internal backup battery, write protection of CMOS RAM or EEPROM, and a watchdog function.

The internal +3V, 125mAh lithium battery connects to the μ P supervisory circuit through external pin strapping, minimizing battery drain during shipping.

The MAX1691 is shipped in special nonconductive material. **Note: Storing the MAX1691 in conductive foam will discharge the internal battery.**

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μ P Power Monitoring

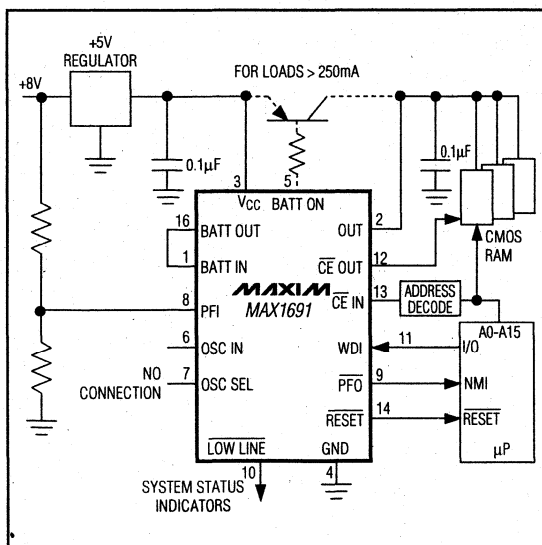
Features

- ♦ Internal 3V, 125mAh Lithium Battery
- ♦ 200ms Power OK / Reset Time Delay
- ♦ 1 μ A Standby Current, 35 μ A Operating Current
- ♦ On-Board Gating of Chip-Enable Signals, 10ns Max Delay
- ♦ Voltage Monitor for Power-Fail or Low-Battery Warning
- ♦ 16-Pin, 0.6" Plastic DIP Module

Ordering Information

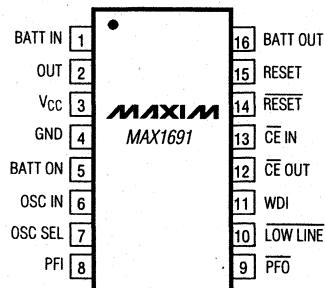
PART	TEMP. RANGE	PIN-PACKAGE
MAX1691CHE	0°C to +70°C	16 Plastic 0.6" Wide DIP Module

Typical Operating Circuit



Pin Configuration

TOP VIEW



0.6" Wide DIP Module



Integrated μ P Supervisor Module with Lithium Backup Battery

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V_{CC} -0.3V to +6V
All Other Inputs (Note 1) -0.3V to (V_{OUT} + 0.3V)

Input Current

BATT OUT 0mA to -25mA
V_{CC} Peak 1.0A
V_{CC} Continuous 250mA
BATT IN Peak 250mA
BATT IN Continuous 25mA
GND $\pm$ 25mA
All Other Outputs $\pm$ 25mA

Continuous Power Dissipation

Plastic DIP Module (derate 8.70mW/ $^{\circ}$ C) 696mW

Operating Temperature Range 0 $^{\circ}$ C to +70 $^{\circ}$ C

Storage Temperature Range -40 $^{\circ}$ C to +70 $^{\circ}$ C

Lead Temperature (soldering, 10sec) +260 $^{\circ}$ C

Note 1: The input voltage limits on PFI and WDI may be exceeded if the current into these pins is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V, V_{BATT IN} = 2.8V applied externally, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V _{CC}			0	5.0	5.5	V
Output Voltage, V _{OUT}	V _{CC} = 4.5V	I _{OUT} = 25mA	V _{CC} - 0.05	V _{CC} - 0.02		V
		I _{OUT} = 250mA	V _{CC} - 0.3	V _{CC} - 0.2		
V _{CC} to OUT On-Resistance	V _{CC} = 4.5V		0.8		1.2	Ω
V _{OUT} in Battery-Backup Mode	V _{CC} < V _{BATT IN} , I _{OUT} = 100μA		V _{BATT IN} - 0.25			V
Supply Current in Normal Operating Mode (Excludes I _{OUT})	V _{CC} > V _{BATT IN}		35		100	μA
Supply Current in Battery-Backup Mode (Excludes I _{OUT}) (Note 2)	V _{CC} > V _{BATT IN} - 1.2V	T _A = +25°C	0.04		1	μA
		T _A = T _{MIN} to T _{MAX}	5			
V _{BATT IN} Standby Current (Note 3)	V _{BATT IN} + 0.2V ≤ V _{CC}	T _A = +25°C	-0.1		0.02	μA
		T _A = T _{MIN} to T _{MAX}	-1.0		0.02	
Battery-Switchover Threshold	Power-up		V _{BATT IN} + 0.03		V	
	Power-down		V _{BATT IN} - 0.03			
Battery-Switchover Hysteresis			60			mV
BATT ON Output Low Voltage	I _{SINK} = 3.2mA				0.4	V
BATT ON Output Short-Circuit Current	Sink current		60			mA
	Source current		1	15	100	μA
Battery Capacity (Note 4)			125			mAh
Internal Battery Voltage (Note 4)			2.9			V
RESET AND WATCHDOG TIMER						
Reset Threshold Voltage			4.50	4.65	4.75	V
Reset Threshold Hysteresis			15			mV
V _{CC} to RESET Delay	Power-down		80			μs
LOW LINE to RESET Delay			800			ns
Reset Active Timeout Period, Internal Oscillator	Power-up		140	200	280	ms

Integrated μ P Supervisor Module with Lithium Backup Battery

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 4.75V$ to $5.5V$, $V_{BATT IN} = 2.8V$ applied externally, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $+25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Active Timeout Period, External Clock	Power-up		2048		Clock Cycles
Watchdog Timeout Period, Internal Oscillator	Long period	1.00	1.60	2.25	sec
	Short period	70	100	140	ms
Watchdog Timeout Period, External Clock	Long period		4096		Clock Cycles
	Short period		1024		Clock Cycles
Minimum Watchdog Input Pulse Width	V _{IL} = 0.8V, (V _{IH} = 0.75) (V _{CC})	100			ns
RESET Output Voltage	I _{SINK} = 50μA, V _{CC} = 1V, V _{BATT IN} = 0V, V _{CC} falling		0.004	0.300	V
	I _{SINK} = 3.2mA, V _{CC} = 4.25V		0.1	0.4	
	I _{SOURCE} = 1.6mA, V _{CC} = 5V	3.5			
RESET Output Short-Circuit Current	Output sink current		60		mA
	Output source current		7	20	
RESET Output Voltage Low (Note 5)	I _{SINK} = 3.2mA		0.1	0.4	V
RESET Output Short-Circuit Current (Note 5)	Output sink current		60		mA
LOW LINE Output Voltage	I _{SINK} = 3.2mA, V _{CC} = 4.25V			0.4	V
	I _{SOURCE} = 1μA, V _{CC} = 5V	3.5			
LOW LINE Output Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	μA
WDI Threshold Voltage (Note 6)	V _{IH}	0.75 x V _{CC}			V
	V _{IL}			0.8	
WDI Input Current	WDI = 0V	-50	-10		μA
	WDI = V _{OUT}		20	50	
POWER-FAIL COMPARATOR					
PFI Input Threshold	V _{CC} = 5V	1.20	1.25	1.30	V
PFI Leakage Current			±0.01	±25	nA
PFO Output Voltage	I _{SINK} = 3.2mA			0.4	V
	I _{SOURCE} = 1μA, V _{CC} = 5V	3.5			
PFO Output Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	μA
PFI to PFO Delay	V _{IN} = -20mV, V _{OD} = 15mV		25		μs
	V _{IN} = 20mV, V _{OD} = 15mV		60		
CHIP-ENABLE GATING					
CE IN Leakage Current	Disabled mode		±0.005	±1	μA
CE IN to CE OUT Resistance (Note 7)	Enabled mode		75	150	Ω
CE OUT Short-Circuit Current (Reset Active)	Disabled mode, CE OUT = 0V	0.10	0.75	2.00	mA
CE IN to CE OUT Propagation Delay (Note 8)	50Ω source impedance driver, C _{LOAD} = 50pF		6	10	ns
CE OUT Output Voltage High (Reset Active)	V _{CC} = 5V, I _{OUT} = -100μA	3.5			V
	V _{CC} = 0V, V _{BATT IN} = 2.8V, I _{OUT} = 1μA	2.7			
RESET to CE OUT Delay	Power-down		12		μs

Integrated μ P Supervisor Module with Lithium Backup Battery

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 4.75V$ to $5.5V$, $V_{BATT IN} = 2.8V$ applied externally, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL OSCILLATOR					
OSC IN Leakage Current	OSC SEL = 0V		0.10	± 5	μA
OSC IN Input Pull-Up Current	OSC SEL = V_{OUT} or floating, OSC IN = 0V		10	100	μA
OSC SEL Input Pull-Up Current	OSC SEL = 0V		10	100	μA
OSC IN Frequency Range	OSC SEL = 0V		50		kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V, $C_{OSC} = 47pF$		100		kHz

Note 2: The supply current drawn from the battery excluding I_{OUT} typically goes to $18\mu A$ when $(V_{BATT IN} - 1V) < V_{CC} < V_{BATT IN}$. In most applications, this is a brief period as V_{CC} falls through this region.

Note 3: "+" = battery-discharging current, "-" = battery-charging current.

Note 4: See *Typical Operating Characteristics*.

Note 5: RESET is an open-drain output and sinks current only.

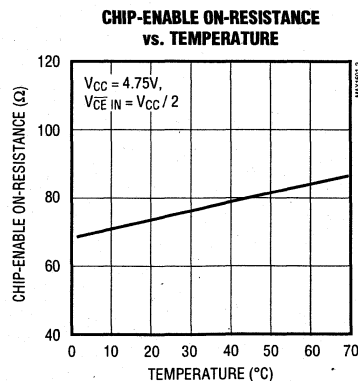
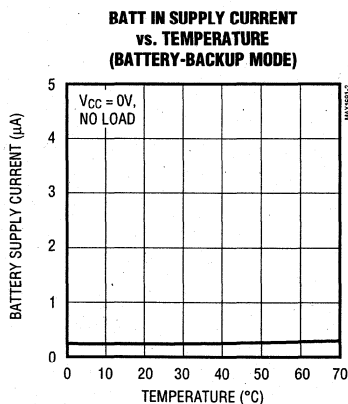
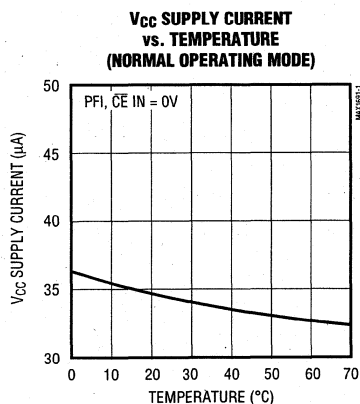
Note 6: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

Note 7: The chip-enable resistance is tested with $V_{CC} = 4.75V$, $V_{CE IN} = V_{CE OUT} = V_{CC} / 2$.

Note 8: The chip-enable propagation delay is measured from the 50% point at $\overline{CE IN}$ to the 50% point at $\overline{CE OUT}$.

Typical Operating Characteristics

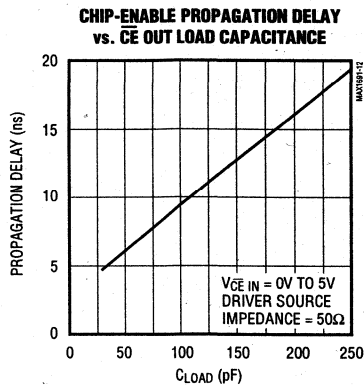
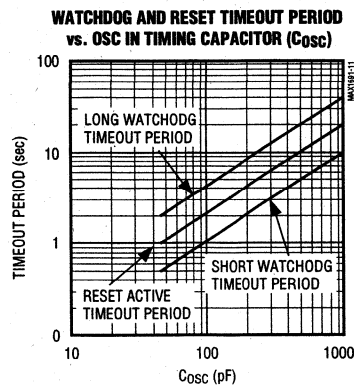
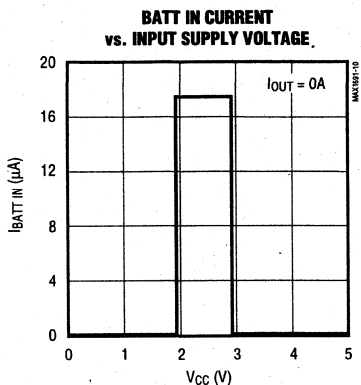
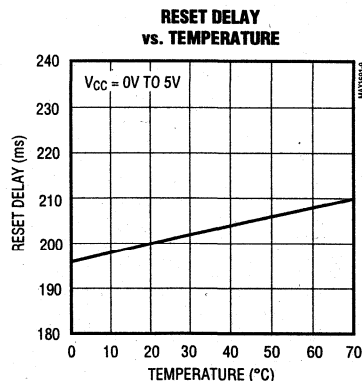
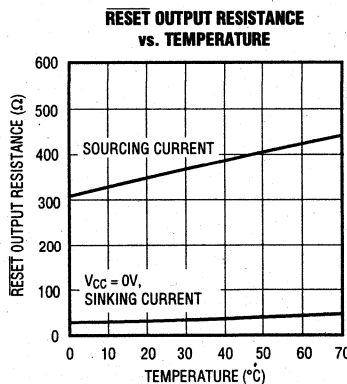
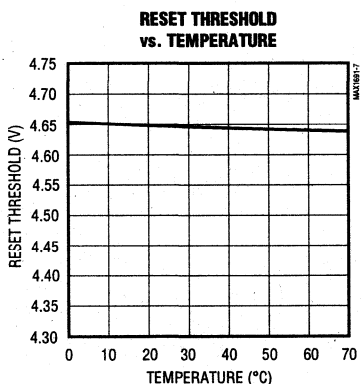
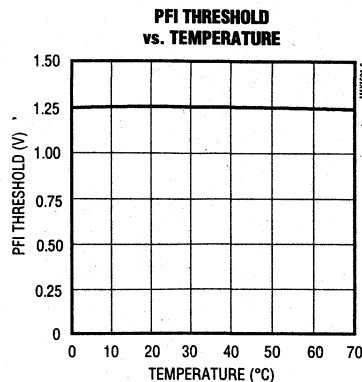
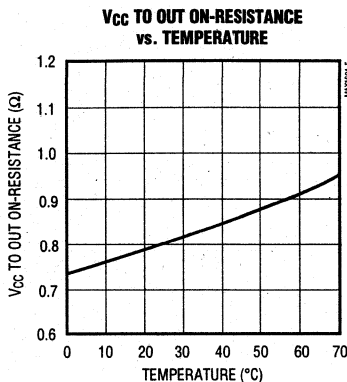
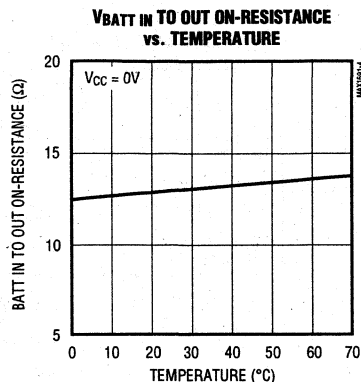
($V_{BATT IN} = 2.8V$ externally applied, $V_{CC} = 5.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



Integrated μ P Supervisor Module with Lithium Backup Battery

Typical Operating Characteristics (continued)

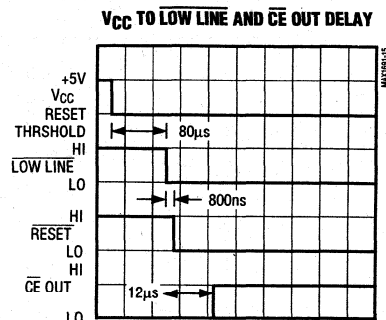
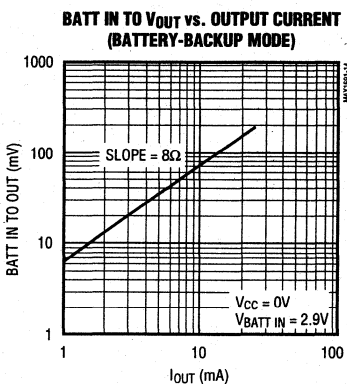
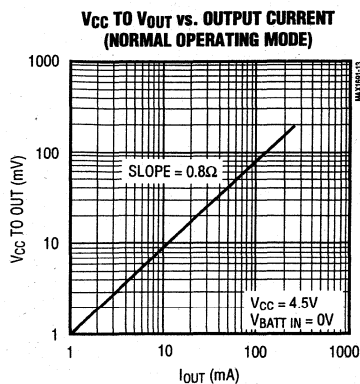
($V_{BATT\ IN} = 2.8V$ externally applied, $V_{CC} = 5.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



Integrated μ P Supervisor Module with Lithium Backup Battery

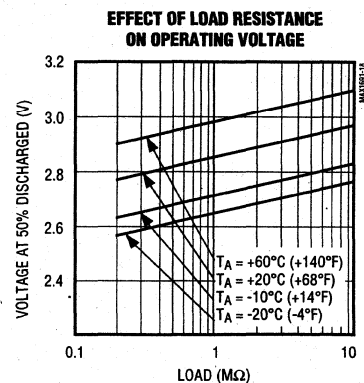
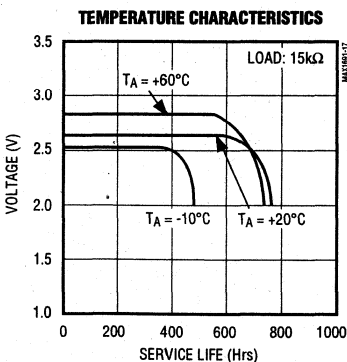
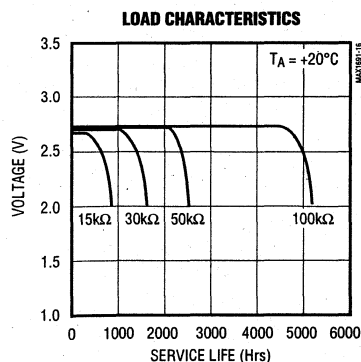
Typical Operating Characteristics (continued)

($V_{BATT\ IN} = 2.8V$ externally applied, $V_{CC} = 5.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



Typical Battery Characteristics*

(Note 9)



*Source: Rayovac

Note 9: Nominal voltage is 3.0V, nominal capacity is 130mAh at 30k Ω to 2.0V at +21°C. Typical storage life is less than 0.5% per year at +21°C. Operating temperature range is -40°C to +70°C; prolonged operation and/or storage at elevated temperatures affects life and reliability.

Integrated μ P Supervisor Module with Lithium Backup Battery

Pin Description

PIN	NAME	FUNCTION
1	BATT IN	Backup-battery input. Connect to BATT OUT.
2	OUT	Output supply voltage connects to VCC when VCC is greater than VBATT IN and above the reset threshold. When VCC falls below VBATT IN and is below the reset threshold, OUT connects to BATT IN. Connect a 0.1 μ F capacitor from OUT to GND.
3	VCC	Input supply voltage, +5V input.
4	GND	Ground. 0V reference for all signals. Connected to the negative terminal of the internal battery.
5	BATT ON	Battery-on output goes high when OUT switches to BATT IN. BATT ON goes low when OUT switches to VCC. Connect the base of a PNP to BATT ON for OUT current requirements greater than 250mA.
6	OSC IN	External oscillator input. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. The timing can be adjusted by connecting an external capacitor to this pin (Figure 2). When OSC SEL is high or floating, OSC IN selects between fast and slow watchdog timeout periods.
7	OSC SEL	Oscillator select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and the watchdog timeout period. Setting OSC SEL low enables OSC IN (Table 1). OSC SEL has a 10 μ A internal pull-up.
8	PFI	Power-fail input is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, PFO goes low. Connect PFI to GND or OUT when not used.
9	PFO	Power-fail output is the output of the power-fail comparator. PFO goes low when PFI is less than 1.25V. PFO is an uncommitted comparator, and has no effect on any other internal circuitry.
10	LOW LINE	LOW LINE output goes low when VCC falls below the reset threshold. It returns high as soon as VCC rises above the reset threshold.
11	WDI	Watchdog input—a three level input. If WDI remains either high or low for longer than the watchdog timeout period, reset is asserted. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between OUT and GND that sets it to mid-supply when left unconnected.
12	CE OUT	Chip-enable output goes low only when CE IN is low and VCC is above the reset threshold. If CE IN is low when reset is asserted, CE OUT will stay low for 12 μ s or until CE IN goes high, whichever occurs first.
13	CE IN	Chip-enable input to CE gating circuit. Connect to GND or OUT if not used.
14	RESET	RESET output goes low whenever VCC falls below the reset threshold. RESET remains low typically for 200ms after VCC crosses the reset threshold on power-up.
15	RESET	Active-high reset output is open drain and the inverse of RESET.
16	BATT OUT	Battery output connects to the positive terminal of the internal 125mAh lithium battery. Connect BATT OUT to BATT IN.

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Integrated μ P Supervisor Module with Lithium Backup Battery

Detailed Description

The MAX1691 combines a MAX691A integrated circuit and a 125mAh battery in one package. All pins on the MAX691A are available on the MAX1691 except WDO. The MAX1691 is not pin compatible with the MAX691A.

RESET and RESET Outputs

The MAX1691's $\overline{\text{RESET}}$ and RESET outputs ensure the μ P (with reset inputs either asserted high or low) powers up in a known state and prevent code execution errors during power-down or brownout conditions.

The active-low $\overline{\text{RESET}}$ output both sources and sinks current, while the open-drain RESET output sinks current only. For a battery voltage $\geq 2\text{V}$, $\overline{\text{RESET}}$ and RESET remain valid for V_{CC} from 0V to 5.5V. $\overline{\text{RESET}}$ and RESET are asserted when V_{CC} falls below the 4.65V reset threshold and typically remain asserted for 200ms after V_{CC} rises above the reset threshold on power-up (Figure 1). The MAX1691 battery switchover comparator does not affect reset assertion. However, both reset outputs are asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter battery-backup mode.

Watchdog Function

The watchdog monitors μ P activity via the watchdog input (WDI). If the μ P becomes inactive, $\overline{\text{RESET}}$ and

RESET are asserted. To use the watchdog function, connect WDI to a bus line or μ P input/output (I/O) line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), $\overline{\text{RESET}}$ and RESET are asserted (see *RESET and RESET Outputs* section).

WDI Watchdog Input

Changing WDI's state (high-to-low, low-to-high, or a minimum 100ns pulse) during the watchdog period resets the watchdog timer. The watchdog timer default period is 1.6sec.

Disable the watchdog function by floating WDI. An internal resistor network (100k Ω equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Selecting Alternative Watchdog and Reset Timeout Periods

The OSC SEL and OSC IN inputs control the watchdog and reset timeout periods. Floating OSC SEL and OSC IN or tying them both to OUT selects the nominal 1.6sec watchdog timeout period and 200ms reset timeout period. Connecting OSC IN to GND and floating or

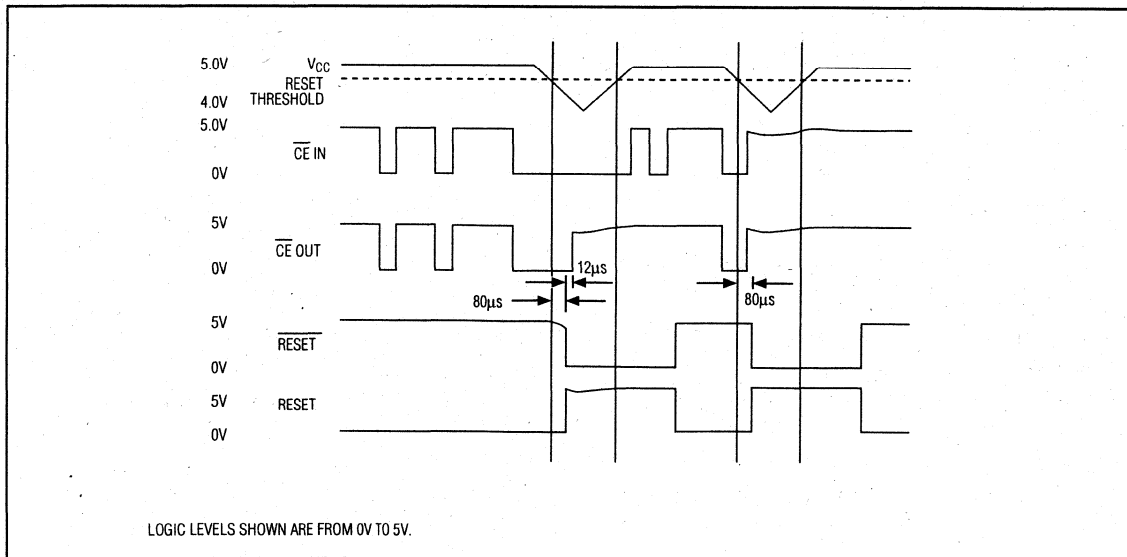


Figure 1. Reset and Chip-Enable Timing

Integrated μ P Supervisor Module with Lithium Backup Battery

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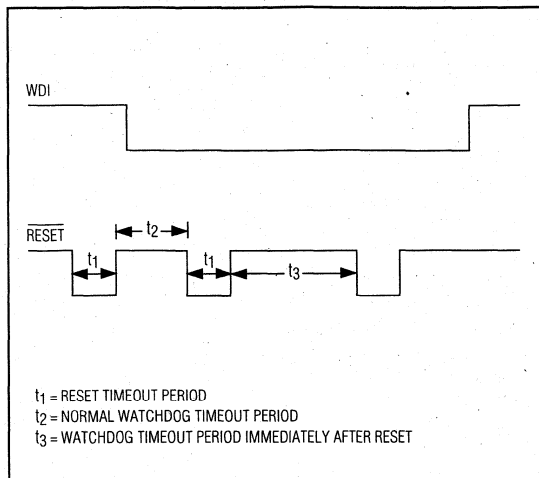


Figure 2. Watchdog Timeout Period and Reset Active Time

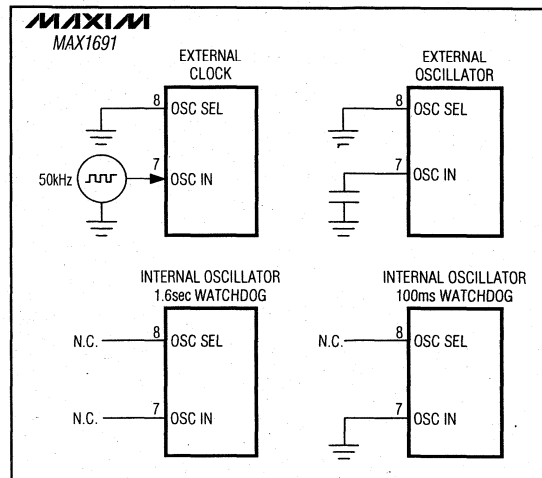


Figure 3. Oscillator Circuits

Table 1. Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
Low	External clock input	1-24 clks	4096 clks	2048 clks
Low	External capacitor	$(600/47\text{pF} \times \text{C})\text{ms}$	$(2.4/47\text{pF} \times \text{C})\text{sec}$	$(1200/47\text{pF} \times \text{C})\text{ms}$
Floating	Low	100ms	1.6sec	200ms
Floating	Floating	1.6sec	1.6sec	200ms

connecting OSC SEL to OUT selects the 100ms normal watchdog timeout delay and 1.6sec delay immediately after reset. The reset timeout delay remains 200ms (Figure 2). Select alternative timeout periods by connecting OSC SEL to GND and a capacitor between OSC IN and GND or externally driving OSC IN (see Table 1 and Figure 3).

Chip-Enable Signal Gating

The MAX1691 provides internal gating of chip-enable signals to prevent erroneous data from being written to CMOS RAM in case of power failure. During normal operation, the chip-enable gate is enabled and passes all chip-enable (CE) transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX1691 uses a series transmission gate from $\overline{\text{CE}}$ IN to $\overline{\text{CE}}$ OUT (Figure 4).

The 10ns (max) CE propagation delay from $\overline{\text{CE}}$ IN to $\overline{\text{CE}}$ OUT makes the MAX1691 compatible with most μ Ps (Figure 5 shows the test circuit for CE propagation delay).

$\overline{\text{CE}}$ IN Chip-Enable Input

$\overline{\text{CE}}$ IN is high impedance (disabled mode) while RESET and $\overline{\text{RESET}}$ are asserted.

During a power-down sequence where V_{CC} falls below the reset threshold, or when a watchdog fault occurs, $\overline{\text{CE}}$ IN assumes a high-impedance state when the voltage at $\overline{\text{CE}}$ IN goes high or 15 μ s after reset is asserted, whichever occurs first (Figure 1).

During a power-up sequence, $\overline{\text{CE}}$ IN remains high impedance regardless of CE IN activity until reset is deasserted following the reset timeout period. In the low-impedance mode, CE IN's impedance appears as a 75 Ω resistor in series with the load at $\overline{\text{CE}}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{\text{CE}}$ IN and the capacitive loading on the chip-enable output ($\overline{\text{CE}}$ OUT) (see Chip-Enable Propagation Delay vs. $\overline{\text{CE}}$ OUT Load Capacitance in the *Typical Operating Characteristics*). The CE propagation delay

Integrated μ P Supervisor Module with Lithium Backup Battery

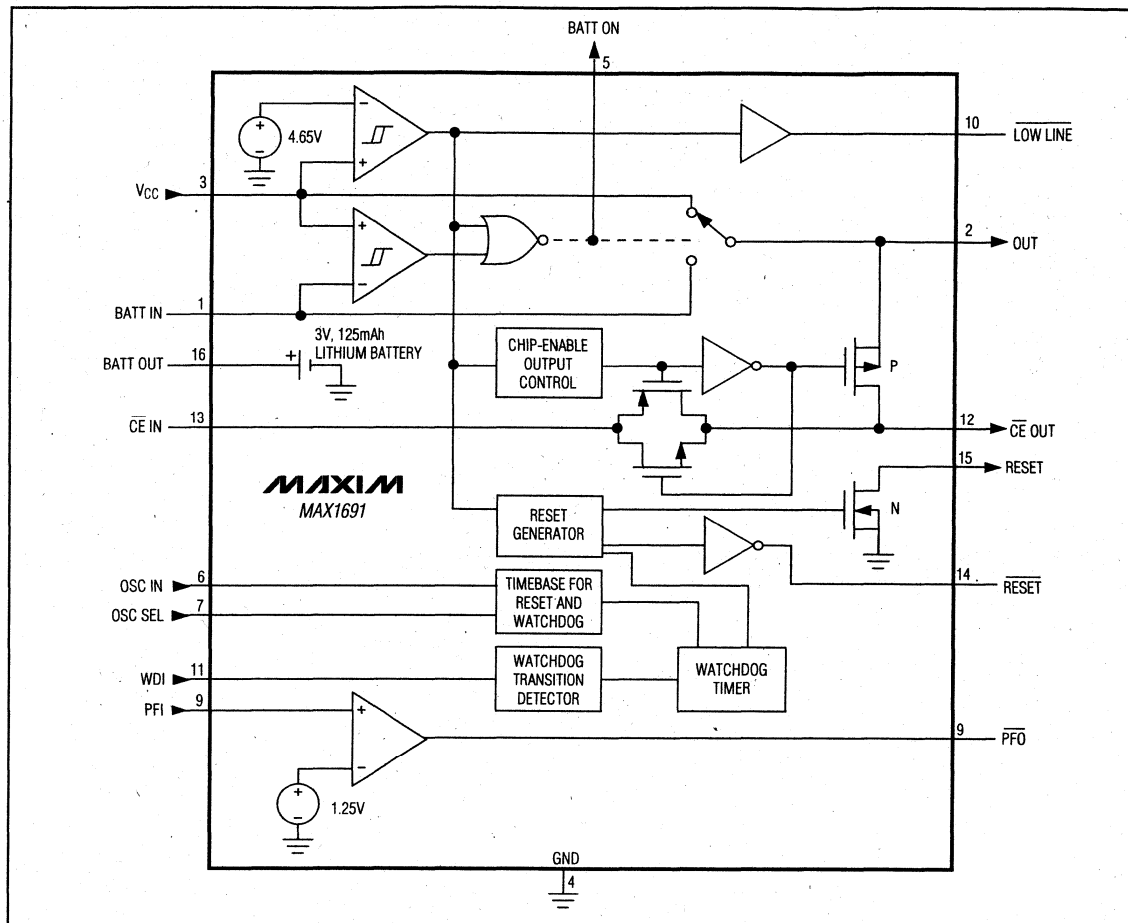


Figure 4. Block Diagram

is production tested from the 50% point of $\overline{\text{CE IN}}$ to the 50% point of $\overline{\text{CE OUT}}$ using a 50Ω driver and 50pF of load capacitance (Figure 5). For minimum propagation delay, minimize the capacitive load at $\overline{\text{CE OUT}}$ and use a low output impedance driver.

Chip-Enable Output $\overline{\text{CE OUT}}$

In the enabled mode, $\overline{\text{CE OUT}}$'s impedance is equivalent to 75Ω in series with the source driving $\overline{\text{CE IN}}$. In the disabled mode, the 75Ω analog switch is off and $\overline{\text{CE OUT}}$ is pulled to OUT. This source turns off when the analog gate is enabled.

LOW LINE Output

$\overline{\text{LOW LINE}}$ is the buffered output of the reset threshold comparator and is pulled low when V_{CC} is below the reset threshold. For normal operation (V_{CC} above the reset threshold), $\overline{\text{LOW LINE}}$ is pulled to OUT.

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the IC's other functions. Common uses include low-battery indication (Figure 6) and early power-fail warning (see *Typical Operating Circuit*).

Integrated μ P Supervisor Module with Lithium Backup Battery

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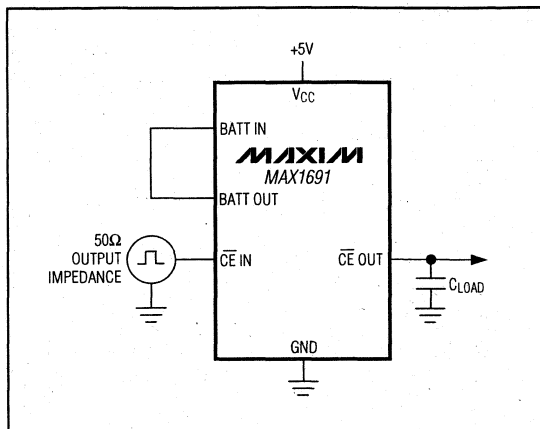


Figure 5. CE Propagation Delay Test Circuit

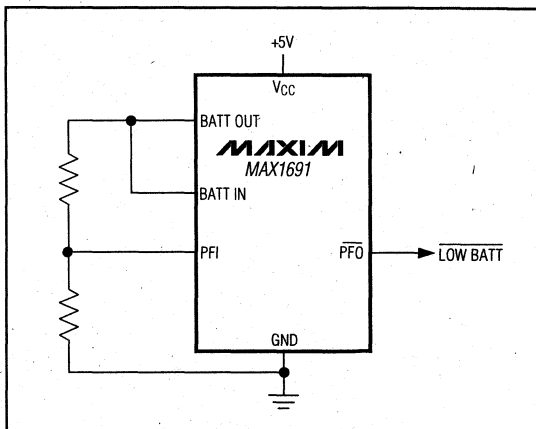


Figure 6. Low-Battery Indicator

PFI Power-Fail Input

PFI is the power-fail comparator's input. PFI has a guaranteed maximum input leakage of $\pm 25\text{nA}$ over temperature, so the current through the resistive divider connected to PFI should be at least $1\mu\text{A}$ to maintain trip point accuracy. The typical comparator delay is $25\mu\text{s}$ from V_{IL} to V_{OL} , and $70\mu\text{s}$ from V_{IH} to V_{OH} . If unused, connect PFI to ground.

PFO Power-Fail Output

The power-fail output ($\overline{\text{PFO}}$) goes low when PFI goes below 1.25V . It typically sinks 3.2mA with a 0.1V saturation voltage. With PFI above 1.25V , $\overline{\text{PFO}}$ is pulled to OUT with only $1\mu\text{A}$ source capability, so an external pull-up resistor is often required.

Battery-Backup Mode

The MAX1691 requires two conditions to switch to battery-backup mode: (1) V_{CC} must be below the reset threshold, and (2) V_{CC} must be below $V_{\text{BATT IN}}$. Table 2 lists the status of the inputs and outputs in battery-backup mode.

BATT ON Output

The battery-on (BATT ON) output indicates the status of the internal V_{CC} /battery switchover comparator, which in turn controls the internal V_{CC} and battery switches. For V_{CC} greater than $V_{\text{BATT IN}}$ (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at less than 0.1V saturation voltage. In battery-backup mode, BATT ON is pulled up to OUT. Use BATT ON to indicate battery switchover status or to supply base drive to an external PNP pass transistor for higher current applications (see *Typical Operating Circuit*).

Input Supply Voltage

The input supply voltage (V_{CC}) should be a regulated $+5\text{V}$. V_{CC} connects to OUT through a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA . The parallel diode carries any current in excess of 250mA . Both the switch and the diode have impedances less than 1Ω . The maximum continuous current is 250mA , but power-on transients may reach a maximum of 1A without damage (Figure 7).

Backup-Battery Input

The backup-battery input (BATT IN) is similar to the V_{CC} input except the PMOS switch and parallel diode are much smaller. Accordingly, the on-resistances of both the diode and the switch are each approximately 10Ω . Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA . The reverse leakage of BATT IN is less than $1\mu\text{A}$ over temperature and supply voltage. To use the internal 125mAh backup battery, connect BATT IN to BATT OUT.

Output Supply Voltage

The output supply voltage (OUT) pin internally connects to the IC's substrate and supplies current to the external system and internal circuitry. All open-circuit outputs except RESET will, for example, assume V_{OUT} in their high states and not the V_{CC} voltage. At the maximum source current of 250mA , V_{OUT} is typically 200mV below V_{CC} . Decouple this terminal with a $0.1\mu\text{F}$ capacitor to GND.

Integrated μ P Supervisor Module with Lithium Backup Battery

Table 2. Input and Output Status in Battery-Backup Mode

PIN	NAME	STATUS
1	BATT IN	Supply current is 1 μ A maximum.
2	OUT	OUT is connected to BATT IN through an internal PMOS switch.
3	V _{CC}	Battery switchover comparator monitors V _{CC} for active switchover.
4	GND	GND, 0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to V _{OUT} .
6	OSC IN	OSC IN is ignored.
7	OSC SEL	OSC SEL is ignored.
8	PFI	The power-fail comparator remains active in battery-backup mode until V _{CC} < V _{BATT IN} - 1.2V, below which PFI is inactive.
9	PFO	The power-fail comparator remains active in battery-backup mode until V _{CC} < V _{BATT IN} - 1.2V, below which PFO is inactive.
10	LOWLINE	Logic low.
11	WDI	Watchdog is ignored.
12	$\overline{\text{CE}}$ IN	High impedance.
13	$\overline{\text{CE}}$ OUT	Logic high. The open-circuit voltage is equal to V _{OUT} .
14	RESET	Logic low.
15	RESET	High impedance.
16	BATT OUT	Connect BATT OUT to BATT IN.

Applications Information

The MAX1691 is not short-circuit protected. Shorting OUT to ground will destroy the device.

If long leads connect to the chip inputs, ensure these leads are free from ringing and other conditions that would forward bias the chip's protection diodes.

Storing the MAX1691 in conductive foam can slowly discharge the internal battery.

There are three distinct modes of operation:

- (1) Normal operating mode with all circuitry powered up. Typical supply current from V_{CC} is 35 μ A while only leakage currents (<1 μ A) flow from the battery.
- (2) Battery-backup mode where V_{CC} is typically within 1.2V below V_{BATT IN}. All circuitry is powered up and the supply current from the battery is typically less than 60 μ A.
- (3) Battery-backup mode where V_{CC} is less than V_{BATT IN} by at least 1.2V. BATT IN supply current is 1 μ A max.

Alternative CE Gating

Using memory devices with both CE and $\overline{\text{CE}}$ inputs allows the CE loop to be bypassed. To do this, con-

nect $\overline{\text{CE}}$ IN to ground, pull up $\overline{\text{CE}}$ OUT to OUT and connect CE OUT to the CE input of each memory device as in Figure 8. The CE input of each part then connects directly to the chip select logic, which then does not have to be gated.

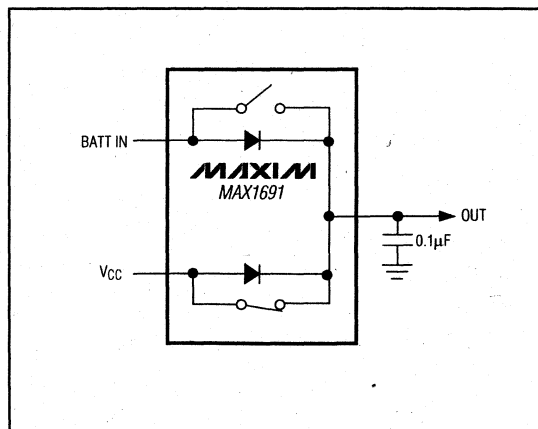
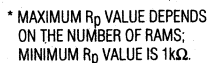


Figure 7. V_{CC} and BATT IN to OUT Switch

MAX 1691



*** OPTIONAL**

$$V_{TRIP} = 1.25V / \left(\frac{R_2}{R_1 + R_2} \right)$$

$$V_H = 1.25V / \left(\frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} \right)$$

$$\frac{V_L - 1.25V}{R_1} + \frac{5V - 1.25V}{R_3} = \frac{1.25V}{R_2}$$

Adding Hysteresis to the Power-Fail Comparator

Monitoring a Negative Voltage

NOTE: V_{TRIP} IS NEGATIVE.

MAXIM

Integrated μ P Supervisor Module with Lithium Backup Battery

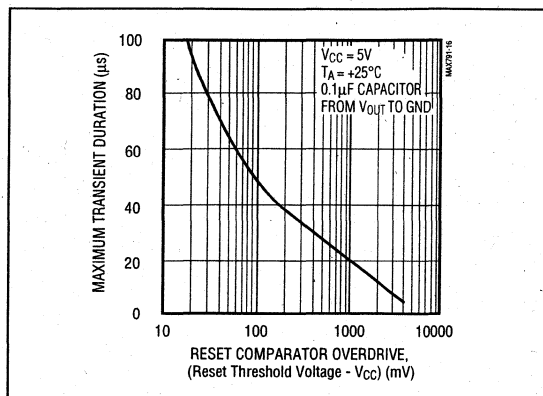


Figure 11. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Negative-Going V_{CC} Transients

While issuing resets to the μ P during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches). It is usually undesirable to reset the μ P when V_{CC} experiences only small glitches.

Figure 11 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40 μ s or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Connecting a Timing Capacitor at OSC IN

When OSC SEL is connected to ground, OSC IN disconnects from its internal 10 μ A (typ) pull-up and is internally connected to a ± 100 nA current source. When a capacitor is connected from OSC IN to ground (to select alternative reset and watchdog timeout periods), the current source charges and discharges the timing capacitor to create the oscillator that controls the reset and watchdog timeout period. To prevent timing errors or oscillator start-up problems, minimize external current leakage sources at this pin, and locate the capacitor as close to OSC IN as possible. The sum of

PC board leakage + OSC capacitor leakage must be small compared to ± 100 nA.

Maximum V_{CC} Fall Time

The V_{CC} fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/ μ s. A standard rule of thumb for filter capacitance on most regulators is on the order of 100 μ F per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial V_{CC} fall rate is just the inverse or 1A/100 μ F = 0.01V/ μ s. The V_{CC} fall rate decreases with time as V_{CC} falls exponentially, which more than satisfies the maximum fall-time requirement.

Watchdog Software Considerations

A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 12 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

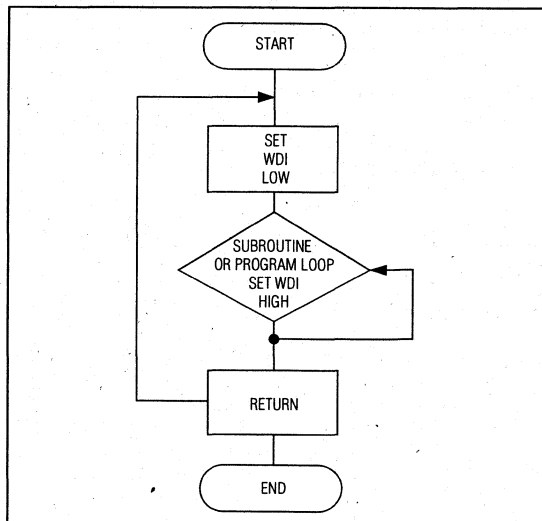


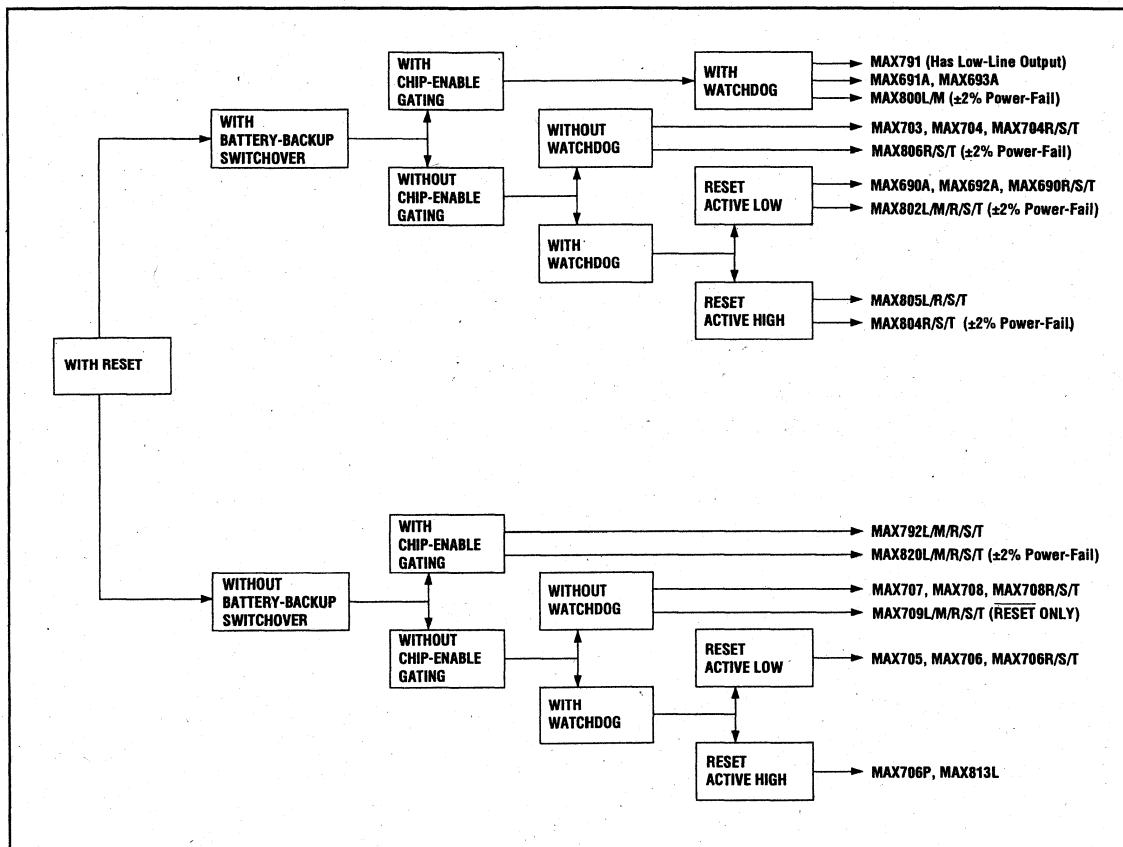
Figure 12. Watchdog Flow Diagram

Integrated μ P Supervisor Module with Lithium Backup Battery

Product Selection Guide

MAX1691

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3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

General Description

The MAX793/MAX794/MAX795 microprocessor (μ P) supervisory circuits monitor and control the activities of +3.0V/+3.3V μ Ps by providing backup-battery switchover, among other features such as low-line indication, μ P reset, write protection for CMOS RAM, and a watchdog (see the *Selector Guide* below). The backup-battery voltage can exceed V_{CC} , permitting the use of 3.6V lithium batteries in systems using 3.0V to 3.3V for V_{CC} .

The MAX793/MAX795 offer a choice of reset threshold voltage range (denoted by suffix letter): 3.00V to 3.15V (T), 2.85V to 3.00V (S), and 2.55V to 2.70V (R). The MAX794's reset threshold is set externally with a resistor divider. The MAX793/MAX794 are available in 16-pin DIP and narrow SO packages, and the MAX795 comes in 8-pin DIP and SO packages. For similar devices designed for 5V systems, see the μ P Supervisory Circuits table at the back of this data sheet.

Selector Guide

FEATURE	MAX793	MAX794	MAX795
Active-Low Reset	✓	✓	✓
Active-High Reset	✓	✓	
Programmable Reset Threshold		✓	
Low-Line Early Warning Output	✓	✓	
Backup-Battery Switchover	✓	✓	✓
External Switch Driver	✓	✓	✓
Power-Fail Comparator	✓	✓	
Battery OK Output	✓		
Watchdog Input	✓	✓	
Battery Freshness Seal	✓	✓	
Manual Reset Input	✓	✓	
Chip-Enable Gating	✓	✓	✓
Pins-Package	16-DIP/SO	16-DIP/SO	8-DIP/SO

Applications

Battery-Powered Computers and Controllers
 Embedded Controllers
 Intelligent Controllers
 Critical μ P Power Monitoring
 Portable Equipment

Pin Configurations appear at end of data sheet.

Features

MAX793/MAX794/MAX795

- ♦ Precision Supply-Voltage Monitor:
 Fixed Reset Trip Voltage (MAX793/MAX795)
 Adjustable Reset Trip Voltage (MAX794)
- ♦ Guaranteed Reset Assertion to $V_{CC} = 1V$
- ♦ Backup-Battery Power Switching—Battery Voltage Can Exceed V_{CC}
- ♦ On-Board Gating of Chip-Enable Signals—7ns Max Propagation Delay

MAX793/MAX794 Only

- ♦ Battery Freshness Seal
- ♦ Battery OK Output (MAX793)
- ♦ Uncommitted Voltage Monitor for Power-Fail or Low-Battery Warning
- ♦ Independent Watchdog Timer (1.6sec timeout)
- ♦ Manual Reset Input

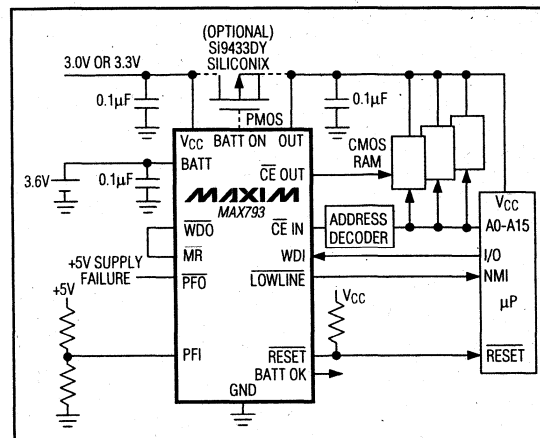
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX793_CPE	0°C to +70°C	16 Plastic DIP
MAX793_CSE	0°C to +70°C	16 Narrow SO
MAX793_EPE	-40°C to +85°C	16 Plastic DIP
MAX793_ESE	-40°C to +85°C	16 Narrow SO

Ordering Information continued on last page.

* The MAX793/MAX795 offer a choice of reset threshold voltage. Select the letter corresponding to the desired reset threshold voltage range (T = 3.00V to 3.15V, S = 2.85V to 3.00V, R = 2.55V to 2.70V) and insert it into the blank to complete the part number. The MAX794's reset threshold is adjustable.

Typical Operating Circuit



MAXIM

Maxim Integrated Products 5-21

Call toll free 1-800-998-8800 for free samples or literature.

MAX793/MAX794/MAX795

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3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V_{CC}-0.3V to 6.0V

V_{BATT}-0.3V to 6.0V

All Other Inputs-0.3V to the higher of V_{CC} or V_{BATT}

Continuous Input Current

V_{CC}200mA

V_{BATT}50mA

GND20mA

Output Current

V_{OUT}200mA

All Other Outputs20mA

Continuous Power Dissipation (T_A = +70°C)

8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)727mW

8-Pin SO (derate 5.88mW/°C above +70°C)471mW

16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)842mW

16-Pin Narrow SO (derate 9.52mW/°C above +70°C)696mW

Operating Temperature Ranges

MAX793_C_/_MAX794C_/_MAX795_C_ 0°C to +70°C

MAX793_E_/_MAX794E_/_MAX795_E_-40°C to +85°C

Storage Temperature Range-65°C to +160°C

Lead Temperature (soldering, 10sec)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.17V to 5.5V for the MAX793T/MAX795T, V_{CC} = 3.02V to 5.5V for the MAX793S/MAX795S, V_{CC} = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, V_{BATT} = 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V _{CC} , V _{BATT} (Note 1)		MAX79_C	1.0		5.5	V
		MAX79_E	1.1		5.5	
V _{CC} Supply Current (excluding I _{OUT} , I _{CE} OUT)	ISUPPLY	MAX793/MAX794, MR = V _{CC}	V _{CC} < 3.6V	46	60	μA
			V _{CC} < 5.5V	62	80	
		MAX795	V _{CC} < 3.6V	35	50	
			V _{CC} < 5.5V	49	70	
V _{CC} Supply Current in Battery-Backup Mode (excluding I _{OUT})	ISUPPLY	V _{CC} = 2.1V, V _{BATT} = 2.3V	MAX793/MAX794	32	45	μA
			MAX795	24	35	
BATT Supply Current (excluding I _{OUT}) (Note 2)					1	μA
BATT Leakage Current, Freshness Seal Enabled		V _{CC} = 0V, V _{OUT} = 0V			1	μA
Battery Leakage Current (Note 3)					0.5	μA
OUT Output Voltage in Normal Mode	V _{OUT}	I _{OUT} = 75mA	V _{CC} - 0.3	V _{CC} - 0.125		V
		I _{OUT} = 30mA (Note 4)	V _{CC} - 0.12	V _{CC} - 0.050		
		I _{OUT} = 250μA (Note 4)	V _{CC} - 0.001	V _{CC} - 0.5mV		
OUT Output Voltage in Battery-Backup Mode	V _{OUT}	V _{BATT} = 2.3V	I _{OUT} = 250μA	V _{BATT} - 0.1	V _{BATT} - 0.034	V
			I _{OUT} = 1mA		V _{BATT} - 0.14	
Battery Switch Threshold (V _{CC} falling)	V _{CC} - V _{BATT}	V _{SW} > V _{CC} > 1.75V (Note 5)		20	65	mV
	V _{SW}	V _{BATT} > V _{CC} (Note 6)	MAX793T/MAX795T	2.69	2.82	2.95
			MAX793S/MAX795S	2.55	2.68	2.80
			MAX793R/MAX795R/MAX794	2.30	2.41	2.52
Battery Switch Threshold (V _{CC} rising) (Note 7)	V _{CC} - V _{BATT}	This value is identical to the reset threshold, V _{CC} rising for V _{BATT} > V _{RST}				
		V _{BATT} < V _{RST}		25	65	mV

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

ELECTRICAL CHARACTERISTICS (continued)

(VCC = 3.17V to 5.5V for the MAX793T/MAX795T, VCC = 3.02V to 5.5V for the MAX793S/MAX795S, VCC = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, VBATT = 3.6V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Threshold (Note 8)	VRST	VCC Falling	MAX793T/MAX795T	3.00	3.075	3.15	V
			MAX793S/MAX795S	2.85	2.925	3.00	
			MAX793R/MAX795R	2.55	2.625	2.70	
		VCC Rising	MAX793T/MAX795T	3.00	3.085	3.17	
			MAX793S/MAX795S	2.85	2.935	3.02	
			MAX793R/MAX795R	2.55	2.635	2.72	
RESET IN Threshold (MAX794 only)	VRST IN	VCC Falling	1.212	1.240	1.262	V	
VCC Rising		1.212	1.250	1.282			
RESET IN Leakage Current (MAX794 only)			-25	2	25	nA	
Reset Timeout Period	tRP	VCC < 3.6V	140	200	280	ms	
LOWLINE-to-Reset Threshold, (V LOWLINE - VRST), VCC Falling	VLR	MAX793	30	45	60	mV	
		MAX794	5	15	25		
Low-Line Comparator Hysteresis		MAX793		10		mV	
		MAX794		10		mV	
LOWLINE Threshold, VCC Rising	VLL	MAX793T/MAX795T			3.23	V	
		MAX793S/MAX795S			3.08		
		MAX793R/MAX795R			2.78		
		MAX794			1.317		
PFI Input Threshold	VTH	VPFI falling	1.212	1.240	1.262	V	
		VPFI rising	1.212	1.250	1.287		
PFI Input Current			-25	2	25	nA	
PFI Hysteresis, PFI Rising				10	20	mV	
BATT OK Threshold (MAX793)	VBOK		2.00	2.25	2.50	V	
INPUT AND OUTPUT LEVELS							
RESET Output Voltage High	VOH	ISOURCE = 300µA, VCC = VRST min	0.8VCC	0.86VCC		V	
BATT OK, BATT ON, WDO, LOWLINE Output Voltage High	VOH	ISOURCE = 300µA, VCC = VRST max	0.8VCC	0.86VCC		V	
PFO Output Voltage High	VOH	ISOURCE = 65µA, VCC = VRST max	0.8VCC			V	
BATT ON Output Voltage High	VOH	ISOURCE = 100µA, VCC = 2.3V, VBATT = 3V	0.8VBATT			V	
RESET Output Leakage Current (Note 9)	I _{LEAK}	VCC = VRST max	-1		-1	µA	
PFO Output Short to GND Current	I _{SC}	VCC = 3.3V, V PFO = 0V		180	500	µA	
PFO, RESET, RESET, WDO, LOWLINE Output Voltage Low	VOL	ISINK = 1.2mA; RESET, LOWLINE tested with VCC = VRST min; RESET, BATTOK, WDO tested with VCC = VRST max		0.08	0.2VCC	V	

MAX793/MAX794/MAX795

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3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 3.17V$ to $5.5V$ for the MAX793T/MAX795T, $V_{CC} = 3.02V$ to $5.5V$ for the MAX793S/MAX795S, $V_{CC} = 2.72V$ to $5.5V$ for the MAX793R/MAX794/MAX795R, $V_{BATT} = 3.6V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET Output Voltage Low	VOL	MAX79_C, VBATT = VCC = 1.0V, ISINK = 40μA		0.13	0.3	V
		MAX79_E, VBATT = VCC = 1.2V, ISINK = 200μA		0.17	0.3	
BATT ON Output Voltage Low	VOL	ISINK = 3.2mA, VCC = VRST max			0.2VCC	V
All Inputs Including PFO (Note 10)	VIH	VRST max < VCC < 5.5V			0.7VCC	V
	VIL			0.3VCC		
MANUAL RESET INPUT						
MR Pulse Width	tMR	MAX793/MAX794 only	100	50		ns
MR-to-Reset Delay	tMD	MAX793/MAX794 only		75	250	ns
MR Pull-Up Current		MAX793/MAX794 only, MR = 0V	25	70	250	μA
CHIP-ENABLE GATING						
CE IN Leakage Current	I _{LEAK}	Disable mode		±10		nA
CE IN-to-CE OUT Resistance		Enable mode, VCC = VRST max		46		Ω
CE IN-to-CE OUT Propagation Delay		VCC = VRST max, Figure 9		2	7	ns
CE OUT Drive from CE IN	VOH	VCC = VRST max, IOUT = -1mA, VCE IN = VCC	0.8VCC			V
	VOL	VCC = VRST max, IOUT = 1.6mA, VCE IN = 0V			0.2VCC	
Reset to CE OUT High Delay				10		μs
CE OUT Output Voltage High (reset active)	VOH	IOH = 500μA, VCC < 2.3V	0.8VBATT			V
WATCHDOG (MAX793/MAX794 only)						
WDI Input Current		0V < VCC < 5.5V	-1	0.01	1	μA
Watchdog Timeout Period	tWD		1.00	1.60	2.25	sec
WDI Pulse Width			1.00			ns

Note 1: V_{CC} supply current, logic input leakage, watchdog functionality (MAX793/MAX794), $\overline{MR}$ functionality (MAX793/MAX794), PFI functionality (MAX793/MAX794), state of RESET and RESET (MAX793/MAX794) tested at $V_{BATT} = 3.6V$ and $V_{CC} = 5.5V$. The state of RESET is tested at $V_{CC} = V_{CC}$ min.

Note 2: Tested at $V_{BATT} = 3.6V$, $V_{CC} = 3.5V$ and $0V$. The battery current will rise to $10\mu A$ over a narrow transition window around $V_{CC} = 1.9V$.

Note 3: Leakage current into the battery is tested under the worst-case conditions at $V_{CC} = 5.5V$, $V_{BATT} = 1.8V$ and $V_{CC} = 1.5V$, $V_{BATT} = 1.0V$.

Note 4: Guaranteed by design.

Note 5: When $V_{SW} > V_{CC} > V_{BATT}$, OUT remains connected to V_{CC} until V_{CC} drops below V_{BATT} . The V_{CC} -to- V_{BATT} comparator has a small 15mV typical hysteresis to prevent oscillation. For $V_{CC} < 1.75V$ (typical), OUT switches to BATT regardless of V_{BATT} .

Note 6: When $V_{BATT} > V_{CC} > V_{SW}$, OUT remains connected to V_{CC} until V_{CC} drops below the battery switch threshold (V_{SW}).

Note 7: OUT switches from BATT to V_{CC} when V_{CC} rises above the reset threshold, if $V_{BATT} > V_{RST}$. In this case, switchover back to V_{CC} occurs at the exact voltage that causes reset to be asserted, however switchover occurs 200ms prior to reset. If $V_{BATT} < V_{RST}$, OUT switches from BATT to V_{CC} when V_{CC} exceeds V_{BATT} .

Note 8: The reset threshold tolerance is wider for V_{CC} rising than for V_{CC} falling to accommodate the 10mV typical hysteresis, which prevents internal oscillation.

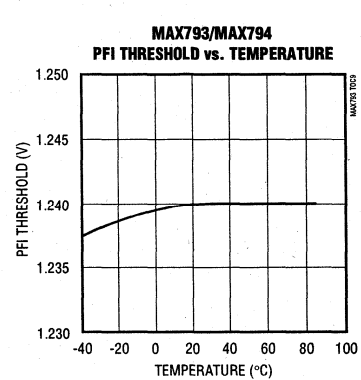
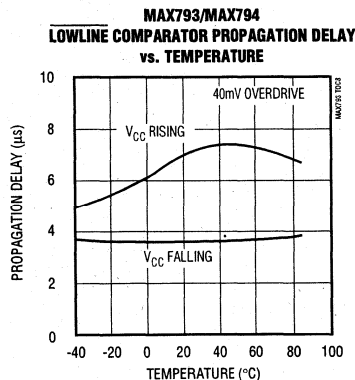
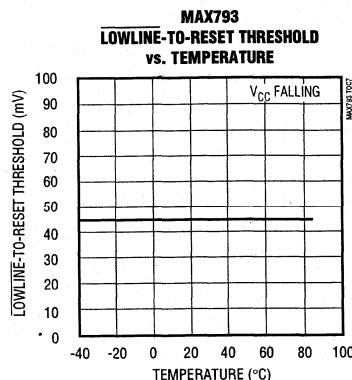
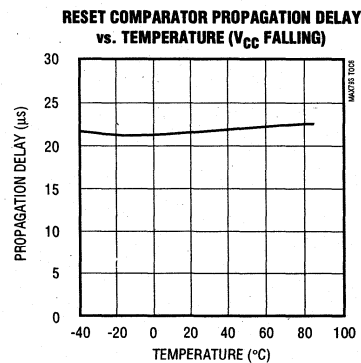
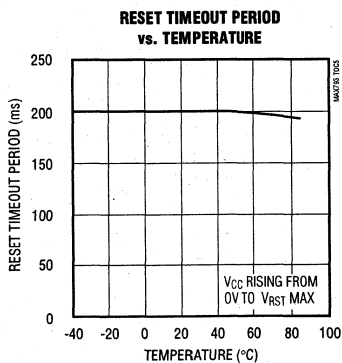
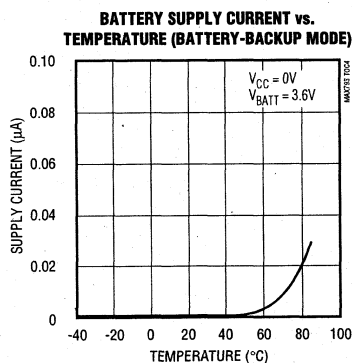
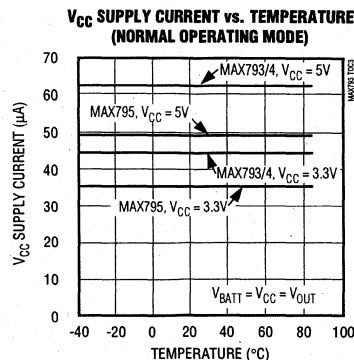
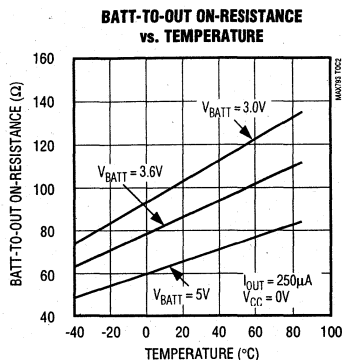
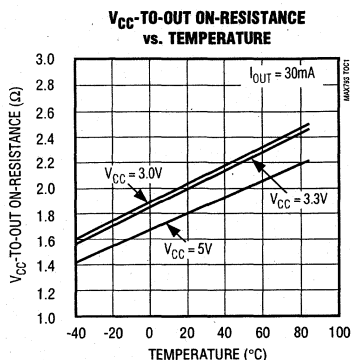
Note 9: The leakage current into or out of the RESET pin is tested with RESET not asserted (RESET output high impedance).

Note 10: PFO is normally an output, but is used as an input when activating the battery freshness seal.

3.0V/3.3V/Adjustable Microprocessor Supervisory Circuits

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



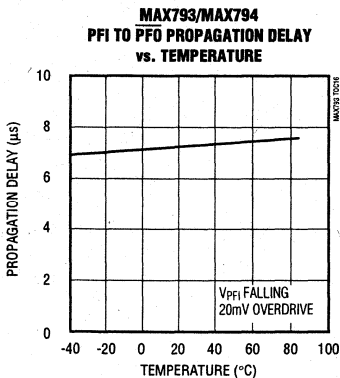
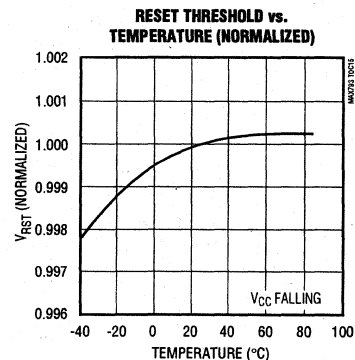
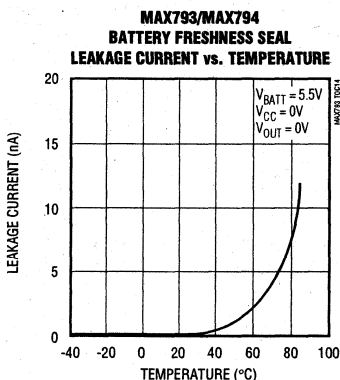
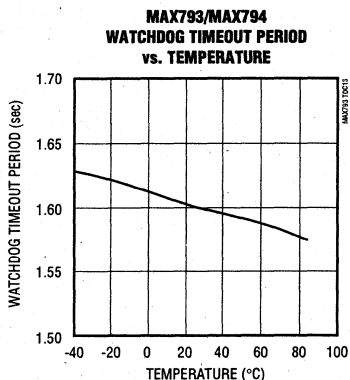
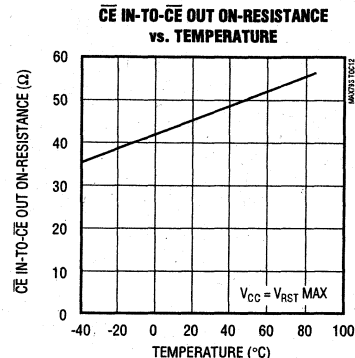
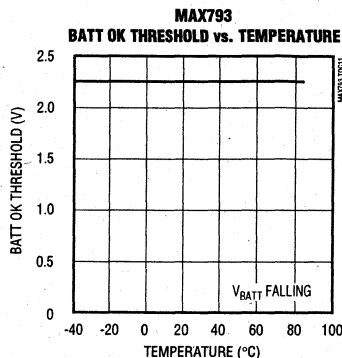
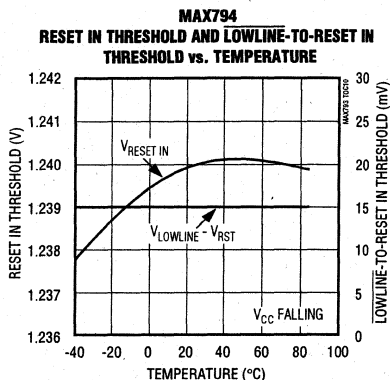
MAX793/MAX794/MAX795

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3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Pin Description

MAX793/MAX794/MAX795

5

PIN		NAME	FUNCTION
MAX793/ MAX794	MAX795		
1	1	OUT	Supply Output for CMOS RAM. When V _{CC} rises above the reset threshold or above V _{BATT} , OUT is connected to V _{CC} through an internal P-channel MOSFET switch. When V _{CC} falls below V _{SW} and V _{BATT} , BATT connects to OUT.
2	2	V _{CC}	Main Supply Input
3	—	BATT OK (MAX793)	Battery Status Output. High in normal operating mode when V _{BATT} exceeds V _{BOK} , otherwise low. V _{BATT} is checked continuously. Disabled and logic low while V _{CC} is below V _{SW} .
		RESET IN (MAX794)	Reset Input. Connect to an external resistor divider to select the reset threshold. The reset threshold can be programmed anywhere in the V _{SW} to 5.5V range.
4	—	PFI	Power-Fail Comparator Input. When PFI is less than V _{PFT} or when V _{CC} falls below V _{SW} , PFO goes low; otherwise, PFO remains high (see <i>Power-Fail Comparator</i> section). Connect to ground if unused.
5	3	BATT ON	Logic Output/External Bypass Switch-Driver Output. High when OUT switches to BATT. Low when OUT switches to V _{CC} . Connect the base/gate of PNP/PMOS transistor to BATT ON for I _{OUT} requirements exceeding 75mA.
6	4	GND	Ground
7	—	PFO	Power-Fail Comparator Output. When PFI is less than V _{PFT} or when V _{CC} falls below V _{SW} , PFO goes low; otherwise, PFO remains high. PFO is also used to enable the battery freshness seal (see <i>Battery Freshness Seal</i> , and <i>Power-Fail Comparator</i> sections).
8	—	MR	Manual Reset Input. A logic low on MR asserts reset. Reset remains asserted as long as MR is low and for 200ms after MR returns high. The active-low input has an internal 70μA pull-up current. In can be driven from a TTL- or CMOS-logic line or shorted to ground with a switch. Leave open if unused.
9	—	WDO	Watchdog Output. WDO goes low if WDI remains either high or low for longer than the watchdog timeout period. WDO returns high on the next transition of WDI. WDO is a logic high for V _{SW} < V _{CC} < V _{RST} , and low when V _{CC} is below V _{SW} .
10	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and WDO goes low. WDO returns high on the next transition of WDI. Connect WDO to MR to generate a reset due to a watchdog fault.
11	5	CE IN	Chip-Enable Input. The input to the chip-enable gating circuit. Connect to GND if unused
12	6	CE OUT	Chip-Enable Output. CE OUT goes low only when CE IN is low and reset is not asserted. If CE IN is low when reset is asserted, CE OUT will remain low for 10μs or until CE IN goes high, whichever occurs first. CE OUT is pulled up to OUT.
13	—	RESET	Active-High Reset Output. Sources and sinks current. RESET is the inverse of $\overline{\text{RESET}}$.
14	—	LOWLINE	Early Power-Fail Warning Output. Low when V _{CC} falls to V _{L_R} . This output can be used to generate an NMI to provide early warning of imminent power-failure.
15	7	RESET	Open-Drain, Active-Low Reset Output. Pulses low for 200ms when triggered, and stays low whenever V _{CC} is below the reset threshold or when MR is a logic low. It remains low for 200ms after either V _{CC} rises above the reset threshold, the watchdog triggers a reset (WDO connected to MR), or MR goes low to high.
16	8	BATT	Backup-Battery Input. When V _{CC} falls below V _{SW} and V _{BATT} , OUT switches from V _{CC} to BATT. When V _{CC} rises above the reset threshold or above V _{BATT} , OUT reconnects to V _{CC} . V _{BATT} may exceed V _{CC} . Connect V _{CC} , OUT, and BATT together if no battery is used.

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Detailed Description

General Timing Characteristics

The MAX793/MAX794/MAX795 are designed for 3.3V and 3V systems, and provide a number of supervisory functions (see the *Selector Guide* on the front page). Figures 1 and 2 show the typical timing relationships of the various outputs during power-up and power-down with typical V_{CC} rise and fall times.

Manual Reset Input (MAX793/MAX794)

Many microprocessor-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX793/MAX794, a logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{RP} (200ms) after it returns high. During the first half of the reset time-

out period (t_{RP}), the state of $\overline{MR}$ is ignored if $\overline{PFO}$ is externally forced low, to facilitate enabling the battery freshness seal. $\overline{MR}$ has an internal 70 μ A pull-up current, so it can be left open if it is not used. This input can be driven with TTL- or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1 μ F capacitor from $\overline{MR}$ to ground to provide additional noise immunity.

Reset Outputs

A microprocessor's (μ P's) reset input starts the μ P in a known state. These MAX793/MAX794/MAX795 μ P supervisory circuits assert a reset to prevent code execution errors during power-up, power-down, and

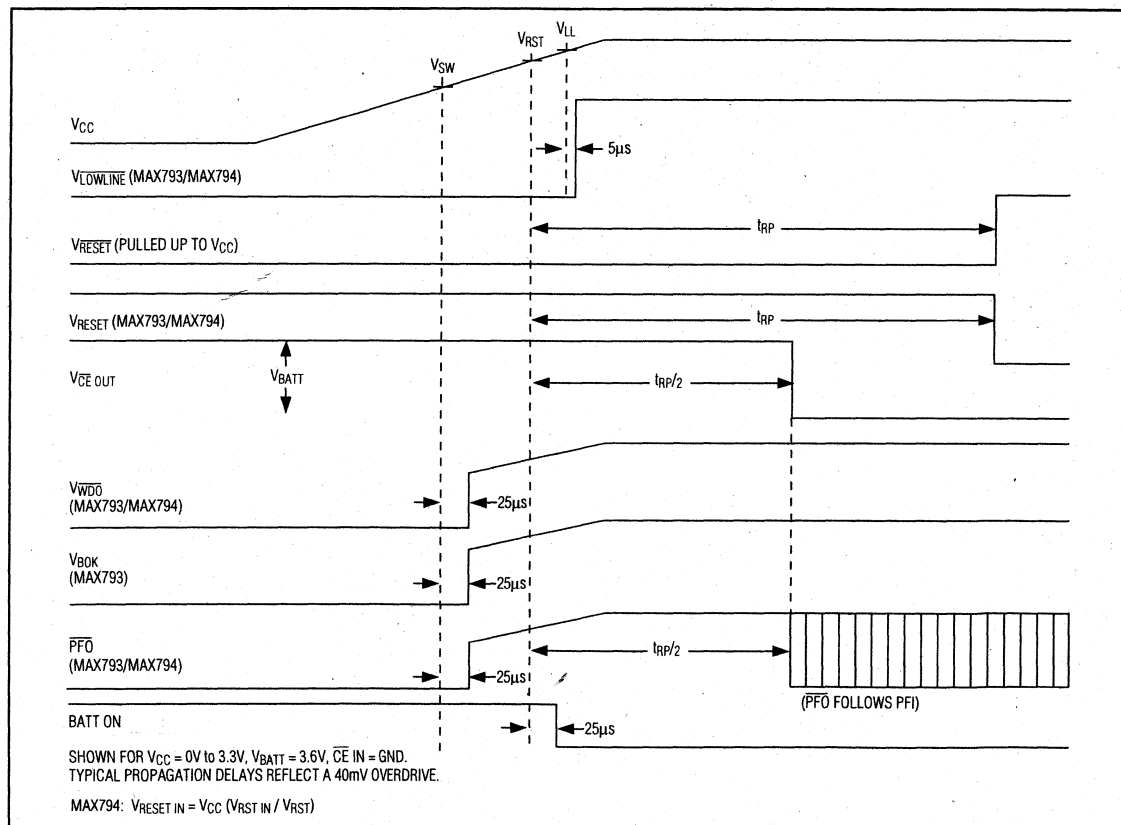


Figure 1. Timing Diagram, V_{CC} Rising

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brownout conditions. $\overline{\text{RESET}}$ is guaranteed to be a logic low for $0\text{V} < V_{\text{CC}} < V_{\text{RST}}$, provided V_{BATT} is greater than 1V . Without a backup battery ($V_{\text{BATT}} = V_{\text{CC}} = V_{\text{OUT}}$), $\overline{\text{RESET}}$ is guaranteed valid for $V_{\text{CC}} \geq 1\text{V}$. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period (TRP); after this interval, $\overline{\text{RESET}}$ becomes high impedance (Figure 2). $\overline{\text{RESET}}$ is an open-drain output, and requires a pull-up resistor to V_{CC} (Figure 3). Use a $4.7\text{k}\Omega$ to $1\text{M}\Omega$ pull-up resistor that will provide sufficient current to assure the proper logic levels to the μP .

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{\text{RESET}}$ goes low. Each time $\overline{\text{RESET}}$ is asserted, it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold, the internal timer restarts.

The watchdog output ($\overline{\text{WDO}}$) can also be used to initiate a reset. See the *Watchdog Output* section.

The RESET output is the inverse of the $\overline{\text{RESET}}$ output, and it can both source and sink current.

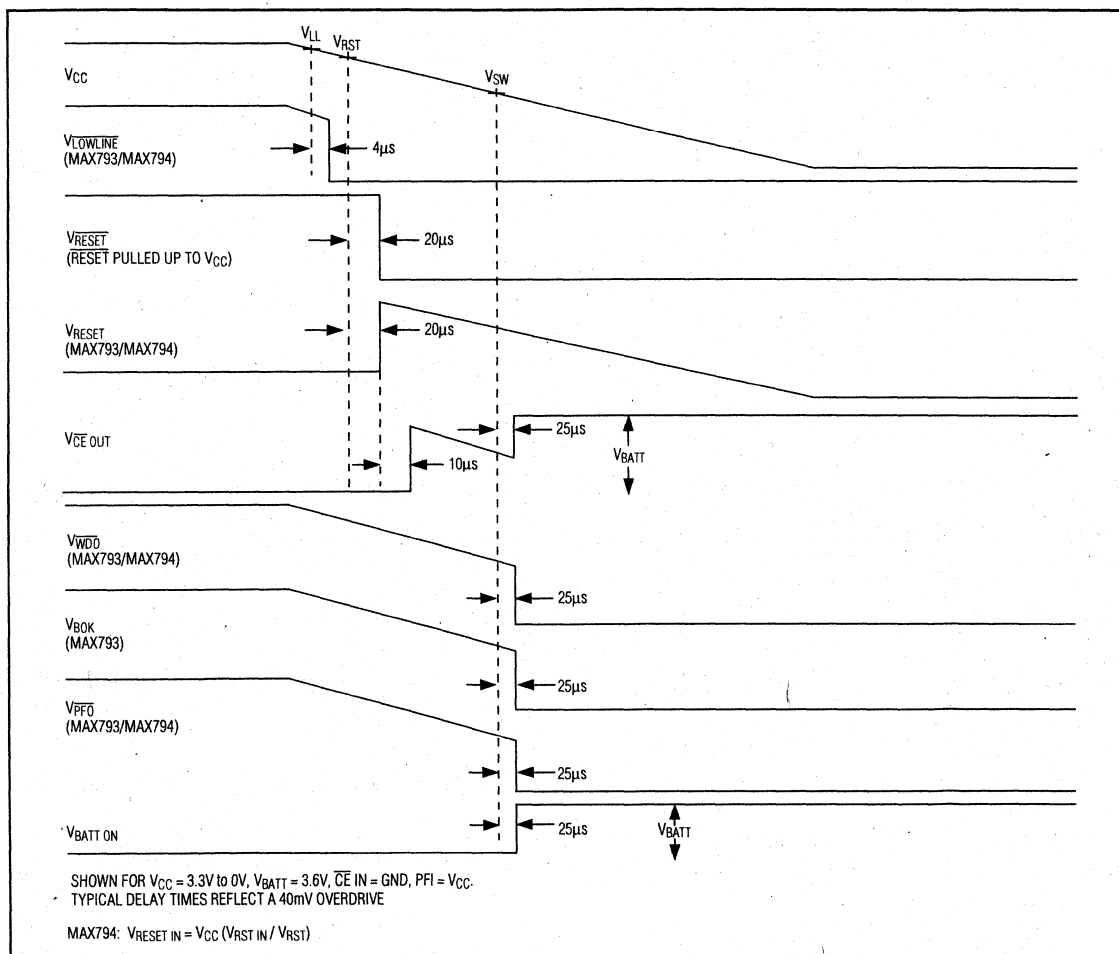


Figure 2. Timing Diagram, V_{CC} Falling

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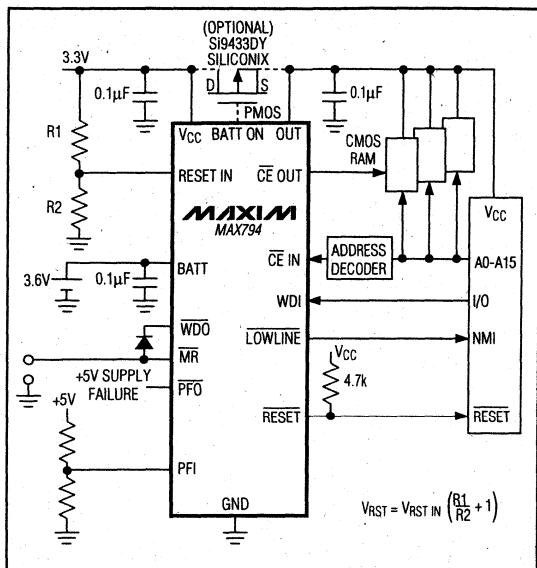


Figure 3. MAX794 Standard Application Circuit

Reset Threshold

The MAX793T/MAX795T are intended for 3.3V systems with a $\pm 5\%$ power-supply tolerance and a 10% systems tolerance. Except when MR is asserted, reset will not assert as long as the power supply remains above 3.15V (3.3V - 5%). Reset is guaranteed to assert before the power supply falls below 3.0V (3.3V - 10%).

The MAX793S/MAX795S are designed for 3.3V $\pm 10\%$ power supplies. Except when MR is asserted, they are guaranteed not to assert reset as long as the supply remains above 3.0V (3.0V is just above 3.3V - 10%). Reset is guaranteed to assert before the power supply falls below 2.85V (3.3V - 14%).

The MAX793R/MAX795R are optimized to monitor 3.0V $\pm 10\%$ power supplies. Reset will not occur until VCC falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the supply falls below 2.55V (3.0V - 15%).

Program the MAX794's reset threshold with an external voltage divider to RESET IN. The reset-threshold tolerance will be a combination of the RESET IN tolerance and the tolerance of the resistors used to make the external voltage divider. Calculate the reset threshold as follows:

$$V_{RST} = V_{RST\ IN} (R1 / R2 + 1)$$

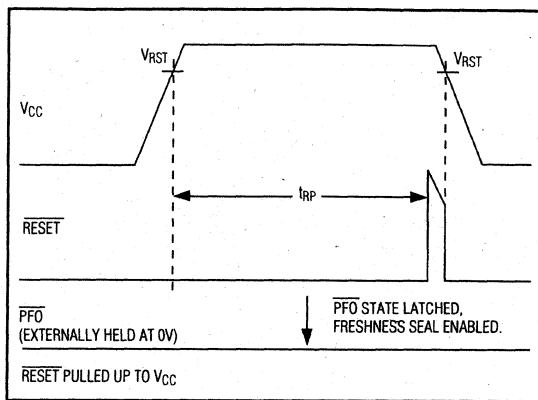


Figure 4. Battery Freshness Seal Enable Timing

Using the standard application circuit (Figure 3), the reset threshold may be programmed anywhere in the range of V_{SW} (the battery switch threshold) to 5.5V. Reset is asserted when VCC falls below V_{SW}.

Battery Freshness Seal

The MAX793/MAX794's battery freshness seal disconnects the backup battery from internal circuitry until it is needed. This allows an OEM to ensure that the backup battery connected to BATT will be fresh when the final product is put to use. To enable the freshness seal, connect a battery to BATT, ground PFO, bring VCC above the reset threshold and hold it there until reset is deasserted following the reset timeout period, then bring VCC back down again (Figure 4). Once the battery freshness seal is enabled (disconnecting the backup battery from the internal circuitry and anything connected to OUT), it remains enabled until VCC is brought above V_{RST}. Note that connecting PFO to MR will not interfere with battery freshness seal operation.

BATT OK Output (MAX793)

BATT OK indicates the status of the backup battery. When reset is not asserted, the MAX793 checks the battery voltage continuously. If V_{BATT} is below V_{BOK} (2.0V min), BATT OK goes low; otherwise, it remains pulled up to VCC. BATT OK also goes low when VCC goes below V_{SW}.

Watchdog Input (MAX793/MAX794)

In the MAX793/MAX794, the watchdog circuit monitors the μP 's activity. If the μP does not toggle the watchdog input (WDI) within 1.6sec, WDO goes low. The internal 1.6sec timer is cleared and WDO returns high

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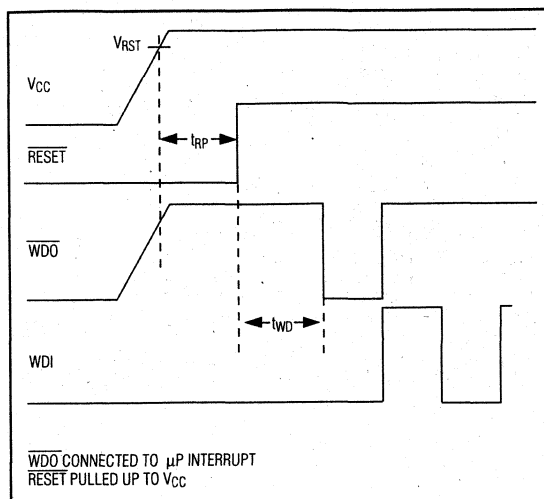


Figure 5. Watchdog Timing Relationship

either when a reset occurs or when a transition (low-to-high or high-to-low) takes place at WDI. As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is released or WDI changes state, the timer starts counting (Figure 5). WDI can detect pulses as short as 100ns. Unlike the 5V MAX690 family, the watchdog function **cannot** be disabled.

Watchdog Output (MAX793/MAX794)

In the MAX793/MAX794, WDO remains high (WDO is pulled up to VCC) if there is a transition or pulse at WDI during the watchdog timeout period. WDO goes low if no transition occurs at WDI during the watchdog timeout period. The watchdog function is disabled and WDO is a logic high when reset is asserted if VCC is above VSW. WDO is a logic low when VCC is below VSW.

If a system reset is desired on every watchdog fault, simply diode-OR connect WDO to MR (Figure 6). When a watchdog fault occurs in this mode, WDO goes low, pulling MR low, which causes a reset pulse to be issued. Ten microseconds after reset is asserted, the watchdog timer clears and WDO returns high. This delay results in a 10μs pulse at WDO, allowing external circuitry to "capture" a watchdog fault indication. A continuous high or low on WDI will cause 200ms reset pulses to be issued every 1.6sec.

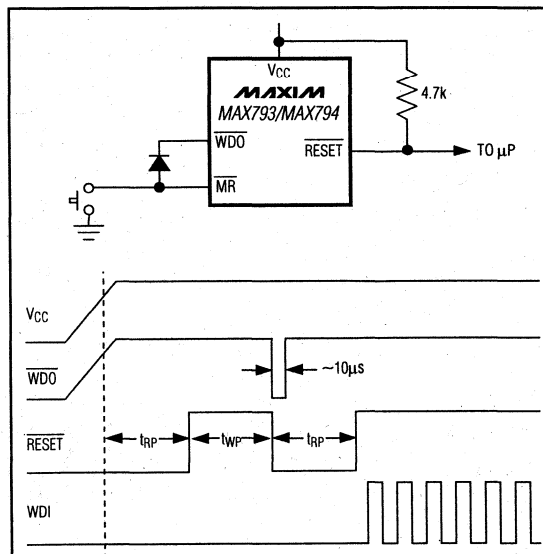


Figure 6. Generating a Reset on Each Watchdog Fault

Chip-Enable Signal Gating

Internal gating of chip-enable (CE) signals prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX793/MAX794/MAX795 use a series transmission gate from CE IN to CE OUT (Figure 7). During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from CE IN to CE OUT enables these μP supervisors to be used with most μPs. If CE IN is low when reset asserts, CE OUT remains low for typically 10μs to permit completion of the current write cycle.

Chip-Enable Input

The CE transmission gate is disabled and CE IN is high impedance (disabled mode) while reset is asserted. During a power-down sequence when VCC passes the reset threshold, the CE transmission gate disables and CE IN immediately becomes high impedance if the voltage at CE IN is high. If CE IN is low when reset asserts, the CE transmission gate will disable at the moment CE IN goes high, or 10μs after reset asserts, whichever occurs first (Figure 8). This permits the current write cycle to complete during power-down.

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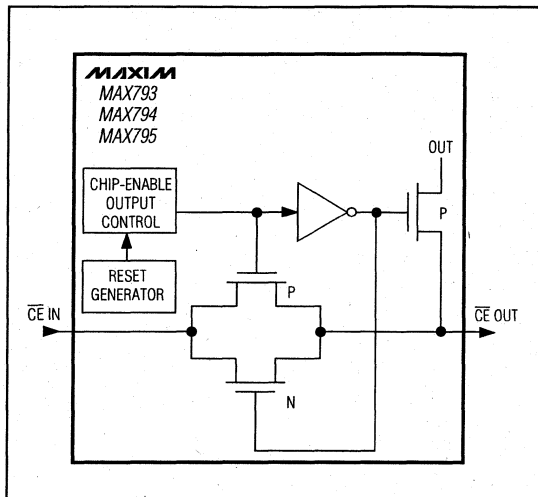


Figure 7. Chip-Enable Transmission Gate

The CE transmission gate remains disabled and $\overline{\text{CE IN}}$ remains high impedance (regardless of $\overline{\text{CE IN}}$ activity) for the first half of the reset timeout period ($t_{RP}/2$), any time a reset is generated. While disabled, $\overline{\text{CE IN}}$ is high impedance. When the CE transmission gate is enabled, the impedance of $\overline{\text{CE IN}}$ appears as a 46Ω resistor in series with the load at CE OUT.

The propagation delay through the CE transmission gate depends on V_{CC} , the source impedance of the drive connected to $\overline{\text{CE IN}}$, and the loading on CE OUT (see the Chip-Enable Propagation Delay vs. $\overline{\text{CE OUT}}$ Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{\text{CE IN}}$ to the 50% point on $\overline{\text{CE OUT}}$ using a 50Ω driver and 50pF of load capacitance (Figure 9). For minimum propagation delay, minimize the capacitive load at CE OUT, and use a low-output-impedance driver.

Chip-Enable Output

When the CE transmission gate is enabled, the impedance of $\overline{\text{CE OUT}}$ is equivalent to a 46Ω resistor in series with the source driving $\overline{\text{CE IN}}$. In the disabled mode, the transmission gate is off and an active pull-up connects $\overline{\text{CE OUT}}$ to OUT (Figure 8). This pull-up turns off when the transmission gate is enabled.

Early Power-Fail Warning (MAX793/MAX794)

Critical systems often require an early warning indicating that power is failing. This warning provides time for the μP to store vital data and take care of any additional "housekeeping" functions, before the power supply gets too far out of tolerance for the μP to operate reliably. The MAX793/MAX794 offer two methods of achieving this early warning. If access to the unregulated supply is feasible, the power-fail comparator input (PFI) can be connected to the unregulated supply

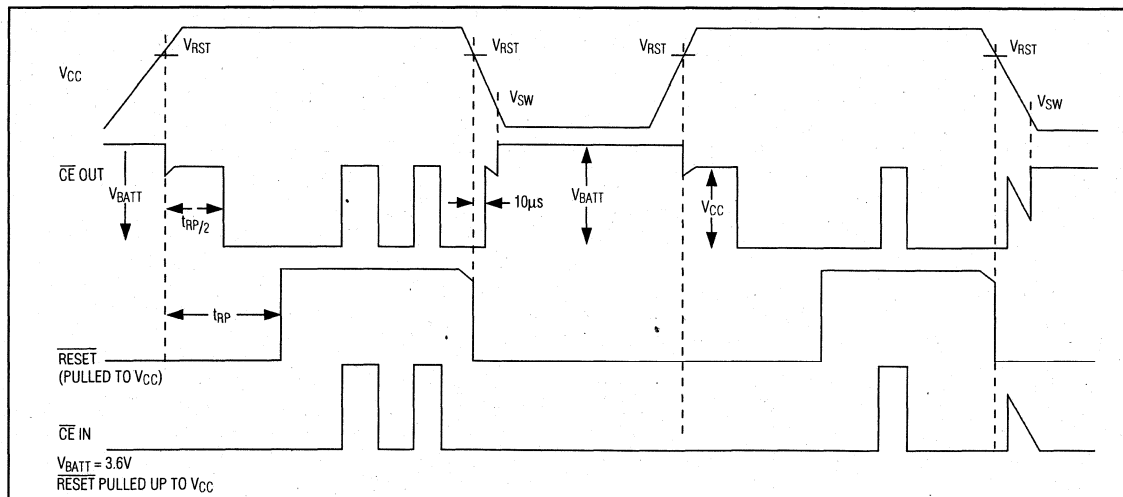


Figure 8. Chip-Enable Timing

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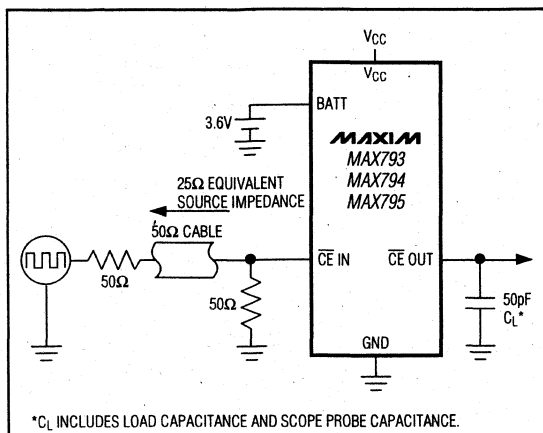


Figure 9. CE Propagation Delay Test Circuit

through a voltage divider, with the power-fail comparator output (PFO) providing the NMI to the μP (Figure 10). If there is no easy access to the unregulated supply, the LOWLINE output can be used to generate an NMI to the μP (see *LOWLINE Output* section).

LOWLINE Output (MAX793/MAX794)

The low-line comparator monitors V_{CC} with a threshold voltage typically 45mV above the reset threshold (10mV of hysteresis) for the MAX793, and 15mV above RESET IN (4mV of hysteresis) for the MAX794. For normal operation (V_{CC} above the reset threshold), LOWLINE is

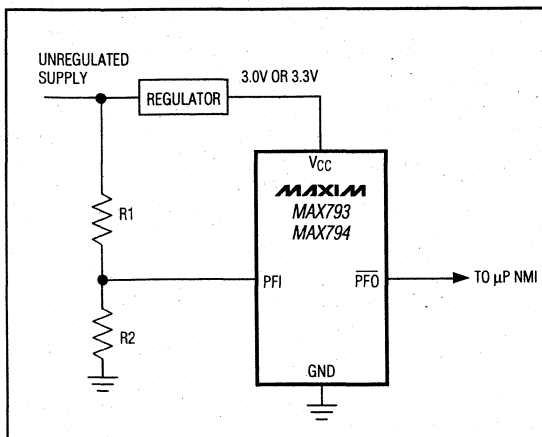


Figure 10. Using the Power-Fail Comparator to Generate Power-Fail Warning

pulled to V_{CC} . Use LOWLINE to provide an NMI to the μP when power begins to fall.

In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must also contend with a more rapid V_{CC} fall time, such as when the main battery is disconnected or a high-side switch is opened during normal operation, use capacitance on the V_{CC} line to provide time to execute the shutdown routine (Figure 11).

First, calculate the worst-case time required for the system to perform its shutdown routine. Then, with the worst-case shutdown time, the worst-case load current, and the minimum low-line to reset threshold (V_{LR} min), calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted:

$$C_{HOLD} > I_{LOAD} \times t_{SHDN} / V_{LR}$$

where I_{LOAD} is the current being drained from the capacitor, V_{LR} is the low-line to reset threshold difference ($V_{LL} - V_{RST}$), and t_{SHDN} is the time required for the system to complete an orderly shutdown routine.

Power-Fail Comparator (MAX793/MAX794)

The MAX793/MAX794's PFI input is compared to an internal reference. If PFI is less than the power-fail threshold (V_{PFT}), PFO goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply (Figure 12). However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

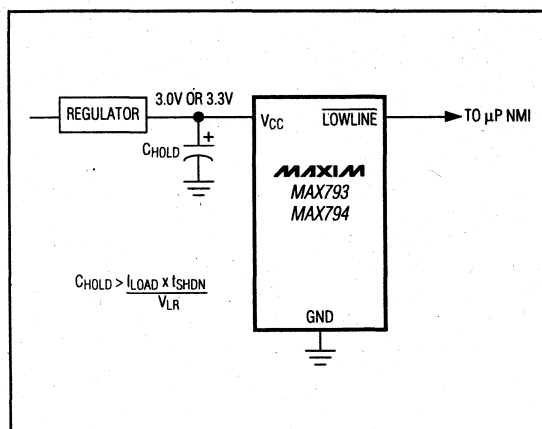


Figure 11. Using LOWLINE to Provide Power-Fail Warning to the μP

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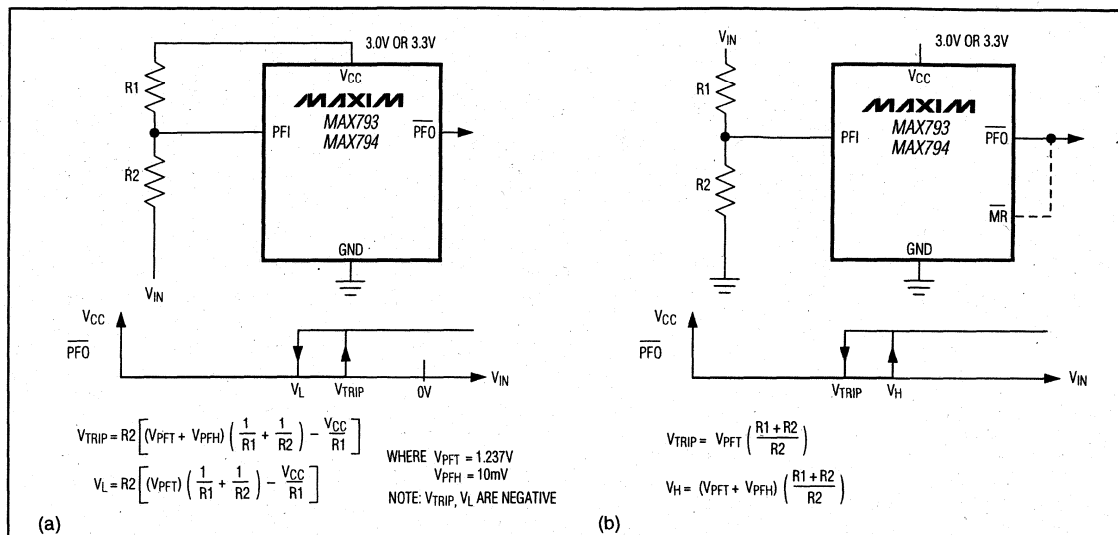


Figure 12. Using the Power-Fail Comparator to Monitor an Additional Power Supply: (a) V_{IN} Is Negative, (b) V_{IN} Is Positive

The power-fail comparator turns off and $\overline{PFO}$ goes low when V_{CC} falls below V_{SW} on power-down. During the first half of the reset timeout period (t_{RP}), $\overline{PFO}$ is forced high, irrespective of V_{PFI} . At the beginning of the second half of t_{RP} , the power-fail comparator is enabled and $\overline{PFO}$ follows PFI . If the comparator is unused, connect PFI to ground and leave $\overline{PFO}$ unconnected. $\overline{PFO}$ may be connected to $\overline{MR}$ so that a low voltage on PFI will generate a reset (Figure 12b). In this configuration, when the monitored voltage causes PFI to fall below V_{PFT} , $\overline{PFO}$ pulls $\overline{MR}$ low, causing a reset to be asserted. Reset remains asserted as long as $\overline{PFO}$ holds $\overline{MR}$ low, and for 200ms after $\overline{PFO}$ pulls $\overline{MR}$ high when the monitored supply is above the programmed threshold.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at BATT, the devices automatically switch RAM to backup power when V_{CC} falls. In order to allow the backup battery (e.g., a 3.6V lithium cell) to have a higher voltage than V_{CC} , this family of μP supervisors (designed for 3.3V and 3V systems) does not always connect BATT to OUT when V_{BATT} is greater than V_{CC} . BATT connects to OUT (through a 140 Ω switch) either when V_{CC} falls below V_{SW} and

V_{BATT} is greater than V_{CC} , or when V_{CC} falls below 1.75V (typ) regardless of the BATT voltage.

Switchover at V_{SW} ensures that battery-backup mode is entered before V_{OUT} gets too close to the 2.0V minimum required to reliably retain data in most CMOS RAM, (switchover at higher V_{CC} voltages would decrease backup-battery life). When V_{CC} recovers, switchover is deferred either until V_{CC} crosses V_{BATT} if V_{BATT} is below V_{RST} , or when V_{CC} rises above the reset threshold (V_{RST}) if V_{BATT} is above V_{RST} . This power-up switchover technique prevents V_{CC} from charging the backup battery through OUT when using an external transistor driven by BATT ON. OUT connects to V_{CC} through a 4 Ω (max) PMOS power switch when V_{CC} crosses the reset threshold (Figure 13).

BATT ON (MAX793/MAX794)

BATT ON is high when OUT is connected to BATT. Although BATT ON can be used as a logic output to indicate the battery switchover status, it is most often used as a gate or base drive for an external pass transistor for high-current applications (see *Driving an External Switch with BATT ON* in the *Applications Information* section). When V_{CC} exceeds V_{RST} on power-up, BATT ON sinks 3.2mA at 0.4V. In battery-backup mode, this terminal sources 100 μA from BATT.

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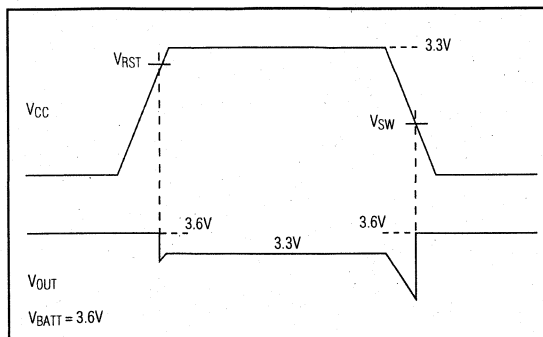


Figure 13. Battery Switchover Timing

Table 1. Input and Output Status in Battery-Backup Mode

PIN NAME	STATUS
OUT	Connected to BATT through an internal 140Ω switch
VCC	Disconnected from OUT
BATT ON	Pulled up to BATT
BATT OK	Logic low
PFI	Disabled
PFO	Logic low
MR	Disabled, but still pulled up to VCC
WDO	Logic low
WDI	Disabled
RESET	Logic low
RESET	Pulled up to VCC
BATT	Connected to OUT
LOWLINE	Logic low
CE IN	High impedance
CE OUT	Pulled to BATT

Applications Information

These μ P supervisory circuits are not short-circuit protected. Shorting VOUT to ground, excluding power-up transients such as charging a decoupling capacitor, destroys the device. Decouple both VCC and BATT pins to ground by placing 0.1 μ F ceramic capacitors as close to the device as possible.

Driving an External Switch with BATT ON

BATT ON can be directly connected to the base of a PNP transistor or the gate of a PMOS transistor. The PNP connection is straightforward: connect the emitter

to VCC, the collector to OUT, and the base to BATT ON (Figure 14a). No current-limiting resistor is required, but a resistor connecting the base of the PNP to BATT ON can be used to limit the current drawn from VCC, prolonging battery life in portable equipment.

If you are using a PMOS transistor, however, it must be connected backwards from the traditional method. Connect the gate to BATT ON, the drain to VCC, and the source to OUT (Figure 14b). This method orients the body diode from VCC to OUT and prevents the backup battery from discharging through the FET when its gate is high. Two PMOS transistors in the Siliconix LITTLE FOOT™ series are specified with VGS down to -2.7V. The Si9433DY has a maximum 100mΩ drain-source on-resistance with 2.7V of gate drive and a 2A drain-source current. The Si9434DY specifies a 60mΩ drain-source on-resistance with 2.7V of gate drive and a 5.1A drain-source current.

Using a SuperCap™ as a Backup Power Source

SuperCaps™ are capacitors with extremely high capacitance values (e.g., order of 0.47F) for their size. Figure 15 shows two ways to use a SuperCap as a backup power source. The SuperCap can be connected through a diode to the 3V input (Figure 15a); or, if a 5V supply is also available, the SuperCap can be charged up to the 5V supply (Figure 15b), allowing a longer backup period. Since VBATT can exceed VCC while VCC is above the reset threshold, there are no special precautions when using these μ P supervisors with a SuperCap.

Operation without a Backup Power Source

These μ P supervisors were designed for battery-backed applications. If a backup battery is not used, connect BATT, OUT, and VCC together, or use a different μ P supervisor. See the μ P Supervisory Circuits table at the end of this data sheet.

Replacing the Backup Battery

The backup power source can be removed while VCC remains valid, without danger of triggering a reset pulse, provided that BATT is decoupled with a 0.1 μ F capacitor to ground. As long as VCC stays above the reset threshold, battery-backup mode cannot be entered.

™ LITTLE FOOT is a trademark of Siliconix Inc.
SuperCap is a trademark of Baknor Industries.

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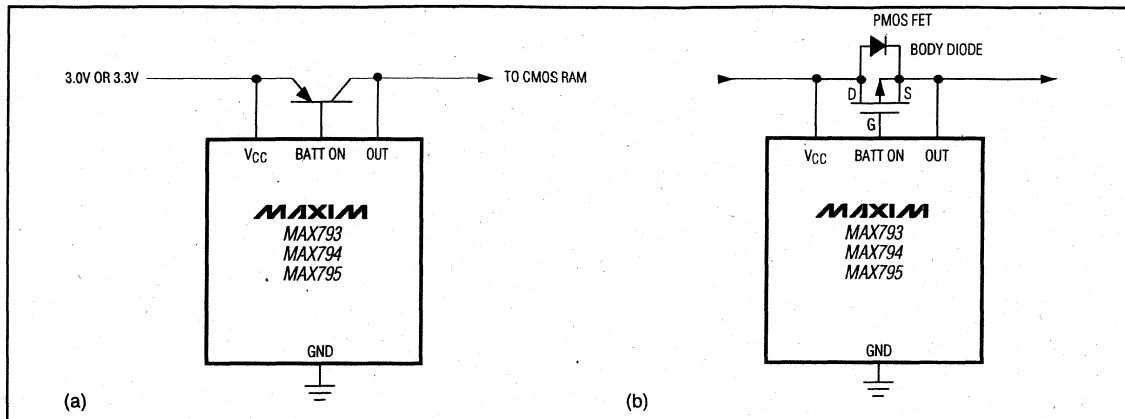


Figure 14. Driving an External Transistor with BATT ON

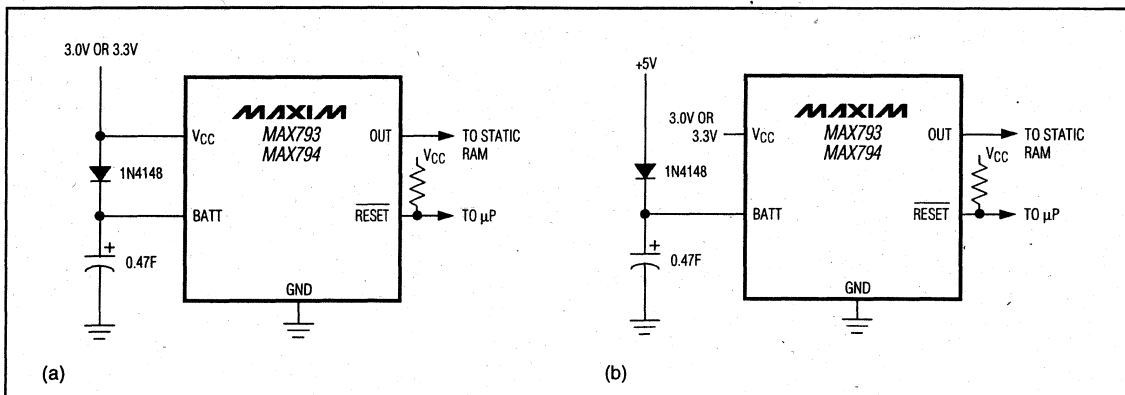


Figure 15. Using a SuperCap™ as a Backup Source

Adding Hysteresis to the Power-Fail Comparator (MAX793/MAX794)

The power-fail comparator has a typical input hysteresis of 10mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see the section *Monitoring an Additional Power Supply*).

If additional noise margin is desired, connect a resistor between PFO and PFI as shown in Figure 16a. Select the ratio of R1 and R2 such that PFI sees V_{PFI} when V_{IN} falls to its trip point (V_{TRIP}). R3 adds the additional hysteresis and should typically be more than 10 times the value of R1 or R2. The hysteresis window extends both above (V_H) and below (V_L) the original trip point (V_{TRIP}).

Connecting an ordinary signal diode in series with R3, as shown in Figure 16b, causes the lower trip point (V_L) to coincide with the trip point without hysteresis (V_{TRIP}), so the entire hysteresis window occurs above V_{TRIP} . This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold. The current through R1 and R2 should be at least 1μA to ensure that the 25nA (max over temperature) PFI input current does not shift the trip point. R3 should be larger than 82kΩ so it does not load down the PFO pin. Capacitor C1 is optional, and adds noise rejection.

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MAX793/MAX794/MAX795

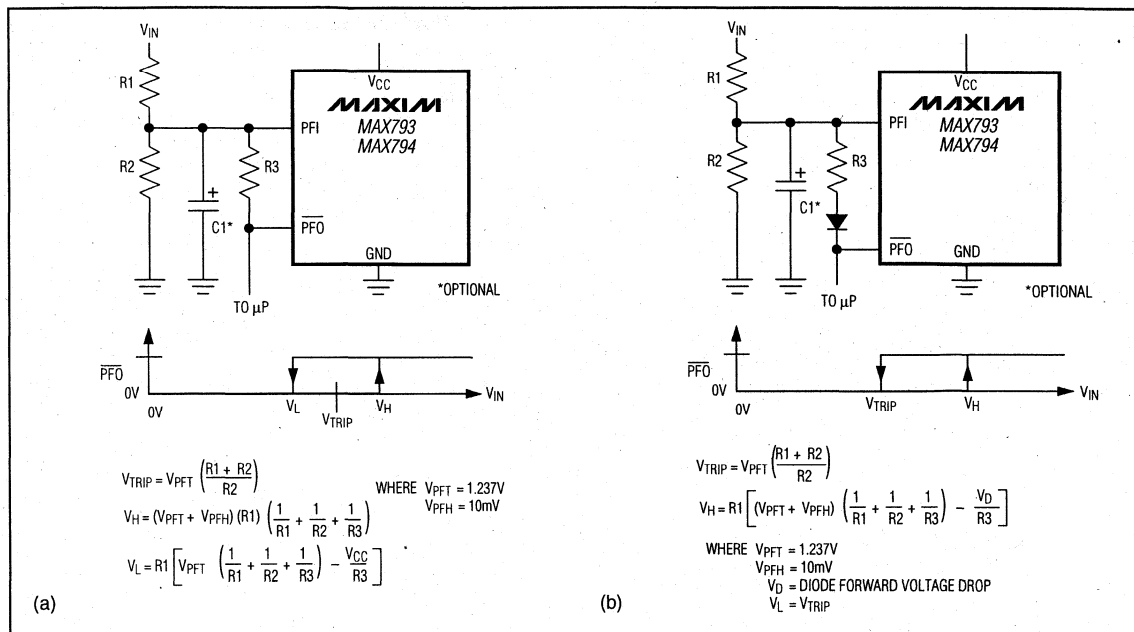


Figure 16. Adding Hysteresis to the Power-Fail Comparator: (a) Symmetrical Hysteresis, (b) Hysteresis Only on Rising V_{IN}

Monitoring an Additional Power Supply

These μP supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI. $\overline{PFO}$ can be used to generate an interrupt to the μP or to cause reset to assert (Figure 12).

Interfacing to μP s with Bidirectional Reset Pins

Since the $\overline{RESET}$ output is open drain, the MAX793/MAX794/MAX795 interface easily with μP s that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the $\overline{RESET}$ output of the μP supervisor directly to the $\overline{RESET}$ input of the microcontroller with a single pull-up resistor allows either device to assert reset (Figure 17).

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches) while issuing resets to the μP during power-up, power-down, and brownout conditions. Therefore, resetting the μP when V_{CC} experiences only small glitches is usually not recommended.

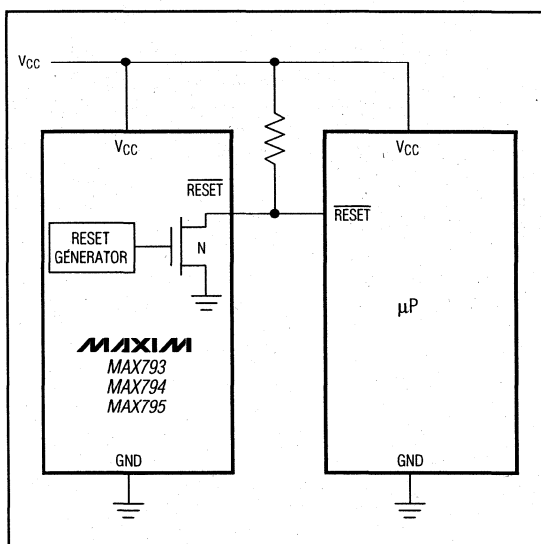


Figure 17. Interfacing to μP s with Bidirectional Reset I/O

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Figure 18 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going VCC pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going VCC transient can typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC transient that goes 40mV below the reset threshold and lasts for 10 μ s or less will not cause a reset pulse to be issued.

A 0.1 μ F bypass capacitor mounted close to the VCC pin provides additional transient immunity.

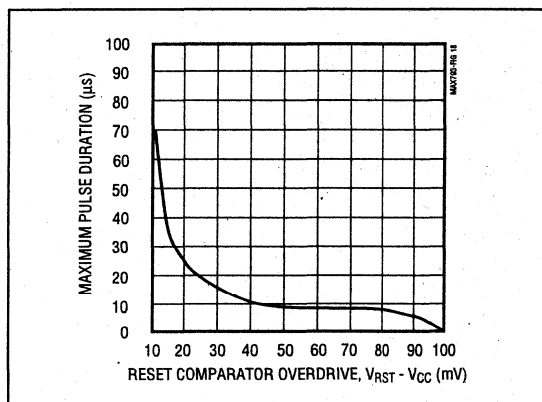


Figure 18. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Watchdog Software Considerations

There is a way to help the watchdog timer monitor software execution more closely, which involves setting and resetting the watchdog input at different points in the program rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 19 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

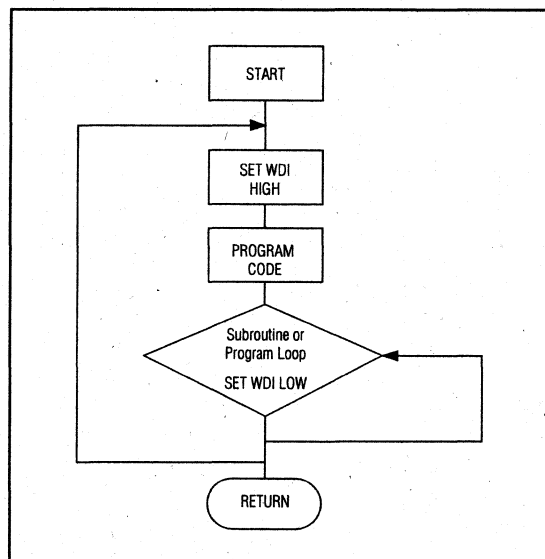


Figure 19. Watchdog Flow Diagram

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	RESET Valid to VCC = 1V	Nominal Watchdog Timeout Period (sec), if Available	Separate Watchdog Output	Backup-Battery Switch	VCC-to-VOUT On Resistance Max (Ω)	VART-to-VOUT Max (Ω)	CE Write Protect	Power-Fail Comparator	Manual-Reset Input	Low-Line Output	Battery-On Output	Supply Operating Mode max (typ) mA	Supply Backup Mode max (typ) µA	Pins
MAX1232	4.374/62	250	✓	✓	✓	0.150(9)/1.2	✓	✓	10	400	✓	✓	✓	✓	✓	0.2(0.05)	5(0.05)	8
MAX6904/692A	4.654/40	140	✓	✓	✓	1.6	✓	✓	10	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX6908/S/T	2.632/933/08	140	✓	✓	✓	1.6	✓	✓	6	400	✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	16
MAX691A/693A	4.654/40	140	✓	✓	✓	1.6adj.	✓	✓	1.2	25	✓	✓	✓	✓	✓	0.1(0.035)	5(0.04)	16
MAX1691†	The MAX1691 is a module with the MAX691A and a 125mAµh lithium battery.																	
MAX696	Adj.	35adj.	✓	✓	✓	1.6adj.	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	16
MAX697	Adj.	35adj.	✓	✓	✓	1.6adj.	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	16
MAX700	4.654adj.	200	✓	✓	✓	1.6adj.	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.2(0.1)	5(0.05)	8
MAX703/704	4.654/40	140	✓	✓	✓	✓	✓	✓	10	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX704/S/T	2.632/933/08	140	✓	✓	✓	✓	✓	✓	6	400	✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	8
MAX705/706	4.654/40	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX706P	2.63	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX706/S/T	2.632/933/08	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX707/708	4.654/40	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX708/S/T	2.632/933/08	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX709	4.65	140	✓	✓	✓	1	✓	✓	1.2	25	✓	✓	✓	✓	✓	0.15(0.06)	5(0.04)	16
MAX709L	4.654/40	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.15(0.07)	5(0.04)	16
MAX709L/N/R/S/T	2.632/933/08	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.15(0.07)	5(0.04)	16
MAX709L/S/UT	2.632/933/07/3/08	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	16
MAX794	Adj.	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	16
MAX795/S/UT	2.632/933/07/3/08	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	16
MAX800/L/N	4.604/40	140	✓	✓	✓	1.6adj.	✓	✓	1.2	25	✓	✓	✓	✓	✓	0.1(0.035)	5(0.04)	16
MAX800/L/N/M†	4.684/584/43	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	8
MAX802L/N/R/S/T	4.604/40	140	✓	✓	✓	1.6	✓	✓	10	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX804R/S/T	2.632/933/08	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	8
MAX805L/R/S/T	4.652/63/2.933/08	140	✓	✓	✓	1.6	✓	✓	10	400	✓	✓	✓	✓	✓	0.35(0.2)	5(0.05)	8
MAX806R/S/T	2.632/933/08	140	✓	✓	✓	✓	✓	✓	6	400	✓	✓	✓	✓	✓	0.5(0.4)	1(0.4)	8
MAX807L/N/M†	4.684/584/43	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	8
MAX808L/N/M†	4.684/584/43	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	8
MAX809L/N/R/S/T	4.654/40	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.06(0.024)	TBD	16
MAX810L/N/R/S/T	2.632/933/08	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.06(0.024)	TBD	3
MAX813L	4.65	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.35(0.2)	TBD	8
MAX814L/N/NT†	4.804/704/553/03	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	8
MAX815L/N/NT†	4.804/704/553/03	140	✓	✓	✓	1.6	✓	✓	✓	✓	✓	✓	✓	✓	✓	TBD	TBD	8
MAX816†	Adj./4.19	140	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.15(0.07)	TBD	16
MAX820L/N/R/S/T	4.654/40	140	✓	✓	✓	1	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.15(0.07)	TBD	16
MAX1210	2.632/933/08	140	✓	✓	✓	✓	✓	✓	2.5	667	✓	✓	✓	✓	✓	0.5(0.23)	0.1(0.002)	8

† Future product—contact factory for availability. Specifications are preliminary.

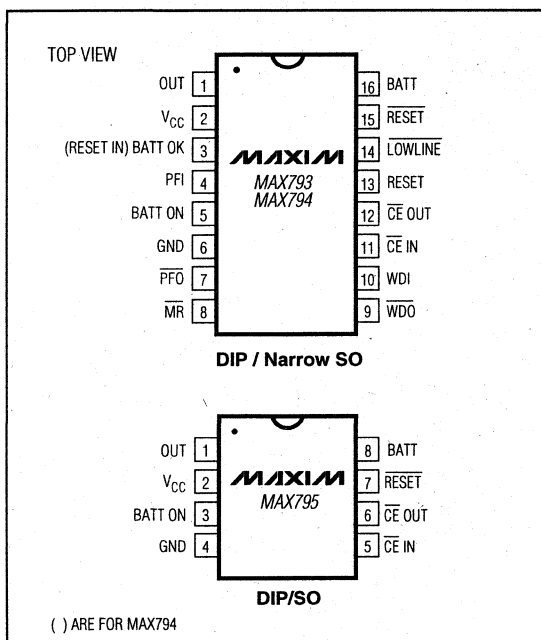
3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE
MAX794CPE	0°C to +70°C	16 Plastic DIP
MAX794CSE	0°C to +70°C	16 Narrow SO
MAX794EPE	-40°C to +85°C	16 Plastic DIP
MAX794ESE	-40°C to +85°C	16 Narrow SO
MAX795_CPA	0°C to +70°C	8 Plastic DIP
MAX795_CSA	0°C to +70°C	8 SO
MAX795_EPA	-40°C to +85°C	8 Plastic DIP
MAX795_ESA	-40°C to +85°C	8 SO

* The MAX793/MAX795 offer a choice of reset threshold voltage. Select the letter corresponding to the desired reset threshold voltage range (T = 3.00V to 3.15V, S = 2.85V to 3.00V, R = 2.55V to 2.70V) and insert it into the blank to complete the part number. The MAX794's reset threshold is adjustable.

Pin Configurations



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

μ P Supervisory Circuit with $\pm 1.5\%$ Reset Accuracy

MAX807

General Description

The MAX807 microprocessor (μ P) supervisory circuit reduces the complexity and number of components needed to monitor power-supply and battery-control functions in μ P systems. A $70\mu\text{A}$ supply current makes the MAX807 ideal for use in portable equipment, while a 6ns chip-enable propagation delay and 250mA output current capability (20mA in battery-backup mode) make it suitable for larger, higher-performance equipment.

The MAX807 comes in 16-pin DIP and SO packages, and provides the following functions:

- 1) μ P reset. The active-low $\overline{\text{RESET}}$ output is asserted during power-up, power-down, and brownout conditions, and is guaranteed to be in the correct state for V_{CC} down to 1V .
- 2) Active-high RESET output.
- 3) Manual-reset input.
- 4) Two-stage power-fail warning. A separate low-line comparator compares V_{CC} to a threshold 30mV above the reset threshold. This low-line comparator is more accurate than those in previous μ P supervisors.
- 5) Backup-battery switchover for CMOS RAM, real-time clocks, μ Ps, or other low-power logic.
- 6) Write protection of CMOS RAM or EEPROM.
- 7) 2.275V threshold detector—provides for power-fail warning and low-battery detection, or monitors a power supply other than $+5\text{V}$.
- 8) BATT OK status flag indicates that the backup-battery voltage is above 2.275V .
- 9) Watchdog-fault output—asserted if the watchdog input has not been toggled within a preset timeout period.

Applications

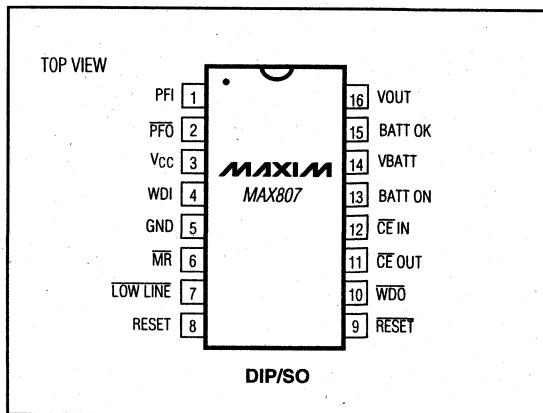
Computers
Controllers
Intelligent Instruments
Critical μ P Power Monitoring
Portable/Battery-Powered Equipment

Features

- ◆ Precision 4.675V (MAX807L) or 4.425V (MAX807M), or 4.575V (MAX807N) Voltage Monitoring
- ◆ 140ms Power OK / Reset Time Delay
- ◆ $\overline{\text{RESET}}$ and RESET Outputs
- ◆ Independent Watchdog Timer
- ◆ $1\mu\text{A}$ Standby Current
- ◆ Power Switching:
 250mA in V_{CC} Mode
 20mA in Battery-Backup Mode
- ◆ On-Board Gating of Chip-Enable Signals:
Memory Write-Cycle Completion
 6ns CE Gate Propagation Delay
- ◆ MaxCap™ and SuperCap™ Compatible
- ◆ Voltage Monitor for Power-Fail or Low-Battery Warning
- ◆ Backup-Battery Monitor
- ◆ Guaranteed $\overline{\text{RESET}}$ Valid to $V_{\text{CC}} = 1\text{V}$

Pin Configuration

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SuperCap is a trademark of Baknor Industries. MaxCap is a trademark of the Carborundum Corp.

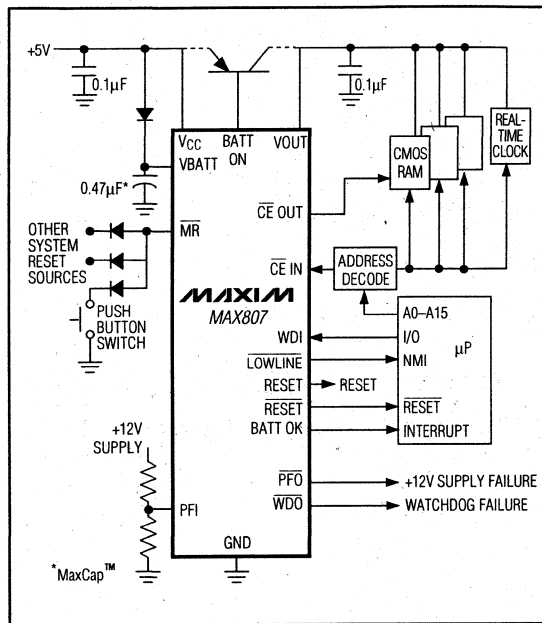
MAXIM

Maxim Integrated Products 5-41

Call toll free 1-800-998-8800 for free samples or literature.

μP Supervisory Circuit with ±1.5% Reset Accuracy

Typical Operating Circuit



Ordering Information

PART [†]	TEMP. RANGE	PIN-PACKAGE
MAX807_CPE	0°C to +70°C	16 Plastic DIP
MAX807_CSE	0°C to +70°C	16 Wide SO
MAX807_EPE	-40°C to +85°C	16 Plastic DIP
MAX807_EWE	-40°C to +85°C	16 Wide SO
MAX807_MJE	-55°C to +125°C	16 Cerdip

[†] This part offers a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.

SUFFIX	RESET THRESHOLD (V)		
	MIN	TYP	MAX
L	4.60	4.675	4.75
N	4.50	4.575	4.65
M	4.35	4.425	4.50



3-Pin Microprocessor Reset Circuit

General Description

The MAX809/MAX810 are microprocessor (μ P) supervisory circuits used to monitor the power supplies in μ P and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits.

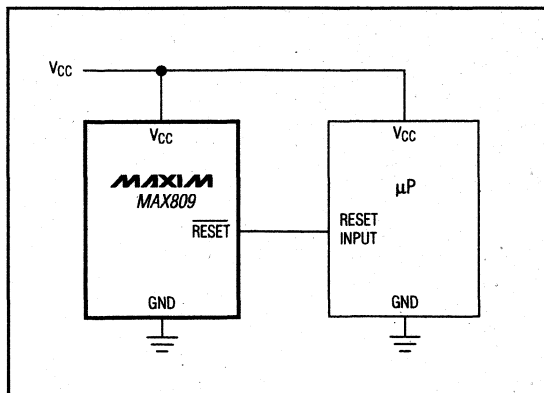
These circuits perform a single function: They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The only difference between the two devices is that the MAX809 has an active-low $\overline{\text{RESET}}$ output (which is guaranteed to be in the correct state for V_{CC} down to 1V), while the MAX810 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC} . Reset thresholds suitable for operation with a variety of supply voltages are available.

Low supply current makes the MAX809/MAX810 ideal for use in portable equipment. The MAX809/MAX810 come in a 3-pin SOT-23 package.

Applications

Computers
Controllers
Intelligent Instruments
Critical μ P and μ C Power Monitoring
Portable/Battery-Powered Equipment

Typical Operating Circuit



Features

- ◆ Precision Monitoring of 3V, 3.3V, and 5V Power-Supply Voltages
- ◆ Fully Specified Over Temperature
- ◆ 140ms Min Power-On Reset Pulse Width;
RESET Output (MAX809)
RESET Output (MAX810)
- ◆ 17 μ A Supply Current
- ◆ Guaranteed RESET Valid to $V_{CC} = 1\text{V}$ (MAX809)
- ◆ Power Supply Transient Immunity
- ◆ No External Components
- ◆ 3-Pin SOT-23 Package

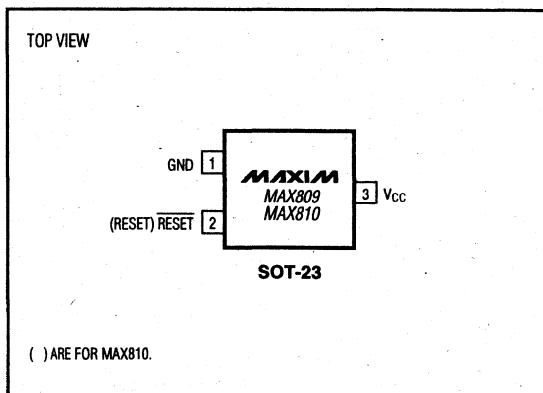
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX809_EUR-T	-40°C to +85°C	3 SOT-23
MAX810_EUR-T	-40°C to +85°C	3 SOT-23

† Insert the desired suffix letter (from the table below) into the blank to complete the part number:

SUFFIX	RESET THRESHOLD (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63

Pin Configuration



MAX809/MAX810

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3-Pin Microprocessor Reset Circuit

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V _{CC}	-0.3V to 6.0V
RESET, RESET	-0.3V to (V _{CC} + 0.3V)
Input Current, V _{CC}	20mA
Output Current, RESET, RESET	20mA
Rate of Rise, V _{CC}	100V/μs

Continuous Power Dissipation (T_A = +70°C)

SOT-23 (derate above +70°C by 4mW/°C)	320mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full range, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 5V for L/M versions, V_{CC} = 3.3V for T/S versions, and V_{CC} = 3V for R version.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CC} Range		T _A = 0°C to +70°C	1.0		5.5	V
		T _A = -40°C to +85°C	1.2		5.5	
Supply Current	I _{CC}	V _{CC} < 5.5V, MAX8_ _L /M		24	60	μA
		V _{CC} < 3.6V, MAX8_ _R /S/T		17	50	
Reset Threshold (Note 2)	V _{TH}	MAX8_ _L	T _A = +25°C		4.56	V
			T _A = -40°C to +85°C		4.63	
		MAX8_ _M	T _A = +25°C		4.31	
			T _A = -40°C to +85°C		4.38	
		MAX8_ _T	T _A = +25°C		4.25	
			T _A = -40°C to +85°C		4.45	
		MAX8_ _S	T _A = +25°C		3.04	
			T _A = -40°C to +85°C		3.08	
		MAX8_ _R	T _A = +25°C		3.00	
			T _A = -40°C to +85°C		3.15	
Reset Threshold Tempco				30		ppm/°C
V _{CC} to Reset Delay (Note 2)		V _{CC} = V _{TH} to (V _{TH} - 100mV)		20		μs
Reset Active Timeout Period			140	240	560	ms
RESET Output Voltage Low (MAX809)	V _{OL}	V _{CC} = V _{TH} min, I _{SINK} = 1.2mA, MAX809R/S/T			0.3	V
		V _{CC} = V _{TH} min, I _{SINK} = 3.2mA, MAX809L/M			0.4	
		V _{CC} > 1.0V, I _{SINK} = 50μA			0.3	
RESET Output Voltage High (MAX809)	V _{OH}	V _{CC} > V _{TH} max, I _{SOURCE} = 500μA, MAX809R/S/T	0.8V _{CC}			V
		V _{CC} > V _{TH} max, I _{SOURCE} = 800μA, MAX809L/M	V _{CC} - 1.5			
RESET Output Voltage Low (MAX810)	V _{OL}	V _{CC} = V _{TH} max, I _{SINK} = 1.2mA, MAX810R/S/T			0.3	V
		V _{CC} = V _{TH} max, I _{SINK} = 3.2mA, MAX810L/M			0.4	
RESET Output Voltage High (MAX810)	V _{OH}	1.8V < V _{CC} < V _{TH} min, I _{SOURCE} = 150μA	0.8V _{CC}			V

Note 1: Production testing done at T_A = +25°C, over temperature limits guaranteed by design only.

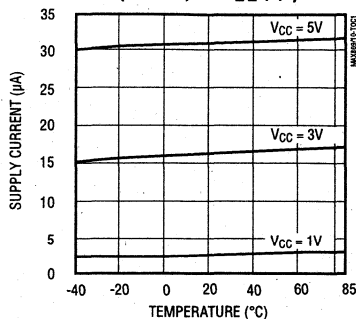
Note 2: RESET Output for MAX809, ~~RESET~~ Output for MAX810.

3-Pin Microprocessor Reset Circuit

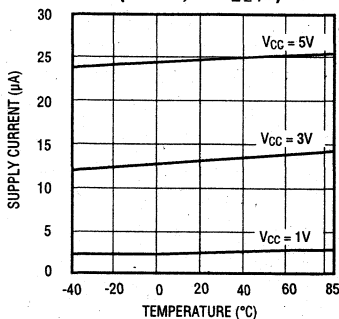
Typical Operating Characteristics

MAX809/MAX810

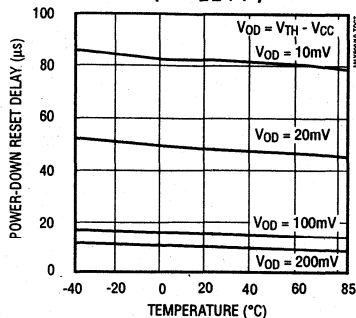
SUPPLY CURRENT vs. TEMPERATURE
(NO LOAD, MAX8_R/S/T)



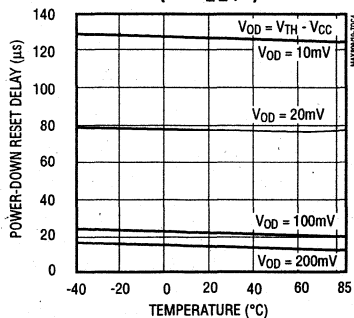
SUPPLY CURRENT vs. TEMPERATURE
(NO LOAD, MAX8_L/M)



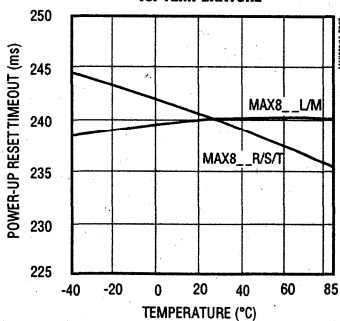
POWER-DOWN RESET DELAY vs. TEMPERATURE
(MAX8_R/S/T)



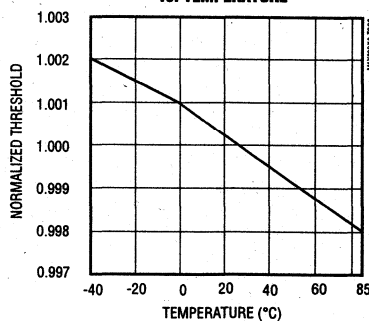
POWER-DOWN RESET DELAY vs. TEMPERATURE
(MAX8_L/M)



POWER-UP RESET TIMEOUT
vs. TEMPERATURE



NORMALIZED RESET THRESHOLD
vs. TEMPERATURE



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3-Pin Microprocessor Reset Circuit

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	RESET (MAX809)	RESET Output remains low while V _{CC} is below the reset threshold, and for 240ms after V _{CC} rises above the reset threshold.
	RESET (MAX810)	RESET Output remains high while V _{CC} is below the reset threshold, and for 240ms after V _{CC} rises above the reset threshold.
3	V _{CC}	Supply Voltage (+5V, +3.3V, or +3.0V)

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the microprocessor (μ P) during power-up, power-down, and brownout conditions, the MAX809/MAX810 are relatively immune to short duration negative-going V_{CC} transients (glitches).

Figure 1 shows typical transient duration vs. reset comparator overdrive, for which the MAX809/MAX810 do **not** generate a reset pulse. The graph was generated using a negative-going pulse applied to V_{CC}, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, for the MAX809L and MAX810M, a V_{CC} transient that goes 100mV below the reset threshold and lasts 20 μ s or less will not cause a reset pulse. A 0.1 μ F bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

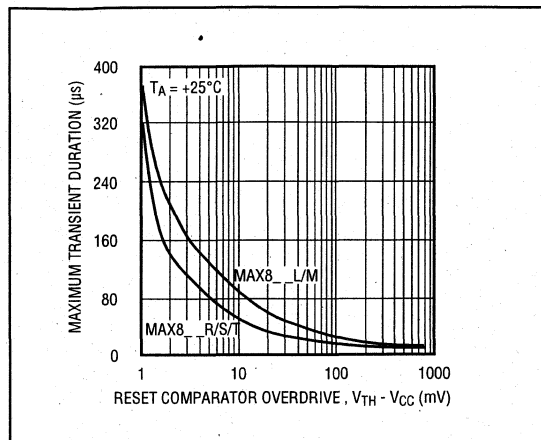


Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Ensuring a Valid Reset Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX809 RESET output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undetermined voltages. This presents no problem in most applications, since most μ P and other circuitry is inoperative with V_{CC} below 1V. However, in applications where RESET must be valid down to 0V, adding a pull-down resistor to RESET causes any stray leakage currents to flow to ground, holding RESET low (Figure 2). R1's value is not critical; 100k Ω is large enough not to load RESET and small enough to pull RESET to ground.

A 100k Ω pull-up resistor to V_{CC} is also recommended for the MAX810, if RESET is required to remain valid for V_{CC} < 1V.

3-Pin Microprocessor Reset Circuit

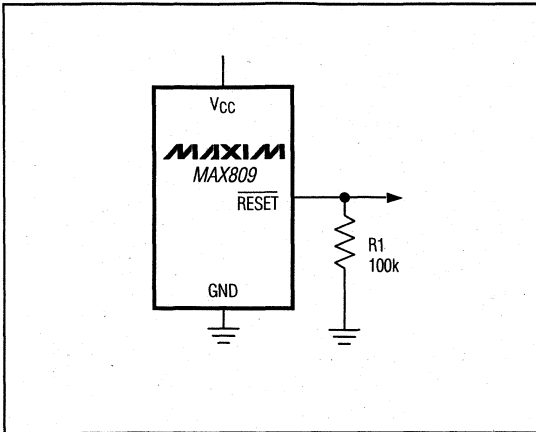


Figure 2. $\overline{\text{RESET}}$ Valid to V_{CC} = Ground Circuit

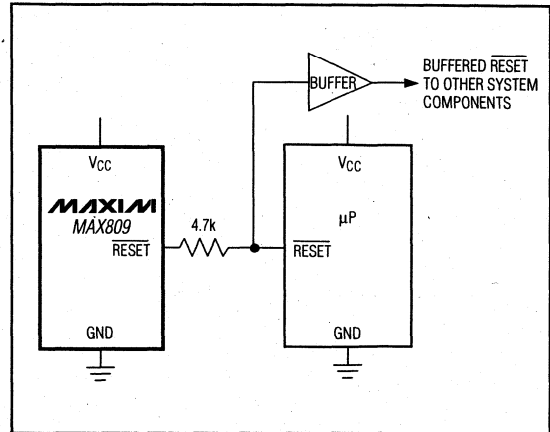


Figure 3. Interfacing to μ Ps with Bidirectional Reset I/O

Interfacing to μ Ps with Bidirectional Reset Pins

μ Ps with bidirectional reset pins (such as the Motorola 68HC11 series) can connect to the MAX809 reset output. If, for example, the MAX809 $\overline{\text{RESET}}$ output is asserted high and the μ P wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7k Ω resistor between the MAX809 $\overline{\text{RESET}}$ output and the μ P reset I/O (Figure 3). Buffer the MAX809 $\overline{\text{RESET}}$ output to other system components.

Benefits of Highly Accurate Reset Threshold

Most μ P supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal sup-

ply voltages. This ensures a reset will **not** occur within 5% of the nominal supply, but **will** occur when the supply is 10% below nominal.

When using ICs rated at only the nominal supply $\pm 5\%$, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The MAX809L/T and MAX810L/T use highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

MAXIM

4-Pin μ P Voltage Monitors with Manual Reset Input

General Description

The MAX811/MAX812 are low-power microprocessor (μ P) supervisory circuits used to monitor power supplies in μ P and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits. The MAX811/MAX812 also provide a debounced manual reset input.

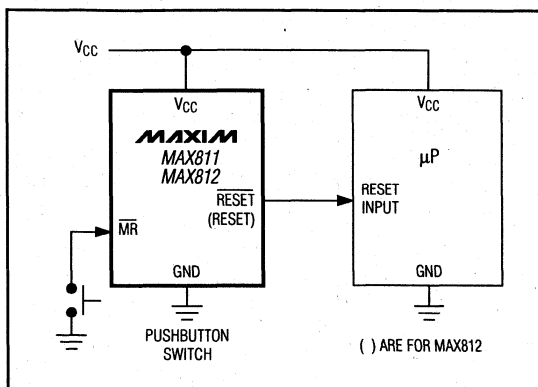
These devices perform a single function: They assert a reset signal whenever the V_{CC} supply voltage falls below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The only difference between the two devices is that the MAX811 has an active-low $\overline{\text{RESET}}$ output (which is guaranteed to be in the correct state for V_{CC} down to 1V), while the MAX812 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC} . Reset thresholds are available for operation with a variety of supply voltages.

Low supply current makes the MAX811/MAX812 ideal for use in portable equipment. The devices come in a 4-pin SOT-143 package.

Applications

Computers
Controllers
Intelligent Instruments
Critical μ P and μ C Power Monitoring
Portable/Battery-Powered Equipment

Typical Operating Circuit



Features

- ◆ Precision Monitoring of 3V, 3.3V, and 5V Power-Supply Voltages
- ◆ 6 μ A Supply Current
- ◆ 140ms Min Power-On Reset Pulse Width; $\overline{\text{RESET}}$ Output (MAX811), RESET Output (MAX812)
- ◆ Guaranteed Over Temperature
- ◆ Guaranteed $\overline{\text{RESET}}$ Valid to $V_{CC} = 1\text{V}$ (MAX811)
- ◆ Power-Supply Transient Immunity
- ◆ No External Components
- ◆ 4-Pin SOT-143 Package

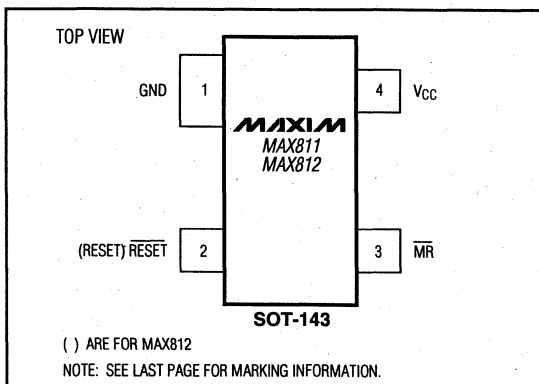
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX811_CUS-T	0°C to +70°C	4 SOT-143
MAX812_CUS-T	0°C to +70°C	4 SOT-143

* This part offers a choice of five different reset threshold voltages. Select the letter corresponding to the desired nominal reset threshold voltage, and insert it into the blank to complete the part number.

RESET THRESHOLD	
SUFFIX	VOLTAGE (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63

Pin Configuration



MAX811/MAX812

5

4-Pin μ P Voltage Monitors with Manual Reset Input

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

VCC-0.3V to 6.0V

All Other Inputs.....-0.3V to (VCC + 0.3V)

Input Current, VCC, MR20mA

Output Current, RESET or RESET.....20mA

Continuous Power Dissipation (TA = +70°C)

SOT-143 (derate 4mW/°C above +70°C).....320mW

Operating Temperature Range.....0°C to +70°C

Storage Temperature Range.....-65°C to +160°C

Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = 5V for L/M versions, VCC = 3.3V for T/S versions, VCC = 3V for R version, TA = 0°C to +70°C, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Range			1.0		5.5	V
Supply Current	ICC	MAX81_L/M, VCC = 5.5V, IOUT = 0A		6	15	μ A
		MAX81_R/S/T, VCC = 3.6V, IOUT = 0A		2.7	10	
Reset Threshold (Note 2)	VTH	MAX81_L	4.50	4.63	4.75	V
		MAX81_M	4.25	4.38	4.50	
		MAX81_T	3.00	3.08	3.15	
		MAX81_S	2.85	2.93	3.00	
		MAX81_R	2.55	2.63	2.70	
Reset Threshold Tempco				30		ppm/°C
VCC to Reset Delay (Note 2)		VOD = 125mV, MAX81_L/M		40		μ s
		VOD = 125mV, MAX81_R/S/T		20		
Reset Active Timeout Period	trp	VCC = VTH(MAX)	140		560	ms
MR Minimum Pulse Width	tMR		10			μ s
MR Glitch Immunity (Note 3)				100		ns
MR to Reset Propagation Delay (Note 2)	tMD			0.5		μ s
MR Input Threshold	VIH	VCC > VTH(MAX), MAX81_L/M	2.3			V
	VIL			0.8		
	VIH	VCC > VTH(MAX), MAX81_R/S/T	0.7 x VCC			
	VIL			0.25 x VCC		
MR Pull-Up Resistance			10	20	30	k Ω
RESET Output Voltage (MAX812)	VOH	ISOURCE = 150 μ A, 1.8V < VCC < VTH(MIN)	0.8VCC			V
	VOL	MAX812R/S/T only, ISINK = 1.2mA, VCC = VTH(MAX)		0.3		
		MAX812L/M only, ISINK = 3.2mA, VCC = VTH(MAX)		0.4		

4-Pin μ P Voltage Monitors with Manual Reset Input

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V for L/M versions, V_{CC} = 3.3V for T/S versions, V_{CC} = 3V for R version, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET Output Voltage (MAX811)	VOL	MAX811R/S/T only, $I_{SINK} = 1.2mA$, $V_{CC} = V_{TH(MIN)}$			0.3	V
		MAX811L/M only, $I_{SINK} = 3.2mA$, $V_{CC} = V_{TH(MIN)}$			0.4	
		$I_{SINK} = 50\mu A$, $V_{CC} > 1.0V$			0.3	
	VOH	MAX811R/S/T only, $I_{SOURCE} = 500\mu A$, $V_{CC} > V_{TH(MAX)}$	0.8 V_{CC}			
		MAX811L/M only, $I_{SOURCE} = 800\mu A$, $V_{CC} > V_{TH(MAX)}$	$V_{CC} - 1.5$			

Note 1: Production testing done at T_A = +25°C, over temperature limits guaranteed by design using six sigma design limits.

Note 2: RESET output for MAX811, RESET output for MAX812.

Note 3: "Glitches" of 100ns or less typically will not generate a reset pulse.

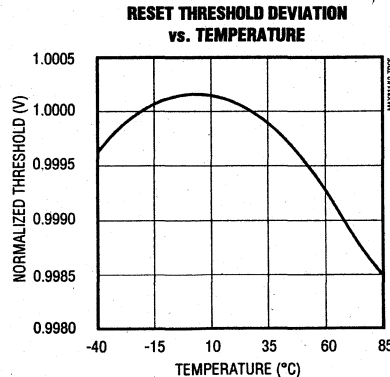
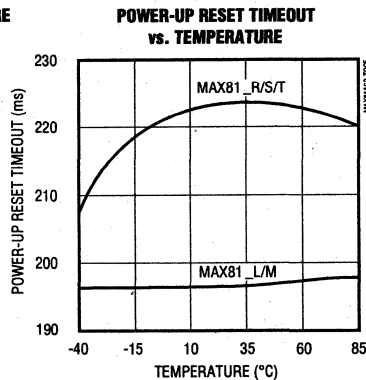
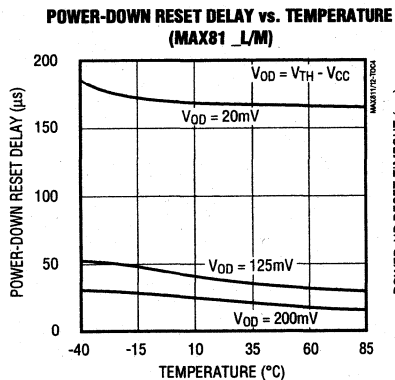
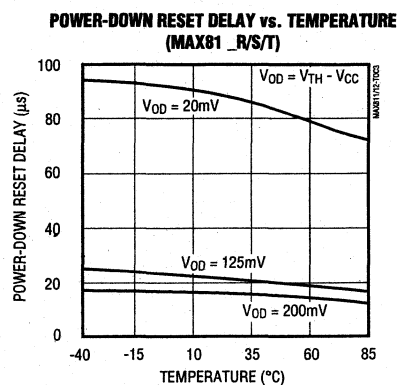
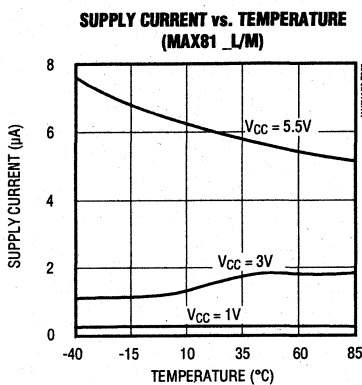
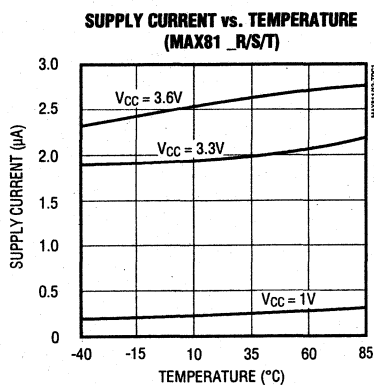
MAX811/MAX812

5

4-Pin μ P Voltage Monitors with Manual Reset Input

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



4-Pin μ P Voltage Monitors with Manual Reset Input

Pin Description

MAX811/MAX812

PIN		NAME	FUNCTION
MAX811	MAX812		
1	1	GND	Ground
2	—	RESET	Active-Low Reset Output. RESET remains low while VCC is below the reset threshold or while MR is held low. RESET remains low for the Reset Active Timeout Period (trp) after the reset conditions are terminated.
—	2	RESET	Active-High Reset Output. RESET remains high while VCC is below the reset threshold or while MR is held low. RESET remains high for Reset Active Timeout Period (trp) after the reset conditions are terminated.
3	3	MR	Manual Reset Input. A logic low on MR asserts reset. Reset remains asserted as long as MR is low and for TBDms after MR returns high. This active-low input has an internal 20k Ω pull-up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused.
4	4	VCC	+5V, +3.3V, or +3V Supply Voltage

Detailed Description

Reset Output

A microprocessor's (μ P's) reset input starts the μ P in a known state. These μ P supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

RESET is guaranteed to be a logic low for $V_{CC} > 1V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps RESET low for the reset timeout period; after this interval, RESET goes high.

If a brownout condition occurs (V_{CC} dips below the reset threshold), RESET goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and RESET goes low. The internal timer starts after V_{CC} returns above the reset threshold, and RESET remains low for the reset timeout period.

The manual reset input (MR) can also initiate a reset. See the *Manual Reset Input* section.

The MAX812 has an active-high RESET output that is the inverse of the MAX811's RESET output.

Manual Reset Input

Many μ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on MR asserts reset. Reset remains asserted while MR is low, and for the Reset Active Timeout Period (trp) after MR returns high. This input has an internal 20k Ω pull-up resistor, so it can be left open if it is not used. MR can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from MR to GND to create a manual-reset function; external debounce circuitry is not required. If MR is driven from long cables or if the device is used in a noisy environment, connecting a 0.1 μ F capacitor from MR to ground provides additional noise immunity.

Reset Threshold Accuracy

The MAX811/MAX812 are ideal for systems using a 5V $\pm 5\%$ or 3V $\pm 5\%$ power supply with ICs specified for 5V $\pm 10\%$ or 3V $\pm 10\%$, respectively. They are designed to meet worst-case specifications over temperature. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range for the system ICs. The thresholds are pre-trimmed and exhibit tight distribution, reducing the range over which an undesirable reset may occur.

4-Pin μ P Voltage Monitors with Manual Reset Input

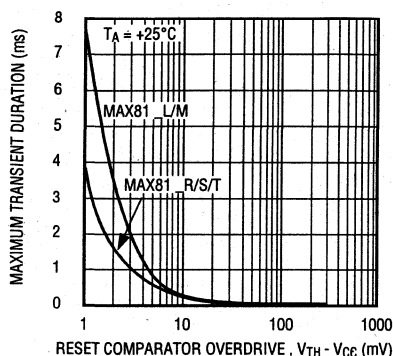


Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Comparator Overdrive

Applications Information

Negative-Going VCC Transients

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, the MAX811/MAX812 are relatively immune to short duration negative-going VCC transients (glitches).

Figure 1 shows typical transient durations vs. reset comparator overdrive, for which the MAX811/MAX812 do not generate a reset pulse. This graph was generated using a negative-going pulse applied to VCC, starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going VCC transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC transient that goes 125mV below the reset threshold and lasts 40 μ s or less (MAX811_L/M) or 20 μ s or less (MAX811_T/S/R) will not cause a reset pulse to be issued. A 0.1 μ F capacitor mounted as close as possible to VCC provides additional transient immunity.

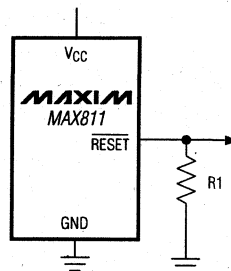


Figure 2. $\overline{\text{RESET}}$ Valid to VCC = Ground Circuit

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to VCC = 0V

When VCC falls below 1V, the MAX811 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS-logic inputs connected to the $\overline{\text{RESET}}$ output can drift to undetermined voltages. This presents no problem in most applications, since most μ P and other circuitry is inoperative with VCC below 1V. However, in applications where the $\overline{\text{RESET}}$ output must be valid down to 0V, adding a pull-down resistor to the $\overline{\text{RESET}}$ pin will cause any stray leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low (Figure 2). R1's value is not critical; 100k Ω is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

A 100k Ω pull-up resistor to VCC is also recommended for the MAX812 if $\overline{\text{RESET}}$ is required to remain valid for VCC < 1V.

4-Pin μ P Voltage Monitors with Manual Reset Input

Interfacing to μ Ps with Bidirectional Reset Pins

μ Ps with bidirectional reset pins (such as the Motorola 68HC11 series) can contend with the MAX811/MAX812 reset outputs. If, for example, the MAX811 RESET output is asserted high and the μ P wants to pull it low, indeterminate logic levels may result. To correct such cases, connect a $4.7\text{k}\Omega$ resistor between the MAX811 RESET (or MAX812 RESET) output and the μ P reset I/O (Figure 3). Buffer the reset output to other system components.

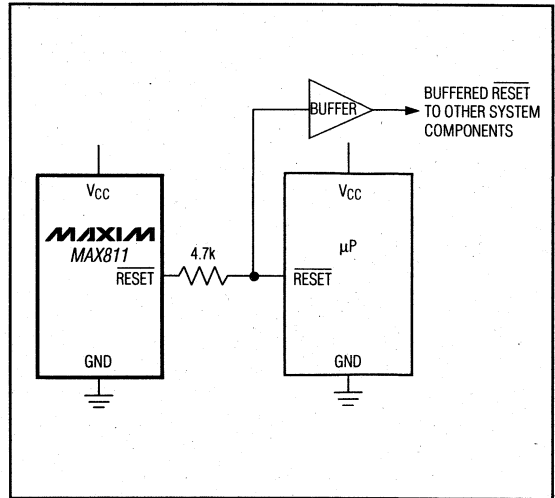


Figure 3. Interfacing to μ Ps with Bidirectional Reset I/O

MAX811/MAX812

MAXIM

±1% Accuracy, Low-Power, +3V and +5V μP Supervisory Circuits

General Description

The MAX814/MAX815/MAX816 are high-accuracy microprocessor (μP) supervisory circuits that provide power-on reset, watchdog, and power-fail functions. They eliminate manual trimming and improve reliability in critical applications needing high-accuracy reset thresholds. The $\overline{\text{RESET}}$ output is guaranteed to be in the correct state for V_{CC} down to 1V. The reset comparator is designed to ignore fast transients on V_{CC} . Reset thresholds are available for operation with a variety of 3V and 5V supply voltages.

A 75μA maximum supply current makes the MAX814/MAX815/MAX816 ideal for use in portable equipment. All three devices are available in 8-pin DIP and SO packages. See the *Selector Table* below for a review of features.

Selector Table

FEATURE	MAX814	MAX815	MAX816
RESET Output	✓	✓	✓
RESET Output	✓	✓	✓
Manual Reset	✓	✓	✓
VCC Reset Voltage	K, L, N, T	K, L, N, T	Adjustable
Power-Fail Monitor	✓	✓	✓
Low-Line Detector	✓		
Watchdog Circuit		✓	

Applications

Medical Equipment
Controllers
Intelligent Instruments
Critical μP Power Monitoring
Portable/Battery-Powered Equipment
Set-Top Boxes

Features

- ♦ ±1% Worst-Case Reset Threshold Accuracy
- ♦ 4.8V, 4.7V, 4.55V, 3.03V, or Adjustable Reset Thresholds
- ♦ ±1% Low-Line Threshold Accuracy (MAX814)
60mV Above Reset Threshold
- ♦ 200ms Reset Time Delay
- ♦ Active-Low $\overline{\text{RESET}}$ Output
Active-High RESET Output (MAX814/MAX816)
- ♦ 75μA Max Supply Current
- ♦ Guaranteed $\overline{\text{RESET}}$ Valid to $V_{CC} = 1V$
- ♦ Manual Reset Input
- ♦ ±2% Power-Fail Comparator
- ♦ Independent Watchdog with 1.56sec Timeout (MAX815)
- ♦ Power-Supply Glitch Immunity
- ♦ 8-Pin SO and DIP Packages

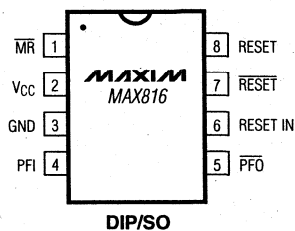
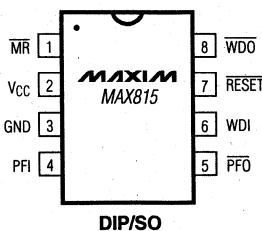
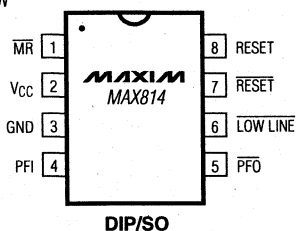
Reset Trip Thresholds

MAX814/MAX815		
SUFFIX	RESET TRIP THRESHOLD	
	MIN (V)	MAX (V)
K	4.75	4.85
L	4.65	4.75
N	4.50	4.60
T	3.00	3.06
MAX816		
—	Adjustable	

Ordering Information appears at end of data sheet.

Pin Configurations

TOP VIEW



±1% Accuracy, Low-Power, +3V and +5V μP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect GND)	
V _{CC}	-0.3V to +6.0V
All Other Pins (Note 1)	-0.3V to (V _{CC} + 0.3V)
Terminal Current (PFI, RESET IN, MR)	10mA
Terminal Current (all other pins)	20mA
Continuous Power Dissipation (T _A = +25°C)	
Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
SO (derate 5.88mW/°C above +70°C)	471mW

Operating Temperature Ranges	
Commercial	0°C to +70°C
Extended	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, +5V Parts (MAX814/MAX815K, L, N)

(V_{CC} = 4.85V to 5.5V for MAX814K/MAX815K, V_{CC} = 4.75V to 5.5V for MAX814L/MAX815L, V_{CC} = 4.60V to 5.5V for MAX814N/MAX815N, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V _{CC}	MAX814_C, MAX815_C		1.0		5.5	V
		MAX814_E, MAX815_E		1.2		5.5	
Supply Current	I _{SUPPLY}	MAX814_C, MAX815_C				75	μA
		MAX814_E, MAX815_E				85	
Reset Threshold	V _{RT}	MAX814K, MAX815K		4.75		4.85	V
		MAX814L, MAX815L		4.65		4.75	
		MAX814N, MAX815N		4.50		4.60	
Reset Threshold Hysteresis	V _{RT}				0		mV
Reset Pulse Width	t _{RS}			140	200	250	ms
RESET Output Voltage	V _{OH}	MAX814	I _{SOURCE} = 800μA	V _{CC} -1.5			V
	V _{OL}		I _{SINK} = 3.2mA			0.4	
RESET, WDO, PFO, LOW LINE Output Voltage	V _{OH}	I _{SOURCE} = 800μA		V _{CC} -1.5			V
	V _{OL}	I _{SINK} = 3.2mA				0.4	
		MAX814_C/MAX815_C, V _{CC} = 1.0V, I _{SINK} = 50μA				0.3	
		MAX814_E/MAX815_E, V _{CC} = 1.2V, I _{SINK} = 100μA				0.3	
Watchdog Timeout Period	t _{WD}	MAX815		1.12		2.00	sec
WDI Pulse Width	t _{WP}	MAX815		50			ns
WDI Input Threshold	V _{WDI}	MAX815, V _{CC} = 5.0V	Low			0.8	V
			High	2.4			
WDI Input Current	I _{WDI}	WDI = V _{CC} or WDI = 0V		-1.0		1.0	μA
MR to WDO High Delay	t _{WDO}	MAX815 (Note 1)			1		μs
LOW LINE to RESET Differential Threshold	ΔV _{LL}	MAX814_C, V _{CC} falling		50		70	mV
		MAX814_E, V _{CC} falling		48		73	
LOW LINE Threshold	V _{LLT}	MAX814K, V _{CC} rising				4.93	V
		MAX814L, V _{CC} rising				4.83	
		MAX814N, V _{CC} rising				4.68	

±1% Accuracy, Low-Power, +3V and +5V μP Supervisory Circuits

MAX814/MAX815/MAX816

5

ELECTRICAL CHARACTERISTICS, +5V Parts (MAX814/MAX815K, L, N) (continued)

(V_{CC} = 4.85V to 5.5V for MAX814K/MAX815K, V_{CC} = 4.75V to 5.5V for MAX814L/MAX815L, V_{CC} = 4.60V to 5.5V for MAX814N/MAX815N, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MR Pull-Up Current	IMR	MR = 0V	70		240	μA
MR Pulse Width	tMR		150			ns
MR Input Threshold	V _{MRLO}	Low			1.1	V
	V _{MRHI}	High	0.7 x V _{CC}			
MR to RESET Out Delay	tMD	(Note 3)			250	ns
PFI Input Threshold	VPFI	V _{CC} = 5.0V	2.45	2.50	2.55	V
PFI Input Current	IPFI		-15.00	6.0	35.00	nA
LOW LINE, PFO, WDO Assertion Delay		(Note 2)		200		μs

ELECTRICAL CHARACTERISTICS, +3V Parts (MAX814/MAX815T, MAX816)

(V_{CC} = 3.06V to 5.5V for MAX814T/MAX815T and MAX816, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V _{CC}	0°C to +70°C		1.0		5.5	V
		-40°C to +85°C		1.2		5.5	
Supply Current	I _{SUPPLY}	0°C to +70°C				75	μA
		-40°C to +85°C				85	
Reset Threshold	V _{RT}	0°C to +70°C		3.00		3.06	V
		-40°C to +85°C		3.00		3.08	
RESET IN Threshold	V _{RT}	MAX816C		1.683	1.700	1.717	V
		MAX816E		1.678	1.700	1.722	
RESET IN Input Current	I _{RT}	MAX816		-15	6	35	nA
Reset Threshold Hysteresis	V _{RT}				0		mV
Reset Pulse Width	t _{RS}			140	200	250	ms
RESET Output Voltage	V _{OH}	V _{RT(max)} < V _{CC} < 3.6V; MAX814T, MAX816	I _{SOURCE} = 500μA	0.8 x V _{CC}			V
	V _{OL}		I _{SINK} = 1.2mA		0.3		
	V _{OH}	4.5V < V _{CC} < 5.5V; MAX814T, MAX816	I _{SOURCE} = 800μA	V _{CC} - 1.5			
	V _{OL}		I _{SINK} = 3.2mA		0.4		
RESET, WDO, PFO, LOW LINE Output Voltage	V _{OH}	V _{RT(max)} < V _{CC} < 3.6V	I _{SOURCE} = 500μA	0.8 x V _{CC}			V
	V _{OL}		I _{SINK} = 1.2mA		0.3		
	V _{OH}	4.5V < V _{CC} < 5.5V	I _{SOURCE} = 800μA	V _{CC} - 1.5			
	V _{OL}		I _{SINK} = 3.2mA		0.4		
	V _{OL}	T _A = 0°C to +70°C, V _{CC} = 1.0V, I _{SINK} = 50μA			0.3		
					0.3		
Watchdog Timeout Period	t _{WD}	MAX815T		1.12		2.00	sec

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ELECTRICAL CHARACTERISTICS, +3V Parts (MAX814/MAX815T, MAX816) (continued)

(V_{CC} = 3.06V to 5.5V for MAX814T/MAX815T and MAX816, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
WDI Pulse Width	t _{WP}	MAX815T	V _{RT(max)} < V _{CC} < 3.6V 4.5V < V _{CC} < 5.5V	100 50			ns
WDI Input Threshold	V _{WDI}	V _{RT(max)} < V _{CC} < 3.6V; MAX815T	Low			0.8	V
			High	0.7 × V _{CC}			
		V _{CC} = 5.0V; MAX815T	Low			0.8	
			High	2.4			
WDI Input Current	I _{WDI}	WDI = V _{CC} or 0V, MAX815T		-1.0		1.0	μA
MR to WDO High Delay	t _{WDO}	MAX815T (Note 1)			1		μs
LOW LINE to RESET Differential Threshold	ΔV _{LL}	V _{CC} falling, MAX814TC		50		70	mV
		V _{CC} falling, MAX814TE		48		73	
LOW LINE Threshold	V _{LLT}	V _{CC} rising				3.163	V
MR Pull-Up Current	I _{MR}	MR = 0V	V _{RT(max)} < V _{CC} < 3.6V	70		240	μA
			4.5V < V _{CC} < 5.5V	110		370	
MR Pulse Width	t _{MR}	V _{RT(max)} < V _{CC} < 3.6V		500			ns
		4.5V < V _{CC} < 5.5V		150			
MR Input Threshold	V _{MRLO}	Low				1.1	V
	V _{MRHI}	High		0.7 × V _{CC}			
MR to RESET Out Delay	t _{MD}	V _{RT(max)} < V _{CC} < 3.6V; (Note 3)				750	ns
		4.5V < V _{CC} < 5.5V; (Note 3)				250	
PFI Input Threshold	V _{PFI}	V _{CC} = 3.3V, 5V		1.666	1.700	1.734	V
PFI Input Current	I _{PFI}			-15.00	6.0	35.00	nA

Note 1: Applies if WDO is externally connected to MR or if MR is externally driven.

Note 2: On power-up, delay from reset trip threshold crossing to valid outputs.

Note 3: Applies to both RESET and RESET.

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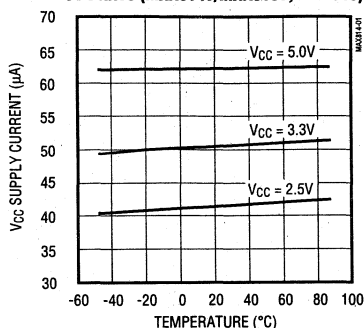
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

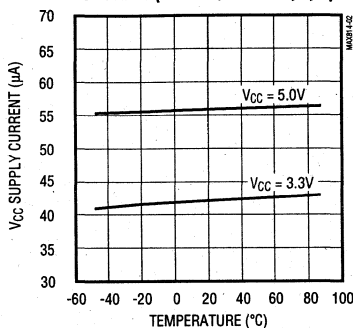
MAX814/MAX815/MAX816

5

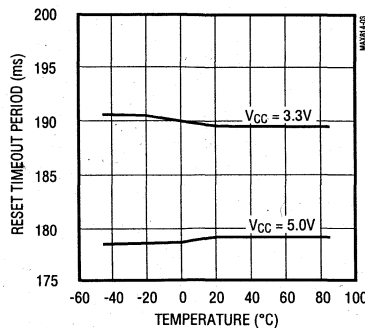
V_{CC} SUPPLY CURRENT vs. TEMPERATURE
3V PARTS (MAX814T/MAX815T, MAX816)



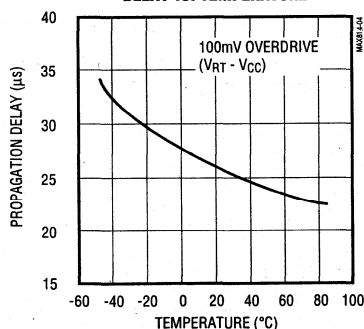
V_{CC} SUPPLY CURRENT vs. TEMPERATURE
5V PARTS (MAX814/MAX815K, L, N)



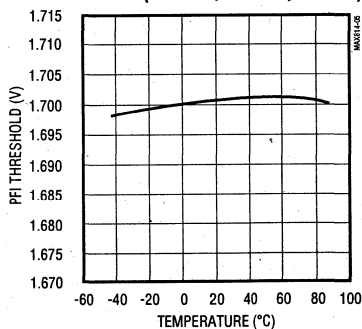
RESET TIMEOUT PERIOD vs. TEMPERATURE



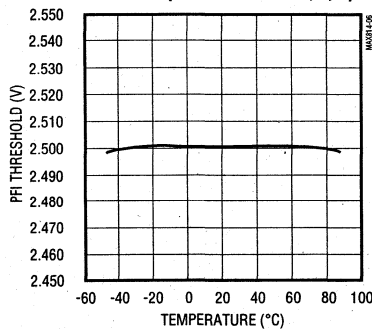
RESET-COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



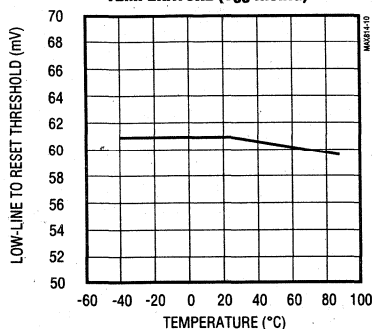
PFI THRESHOLD vs. TEMPERATURE
3V PARTS (MAX814T/MAX815T, MAX816)



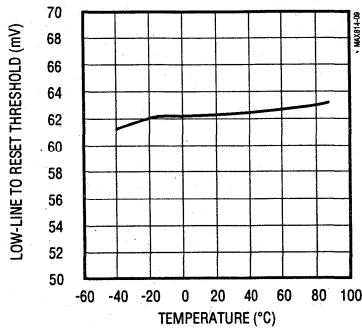
PFI THRESHOLD vs. TEMPERATURE
5V PARTS (MAX814/MAX815K, L, N)



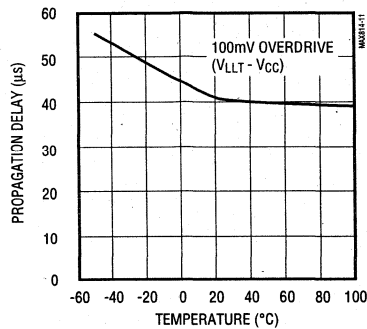
LOW-LINE TO RESET THRESHOLD vs. TEMPERATURE (V_{CC} RISING)



LOW-LINE TO RESET THRESHOLD vs. TEMPERATURE (V_{CC} FALLING)



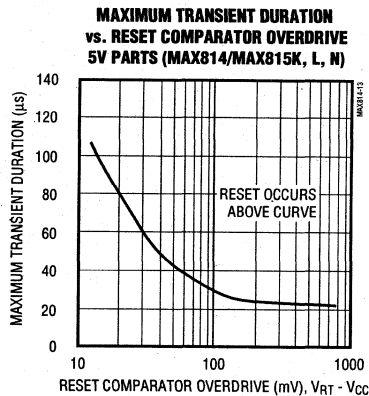
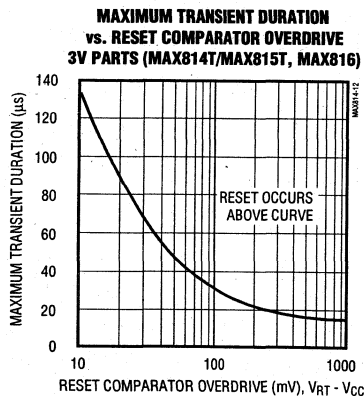
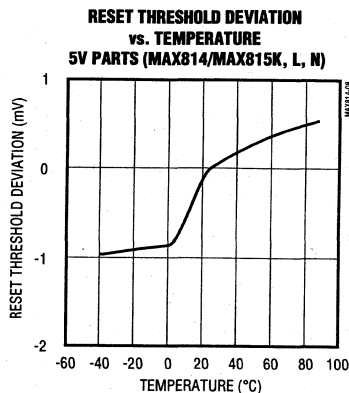
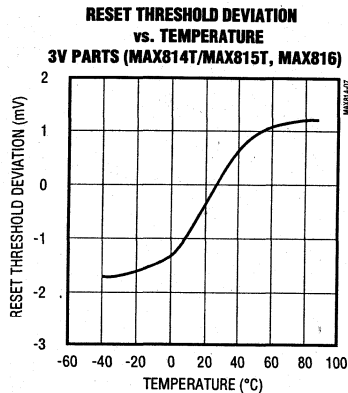
LOW-LINE COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



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Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



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Pin Description

PIN			NAME	FUNCTION
MAX814	MAX815	MAX816		
1	1	1	$\overline{\text{MR}}$	Manual-Reset Input. Triggers a reset when pulled below 1.10V. This active-low input has an internal 150μA pull-up current to V _{CC} , and can be driven with CMOS logic or shorted to GND with a switch or transistor.
2	2	—	V _{CC}	Positive Power-Supply Input. When V _{CC} is below the reset threshold voltage*, RESET is low, and remains low for a minimum of 140ms after it rises above the threshold.
—	—	2		Positive Power-Supply Input. On the MAX816, RESET is controlled by RESET IN, not V _{CC} .
3	3	3	GND	Ground
4	4	4	PFI	Power-Fail Input. The PFI threshold voltage is 1.70V on the MAX816 and on MAX814/MAX815 parts with the T suffix. It is 2.50V on MAX814/MAX815 parts with K, L, and N suffixes. Connect PFI to GND or V _{CC} when not used.
5	5	5	PFO	Power-Fail Output. When PFI is below its threshold, $\overline{\text{PFO}}$ is low; otherwise it is high.
—	6	—	WDI	Watchdog CMOS Input. If WDI remains high or low for more than 1.56sec, the watchdog timer times out, and WDO goes low. The timer is reset to zero on each WDI transition.
6	—	—	$\overline{\text{LOW LINE}}$	Low-Line Output. Normally high, $\overline{\text{LOW LINE}}$ goes low when V _{CC} falls 60mV above the reset threshold. It returns high as soon as V _{CC} rises above the low-line threshold.
—	—	6	RESET IN	Reset Comparator Input. Reference is 1.70V. When RESET IN is below 1.70V, RESET is low, and remains low for a minimum of 140ms after it rises above the reference.
7	7	7	$\overline{\text{RESET}}$	Reset Output. Normally high, active low. Controlled by $\overline{\text{MR}}$ and reset comparator.
—	8	—	WDO	Watchdog Output. Normally high, WDO goes low whenever the V _{CC} reset threshold comparator input voltage is low or when the watchdog timer times out. There is no appreciable delay going either direction when the V _{CC} threshold comparator toggles.
8	—	8	RESET	Reset Output. Active high. The inverse of $\overline{\text{RESET}}$.

*Reset Threshold Voltage is determined by part number suffix: K = 4.80V, L = 4.70V, N = 4.55V, T = 3.03V.

Detailed Description

The MAX814/MAX815/MAX816 are high-accuracy, low-power microprocessor (μP) supervisory circuits. They have μP-reset, watchdog-timer, and power-fail functions. Typical applications illustrating their similarities and differences are shown in Figures 1, 2, and 3. Figures 4, 5, and 6 show the block diagrams of these parts.

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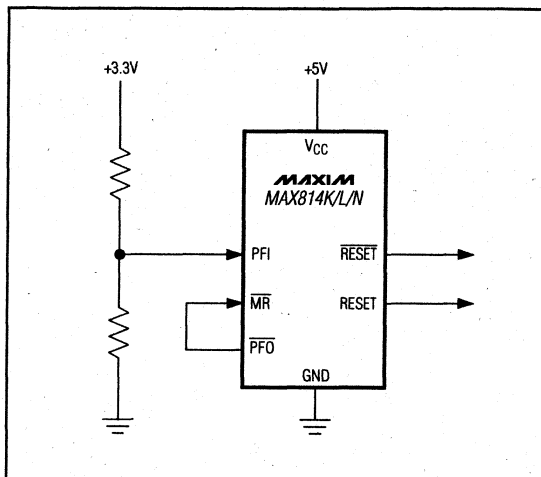


Figure 1a. Typical Application for Dual +3.3V and +5V Systems

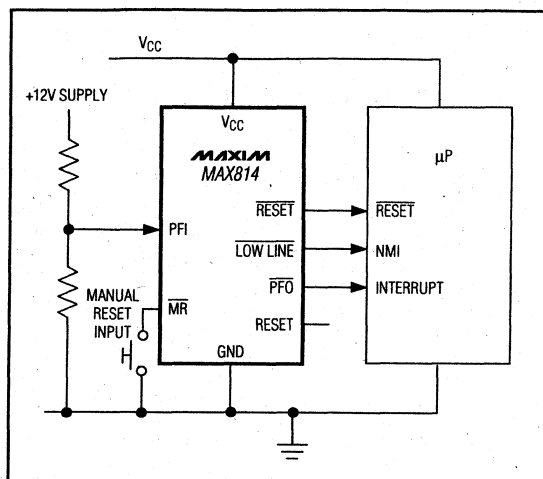


Figure 1b. MAX814 Typical Application

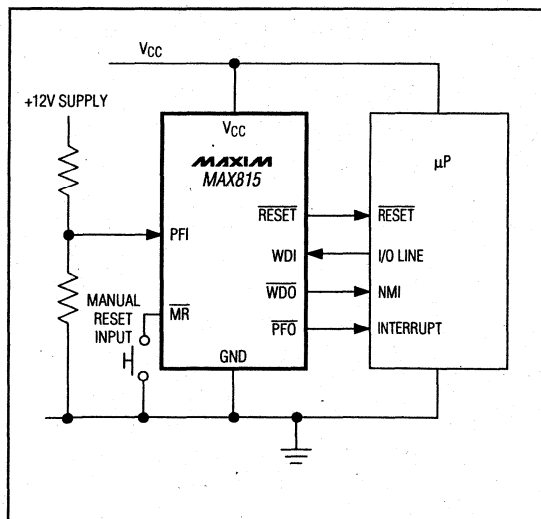


Figure 2. MAX815 Typical Application

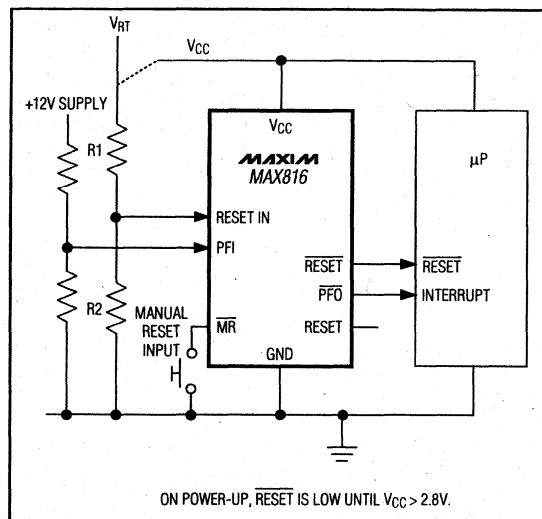


Figure 3. MAX816 Typical Application

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MAX814/MAX815/MAX816

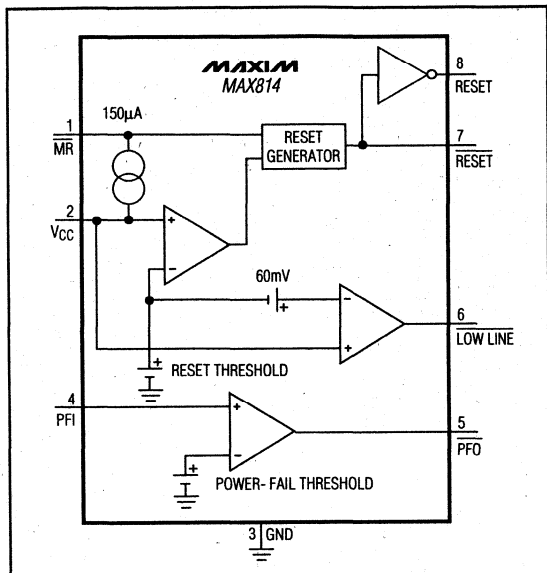


Figure 4. MAX814 Block Diagram

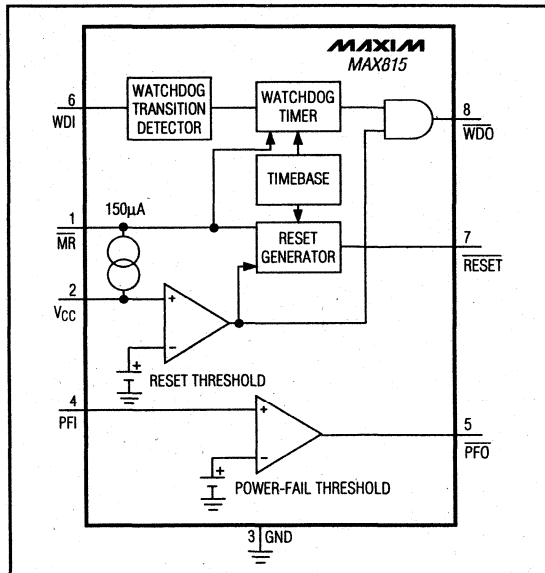


Figure 5. MAX815 Block Diagram

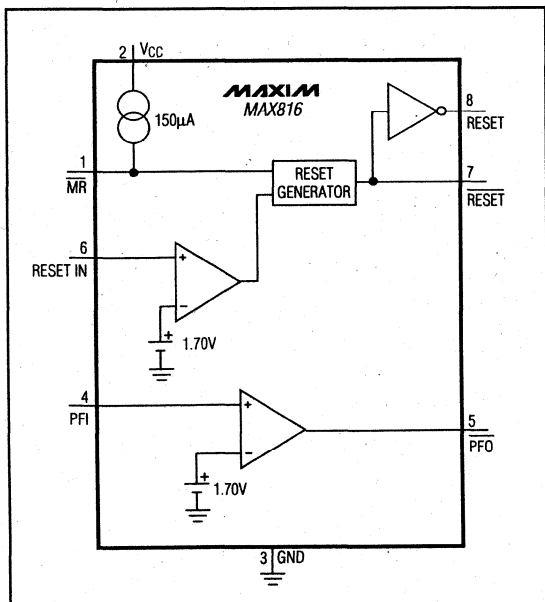


Figure 6. MAX816 Block Diagram

Reset Output

A μP's reset input starts the μP in a known state. Whenever the μP is in an unknown state, it should be held in reset. The MAX814/MAX815/MAX816 assert reset during power-up, power-down, or brownout conditions.

On power-up, once VCC reaches 1V, RESET is a guaranteed logic low of 0.4V or less. As VCC rises, RESET stays low. As VCC rises above the reset threshold, an internal timer releases RESET after 200ms. RESET also pulses low whenever VCC dips below the reset threshold (i.e., brownout condition). If brownout occurs in the middle of a previously initiated reset, the internal timer is reset and the output remains low for at least another 140ms after the brownout ends. On power-down, once VCC falls below the reset threshold, RESET stays low and is guaranteed to be less than 0.3V until VCC drops below 1V.

The MAX814 and MAX816 also offer active-high RESET outputs. They are the inverse of the RESET outputs.

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Reset Threshold

The MAX814/MAX815 have fixed, factory-set reset thresholds, signified by the first suffix letter in the part number (see Figure 7 for more information on reset ranges). The MAX816 has an adjustable reset threshold.

MAX814/MAX815 K-suffix parts have a minimum reset threshold set to 4.75V, worst case. They are intended for 5.0V systems with a ±4% or better power-supply tolerance design that must meet worst-case system parameters over time, temperature, line, and load variations. Typically, the reset threshold (V_{RT}) is greater than or equal to the minimum IC operating voltage ($V_{IC(MIN)}$). The "K" series 1%-tolerance reset threshold allows a larger range of power-supply tolerance. System ICs

that have a tight operating supply range, like the 386/486 μPs, need a RESET initiated at a minimum threshold of 4.75V, worst case.

L-suffix parts have a minimum reset threshold set to 4.65V, worst case. They are intended for 5.0V systems with a ±5% power-supply tolerance. Typically, the reset threshold is less than or equal to the minimum power-supply voltage, allowing system operation over the complete power-supply range. A reset is initiated at 4.75V maximum. The 1% "L" version maximizes the System IC Guard-Band Range.

N-suffix parts have a minimum reset threshold set to 4.55V, worst case. They are intended for 5.0V systems with a ±10% IC system. Typically, the reset threshold

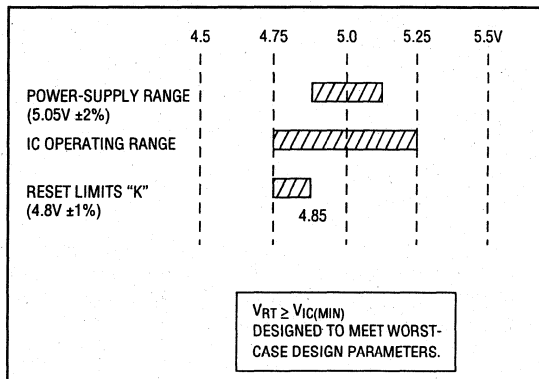


Figure 7a. K Suffix Design Range

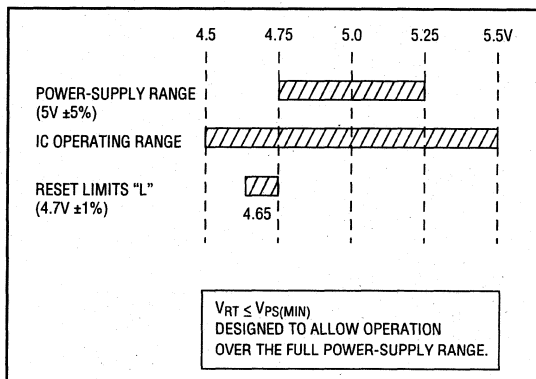


Figure 7b. L Suffix Design Range

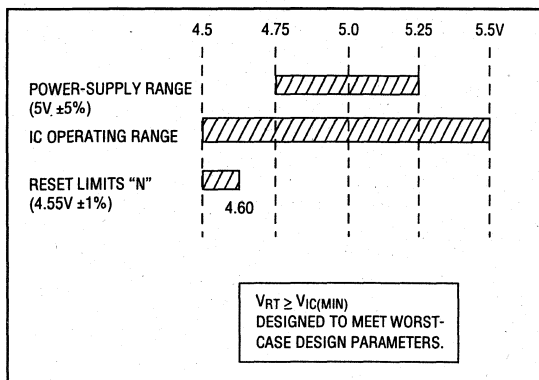


Figure 7c. N Suffix Design Range

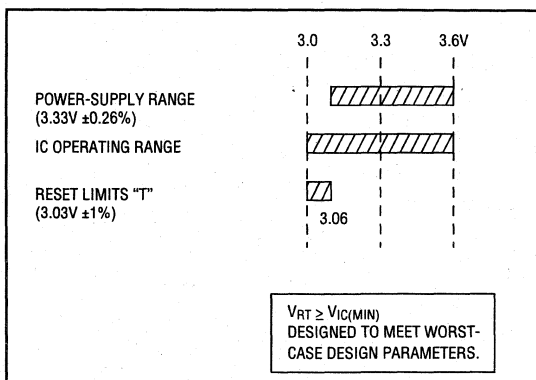


Figure 7d. T Suffix Design Range

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(V_{RT}) is greater than or equal to the minimum IC operating voltages (V_{ICMIN}). The 1% "L" series allows the use of a 5V ±5% power supply, and guarantees system operation over worst-case conditions, maximizing the Power-Supply Guard-Band Range.

T-suffix parts have a minimum reset threshold set to 3.00V, worst case. They are intended for 3.3V systems (3.33V ±0.26V) with a 7.8% or better power-supply tolerance. Typically, the reset threshold (V_{RT}) is greater than or equal to the minimum IC operating voltages (V_{ICMIN}).

The MAX816 has an adjustable reset threshold, set with an external resistive divider (Figure 3). The voltage on the RESET IN pin is monitored, not the voltage on V_{CC}. The RESET IN threshold is 1.700V, and has very high impedance and 35nA maximum leakage. Calculate the trip point, V_{RT}, as follows:

$$V_{RT} = \frac{V_{RIT} \times (R1 + R2)}{R2}$$

where V_{RT} = the desired reset threshold, V_{RIT} is the RESET IN threshold (1.700V), R1 is the resistor connected between V_{RT} and RESET IN, and R2 is the resistor connected between RESET IN and GND.

Resistors R1 and R2 can have very high values. The usual procedure is to set R2 to some conveniently high value (100kΩ, for example) and calculate R1 based on the desired reset threshold, using the following formula:

$$R1 = R2 \times \left[(V_{RT} / V_{RIT}) - 1 \right]$$

The MAX816 can achieve ±1.2% accuracy with 0.1% resistors.

Watchdog Timer (MAX815)

The watchdog circuit monitors the μP's activity. If the μP does not toggle the watchdog input (WDI) within the watchdog timeout period (t_{WP}), WDO goes low (Figure 8). WDO also goes low during reset conditions. Whenever V_{CC} is below the reset threshold, WDO stays low; however, unlike RESET, WDO does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, WDO goes high with no delay (Figure 9).

Typically, WDO is connected to the non-maskable interrupt (NMI) of a μP. When V_{CC} drops below the reset threshold, WDO goes low whether or not the watchdog timer has timed out (Figure 9). This would normally trigger an NMI interrupt, but RESET goes low simultaneously and thus overrides the NMI interrupt.

Connecting WDO to MR enables the watchdog timeout to generate a reset in the MAX815.

Early Power-Fail Warning

Critical systems often require early warning to indicate when power is failing. This warning provides time for the μP to store vital data and take care of any additional "housekeeping" before the power supply gets too far out of tolerance for the μP to operate reliably.

Power-Fail Comparator

The power-fail comparator is intended as an undervoltage detector to signal a failing power supply. However, the comparator does not need to be dedicated to this function, because it is completely separate from the rest of the circuitry. To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see Figures 1, 2, and 3). Choose the voltage divider ratio, so the voltage at PFI falls below V_{PFI} just before the monitored voltage drops out. Use PFO to interrupt the μP, so it can prepare for an orderly power-down.

The power-fail input (PFI) is compared to an internal reference. If the voltage on PFI is less than the power-fail reference, PFO sinks at least 1.2mA to GND; otherwise it sources at least 300μA from V_{CC}. The reference is 2.50V in the MAX814/MAX815 with K, L, N suffixes, or 1.70V with the T suffix. It is also 1.70V in the MAX816.

LOW LINE Output (MAX814)

The low-line detector is a separate comparator that monitors V_{CC} with a typical threshold voltage of 60mV above the normal reset threshold, with 2mV of hysteresis (Figure 9). If V_{CC} rises faster than 10μs/V, insert a 100pF capacitor from LOW LINE to GND to ensure proper start-up. For normal operation (V_{CC} above the reset threshold), LOW LINE is pulled to V_{CC}. Use LOW LINE to provide an NMI to the μP when power begins to fall. In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered, and before reset asserts. If the system must also contend with a more rapid V_{CC} fall time—such as when the main battery is disconnected or a high-side switch is opened during operation—use capacitance on the V_{CC} line to provide time to execute the shutdown routine. First, calculate the worst-case time required for the system to perform its shutdown routine. Then use the worst-case shutdown time (t_{SHDN}), worst-case load current (I_{LOAD}), and minimum low-line to reset threshold (V_{LR}) to calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted.

$$C_{HOLD} = \frac{I_{LOAD} \times t_{SHDN}}{V_{LR}}$$

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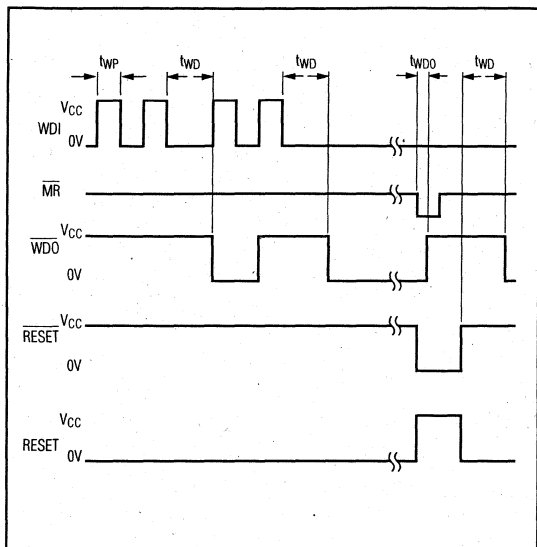


Figure 8. MAX815 Watchdog Timing

where CHOLD is the capacitance (in Farads), ILOAD is the current being drained from the capacitor (in Amperes), and VLR is the low-line to reset threshold difference (in Volts).

Manual Reset

Many μ P-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low, and for t_{RS} (200ms) after $\overline{\text{MR}}$ returns high. This input has an internal pull-up resistor, so it can be left open if not used. $\overline{\text{MR}}$ can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs.

Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual-reset function; external debounce circuitry is not required.

The watchdog circuit can be used to force a reset in the MAX815 by connecting $\overline{\text{WDO}}$ to $\overline{\text{MR}}$. If $\overline{\text{MR}}$ is driven from long cables, or the device is used in a noisy environment, connect a 0.1 μ F capacitor to ground to provide additional noise immunity.

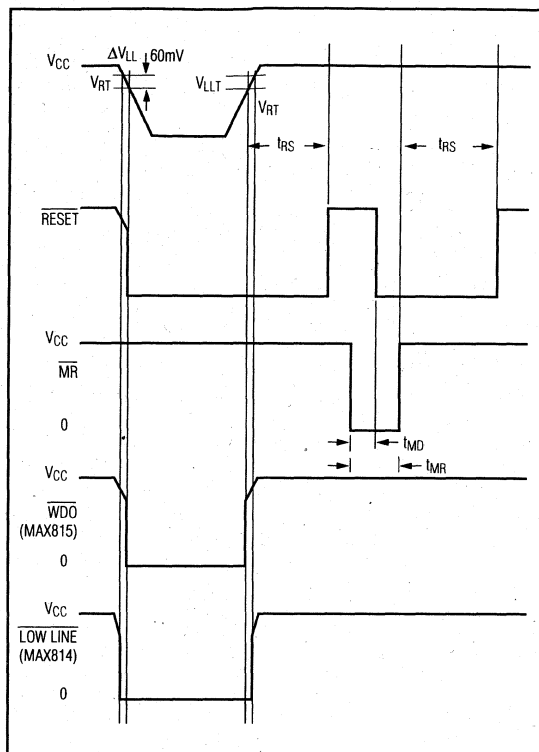


Figure 9. Timing Diagram

Applications Information

Low-Voltage Operation

The $\overline{\text{LOW LINE}}$, $\overline{\text{PFO}}$, and $\overline{\text{WDO}}$ outputs will be locked to logic low when the power supply drops below the lock-out threshold (typically 1V below the reset threshold).

Ensuring a Valid RESET Output Down to $V_{\text{CC}} = 0\text{V}$

When V_{CC} falls below 1V, the $\overline{\text{RESET}}$ output no longer sinks current, but becomes an open circuit. High-impedance CMOS-logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{\text{RESET}}$ pin as shown in Figure 10, any stray charge or leakage currents will be drained to ground, holding $\overline{\text{RESET}}$ low. Resistor value R_1 is not critical. It should be about 100k Ω —large enough not to load $\overline{\text{RESET}}$, and small enough to pull $\overline{\text{RESET}}$ to ground.

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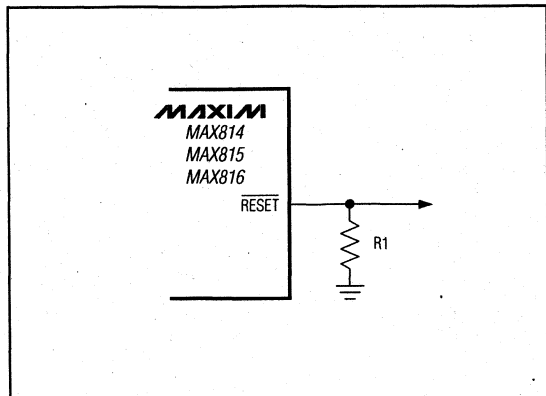


Figure 10. RESET Valid to Ground Circuit

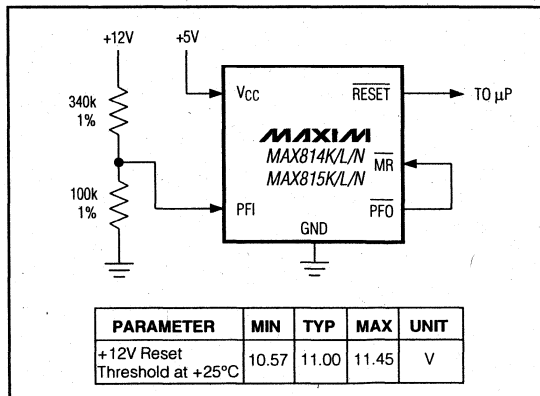


Figure 11. Monitoring Both +5V and +12V

Monitoring Voltages Other than VCC

Monitor voltages other than the VCC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10-times the sum of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be asserted on other voltages in addition to the +5V VCC line. Connect PFO to MR to initiate a reset when PFI drops below 2.50V (K, L, N suffix) or 1.70V (T suffix or MAX816). Figure 11 shows the MAX814K/L/N/ MAX815K/L/N configured to assert RESET when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 12). When the negative rail is good (a negative voltage of large magnitude), PFO is low. When the negative rail is degraded (a negative voltage of lesser magnitude), PFO is high. By adding the resistors and transistor as shown, a high PFO triggers reset. As long as PFO remains high, the MAX814/MAX815/ MAX816 will keep reset asserted (RESET = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the VCC line, and the resistor.

Watchdog Software Considerations

A way to help the watchdog timer keep closer tabs on software execution involves setting and resetting the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 13 shows an example flow diagram where the I/O driving the watchdog input is set low at the beginning of the program, set high at the beginning of every subroutine, then set low at the end of every subroutine. If the program should hang in any subroutine, the I/O is continually set high and the watchdog timer is allowed to time out, causing a reset to be issued.

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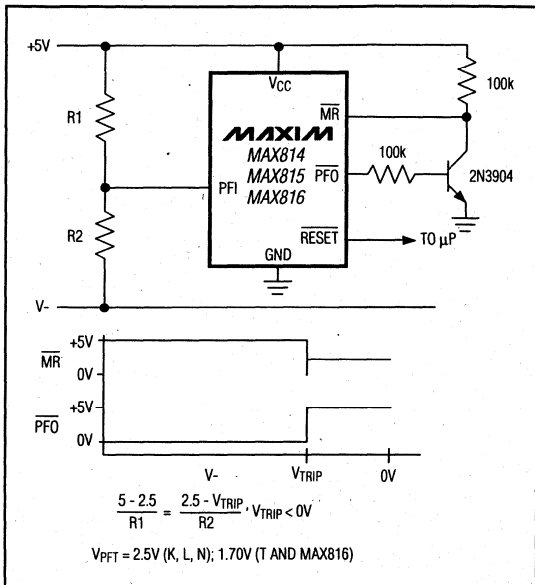


Figure 12. Monitoring a Negative Voltage

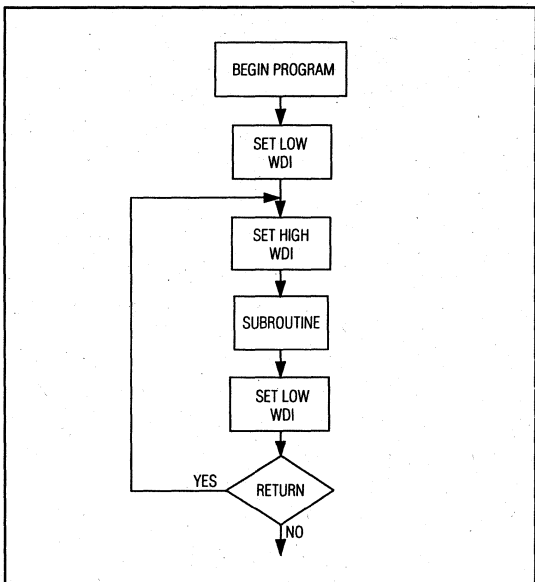


Figure 13. Flow Chart of WDI Implementation

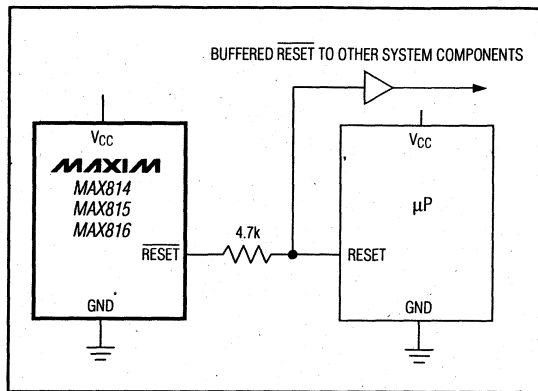


Figure 14. Interfacing to µPs with Bidirectional Reset I/O

Negative-Going Vcc Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the MAX814/MAX815/MAX816 series is relatively immune to short duration negative-going VCC transients (glitches). The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Comparator Overdrive, for which a reset is not generated. The graph was made using a negative-going pulse applied to VCC, starting 1.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going VCC transient may have without causing a reset pulse. As the magnitude of the transient increases (goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC that goes 100mV below the reset threshold and lasts 30µs or less will not cause a reset pulse to be issued.

A 0.1µF bypass capacitor mounted as close as possible to pin 2 (VCC) provides additional transient immunity.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can cause a conflict with the RESET output. If, for example, the RESET output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the RESET output and the µP reset I/O, as in Figure 14. Buffer the RESET output to other system components.

$\pm 1\%$ Accuracy, Low-Power, +3V and +5V μ P Supervisory Circuits

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX814_CPA	0°C to +70°C	8 Plastic DIP
MAX814_CSA	0°C to +70°C	8 SO
MAX814_EPA	-40°C to +85°C	8 Plastic DIP
MAX814_ESA	-40°C to +85°C	8 SO
MAX815_CPA	0°C to +70°C	8 Plastic DIP
MAX815_CSA	0°C to +70°C	8 SO
MAX815_EPA	-40°C to +85°C	8 Plastic DIP
MAX815_ESA	-40°C to +85°C	8 SO
MAX816CPA	0°C to +70°C	8 Plastic DIP
MAX816CSA	0°C to +70°C	8 SO
MAX816EPA	-40°C to +85°C	8 Plastic DIP
MAX816ESA	-40°C to +85°C	8 SO

* The MAX814/MAX815 offer a choice of reset threshold voltage. From the Reset Trip Threshold table, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.

Reset Trip Thresholds

MAX814/MAX815		
SUFFIX	RESET TRIP THRESHOLD	
	MIN (V)	MAX (V)
K	4.75	4.85
L	4.65	4.75
N	4.50	4.60
T	3.00	3.06
MAX816		
—	Adjustable	

MAX814/MAX815/MAX816

5



Voltage References

Voltage References, Product Tables and Trees	6-2
MAX6120 1.2V, Micropower, Precision 3-Terminal Voltage Reference—SOT-23 Package*	6-5

*Advance Information—first page of data sheet in preparation.

PRECISION VOLTAGE REFERENCES

1.2 VOLTS	2.5 VOLTS	4.096 VOLTS	5.0 VOLTS	7.5 VOLTS	10.0 VOLTS	-10.0 VOLTS
† MAX6120 ($I_Q = 70\mu A$, 100ppm/°C)	MAX872 ($I_Q = 10\mu A$, 40ppm/°C)	† MAX676 ($<1\text{ppm}/^\circ\text{C}$, low dropout)	MAX675 (12-20ppm/°C)	MX584 (5-30ppm/°C)	MAX670 (3-10ppm/°C)	MX2701 (3-10ppm/°C)
ICL8069 (10-100ppm/°C)	MAX873 ($I_Q = 280\mu A$, 7-20ppm/°C)	MAX874 ($I_Q = 10\mu A$, 40ppm/°C)	† MAX677 ($<1\text{ppm}/^\circ\text{C}$, lowest long-term drift)		MAX671 (1-10ppm/°C)	
	MX580 (10-85ppm/°C)		MAX875 ($I_Q = 280\mu A$, 7-20ppm/°C)		MAX674 (12-20ppm/°C)	
	MX584 (5-30ppm/°C)		MX584 (5-30ppm/°C)		† MAX678 ($<1\text{ppm}/^\circ\text{C}$, lowest long-term drift)	
			REF02 (8.5-250ppm/°C)		MAX876 ($I_Q = 280\mu A$, 7-20ppm/°C)	
					MX2700 (3-10ppm/°C)	
					MX2710 (1-5ppm/°C)	
					MX581 (5-30ppm/°C)	
					MX584 (5-30ppm/°C)	
					REF01 (8.5-65ppm/°C)	

† Future product

Voltage References

Part Number	Voltage (V)	Temp. Drift (ppm/°C max)	Initial Accuracy T _A = +25°C (%F.S. max)	Quiescent Current (mA max)	Noise 0.1Hz-10Hz (μV-p-p), max(typ)	Package Options ¹	Temp. Ranges ²	Features	Price ³ 1000-up (\$)
MAX6120	1.2	100	2	70μA	(15)	SOT-23, SO	E	Micropower three-terminal reference	††
ICL8069	1.2	10 to 100	2	0.05	5 (10Hz to 10kHz)	TO-52, TO-92, SO*	C.E.M	Micropower two-terminal reference	0.65
MAX872	2.5	40	0.2	10μA	(60)	DIP, SO	C.E	Lowest power, lowest dropout precision reference. V _{CC} = V _{OUT} + 200mV	2.12
MAX873	2.5	7 to 20	0.06 to 0.1	0.28	(16)	DIP, SO	C.E.M	Low power/drift, REF43 upgrade	2.95
MAX880	2.5	10 to 85	0.4 to 3	1.5	(60)	TO-52, SO**	C.M	Low-drift bandgap reference	2.33
MX584	2.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, Cerdip	C.M	Low-drift programmable reference	3.09
MAX676	4.096	1 to 2	0.02	10	(1.5)	DIP/SO	C.E.M	Lowest temperature drift in SO package, lowest long-term drift, low dropout	††
MAX874	4.096	40	0.2	10μA	(60)	DIP, SO	C.E	Lowest power, lowest dropout precision reference. V _{CC} = V _{OUT} + 200mV	2.12
MAX675	5.0	12 to 20	0.15	1.4	15	TO-99, DIP, SO, Cerdip	C.E.M	Low-drift, low-noise bandgap reference	3.08
MAX677	5.0	1 to 2	0.02	10	(2)	DIP/SO	C.E.M	Lowest temperature drift in SO package, lowest long-term drift	††
MAX875	5.0	7 to 20	0.06 to 0.1	0.28	(32)	DIP, SO	C.E.M	Low power/drift, REF02 upgrade	2.95
MX584	5.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, Cerdip	C.M	Low-drift programmable reference	3.09
REF02	5.0	8.5 to 250	0.3 to 2	1.4	15	TO-99, DIP, SO, Cerdip	C.M	Low-drift bandgap reference	1.80
MX584	7.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, Cerdip	C.M	Low-drift programmable reference	3.09
MAX670	10.0	3 to 10	0.025	14	50	SB Ceramic	E.M	Kelvin connected, ultra low-drift reference	38.51
MAX671	10.0	1 to 10	0.01	14	50	SB Ceramic	C.E.M	Kelvin connected, ultra low-drift reference	37.41
MAX674	10.0	12 to 20	0.15	1.4	30	TO-99, DIP, SO, Cerdip	C.E.M	Low-drift, low-noise bandgap reference	3.08
MAX678	10.0	1 to 2	0.02	10	(3)	DIP/SO	C.E.M	Lowest temperature drift in SO package, lowest long-term drift	††
MAX876	10.0	7 to 20	0.06 to 0.1	0.28	(64)	DIP, SO	C.E.M	Low power/drift, REF01 upgrade	2.95
MX2700	10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I.M	Ultra low-drift voltage reference	19.61
MX2710	10.0	1 to 5	0.01	14	(30)	SB Ceramic	C	Ultra low-drift voltage reference	24.74
MX381	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-39, SO***	C.M	Low-drift bandgap reference	2.90
MX584	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, Cerdip	C.M	Low-drift programmable reference	3.09
REF01	10.0	8.5 to 65	0.3 to 1	1.4	30	TO-99, DIP, SO, Cerdip	C.M	Low-drift bandgap reference	2.05
MX2701	-10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I.M	Ultra low-drift voltage reference	24.02

* The ICL8069 is available in 2-pin TO-52, 2-pin TO-92, and 8-pin SO packages.

** The MX380 is available in 3-pin TO-52 and 8-pin SO packages.

*** The MX381 is available in 3-pin TO-39 and 8-pin SO packages.

1 Package Options: DIP = Dual-In-Line Package, PLCC = Plastic Leadless Chip Carrier (quad pack), FP = Flat Pack

2 Temp Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/95



Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference

General Description

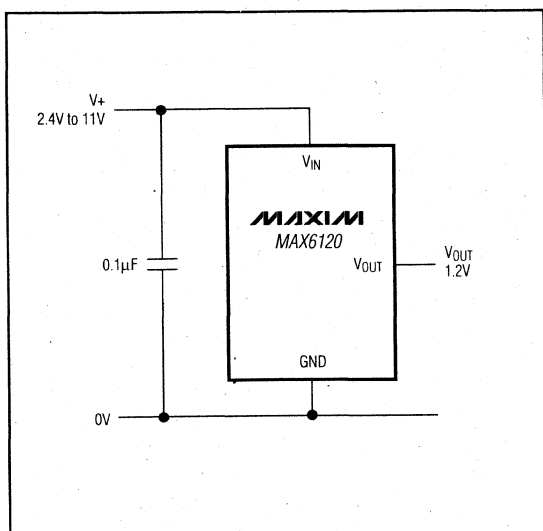
The MAX6120 is the lowest-power 1.2V, precision 3-terminal voltage reference offered in a SOT-23 package. Ideal for 3V battery-powered equipment where power conservation is critical, the MAX6120 is a low-power alternative to existing two-terminal shunt references. Unlike two-terminal references that throw away battery current and require an external series resistor, the MAX6120's 70 μ A maximum supply current (typically only 50 μ A) is independent of the input voltage, which translates to maximum efficiency at all battery voltages.

The MAX6120 operates from a supply voltage as low as 2.4V, and output voltage accuracy over temperature is $\pm 2\%$ for the SOT-23 package. Output voltage*temperature coefficient is typically only 50ppm/ $^{\circ}$ C.

Applications

Battery-Powered Systems
Portable and Hand-Held Equipment
Data Acquisition Systems
Instrumentation and Process Control

Typical Operating Circuit



Features

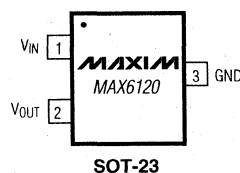
- ◆ 3-Pin SOT-23 Package
- ◆ Supply Current Independent of Input Voltage Over Temperature
- ◆ 70 μ A Max Supply Current
- ◆ 2.4V to 11V Input Voltage Range
- ◆ 50ppm/ $^{\circ}$ C Typical Tempco

Ordering Information

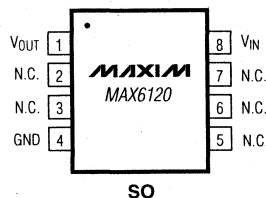
PART	TEMP. RANGE	PIN-PACKAGE
MAX6120ESA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 SO
MAX6120EUR	-40 $^{\circ}$ C to +85 $^{\circ}$ C	3 SOT-23

Pin Configurations

TOP VIEW



SOT-23



SO

MAX6120

6

MAXIM

Maxim Integrated Products 6-5

Call toll free 1-800-998-8800 for free samples or literature.



A/D Converters

A/D Converters, Product Tables and Trees	7-2
MAX100 250Msps, 8-Bit ADC w/ Track/Hold.....	7-9
MAX101 500Msps, 8-Bit ADC w/ Track/Hold.....	7-25
MAX104 1Gsps, 8-Bit ADC w/ Track/Hold*	7-41
MAX110 $\pm 5V$, Low-Cost, 2-Channel, Serial ± 14 -Bit ADC	7-43
MAX111 5V, Low-Cost, 2-Channel, Serial ± 14 -Bit ADC	7-43
MAX146 2.7V, Low-Power, 8-Channel, Serial 12-Bit DAS*	7-65
MAX149 2.7V, Low-Power, 8-Channel, Serial 10-Bit DAS*	7-67
MAX194 85ksps, 14-Bit Serial ADC w/ 10 μA Shutdown	7-69
MAX195 85ksps, 16-Bit Serial ADC w/ 10 μA Shutdown	7-93
MAX196 8-Channel, Multi-Range, 5V, 12-Bit DAS w/ 12-Bit Bus Interface and Fault Protection*	7-119
MAX197 8-Channel, Multi-Range, 5V, 12-Bit DAS w/ 8+4 Bus Interface and Fault Protection	7-121
MAX198 8-Channel, Multi-Range, 5V, 12-Bit DAS w/ 12-Bit Bus Interface and Fault Protection*	7-119
MAX199 8-Channel, Multi-Range, 5V, 12-Bit DAS w/ 8+4 Bus Interface and Fault Protection	7-137

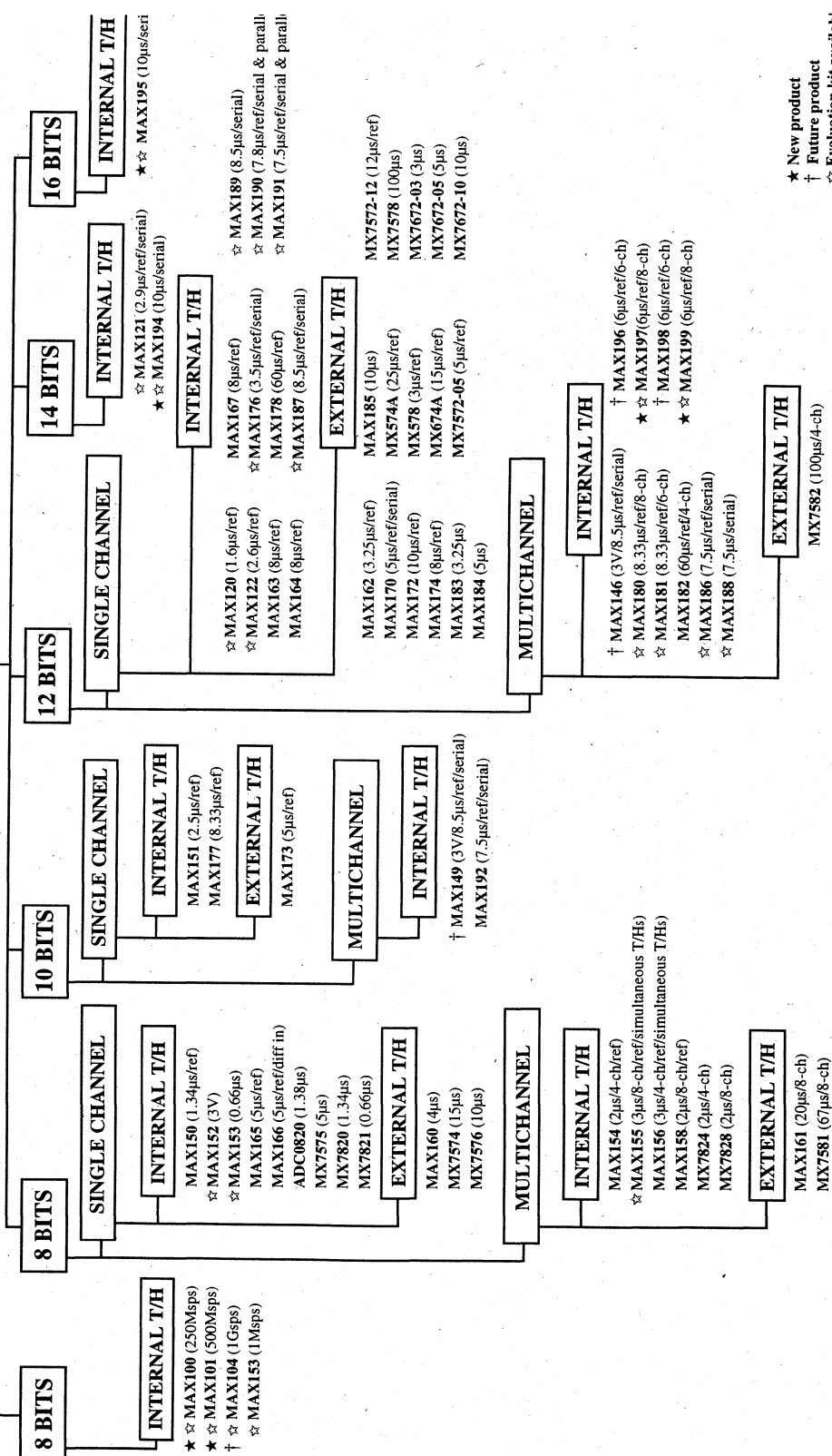
*Advance Information—first page of data sheet in preparation.

A/D CONVERTERS

ULTRA-HIGH-SPEED CONVERSION (<1μs)

FAST CONVERSION (<100μs) (SAR/Flash ADCs)

SLOW CONVERSION (>10ms)



★ New product
† Future product
★ Evaluation kit available

A/D CONVERTERS

see previous page for
FAST CONVERSION (< 100µs)
and ULTRA-HIGH-SPEED
CONVERSION (<1µs)

SLOW CONVERSION
(>10ms)
(Integrating & Σ - Δ ADCs)

LCD DISPLAY

MAX130 (3 1/2 D, B/G)
 MAX131 (3 1/2 D, B/G, L)
 MAX136 (3 1/2 D, B/G, HOLD, L)
 MAX138 (3 1/2 D, B/G, S/S)
 ICL7106 (3 1/2 D, Z)
 ICL7116 (3 1/2 D, Z, HOLD)
 ICL7126 (3 1/2 D, Z, L)
 ICL7129A (4 1/2 D)
 ICL7136 (3 1/2 D, Z, L)

LED DISPLAY

MAX139 (3 1/2 D, B/G, S/S)
 MAX140 (3 1/2 D, B/G, S/S)
 ICL7107 (3 1/2 D, Z)
 ICL7117 (3 1/2 D, Z, HOLD)
 ICL7137 (3 1/2 D, Z, L)

µP INTERFACE

☆ MAX132 (±18 bit, serial, L)
 ☆ MAX133 (±40,000 count, L)
 ☆ MAX134 (±40,000 count, L)
 ☆ MAX135 (±15 bit, L)
 ICL7109 (12 bit, Z)
 ICL7135 (±20,000 count)

Σ - Δ ADCs

★ ☆ MAX110 (±14 bit, serial,
 no ext. components, L)
 ★ ☆ MAX111 (±14 bit, serial,
 no ext. components, L)

★ New product
 ☆ Evaluation kit available

NOTES: HOLD – Includes display-hold input
 S/S – Includes +5V single supply
 B/G – Includes bandgap reference
 Z – Includes zener reference
 L – Low power

Sampling A/D Converters

Part Number	Resolution (Bits)	Sample Rate (kHz max)	Conversion Time (µs max)	Input Channels	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price* 1000-up (\$)
MAX153	8	1000	0.66	1	E	µP/8	+5 or ±5	+5 or ±2.5	Yes	High-speed ADC with 1µA power-down	6.63
MX7821	8	500	0.66	1	E	µP/8	+5 or ±5	+5 or ±2.5		Complete ADC with T/H	7.54
MAX150	8	500	1.34	1	E or I/±2.5	µP/8	+5	+5		Complete ADC with T/H and ref	5.85
MX7820	8	500	1.34	1	E	µP/8	+5	+5		Plug-in replacement for AD7820	7.93
ADC0820	8	400	1.38	1	E	µP/8	+5	+5		Complete ADC with T/H	7.16
MAX152	8	400	1.8	1	E	µP/8	+5	+3 or ±1.5	Yes	3V ADC with 1µA power-down	4.25
MAX154	8	400	2	4	E or I/±2.5	µP/8	+5	+5		4-Ch ADC with T/H and ref	6.45
MAX158	8	400	2	8	E or I/±2.5	µP/8	+5	+5		8-Ch ADC with T/H and ref	6.85
MX7824	8	400	2	4	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MX7828	8	400	2	8	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	250	3.6	4	E or I/±2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-Ch ADC with simul. T/Hs and ref	9.50
MAX156	8	250	3.6	4	E or I/±2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-Ch ADC with simul. T/Hs and ref	7.19
MAX165	8	200	5	1	E or I/±1.23	µP/8	+5	+5		Low-cost sampling ADC with ref	3.95
MAX166	8	200	5	1	E or I/±1.23	µP/8	+5	+5		Differential-input complete ADC	4.20
MX7575	8	200	5	1	E	µP/8	+5	+5		Plug-in replacement for AD7575	3.74
MAX151	10	300	2.5	1	E or I/±4.0	µP/10	+5	+5		Sampling ADC with ref	7.95
MAX192	10	133	7.5	8	I/±4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX149	10	133	8.5	8	I/±2.5	Serial	+5	+2.5, ±1.25		3V, 8-channel, serial DAS	††
MAX177	10 or 12	100	8.33	1	I/±5.25	µP/8 or 12	+5 & -12 to -15	±2.5		MAX167 with 10-bit accuracy	7.96
MAX120	12	500	1.6	1	I/±5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	16.00
MAX122	12	333	2.6	1	I/±5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	12.00
MAX176	12	250	3.5	1	I/±5.0	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	13.20
MAX186	12	133	7.5	8	E or I/±4.096	Serial	+5	+5	Yes	7mW, 10µA power-down	8.95
MAX188	12	133	7.5	8	E	Serial	+5	+5	Yes	MAX186 without reference	8.45
MAX146	12	133	8.5	6	I/±2.5	Serial	+3	+2.5, ±1.25		3V, 8-channel, serial DAS	††
MAX196	12	100	6	8	E or I/±4.096	µP/12	+5	+10, +10, ±5, +5		Multi-range, fault protected, 6-channel	††
MAX197	12	100	6	8	E or I/±4.096	µP/8	+5	+10, +10, ±5, +5	Yes	Multi-range, fault protected, 8-channel	9.90
MAX198	12	100	6	6	E or I/±4.096	µP/12	+5	±4, +4, ±2, +2		Multi-range, fault protected, 6-channel	††
MAX199	12	100	6	8	E or I/±4.096	µP/8	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected, 8-channel	9.90
MAX191	12	100	7.5	1	E or I/±4.096	Serial and µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX163	12	100	8.33	1	I/±5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling ADC with ref	14.40
MAX164	12	100	8.33	1	I/±5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling ADC with ref	14.40
MAX167	12	100	8.33	1	I/±5.0	µP/8 or 12	+5 & -12 to -15	±2.5	Yes	Complete sampling ADC with ref	14.40
MAX180	12	100	8.33	6	E or I/±5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX181	12	100	8.33	6	E or I/±5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX190	12	75	7.8	1	E or I/±4.096	Serial and µP/8	+5	+5	Yes	Use MAX191 for new designs	10.00
MAX187	12	75	8.5	1	E or I/±4.096	Serial	+5	+5	Yes	7mW, 8-pin package	7.45
MAX189	12	75	8.5	1	E	Serial	+5	+5	Yes	MAX187 without reference	6.95
MAX178	12	20	60	1	E or I/±5.0	µP/8 or 12	+5 & +15	+5	Yes	ILSB TUE, has T/H and ref	15.24
MAX182	12	20	60	4	E or I/±5.0	µP/8 or 12	+5 & +15	+5		ILSB TUE, has T/H and ref	17.55
MAX121	14	308	2.9	1	I/±5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC	12.00
MAX194	14	85	9.4	1	E	Serial	±5	+5 or ±5	Yes	with DSP interface, 16-pin pkg.	14.00
MAX195	16	85	10	1	E	Serial	±5	+5 or ±5	Yes	14-bit, high-speed serial ADC	24.00

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Low-Power A/D Converters

Part Number	Resolution (Bits)	Input Channels	Data-Bus Interface (Bits)	Supply Voltage (V)	Supply Current (mA)	Power-Down Current (μ A)	Conversion Time (μ s max)	Reference Voltage* (V)	EV Kit	Features	Price† 1000-up (\$)
MAX152	8	1	μ P/8	+3 or ± 3	1.5	1	1.8	E	Yes	3V ADC with 1 μ A power-down	4.25
MAX153	8	1	μ P/8	+5 or ± 5	8	1	0.66	E	Yes	High-speed ADC with 1 μ A power-down	6.63
MAX192	10	8	Serial	+5	1.5	2	7.5	I/+4.096	Yes	Low power, low cost, small package	2.95**
MAX186	12	8	Serial	+5 or ± 5	1.5	2	7.5	I/+4.096	Yes	7mW, 10 μ A power-down	8.95
MAX187	12	1	Serial	+5	1.5	2	8.5	I/+4.096	Yes	7mW, 8-pin package	7.45
MAX188	12	8	Serial	+5 or ± 5	1	2	7.5	E	Yes	MAX186 without reference	8.45
MAX189	12	1	Serial	+5	1	2	8.5	E	Yes	MAX187 without reference	6.95
MAX191	12	1	Serial and μ P/8	+5 or ± 5	2.5	20	7.5	E or I/+4.096	Yes	15mW, 20 μ A power-down	9.60
MAX194	14	1	Serial	± 5	5.5	10	9.4	E	Yes	14-bit, high-speed serial ADC	14.00
MAX110	14 + sign	2	Serial	± 5	550 μ A	1	20ms	E	Yes	Low-power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	Serial	+5	640 μ A	1	20ms	E	Yes	Low-power, shutdown mode, single supply	4.80
MAX135	15 + sign	1	μ P/8	± 5	60 μ A	1	10ms	E	Yes	High-resolution ADC, <1mW	8.00
MAX195	16	1	Serial	± 5	5.5	10	10	E	Yes	High-speed serial 16-pin ADC	24.00
MAX132	18 + sign	1	Serial	± 5	60 μ A	1	10ms	E	Yes	Serial high-resolution ADC, <1mW	8.00

Multi-Channel A/D Converters

Part Number	Resolution (Bits)	Input Channels	Conversion Time (μ s max)	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up (\$)
MAX154	8	4	2	400	E or I/+2.5	μ P/8	+5	+5		4-Ch ADC with T/H and ref	6.45
MAX1824	8	4	2	400	E	μ P/8	+5	+5		Plug-in replacement for AD7824	8.33
MAX156	8	4	3.6	250	E or I/+2.5	μ P/8	+5 or ± 5	+2.5 or ± 2.5		4-Ch ADC with simult. T/Hs and ref	7.19
MAX158	8	8	2	400	E or I/+2.5	μ P/8	+5	+5		8-Ch ADC with T/H and ref	6.85
MAX1828	8	8	2	400	E	μ P/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	8	3.6	250	E or I/+2.5	μ P/8	+5 or ± 5	+2.5 or ± 2.5	Yes	8-Ch ADC with simult. T/Hs and ref	9.50
MAX161	8	8	20	—	E	μ P/8	+5	+10		8-Ch ADC with RAM buffer	11.12
MAX1581	8	8	66.6	—	E	μ P/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX149	10	8	8.5	133	I/+2.5	Serial	+3	+2.5, ± 1.25		3V, 8-channel DAS	††
MAX192	10	8	133	7.5	I/+4.096	Serial	+5	+5 or ± 2.5		Low power, low cost, small package	2.95**
MAX182	12	4	60	20	E or I/+5.0	μ P/8 or 12	± 5 & +15	+5		ILSB TUE, has T/H and ref	17.55
MAX1582	12	4	100	—	E	μ P/8 or 12	± 5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX196	12	6	6	100	E or I/+4.096	μ P/12	+5	± 10 , +10, ± 5 , +5		Multi-range, fault protected	††
MAX198	12	6	6	100	E or I/+4.096	μ P/12	+5	± 4 , +4, ± 2 , +2		Multi-range, fault protected	††
MAX181	12	6	8.33	100	E or I/-5.0	μ P/8 or 12	+5 & -12 to -15	+5 or ± 2.5	Yes	Data-acquisition system	12.75
MAX197	12	8	6	100	E or I/+4.096	μ P/8	+5	+5 or ± 2.5	Yes	Multi-range, fault protected	9.90
MAX199	12	8	6	100	E or I/+4.096	μ P/8	+5	± 4 , +4, ± 2 , +2	Yes	Multi-range, fault protected	9.90
MAX186	12	8	7.5	133	E or I/+4.096	Serial	+5 or ± 5	+5 or ± 2.5	Yes	7mW, 10 μ A power-down	8.95
MAX188	12	8	7.5	133	E or I/+4.096	Serial	+5 or ± 5	+5 or ± 2.5	Yes	MAX186 without reference	8.45
MAX180	12	8	8.33	100	E or I/-5.0	μ P/8 or 12	+5 & -12 to -15	+5 or ± 2.5	Yes	Data-acquisition system	12.75
MAX146	12	8	8.5	133	I/+2.5	Serial	+3	+2.5 (± 1.25)	Yes	3V, 8-channel DAS	††
MAX187	12	75	1	8.5	E or I/+4.096	Serial	+5	+5	Yes	7mW, 8-pin package	7.45
MAX189	12	75	1	8.5	E	Serial	+5	+5	Yes	MAX187 without reference	6.95
MAX110	14 + sign	2	20ms	—	E	Serial	± 5	± 3	Yes	Low power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	20ms	—	E	Serial	+5	± 2	Yes	Low power, shutdown mode, single supply	4.80

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Serial A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up (\$)
MAX192	10	7.5	8	133	I/+4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX149	10	8.5	8	133	I/+2.5	Serial	+3	+2.5 ±1.25		3V, 8-channel DAS	++
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	13.20
MAX170	12	5	1	—	I/-5.25	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	11.96
MAX186	12	7.5	8	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	8.95
MAX188	12	7.5	8	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	8.45
MAX191	12	7.5	1	100	E or I/+4.096	Serial and µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX190	12	7.8	1	75	E or I/+4.096	Serial and µP/8	+5	+5	Yes	Use MAX191 for new designs	10.00
MAX146	12	8.5	8	133	I/+2.5	Serial	+3	+2.5 ±1.25	Yes	3V, 8-channel DAS	++
MAX187	12	8.5	1	75	E or I/+4.096	Serial	+5	+5	Yes	7mW, 8-pin package	7.45
MAX189	12	8.5	1	75	E	Serial	+5	+5	Yes	MAX187 without reference	6.95
MAX121	14	2.9	1	308	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC with DSP interface	12.00
MAX194	14	9.4	1	85	E	Serial	+5	+5 or ±5	Yes	14-bit, high-speed serial ADC	14.00
MAX110	14 + sign	20ms	2	—	E	Serial	+5	±3	Yes	Low-power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	20ms	2	—	E	Serial	+5	±2	Yes	Low-power, shutdown mode, single supply	4.80
MAX195	16	10	1	85	E	Serial	+5	+5 or ±5	Yes	High-speed, serial, 16-pin ADC, 50mW	24.00
MAX132	18 + sign	10ms	1	—	E	Serial	+5	+0.5	Yes	Serial high-resolution ADC, <1mW	8.00

Integrating and Sigma-Delta A/D Converters

Part Number	Resolution (digits)	Resolution (counts)	Output Type	Supply Voltage (V)	Supply Current (mA), max(typ)	References	EV Kit	Features	Price† 1000-up (\$)
INTEGRATING ADCs									
MAX130	3 1/2	±2000	LCD	+4.5 to +14	0.25(0.1)	Bandgap		Replacement for ICL7106	4.86
MAX131	3 1/2	±2000	LCD	+4.5 to +14	0.1(0.06)	Bandgap		Replacement for ICL7136	4.86
MAX136	3 1/2	±2000	LCD	+9	0.15(0.06)	Bandgap		Hold function, low power	4.32
MAX138	3 1/2	±2000	LCD	+2.25 to +7	0.8(0.2)	Bandgap		± inputs with single supply	4.40
ICL7106	3 1/2	±2000	LCD	+9	1.8(0.6)	Zener		For digital multimeters	4.32
ICL7116	3 1/2	±2000	LCD	+9	1.8(0.8)	Zener		ICL7106 with display hold	4.32
ICL7126	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Use ICL7136 for new designs	4.32
ICL7136	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Low power/noise ICL7106	4.32
MAX139	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		± inputs with single supply	4.40
MAX140	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		Low segment current (2mA)	4.40
ICL7107	3 1/2	±2000	LED	+9	1.8(0.6)	Zener		For digital panel meters	4.32
ICL7117	3 1/2	±2000	LED	+5	1.8(0.8)	Zener		ICL7107 with display hold	4.32
ICL7137	3 1/2	±2000	LED	+5	0.2(0.06)	Zener		Low power when LEDs off	4.32
MAX133	3 3/4	±40,000	µP	+9	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
MAX134	3 3/4	±40,000	µP	+5	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
ICL7109	12 bits + sign	±4096	8-1/16-bit µP/UART	+5	1.5(0.7)	Zener		3-state binary outputs	5.10
ICL7129A	4 1/2	±20,000	Triplexed LCD	+9	1.4(1)	External		Lowest noise ±3µV	7.96
ICL7135	4 1/2	±20,000	Multiplexed BCD	+5	2(1)	External		For DMM, DPM, data loggers	5.48
MAX135	15 bits + sign	±20,000	µP/8	+5	0.125(0.06)	External		Three-state twos-complement outputs	8.00
MAX132	18 bits + sign	±260,000	Serial µP	+5	0.125(0.06)	External	Yes	Serial high-resolution ADC, <1mW	8.00
SIGMA-DELTA ADCs									
MAX110	14 bits + sign	—	Serial	+5	0.95(0.55)	External	Yes	No external components, low power, dual supplies	4.80
MAX111	14 bits + sign	—	Serial	+5	1.2(0.64)	External	Yes	No external components, low power, single supply	4.80

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

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Ultra-High-Speed A/D Converters

Part Number	Resolution (Bits)	Sample Rate (MSPS max)	Input Channels	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up (\$)
MAX153	8	1	1	E	Parallel	+5 or ±5	+5 or ±2.5	Yes	1μA shutdown, SSOP package	6.63
MAX100	8	250	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P	‡
MAX101	8	500	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P	‡
MAX104	8	1000	1	E	Parallel	±5	300mV	Yes	7.3 EIOB at 500, demuxed outputs	††

General-Purpose A/D Converters¹

Part Number	Resolution (Bits)	Conversion Time (μs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up (\$)
MX7821	8	0.66	1	500	E	μP/8	+5 or ±5	+5 or ±2.5		Complete ADC with T/H	7.54
MX7820	8	1.34	1	500	E	μP/8	+5	+5		Plug-in replacement for AD7820	7.93
ADC0820	8	1.38	1	400	E	μP/8	+5	+5		Complete ADC with T/H	7.16
MX7824	8	2	4	400	E	μP/8	+5	+5		Plug-in replacement for AD7824	8.33
MX7828	8	2	8	400	E	μP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX160	8	4	1	-	E	μP/8	+5	+10 or ±5		Ratiometric single-supply ADC	7.20
MX7575	8	5	1	200	E	μP/8	+5	+5		Plug-in replacement for AD7575	3.74
MX7576	8	10	1	-	E	μP/8	+5	+5		Plug-in replacement for AD7576	3.52
MX7574	8	15	1	-	E	μP/8	+5	+10 or ±5		Plug-in replacement for AD7574	4.80
MX7581	8	66.6	8	-	E	μP/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX173	10 or 12	5	1	-	I/-5.25	μP/8 or 12	+5 & -12 to -15	+5		MAX172 with 10-bit accuracy	5.26
MX578	12	3	1	-	E or I/+10.0	Logic	+5 & ±15	±10		Parallel/serial outputs	88.71
MAX162	12	3.25	1	-	I/-5.25	μP/8 or 12	+5 & -12 to -15	+5		High-speed ADC with internal ref	19.20
MAX183	12	3.25	1	-	E	μP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed ADC	9.00
MX7672-03	12	3.25	1	-	E	μP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-03	57.38
MAX184	12	5	1	-	E	μP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed ADC with external ref	8.25
MX7572-05	12	5	1	-	I/-5.25	μP/8 or 12	+5 & -15	+5		Plug-in replacement for AD7572-05	20.00
MX7672-05	12	5	1	-	E	μP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-05	33.66
MAX174	12	8	1	-	E or I/+10.0	μP/8 or 12	+5 & -12 to ±15	±5, ±10, +10 or +20		Upgrades AD574A/AD674A	28.13
MAX185	12	10	1	-	I/-5.25	μP/8 or 12	+5 & -12 to -15	+5		Plug-in upgrade for AD7572-12	9.60
MX7672-10	12	10.4	1	-	E	μP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed ADC with external ref	7.20
MX7572-12	12	10.4	1	-	E	μP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7572-12	14.00
MX674A	12	15	1	-	I/-5.25	μP/8 or 12	+5 & -15	+5, ±10, +10 or +20		Plug-in replacement for AD674A	23.44
MX574A	12	25	1	-	E or I/+10.0	μP/8 or 12	+5 & -12 to ±15	+5, ±10, +10 or +20		Plug-in replacement for AD574A	11.97
MAX178	12	60	1	20	E or I/+5.0	μP/8 or 12	+5 & ±15	+5		ILSB TUE, has T/H and ref	15.24
MX7578	12	100	1	-	E	μP/8 or 12	+5 & ±15	+5		Plug-in replacement for AD7578	16.96
MX7582	12	100	4	-	E	μP/8 or 12	+5 & ±15	+5		Plug-in replacement for AD7582	19.50

1 Not recommended for new designs.

* E = external reference, I = internal reference

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‡ Contact factory for pricing

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

EVALUATION KIT
AVAILABLE**MAXIM****250Mps, 8-Bit ADC with Track/Hold****MAX100****General Description**

The MAX100 ECL-compatible, 250Mps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 125MHz (Nyquist frequency). Designed with Maxim's proprietary advanced bipolar processes, the MAX100 contains a high-performance track/hold (T/H) amplifier and a quantizer in a single ceramic strip-line package.

The innovative design of the internal T/H assures an exceptionally wide input bandwidth of 1.2GHz and aperture delay uncertainty of less than 2ps, resulting in a high 6.8 effective bits performance. Special comparator output design and decoding circuitry reduce out-of-sequence code errors. The probability of erroneous codes occurring due to metastable states is reduced to less than 1 error per 10^{15} clock cycles. Unlike other ADCs, which can have errors that result in false full-scale or zero-scale outputs, the MAX100 keeps the magnitude to less than 1LSB.

The analog input is designed for either differential or single-ended use with a $\pm 270\text{mV}$ range. Sense pins for the reference input allow full-scale calibration of the input range or facilitate ratiometric use. Midpoint tap for the reference string is available for applications that need to modify the output coding for a user-defined bilinear response. Use of separate high-current and low-current ground pins provides better noise immunity and highest device accuracy.

Dual output data paths provide several data output modes for easy interfacing. These modes can be configured as either one or two identical latched ECL outputs. An 8:16 demultiplexer mode that reduces the output data rates to one-half the clock rate is also available.

For applications that require faster data rates, refer to Maxim's MAX101, which allows conversion rates up to 500Mps.

Features

- ♦ 250Mps Conversion Rate
- ♦ 6.8 Effective Bits at 125MHz
- ♦ Less than $\pm 1/2\text{LSB}$ INL
- ♦ 50Ω Differential or Single-Ended Inputs
- ♦ $\pm 270\text{mV}$ Input Signal Range
- ♦ Reference Sense Inputs
- ♦ Ratiometric Reference Inputs
- ♦ Configurable Dual-Output Data Paths
- ♦ Latched, ECL-Compatible Outputs
- ♦ Low Error Rate, Less than 10^{-15} Metastable States
- ♦ Selectable On-Chip 8:16 Demultiplexer
- ♦ 84-Pin Ceramic Flat Pack

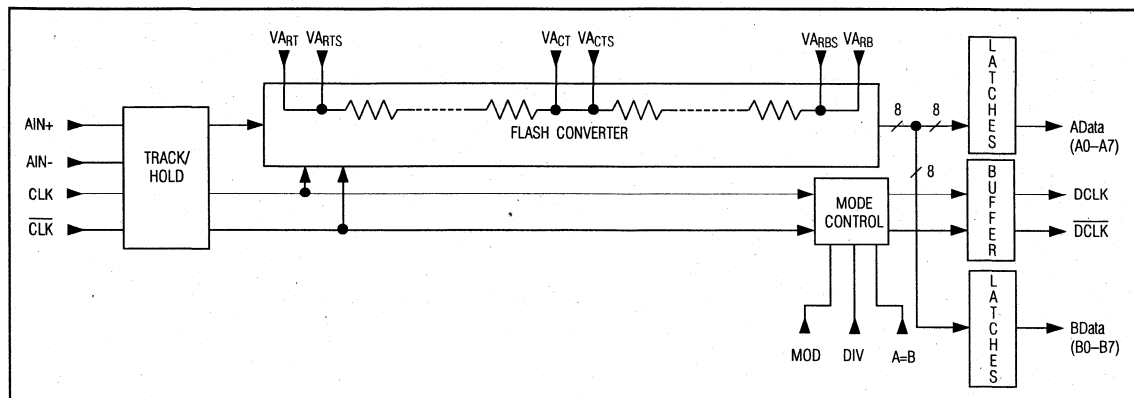
Applications

High-Speed Digital Instrumentation
High-Speed Signal Processing
Medical Systems
Radar/Sonar
High-Energy Physics
Communications

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX100CFR*	0°C to +70°C	84 Ceramic Flat Pack (with heatsink)

*Contact factory for 84-Pin Ceramic Flat Pack without heatsink.

7**Functional Diagram****MAXIM**

Maxim Integrated Products 7-9

Call toll free 1-800-998-8800 for free literature.

250Msps, 8-Bit ADC with Track/Hold

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages		Reference Voltage (V _{ARB})	-1.5V to +0.3V
V _{CC}	0V to +7V	Data Output Current	-33mA
V _{EE}	-7V to 0V	DCLK Output Current	-43mA
V _{CC} - V _{EE}	+12V	Operating Temperature Range	0°C to +70°C
Analog Input Voltage	±2V	Operating Junction Temperature (Note 2)	0°C to +125°C
Digital Input Voltage	-2.3V to +0V	Storage Temperature Range	-65°C to +150°C
Reference Voltage (V _{ART})	-0.3V to +1.5V	Lead Temperature (soldering, 10sec)	+250°C

Note 1: The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high-energy electrostatic fields. Keep unused units in conductive foam or shunt the terminals together. Discharge the conductive foam to the destination socket before insertion.

Note 2: Typical thermal resistance, junction-to-case R_{θJC} = 5°C/W and thermal resistance, junction to ambient (MAX100CA) R_{θJA} = 12°C/W, providing 200 lineal ft/min airflow with heatsink. See *Package Information*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 50Ω to -2V, V_{ART} = 1.02V, V_{ARB} = -1.02V, T_{MIN} to T_{MAX} = 0°C to +70°C, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				8			Bits
Integral Nonlinearity (Note 4)	INL	AData, BData	T _A = +25°C			±0.5	LSB
			T _A = T _{MIN} to T _{MAX}			±0.6	
Differential Nonlinearity	DNL	AData, BData, no missing codes	T _A = +25°C			±0.75	LSB
			T _A = T _{MIN} to T _{MAX}			±0.85	
DYNAMIC SPECIFICATIONS							
Effective Bits	ENOB	f _{CLK} = 250MHz, V _{IN} = 95% full scale (Note 5)	f _{AIN} = 10MHz	7.4			Bits
			f _{AIN} = 50MHz	7.1			
			f _{AIN} = 125MHz	6.8			
Signal-to-Noise Ratio	SNR	f _{AIN} = 50MHz, f _{CLK} = 250MHz, V _{IN} = 95% full scale (Note 6)		44.5			dB
Maximum Conversion Rate	f _{CLK}	(Note 7)		250			Msp/s
Analog Input Bandwidth	BW _{3dB}			1.2			GHz
Aperture Width	t _{AW}	Figure 5		270			ps
Aperture Jitter	t _{AJ}	Figure 5		2			ps
ANALOG INPUT							
Input Voltage Range	V _{IN}	AIN+ to AIN-, Table 2, T _A = T _{MIN} to T _{MAX}	Full scale	230	315		mV
			Zero scale	-305	-215		
Input Offset Voltage	V _{IO}	AIN+, AIN-, T _A = T _{MIN} to T _{MAX}		-17	+32		mV
Least-Significant-Bit Size	LSB	T _A = T _{MIN} to T _{MAX}		1.8	2.5		mV
Input Resistance	R _I	AIN+ and AIN- with respect to GND		49	51		Ω
Input Resistance Temperature Coefficient				0.008			Ω/°C

250Msps, 8-Bit ADC with Track/Hold

MAX100

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 50Ω to -2V, V_{ART} = 1.02V, V_{ARB} = -1.02V, T_{MIN} to T_{MAX} = 0°C to +70°C, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT							
Reference String Resistance	RREF	VART to VARB		116		175	Ω
Reference String Resistance Temperature Coefficient					0.02		Ω/°C
LOGIC INPUTS							
Digital Input Low Voltage (Note 8)	VIL	DIV, MOD, A=B, CLK, $\overline{\text{CLK}}$, TA = TMIN to TMAX				-1.5	V
Digital Input High Voltage (Note 8)	VIH	DIV, MOD, A=B, CLK, $\overline{\text{CLK}}$, TA = TMIN to TMAX		-1.07			V
Digital Input Low Current	IIL	DIV, MOD, A=B = -1.8V, TA = TMIN to TMAX		-5		20	μA
		CLK, $\overline{\text{CLK}}$, VIL = -1.8V (no termination), TA = TMIN to TMAX		0		80	
Digital Input High Current	IIH	DIV, MOD, A=B = -0.8V, TA = TMIN to TMAX		-5		20	μA
		CLK, $\overline{\text{CLK}}$, VIH = -0.8V (no termination), TA = TMIN to TMAX		0		80	
LOGIC OUTPUTS (Note 9)							
Digital Output Low Voltage	VOL	AData, BData, DCLK, $\overline{\text{DCLK}}$	TA = +25°C	-1.95		-1.60	V
			TA = TMIN to TMAX	-1.95		-1.50	
Digital Output High Voltage	VOH	AData, BData, DCLK, $\overline{\text{DCLK}}$	TA = +25°C	-1.02		-0.70	V
			TA = TMIN to TMAX	-1.10		-0.70	
POWER REQUIREMENTS							
Positive Supply Current	ICC	VCC = 5.0V	TA = +25°C		464	670	mA
			TA = TMIN to TMAX			710	
Negative Supply Current	IEE	VEE = -5.2V	TA = +25°C	-750		-560	mA
			TA = TMIN to TMAX	-780			
Common-Mode Rejection Ratio	CMRR	VINCM = ±0.5V	TA = TMIN to TMAX	35			dB
Power-Supply Rejection Ratio	PSRR	TA = TMIN to TMAX	VCC(nom) = ±0.25V	40			dB
			VEE(nom) = ±0.25V	40			

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250Mbps, 8-Bit ADC with Track/Hold

TIMING CHARACTERISTICS

($V_{EE} = -5.2V$, $V_{CC} = +5V$, $R_L = 50\Omega$ to $-2V$, $V_{ART} = 1.02V$, $V_{ARB} = -1.02V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Pulse Width Low	tpWL	CLK, $\overline{CLK}$, Figures 1 and 2		1.9		5.0	ns
Clock Pulse Width High	tpWH	CLK, $\overline{CLK}$, Figures 1 and 2		1.9			ns
CLK to DCLK Propagation Delay	tpD1	DIV = 0, Figure 1		0.8		2.4	ns
		DIV = 1, Figure 2		1.9		5.7	
DCLK to A/BData Propagation Delay	tpD2	DIV = 0, Figure 1		0.5		2.2	ns
		DIV = 1, Figure 2		-1.4		-0.1	
Rise Time	tR	20% to 80%	DCLK		500		ps
			DATA		700		
Fall Time	tF	20% to 80%	DCLK		600		ps
			DATA		550		
Pipeline Delay (Latency)	tNPD	See Figures 3 and 4 and Table 1 (delay depends on output mode)	Divide-by-1 mode		7 1/2	7 1/2	Clock Cycles
			Divide-by-2 mode	AData	7 1/2	7 1/2	
				BData	8 1/2	8 1/2	

Note 3: All devices are 100% production tested at $+25^\circ C$ and are guaranteed by design for $T_A = T_{MIN}$ to T_{MAX} as specified.

Note 4: Deviation from best-fit straight line. See *Integral Nonlinearity* section.

Note 5: See the *Signal-to-Noise Ratio and Effective Bits* section in the *Definitions of Specifications*.

Note 6: SNR calculated from effective bits performance using the following equation: $SNR (dB) = 1.76 + (6.02) (\text{effective bits})$.

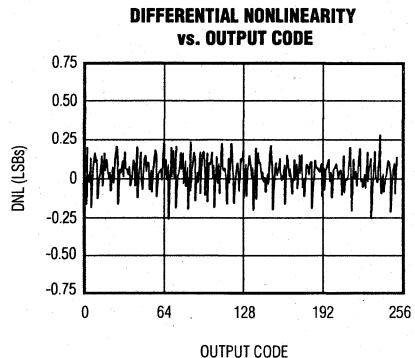
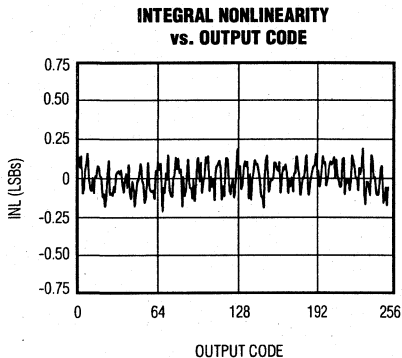
Note 7: Clock pulse width minimum requirements tpWL and tpWH must be observed to achieve stated performance.

Note 8: Functionality guaranteed for $-1.07 \leq V_{IH} \leq -0.7$ and $-2.0 \leq V_{IL} \leq -1.5$.

Note 9: Outputs terminated through 50Ω to $-2.0V$.

Typical Operating Characteristics

($T_A = +25^\circ C$, unless otherwise noted.)



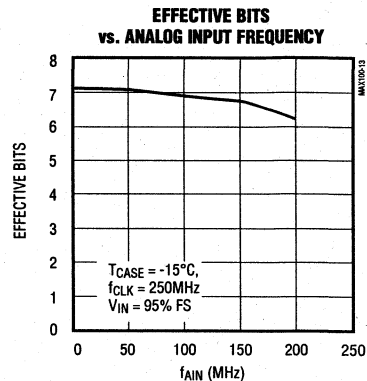
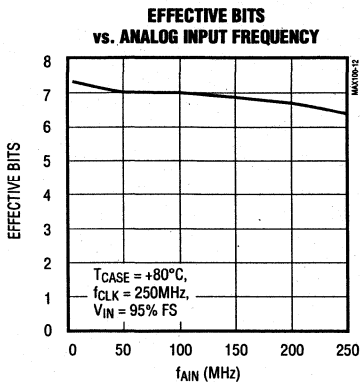
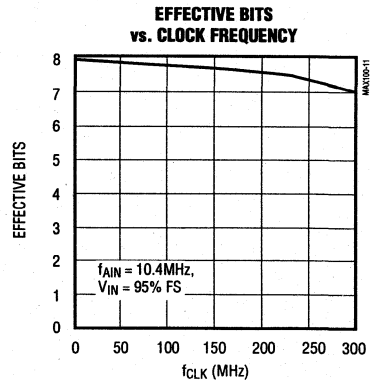
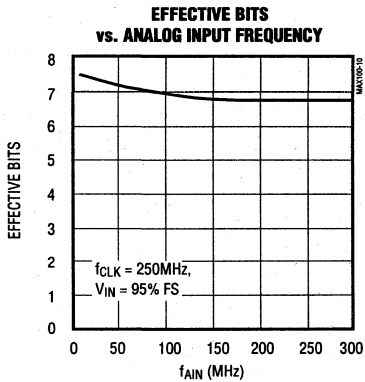
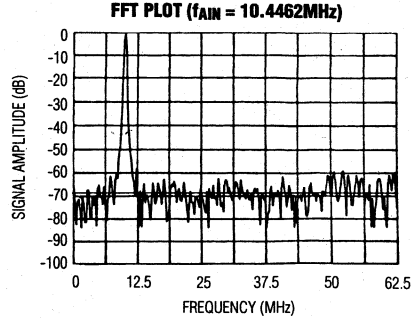
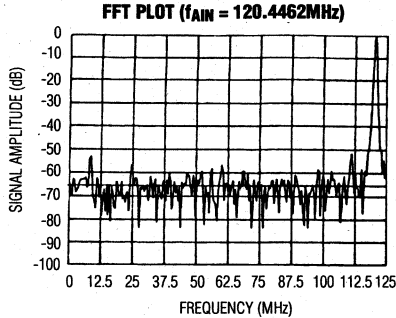
250Mps, 8-Bit ADC with Track/Hold

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX100

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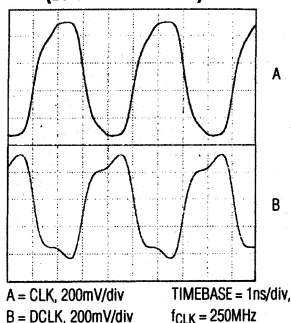


250Mps, 8-Bit ADC with Track/Hold

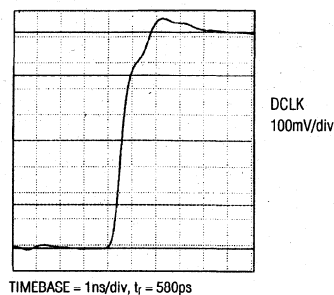
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

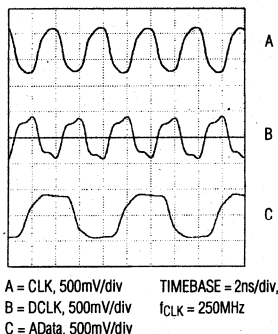
**CLOCK RELATIONSHIP
(DIVIDE-BY-1 MODE)**



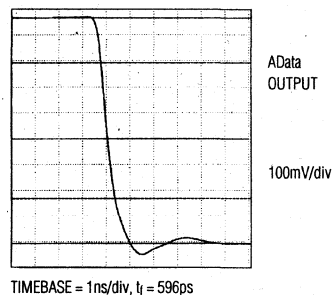
**DIGITAL CLOCK
(POSITIVE EDGE)**



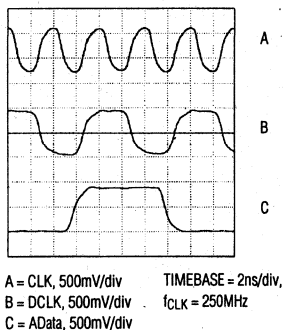
**CLOCK/DATA
(DIVIDE-BY-1 MODE)**



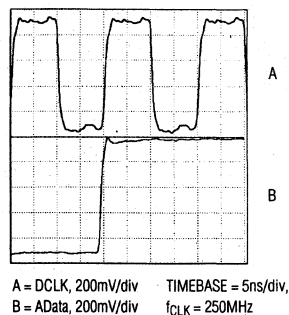
**DATA OUTPUT
(NEGATIVE EDGE)**



**CLOCK/DATA
(DIVIDE-BY-2 MODE)**



**CLOCK/DATA DETAIL
(DIVIDE-BY-5 MODE)**



250Mps, 8-Bit ADC with Track/Hold

Pin Description

MAX100

PIN	NAME	FUNCTION
1	PAD	Internal connection, leave open.
2, 62	CLK	Complementary Differential Clock Inputs. Can be driven from standard 10K ECL with the following considerations: Internally, pins 2 & 62 and 3 & 61 are the ends of a 50Ω transmission line. Either end can be driven, with the other end terminated with 50Ω to -2V. See <i>Typical Operating Circuit</i> .
3, 61	$\overline{\text{CLK}}$	
4, 7, 15, 49, 57, 60, 64, 67, 70, 71, 74, 77, 78, 79, 82, 84	GND	Power-Supply Ground. Connect GND and DGND pins (Note 10).
5, 6, 9, 10, 31, 33, 35, 48, 58, 59, 63, 81, 83	N.C.	No Connect—there is no internal connection to these pins.
8, 21, 43, 56	VCC	Positive power supply, +5V ±5% nominal
11	DIV	Divide Enable Input. DIV and MOD select the output modes. See Table 1.
12	MOD	Modulus. MOD and DIV select the output modes. See Table 1.
13	$\overline{\text{DCLK}}$	Complementary Differential Clock Outputs. Used to synchronize following circuitry: AData and BData outputs are valid t_{PD2} after the rising edge of DCLK. See Figures 1–4.
14	DCLK	
16	A=B	Sets AData equal to BData when asserted (A=B = 1). See Table 1.
17, 20, 23, 26, 36, 39, 42, 45	A7–A0	AData and BData Outputs. A0 and B0 are the LSBs, and A7 and B7 are the MSBs. AData and BData outputs conform to standard 10K ECL logic swings and drive 50Ω transmission lines. Terminate with 50Ω to -2V. See Figures 1–4.
19, 22, 25, 28, 38, 41, 44, 47	B7–B0	
18, 24, 27, 30, 34, 37, 40, 46	DGND	Power-Supply Ground. Connect all ground (GND, DGND) pins together, as described in Note 10.
29	SUB	Circuit Substrate Contact. This pin must be connected to VEE.
32, 69, 80	VEE	Negative Power Supply, -5.2V ±5% nominal
50	VART	Positive Reference Voltage Input (Note 11)
51	VARTS	Positive Reference Voltage Sense (Note 11)

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250Mbps, 8-Bit ADC with Track/Hold

Pin Description (continued)

PIN	NAME	FUNCTION
52	VACTS	Reference Bias Resistor Center-Tap Sense (Note 12)
53	VACT	Reference Bias Resistor Center Tap (Note 12)
54	VARBS	Negative Reference Voltage Sense (Note 11)
55	VARB	Negative Reference Voltage Input (Note 11)
65	TP3	Internal node. Do not connect.
66	TP2	Internal node. Do not connect.
68	TP1	Internal connection. This pin must be connected to GND.
72, 73	AIN+	Analog Inputs, internally terminated with 50Ω to ground. Full-scale linear input range is approximately ±270mV. Drive AIN+ and AIN- differentially for best high-frequency performance.
75, 76	AIN-	

Note 10: Use a multilayer board with a separate layer dedicated to ground. Connect GND and DGND in separate areas in the ground plane (separated by at least 1/4 inch) and at only one location on the board (see *Typical Operating Circuit*).

Note 11: Reference bias supply. Use a separate high-quality supply for these pins. Carefully bypassing these pins to achieve noise-free operation of the reference supplies contributes directly to high ADC accuracy.

Note 12: The center-tap connection of the MAX100 is normally left open. It can be driven with a bias voltage, but should be bypassed carefully (refer to Note 11).

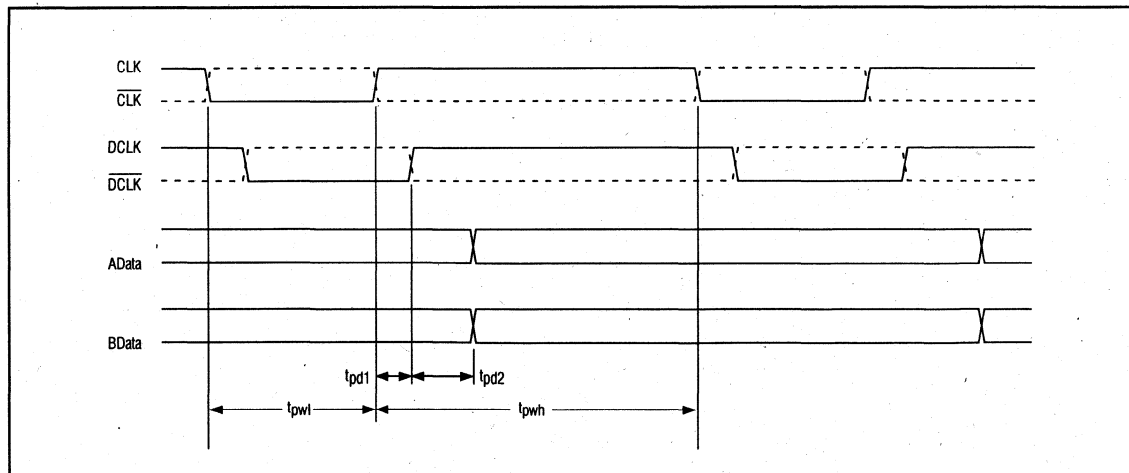


Figure 1. Output Timing: Divide-by-1 Mode (DIV = 0)

250Msps, 8-Bit ADC with Track/Hold

MAX100

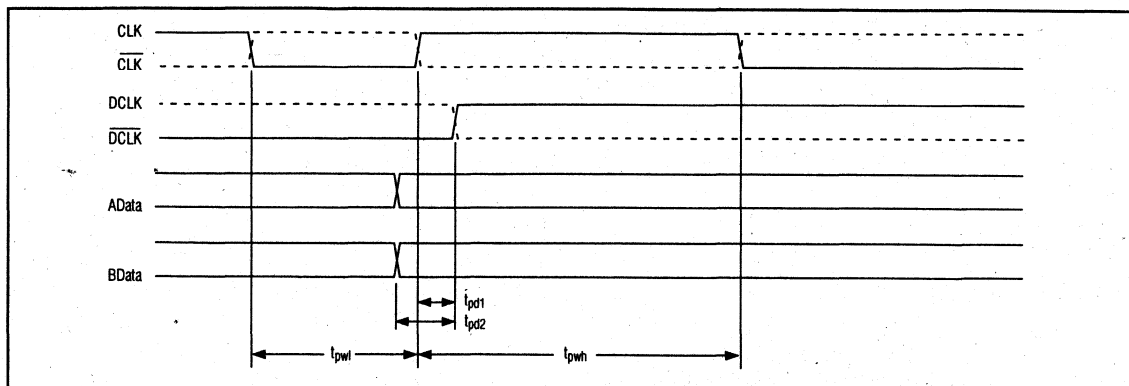


Figure 2. Output Timing: Divide-by-2 or Divide-by-5 Mode (DIV = 1)

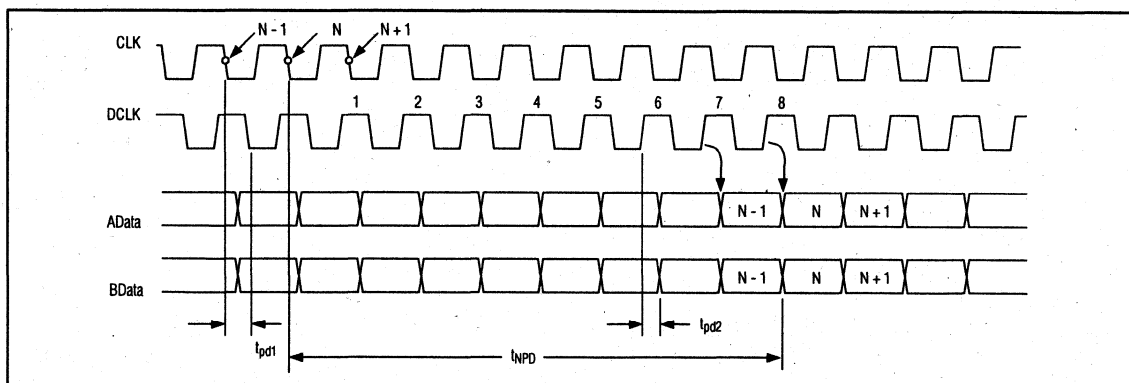


Figure 3. Output Timing: Clock to Data, Divide-by-1 Mode (fast mode, DIV = 0)

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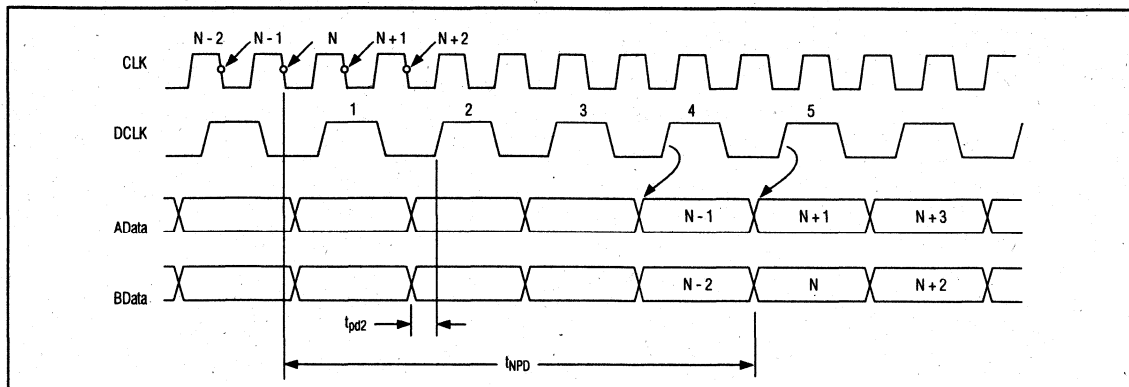


Figure 4. Output Timing: Divide-by-2 Mode (DIV = 1)

250Mps, 8-Bit ADC with Track/Hold

Definitions of Specifications

Signal-to-Noise Ratio and Effective Bits

Signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other analog-to-digital (A/D) output signals. The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: $SNR = (6.02N + 1.76)\text{dB}$, where N is the number of effective bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB. The FFT plots in the *Typical Operating Characteristics* show the output level in various spectral bands.

Effective bits is calculated from a digital record taken from the ADC under test. The quantization error of the ideal converter equals the total error of the device. In addition to ideal quantization error, other sources of error include all DC and AC nonlinearities, clock and aperture jitter, missing output codes, and noise. Noise on references and supplies also degrades effective bits performance.

The ADC's input is a sine wave filtered with an anti-aliasing filter to remove any harmonic content. The digital record taken from this signal is compared against a mathematically generated sine wave. DC offsets, phase, and amplitudes of the mathematical model are adjusted until a best-fit sine wave is found. After subtracting this sine wave from the digital record, the residual error remains. The rms value of the error is applied in the following equation to yield the ADC's effective bits.

$$\text{Effective bits} = N - \log_2 \left(\frac{\text{measured rms error}}{\text{ideal rms error}} \right)$$

where N is the resolution of the converter. In this case, $N = 8$.

The worst-case error for any device will be at the converter's maximum clock rate with the analog input near the Nyquist rate (1/2 the input clock rate).

Aperture Width and Jitter

Aperture width is the time the T/H circuit takes to disconnect the hold capacitor from the input circuit (i.e., to turn off the sampling bridge and put the T/H in hold mode). Aperture jitter is the sample-to-sample variation in aperture delay (Figure 5).

Error Rates

Errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for many

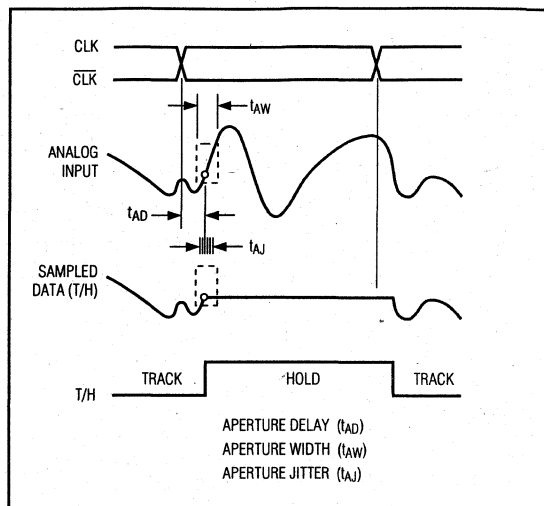


Figure 5. T/H Aperture Timing

typical converters can be incorrect, including false full- or zero-scale output. The MAX100's unique design reduces the magnitude of this type of error to 1LSB, and reduces the probability of the error occurring to less than one in every 10^{15} clock cycles. If the MAX100 were operated at 250MHz, 24 hours a day, this would translate to less than one metastable-state error every 46 days.

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the transfer function from a reference line measured in fractions of 1LSB using a "best straight line" determined by a least square curve fit.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured LSB step and an ideal LSB step size between adjacent code transitions. DNL is expressed in LSBs and is calculated using the following equation:

$$DNL(\text{LSB}) = \frac{[V_{MEAS} - (V_{MEAS-1})] - \text{LSB}}{\text{LSB}}$$

where V_{MEAS-1} is the measured value of the previous code.

A DNL specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

250Msps, 8-Bit ADC with Track/Hold

Detailed Description

Converter Operation

The parallel or "flash" architecture used by the MAX100 provides the fastest multibit conversion of all common integrated ADC designs. The basic element of a flash (as with all other ADC architectures) is the comparator, which has a positive input, a negative input, and an output. If the voltage at the positive input is higher than the negative input (connected to a reference), the output will be high. If the positive input voltage is lower than the reference, the output will be low. A typical n -bit flash consists of $2^n - 1$ comparators with negative inputs evenly spaced at 1LSB increments from the bottom to the top of the reference ladder. For $n = 8$, there will be 255 comparators.

For any input voltage, all the comparators with negative inputs connected to the reference ladder below the input voltage will have outputs of 1, and all comparators with negative inputs above the input voltage will have outputs of 0. Decode logic is provided to convert this information into a parallel n -bit digital word (the output) corresponding to the number of LSBs (minus 1) that the input voltage is above the level set at the bottom of the ladder.

Finally, the comparators contain latch circuitry and are clocked. This allows the comparators to function as described above when, for example, clock is low. When clock goes high (samples) the comparator will latch and hold its state until the clock goes low again.

Track/Hold

As with all ADCs, if the input waveform is changing rapidly during the conversion the effective bits and SNR will decrease. The MAX100 has an internal track/hold (T/H) that increases attainable effective-bits performance and allows more accurate capture of analog data at high conversion rates.

The internal T/H circuit provides two important circuit functions for the MAX100:

- 1) Its nominal voltage gain of 4 reduces the input driving signal to $\pm 270\text{mV}$ differential (assuming a $\pm 1.02\text{V}$ reference).
- 2) It provides a differential 50Ω input that allows easy interface to the MAX100.

Data Flow

The MAX100 contains an internal T/H amplifier that stores the analog input voltage for the ADC to convert. The differential inputs AIN+ and AIN- are tracked continuously between data samples. When a negative CLK edge is applied, the T/H enters hold mode (Figure 5).

When CLK goes low, the most recent sample is presented to the ADC's input comparators. Internal processing of the sampled data is delayed for several clock cycles before it is available at outputs AData or BData. All output data is timed with respect to DCLK and DCLK (Figures 1-4).

Applications Information

Analog Input Ranges

Although the normal operating range is $\pm 270\text{mV}$, the MAX100 can be operated with up to $\pm 500\text{mV}$ on each input with respect to ground. This extended input level includes the analog signal and any DC common-mode voltage.

To obtain a full-scale digital output with differential input drive, a nominal $\pm 270\text{mV}$ must be applied between AIN+ and AIN-. That is, AIN+ = $+135\text{mV}$ and AIN- = -135mV (with no DC offset). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero-scale digital output code, with differential -270mV drive, occurs when AIN+ = -135mV and AIN- = $+135\text{mV}$. Table 2 shows how the output of the converter stays at all ones (full scale) when over ranged or all zeros (zero scale) when under ranged.

For single-ended operation:

- 1) Apply a DC offset to one of the analog inputs, or leave one input open. (Both AIN+ and AIN- are terminated internally with 50Ω to analog ground.)
- 2) Drive the other input with a $\pm 270\text{mV}$ + offset to obtain either full- or zero-scale digital output. If a DC common-mode offset is used, the total voltage swing allowed is $\pm 500\text{mV}$ (analog signal plus offset with respect to ground).

Table 1. Input Voltage Range

INPUT	AIN+** (mV)	AIN-** (mV)	OUTPUT CODE	MSB to LSB
Differential	+135	-135	11111111	full scale
	0	0	10000000	mid scale
	-135	+135	00000000	zero scale
Single Ended	+270	0	11111111	full scale
	0	0	10000000	mid scale
	-270	0	00000000	zero scale

**An offset V_{IO} , as specified in the DC electrical parameters, may be present at the input. Compensate for this offset by either adjusting the reference voltage (V_{ART} or V_{ARB}), or introducing an offset voltage in one of the input terminals AIN+ or AIN-.

MAX100

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250MSPs, 8-Bit ADC with Track/Hold

Table 2. Output Mode Control

DIV	MOD	A=B	DCLK* (MHz)	MODE	DESCRIPTION
0	X	0	250	Divide by 1	Data appears on AData only, BData port inactive (Figure 3).
0	X	1	250	Divide by 1	AData identical to BData (Figure 3).
1	0	0	125	Divide by 2	8:16 demultiplexer mode. AData and BData ports are active. BData carries older sample and AData carries most recent sample (Figure 4).
1	0	1	125	Divide by 2	AData and BData ports are active, both carry identical sampled data. Alternate samples are taken but discarded.
1	1	0	50	Divide by 5	AData port updates data on 5th input CLK. BData port inactive. Other 4 sampled data points are discarded.
1	1	1	50	Divide by 5	AData and BData ports are both active with identical data. Data is updated on output ports every 5th input clock (CLK). The other 4 samples are discarded.

*Input clocks (CLK, $\overline{\text{CLK}}$) = 250MHz for all above combinations. In divide-by-2 or divide-by-5 mode the output clock DCLK will always be a 50% duty-cycle signal. In divide-by-1 mode DCLK will have the same duty cycle as CLK.

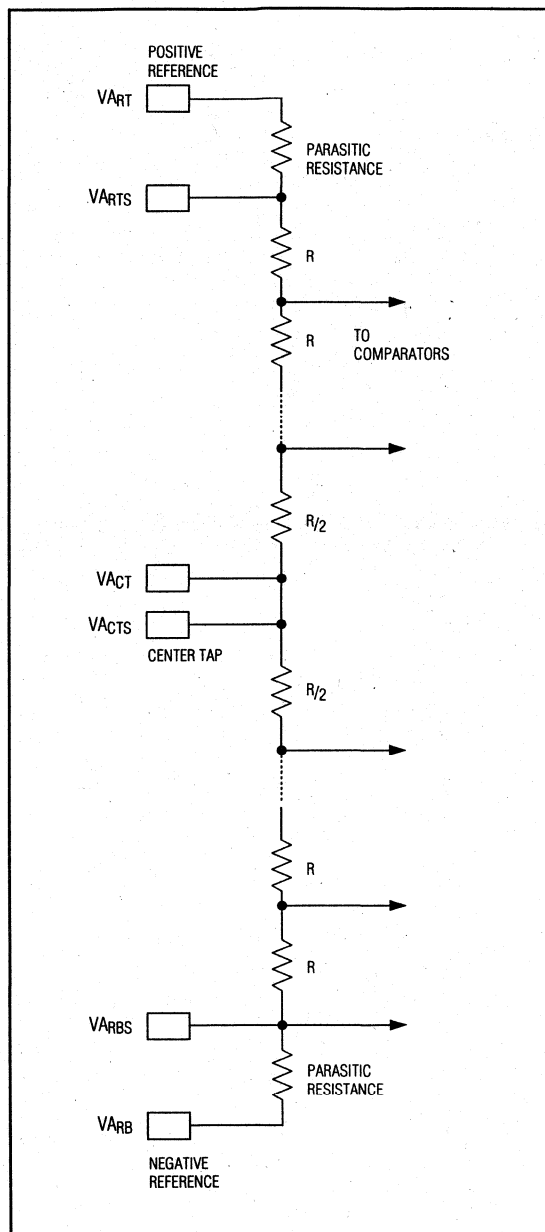


Figure 6. Reference Ladder String

250Mps, 8-Bit ADC with Track/Hold

MAX100

Reference

The ADC's reference resistor is a Kelvin-sensed, center-tapped resistor string that sets the ADC's LSB size and dynamic operating range. Normally, the top and bottom of this string are driven with an op amp, and the center tap is left open. However, driving the center tap is an effective way to modify the output coding to provide a user-defined bilinear response. The buffer amplifier used to drive the top and bottom inputs will need to supply approximately 18mA due to the resistor string impedance of 116 Ω minimum. A reference voltage of $\pm 1.02V$ is normally applied to inputs VART and VARB. This reference voltage can be adjusted up to $\pm 1.4V$ to accommodate extended input requirements (accuracy specifications are guaranteed with $\pm 1.02V$ references). The reference input VARTS, VARBS, and VACTS allow Kelvin sensing of the applied voltages to increase precision.

An RC network at the ADC's reference terminals is needed for best performance. This network consists of a 33 Ω resistor connected in series with the op amp output that drives the reference. A 0.47 μF capacitor must be connected near the resistor at the op amp's output (see *Typical Operating Circuit*). This resistor and capacitor combination should be located within 0.5 inches of the MAX100 package. Any noise on these pins will directly affect the code uncertainty and degrade the ADC's effective-bits performance.

CLK and DCLK

All input and output clock signals are differential. The input clocks, CLK and $\overline{CLK}$, are the primary timing signals for the MAX100. CLK and $\overline{CLK}$ are fed to the internal circuitry from pins 2 & 3 or pins 62 & 61 through an internal 50 Ω transmission line. One pair of CLK/ $\overline{CLK}$ inputs should be driven and the other pair terminated by 50 Ω to -2V. Either pair can be used as the driven inputs (input lines are balanced) for easy circuit connection. A minimum pulse width (tpWL) is required for CLK and $\overline{CLK}$ (Figures 1-4).

For best performance and consistent results, use a low phase-jitter clock source for CLK and $\overline{CLK}$. Phase jitter larger than 2ps from the input clock source reduces the converter's effective-bits performance and causes inconsistent results.

DCLK and $\overline{DCLK}$ are output clock signals derived from the input clocks and are used for external timing of the AData and BData outputs. The MAX100 is characterized to work with maximum input clock frequencies of 250MHz (Table 1). See *Typical Operating Circuit*.

Output Mode Control

DIV, MOD, and A=B are input pins that determine the operating mode of the two output data paths. Six options are available (Table 1). A typical operating configuration (8:16 demultiplexer mode) is set by 1 on DIV, 0 on MOD, and 0 on A=B. This will give the most recent sample at AData with the older data on BData. Both outputs are synchronous and are at half the input clock rate. To terminate the control inputs, use a resistor to -2V or the equivalent circuit resistor combination from DGND to -5.2V up to 1k Ω . When using a diode pull-up to tie an input high, bias the diode "on" with a pull-down resistor to avoid input voltage excursions close to ground. The control inputs are compatible with standard ECL 10K logic levels over temperature.

Layout, Grounding, and Power Supplies

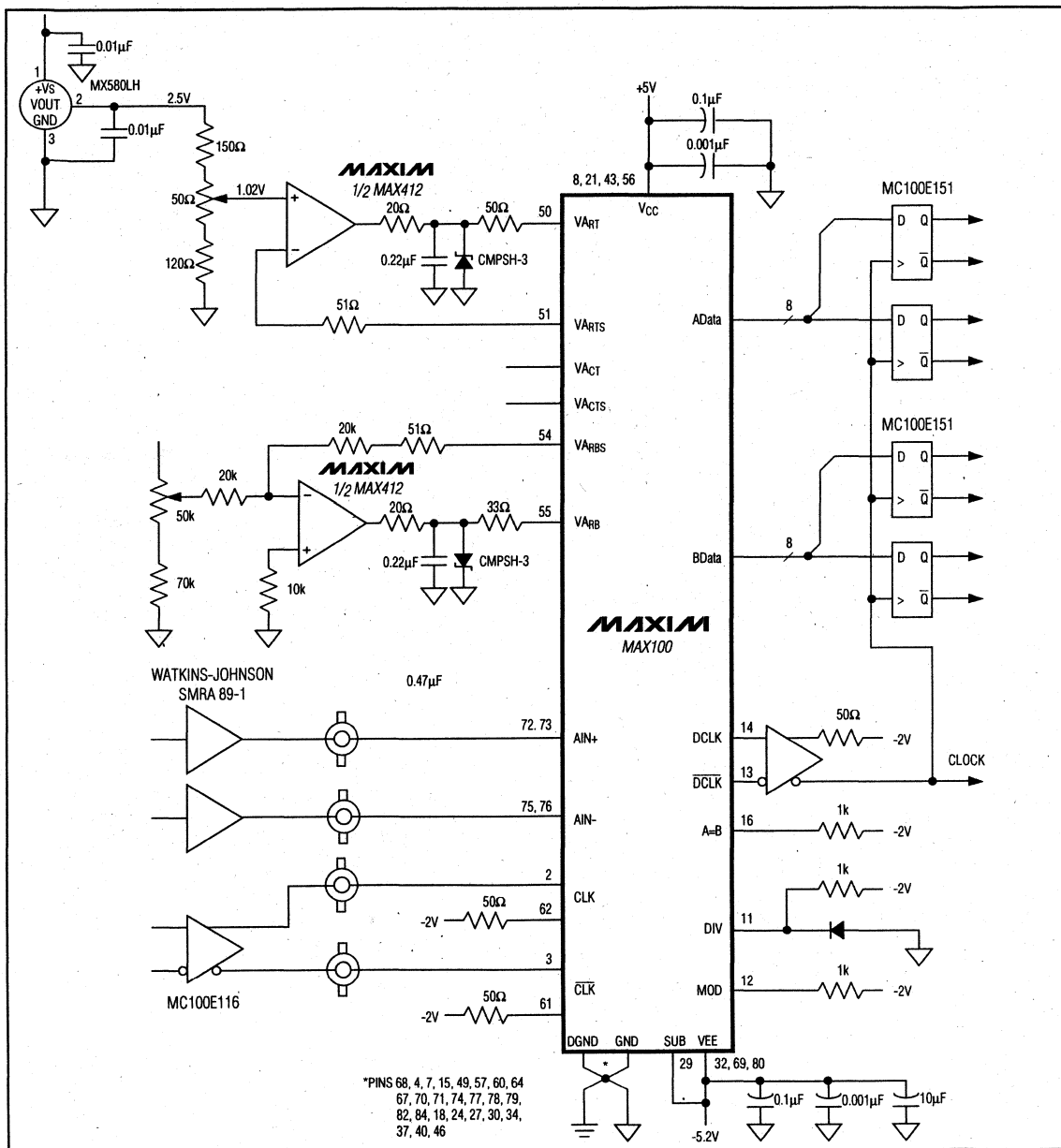
The MAX100 is designed with separate analog and digital ground connections to isolate high-current digital noise spikes. The high-current digital ground, DGND, is connected to the collectors of the output emitter follower transistors. The low-current ground connection is GND, which is a combination of the analog ground and the ground of the low-current digital decode section. The DGND and GND connections should be at the same DC level, and should be connected at only one location on the board. This will provide better noise immunity and highest device accuracy. A ground plane is recommended.

A +5V $\pm 5\%$ supply as well as a -5.2V $\pm 5\%$ supply is needed for proper operation. Bypass the VEE and VCC supply pins to GND with high-quality 0.1 μF and 0.001 μF ceramic capacitors located as close to the package as possible. An evaluation kit with a suggested layout is available.

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250Mbps, 8-Bit ADC with Track/Hold

Typical Operating Circuit

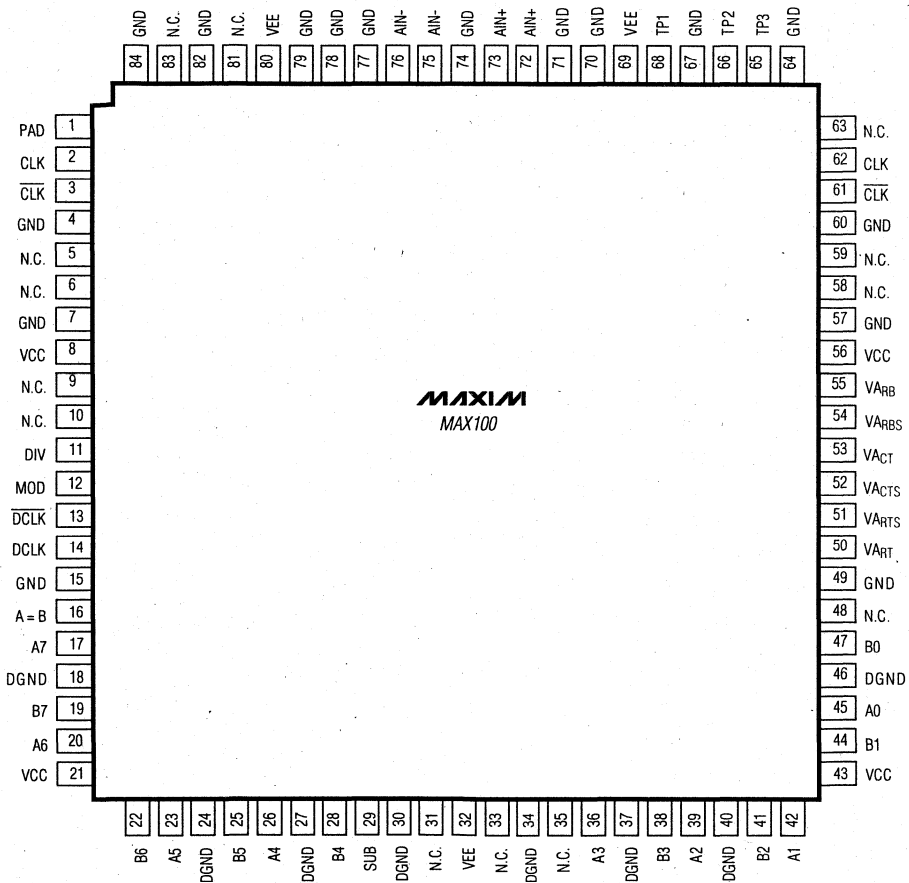


250Mbps, 8-Bit ADC with Track/Hold

Pin Configuration

MAX100

TOP VIEW



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500Mps, 8-Bit ADC with Track/Hold

General Description

The MAX101 ECL-compatible, 500Mps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 250MHz (Nyquist frequency). Dual monolithic converters, driven by the track/hold (T/H), operate on opposite clock edges (time interleaved). Designed with Maxim's proprietary advanced bipolar processes, the MAX101 contains a high-performance T/H amplifier and two quantizers in an 84-pin ceramic flat pack.

The innovative design of the internal T/H assures an exceptionally wide 1.2GHz input bandwidth and aperture delay uncertainty of less than 2ps, resulting in a high 7.0 effective bits at the Nyquist frequency. Special comparator output design and decoding circuitry reduce out-of-sequence code errors. The probability of erroneous codes due to metastable states is reduced to less than 1 error per 10^{15} clock cycles. And, unlike other ADCs that can have errors resulting in false full-scale or zero-scale outputs, the MAX101 keeps the error magnitude to less than 1LSB.

The analog input is designed for either differential or single-ended use with a $\pm 270\text{mV}$ range. Sense pins for the reference input allow full-scale calibration of the input range or facilitate ratiometric use.

Phase adjustment is available to adjust the relative sampling of the converter halves for optimizing converter performance. Input clock phasing is also available for interleaving several MAX101s for higher effective sampling rates.

Features

- ♦ 500Mps Conversion Rate
- ♦ 7.0 Effective Bits Typical at 250MHz
- ♦ 1.2GHz Analog Input Bandwidth
- ♦ Less than $\pm 1/2\text{LSB}$ INL
- ♦ 50Ω Differential or Single-Ended Inputs
- ♦ $\pm 270\text{mV}$ Input Signal Range
- ♦ Ratiometric Reference Inputs
- ♦ Dual Latched Output Data Paths
- ♦ Low Error Rate, Less than 10^{-15} Metastable States
- ♦ 84-Pin Ceramic Flat Pack

Applications

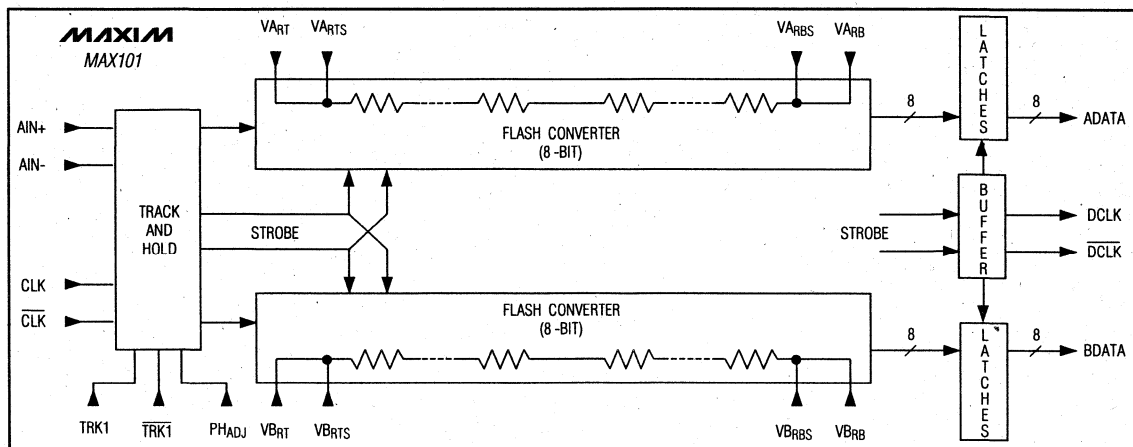
High-Speed Digital Instrumentation
High-Speed Signal Processing
Medical Systems
Radar/Signal Processing
High-Energy Physics
Communications

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX101CFR*	0°C to +70°C	84 Ceramic Flat Pack (with heatsink)

*Contact factory for 84-pin ceramic flat pack without heatsink.

Functional Diagram



500Msps, 8-Bit ADC with Track/Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	DIV10 Input Voltage (V_{IH} , V_{IL}).....	VEE to 0V
VCC.....	Output Current, (I_{Omax}).....	
VEE.....	$T_J < 100^\circ\text{C}$	14mA
VCC - VEE.....	$100^\circ\text{C} < T_J < 125^\circ\text{C}$	12mA
Analog Input Voltage.....	Operating Temperature Range.....	0°C to $+70^\circ\text{C}$
Reference Voltage (V_{ART} , V_{BRT}).....	Operating Junction Temperature (Note 2).....	0°C to $+125^\circ\text{C}$
Reference Voltage (V_{ARB} , V_{BRB}).....	Storage Temperature Range.....	-65°C to $+150^\circ\text{C}$
Clock Input Voltage (V_{IH} , V_{IL}).....	Lead Temperature (soldering, 10sec).....	$+250^\circ\text{C}$

Note 1: The digital control inputs are diode protected. However, limited protection is provided on other pins. Permanent damage may occur on unconnected units under high-energy electrostatic fields. Keep unused units in supplied conductive carrier or shunt the terminals together.

Note 2: Typical thermal resistance, junction-to-case $R_{\theta JC} = 5^\circ\text{C/W}$ and thermal resistance, junction to ambient (MAX101CFR) $R_{\theta JA} = 12^\circ\text{C/W}$, if 200 lineal ft/min airflow is provided. See *Package Information*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{EE} = -5.2\text{V}$, $V_{CC} = +5\text{V}$, $R_L = 100\Omega$ to -2V , V_{ART} , $V_{BRT} = 1.02\text{V}$, V_{ARB} , $V_{BRB} = -1.02\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. T_{MIN} to $T_{MAX} = 0^\circ\text{C}$ to $+70^\circ\text{C}$. Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				8			Bits
Integral Nonlinearity (Note 4)	INL	AData, BData	$T_A = +25^{\circ}\text{C}$			± 0.50	LSB
			$T_A = T_{\text{MIN}}$ to T_{MAX}			± 0.75	
Differential Nonlinearity	DNL	AData, BData, no missing codes	$T_A = +25^{\circ}\text{C}$			± 0.75	LSB
			$T_A = T_{\text{MIN}}$ to T_{MAX}			± 0.85	
DYNAMIC SPECIFICATIONS							
Effective Bits	ENOB	$f_{\text{CLK}} = 500\text{MHz}$, $V_{\text{IN}} = 95\%$ full scale (Note 5)	$f_{\text{AIN}} = 10\text{MHz}$			7.6	Bits
			$f_{\text{AIN}} = 125\text{MHz}$			7.1	
			$f_{\text{AIN}} = 250\text{MHz}$	6.7	7.0		
Signal-to-Noise Ratio	SNR	$f_{\text{AIN}} = 125\text{MHz}$, $f_{\text{CLK}} = 500\text{MHz}$, $V_{\text{IN}} = 95\%$ full scale (Note 6)		44.5			dB
Maximum Conversion Rate	f_{CLK}	(Note 7)		500			Msps
Analog Input Bandwidth	$\text{BW}_{3\text{dB}}$					1.2	GHz
Aperture Width	t_{AW}	Figure 4		270			ps
Aperture Jitter	t_{AJ}	Figure 4		2			ps
ANALOG INPUT							
Input Voltage Range	V_{IN}	AIN+ to AIN-, Table 2, $T_A = T_{\text{MIN}}$ to T_{MAX}	Full scale	230	315	mV	
			Zero scale	-305	-215		
Input Offset Voltage	V_{IO}	AIN+, AIN-, $T_A = T_{\text{MIN}}$ to T_{MAX}		-17	32	mV	
Least Significant Bit Size	LSB	$T_A = T_{\text{MIN}}$ to T_{MAX}		1.8	2.5	mV	
Input Resistance	R_{I}	AIN+, AIN-, to GND		49	51	Ω	
Input Resistance Temperature Coefficient				0.008		$\Omega/^{\circ}\text{C}$	

500Mps, 8-Bit ADC with Track/Hold

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ELECTRICAL CHARACTERISTICS (continued)

($V_{EE} = -5.2V$, $V_{CC} = +5V$, $R_L = 100\Omega$ to $-2V$, V_{ART} , $V_{BRT} = 1.02V$, V_{ARB} , $V_{BRB} = -1.02V$, $T_A = +25^\circ C$, unless otherwise noted. T_{MIN} to $T_{MAX} = 0^\circ C$ to $+70^\circ C$. Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT						
Reference String Resistance	R_{REF}	V_{ART} to V_{ARB}	100		175	Ω
Reference String Resistance Temperature Coefficient				0.02		$\Omega/^\circ C$
LOGIC INPUTS						
Digital Input Low Voltage	V_{IL}	$CLK, \overline{CLK}$ $T_A = T_{MIN}$ to T_{MAX}			-1.50	V
Digital Input High Voltage	V_{IH}	$CLK, \overline{CLK}$ $T_A = T_{MIN}$ to T_{MAX}	-1.1			V
Digital Input High Current	I_{IH}	$DIV10 = 0V$ $T_A = T_{MIN}$ to T_{MAX}	1.1		3.1	mA
Input Bias Current	I_B	$PH_{ADJ} = 0V$ $T_A = T_{MIN}$ to T_{MAX}			40	μA
Clock Input Bias Current	I_{CLK}	$CLK, \overline{CLK} = -0.8V$ (no termination) $T_A = T_{MIN}$ to T_{MAX}			50	μA
LOGIC OUTPUTS (Note 8)						
Digital Output Low Voltage	V_{OL}	AData, BData	$T_A = +25^\circ C$	-1.95	-1.60	V
			$T_A = T_{MIN}$ to T_{MAX}	-1.95	-1.50	
		DCLK, $\overline{DCLK}$	$T_A = +25^\circ C$	-1.3	-1.00	
			$T_A = T_{MIN}$ to T_{MAX}	-1.4	-0.9	
Digital Output High Voltage	V_{OH}	AData, BData, DCLK, $\overline{DCLK}$	$T_A = +25^\circ C$	-1.02	-0.70	V
			$T_A = T_{MIN}$ to T_{MAX}	-1.10	-0.60	
Digital Output Voltage	$V_{OH} - V_{OL}$	DCLK, $\overline{DCLK}$ $T_A = T_{MIN}$ to T_{MAX}	275		445	mV
POWER REQUIREMENTS						
Positive Supply Current	I_{VCC}	$V_{CC} = 5.0V$	$T_A = +25^\circ C$	550	765	mA
			$T_A = T_{MIN}$ to T_{MAX}		1130	
Negative Supply Current	I_{VEE}	$V_{EE} = -5.2V$	$T_A = +25^\circ C$	-935	-750	mA
			$T_A = T_{MIN}$ to T_{MAX}	-975		
Common-Mode Rejection Ratio	CMRR	$V_{INCM} = \pm 0.5V$ $T_A = T_{MIN}$ to T_{MAX}	35			dB
Power-Supply Rejection Ratio	PSRR	$V_{CC}(nom) = \pm 0.25V$ $T_A = T_{MIN}$ to T_{MAX}	40			dB
		$V_{EE}(nom) = \pm 0.25V$	40			

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500Mbps, 8-Bit ADC with Track/Hold

TIMING CHARACTERISTICS

($V_{EE} = -5.2V$, $V_{CC} = +5V$, $R_L = 100\Omega$ to $-2V$, V_{ART} , $V_{BRT} = 1.02V$, V_{ARB} , $V_{BRB} = -1.02V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Pulse Width Low	tpWL	CLK, CLK		0.9		2.5	ns
Clock Pulse Width High	tpWH	CLK, CLK		0.9		2.5	ns
CLK to DCLK Propagation Delay	tpD1	DIV10 = 0, Figures 1, 2		1.2	2.3	3.4	ns
DCLK to A/BData Propagation Delay	tpD2	DIV10 = 0, Figures 1, 2		0.7	1.3	1.8	ns
Rise Time	tR	20% to 80%	DCLK		400		ps
			DATA		850		
Fall Time	tF	20% to 80%	DCLK		400		ps
			DATA		700		
Pipeline Delay (Latency)	tNPD	See Figures 2, 3 and Table 1	Divide-by-1 mode	15		15	Clock Cycles

Note 3: All devices are 100% production tested at $+25^\circ C$ and are guaranteed by design for $T_A = T_{MIN}$ to T_{MAX} as specified.

Note 4: Deviation from best-fit straight line. See *Integral Nonlinearity* section.

Note 5: See the *Signal-to-Noise Ratio and Effective Bits* section in the *Detailed Description of Specifications*.

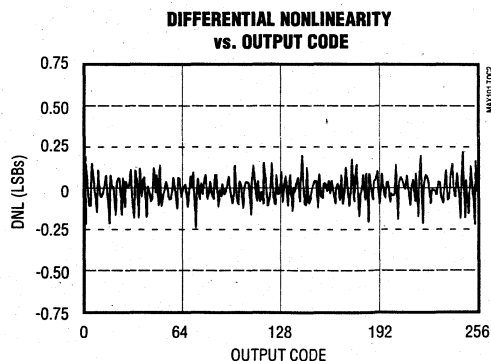
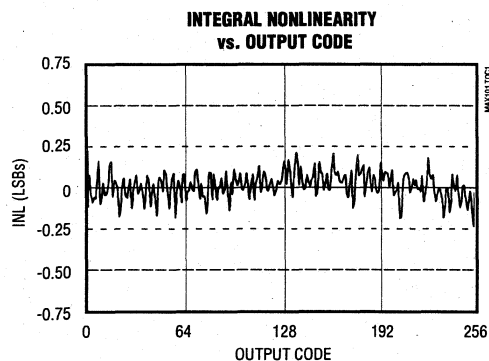
Note 6: SNR calculated from effective bits performance using the following equation: $SNR(dB) = 1.76 + 6.02 \times \text{effective bits}$.

Note 7: Clock pulse width minimum requirements tpWL and tpWH must be observed to achieve stated performance.

Note 8: Outputs terminated through 100Ω to $-2.0V$.

Typical Operating Characteristics

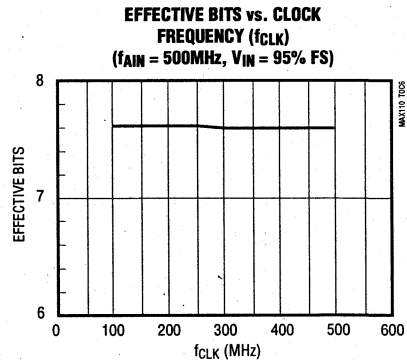
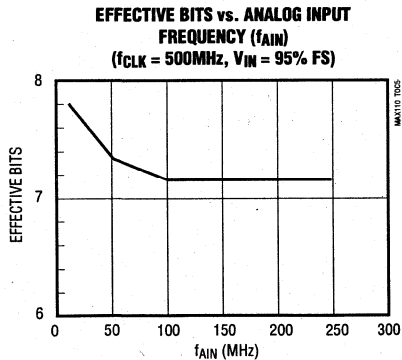
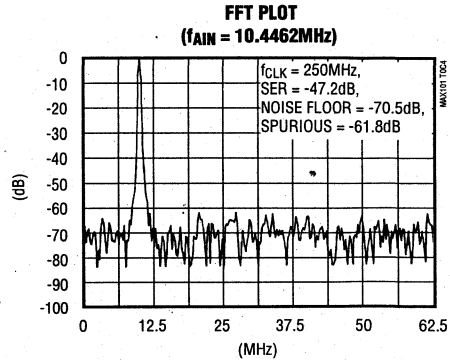
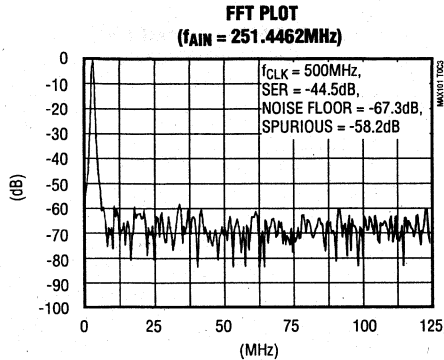
($V_{EE} = -5.2V$, $V_{CC} = +5V$, $R_L = 100\Omega$ to $-2V$, V_{ART} , $V_{BRT} = 1.02V$, V_{ARB} , $V_{BRB} = -1.02V$, $T_A = +25^\circ C$, unless otherwise noted.)



500Mps, 8-Bit ADC with Track/Hold

Typical Operating Characteristics (continued)

($V_{EE} = -5.2V$, $V_{CC} = +5V$, $R_L = 100\Omega$ to $-2V$, V_{ART} , $V_{BRT} = 1.02V$, V_{ARB} , $V_{BRB} = -1.02V$, $T_A = +25^\circ C$, unless otherwise noted.)



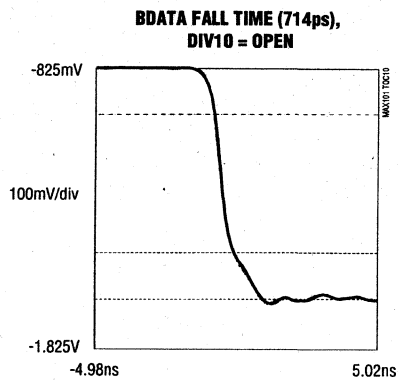
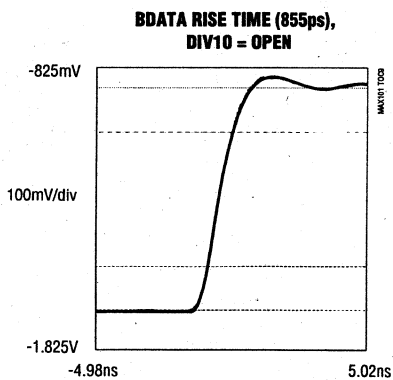
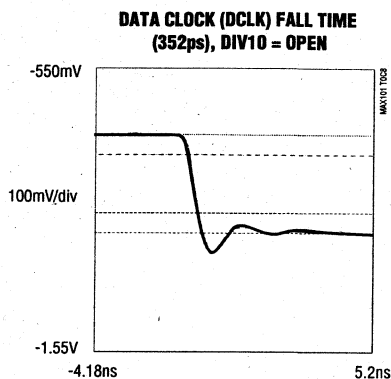
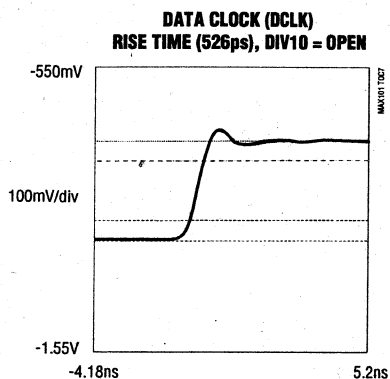
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500Mps, 8-Bit ADC with Track/Hold

Typical Operating Characteristics (continued)

($V_{EE} = -5.2V$, $V_{CC} = +5V$, $R_L = 100\Omega$ to $-2V$, V_{ART} , $V_{BRT} = 1.02V$, V_{ARB} , $V_{BRB} = -1.02V$, $T_A = +25^\circ C$, unless otherwise noted.)



500Msps, 8-Bit ADC with Track/Hold

Pin Description

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PIN	NAME	FUNCTION
1	PAD	Internal connection, leave open.
2, 62	CLK	Complementary Differential Clock Inputs. Can be driven from standard 10KH ECL with the following considerations: Internally, pins 2, 62 and 3, 61 are the ends of a 50Ω transmission line. Either end can be driven with the other end terminated with 50Ω to -2V. See <i>Typical Operating Circuit</i> .
3, 61	$\overline{\text{CLK}}$	
4, 7, 15, 18, 24, 27, 30, 34, 37, 40, 46, 49, 57, 60, 64, 67, 68, 70, 71, 74, 77, 78, 79, 82, 84	GND	Power-Supply Ground
5, 59	TRK1	Phasing inputs (normally left open). See <i>Applications Information</i> section.
6, 58	TRK1	
8, 21, 43, 56, 81	VCC	Positive Power Supply, +5V ±5% nominal
9	VB _{RB}	"B" side negative reference voltage input (Note 9)
10	VB _{RBS}	"B" side negative reference voltage sense (Note 9)
11	TP4	Internal connection, leave pin open.
12	TP3	Internal connection, leave pin open.
13	VB _{RTS}	"B" side positive reference voltage sense (Note 9)
14	VB _{RT}	"B" side positive reference voltage input (Note 9)
16, 48, 63	N.C.	No Connect—no internal connection to these pins.
29	SUB	Circuit Substrate contact. This pin must be connected to VEE.
31	DCLK	Complementary Differential Clock Outputs. Used to synchronize following circuitry: Outputs A0–A7 are valid after DCLK's rising edge. B0–B7 output data are valid after DCLK's falling edge (see Figure 1 for output timing information).
33	$\overline{\text{DCLK}}$	
32, 69, 80	VEE	Negative Power Supply, -5.2V ±5% nominal
35	DIV10	Divide by 10 mode. Leave open for normal operation. Selects test mode when grounded.
36, 38, 39, 41, 42, 44, 45, 47	A7–A0	AData and BData Outputs. A0 and B0 are the LSBs, and A7 and B7 are the MSBs. AData and BData outputs conform to ECL logic swings and drive 100Ω transmission lines. Terminate with 100Ω to -2V (120Ω for T _j > +100°C). See Figures 1–3.
28, 26, 25, 23, 22, 20, 19, 17	B7–B0	

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500Msps, 8-Bit ADC with Track/Hold

Pin Description (continued)

PIN	NAME	FUNCTION
50	VART	"A" side positive reference voltage input (Note 9)
51	VARTS	"A" side positive reference voltage sense (Note 9)
52	TP1	Internal connection, leave pin open.
53	TP2	Internal connection, leave pin open.
54	VARBS	"A" side negative reference voltage sense (Note 9)
55	VARB	"A" side negative reference voltage input (Note 9)
65	TP5	Internal connection, leave pin open.
66	TP6	Internal connection, leave pin open.
72, 73	AIN+	Analog Inputs, internally terminated with 50Ω to ground. Full-scale linear input range is approximately ±270mV. Drive AIN+ and AIN- differentially for best high-frequency performance.
75, 76	AIN-	
83	PHADJ	Phase adjustment for T/H. Normally connected to ground. A phase adjustment of approximately ±18ps can be made by varying this pin's bias point to optimize interleaving between sides A and B (Note 10).

Note 9: VART, VARB, VBRT, and VBRB should be adjusted separately from a well bypassed reference circuit to ensure proper amplitude and offset matching. The sense connections to each of these terminals allows precision setting of the reference voltage. The reference ladder is similar for both converter halves (check electrical section for values). Any noise on these terminals will severely reduce overall performance.

Note 10: Good results are obtained by connecting the PHADJ input to ground. Improve performance by applying a voltage between ±1.25V to this input. The time that the "A" T/H bridge samples relative to the time that the "B" T/H bridge samples can be varied through a ±18ps range.

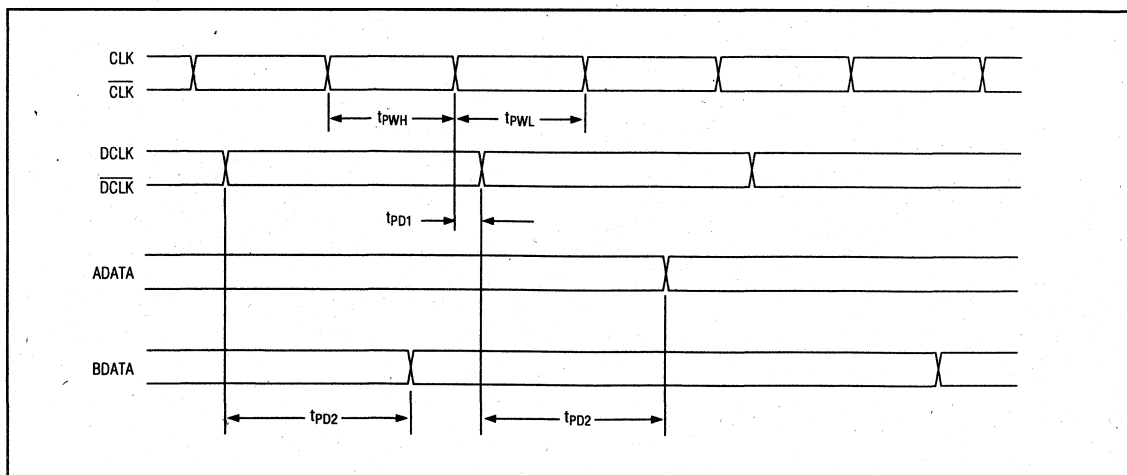


Figure 1. Output Timing, Normal Mode, DIV10 = OPEN

500Mbps, 8-Bit ADC with Track/Hold

MAX101

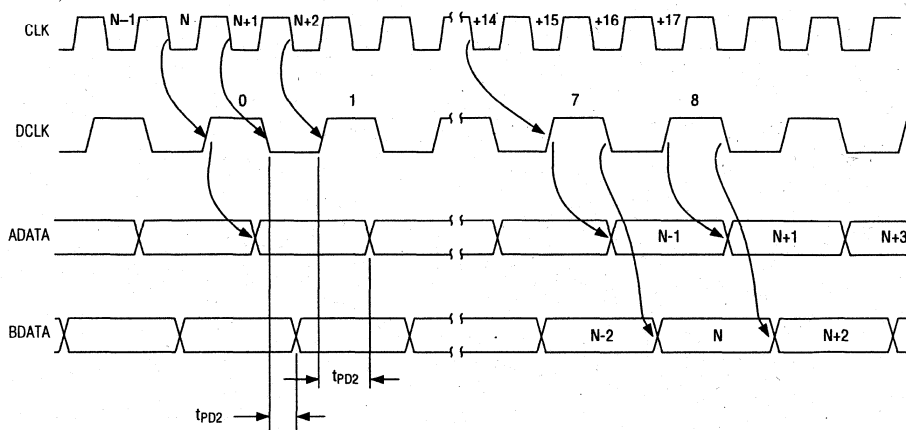


Figure 2. Output Timing, Clock to Data, Normal Mode DIV10 = OPEN

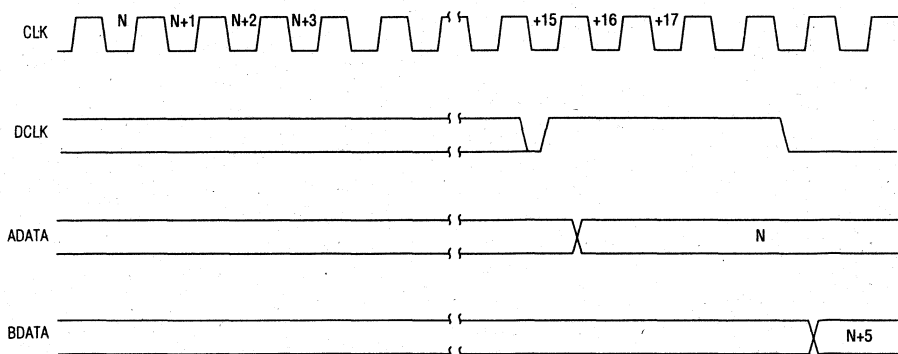


Figure 3. Output Timing, Test Mode (DIV10 = GND)

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500Mps, 8-Bit ADC with Track/Hold

Definitions of Specifications

Signal-to Noise Ratio and Effective Bits

Signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other analog-to-digital (A/D) output signals. The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: $SNR = (6.02N + 1.76)\text{dB}$, where N is the number of effective bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB. The FFT plots in the *Typical Operating Characteristics* show the output level in various spectral bands.

Effective bits is calculated from a digital record taken from the ADC under test. The quantization error of the ideal converter equals the total error of the device. In addition to ideal quantization error, other sources of error include all DC and AC nonlinearities, clock and aperture jitter, missing output codes, and noise. Noise on references and supplies also degrades effective bits performance.

The ADC's input is a sine wave filtered with an anti-aliasing filter to remove any harmonic content. The digital record taken from this signal is compared against a mathematically generated sine wave. DC offsets, phase, and amplitudes of the mathematical model are adjusted until a best-fit sine wave is found. After subtracting this sine wave from the digital record, the residual error remains. The rms value of the error is applied in the following equation to yield the ADC's effective bits.

$$\text{Effective bits} = N - \log_2 \frac{\text{measured rms error}}{\text{ideal rms error}}$$

where N is the resolution of the converter. In this case, $N = 8$.

The worst-case error for any device will be at the converter's maximum clock rate with the analog input near the Nyquist rate (one-half the input clock rate).

Aperture Width and Jitter

Aperture width is the time the T/H circuit takes to disconnect the hold capacitor from the input circuit (i.e., to turn off the sampling bridge and put the T/H in hold mode). Aperture jitter is the sample-to-sample variation in aperture delay (Figure 4).

Error Rates

Errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for many

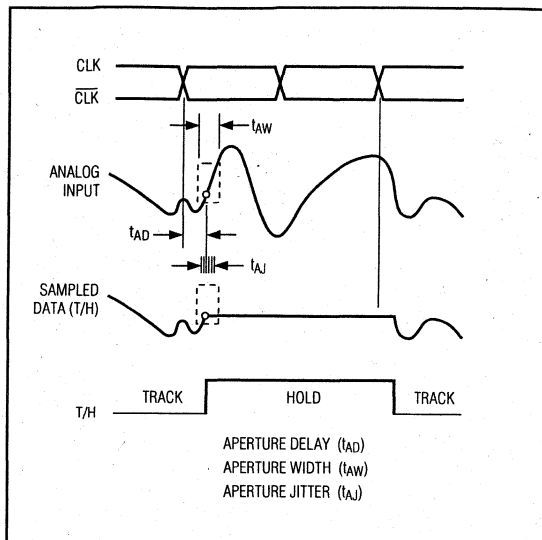


Figure 4. T/H Aperture Timing

typical converters can be incorrect, including false full- or zero-scale output. The MAX101's unique design reduces the magnitude of this type of error to 1LSB, and reduces the probability of the error occurring to less than one in every 10^{15} clock cycles. If the MAX101 were operated at 500MHz, 24 hours a day, this would translate to less than one metastable state error every 46 days.

Integral Nonlinearity

Integral nonlinearity is the deviation of the transfer function from a reference line measured in fractions of 1LSB using a "best straight line" determined by a least square curve fit.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured LSB step and an ideal LSB step size between adjacent code transitions. DNL is expressed in LSBs and is calculated using the following equation:

$$\text{DNL(1LSB)} = \frac{[V_{\text{MEAS}} - (V_{\text{MEAS}} - 1)] - \text{LSB}}{\text{LSB}}$$

where $V_{\text{MEAS}} - 1$ is the measured value of the previous code.

A DNL specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

500Msps, 8-Bit ADC with Track/Hold

Detailed Description

Converter Operation

The parallel or "flash" architecture used by the MAX101 provides the fastest multibit conversion of all common integrated ADC designs. The basic element of a flash, as with all other ADC architectures, is the comparator, which has a positive input, a negative input, and an output. If the voltage at the positive input is higher than the negative input (connected to a reference), the output will be high. If the positive input voltage is lower than the reference, the output will be low. A typical n-bit flash consists of $2^n - 1$ comparators with negative inputs evenly spaced at 1LSB increments from the bottom to the top of the reference ladder. For $n = 8$, there are 255 comparators.

For any input voltage, all the comparators with negative inputs connected to the reference ladder below the input voltage will have outputs of 1 and all comparators with negative inputs above the input voltage will have outputs of 0. Decode logic is provided to convert this information into a parallel n-bit digital word (the output) corresponding to the number of LSBs (minus 1) that the input voltage is above the bottom of the ladder.

The comparators contain latch circuitry and are clocked. This allows the comparators to function as described previously when, for example, clock is low. When clock goes high (samples) the comparator will latch and hold its state until the clock goes low again.

The MAX101 uses a monolithic dual interleaved parallel quantizer chip with two separate 8-bit converters. These converters deliver results to the A and B output latches on alternate negative edges of the input clock.

Track/Hold

As with all ADCs, if the input waveform is changing rapidly during the conversion the effective bits and SNR will decrease. The MAX101 has an internal track/hold (T/H) that increases attainable effective bits performance and allows more accurate capture of analog data at high conversion rates.

The internal T/H circuit provides two important circuit functions for the MAX101:

- 1) Its nominal voltage gain of 4 reduces the input driving signal to $\pm 270\text{mV}$ differential (assuming a $\pm 1.02\text{V}$ reference).
- 2) It provides a differential 50Ω input that allows easy interface to the MAX101.

Table 1. Output Mode Control

DIV10	DCLK* (MHz)	MODE	DESCRIPTION
OPEN	250	Normal Divide by 2	AData and BData valid on opposite DCLK edges (AData on rise, BData on fall).
GND	50	Test Divide by 10	AData and BData valid on opposite DCLK edges (AData on rise, BData on fall). Data sampled at input CLK rate but 4 out of every 5 samples discarded.

* Input clocks (CLK, $\overline{\text{CLK}}$) = 500MHz for all above combinations. In all modes, the output clock DCLK will be a 50% duty cycle signal.

Data Flow

The MAX101's internal T/H amplifier samples the analog input voltage for the ADC to convert. The T/H is split into two sections that operate on alternate negative clock edges. The input clock, CLK, is conditioned by the T/H and fed to the A/D section. The output clock, DCLK, used for output data timing, will be divided by 2 or 10 from the input clock, CLK (Table 1). This would result in an output data rate of 250Mbps on each output port in normal mode and 50Mbps in test mode. The differential inputs, AIN+ and AIN-, are tracked continuously between data samples. When a negative strobe edge is sensed, one-half of the T/H goes into the hold mode (Figure 4). When the strobe is low, the just-acquired sample is presented to the ADC's input comparators. Internal processing of the sampled data takes an additional 15 clock cycles before it is available at the outputs, AData and BData. See Figures 1-3 for timing.

Applications Information

Analog Input Ranges

Although the normal operating range is $\pm 270\text{mV}$, the MAX101 can be operated with up to $\pm 500\text{mV}$ on each input with respect to ground. This extended input level includes the analog signal and any DC common-mode voltage.

To obtain full-scale digital output with differential input drive, a nominal $+270\text{mV}$ must be applied between AIN+ and AIN-. That is, AIN+ = $+135\text{mV}$ and AIN- = -135mV (with no DC offset). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero-scale digital output code, with differential -270mV drive, occurs when AIN+ = -135mV and AIN- = $+135\text{mV}$. Table 2 shows how the output of the converter stays at all ones (full scale) when over-ranged or all zeros (zero scale) when under-ranged.

500Mps, 8-Bit ADC with Track/Hold

Table 2. Input Voltage Range

INPUT	AIN+ (mV)	AIN- (mV)	OUTPUT CODE	MSB to LSB
Differential	+135	-135	11111111	full scale
	0	0	10000000	mid scale
	-135	+135	00000000	zero scale
Single Ended	+270	0	11111111	full scale
	0	0	10000000	mid scale
	-270	0	00000000	zero scale

* An offset V_{IO} , as specified in the DC electrical parameters, will be present at the input. Compensate for this offset by adjusting the reference voltage. Offsets may be different between side A and side B.

For single-ended operation:

- 1) Apply a DC offset to one of the analog inputs, or leave one input open. (Both AIN+ and AIN- are terminated internally with 50Ω to analog ground.)
- 2) Drive the other input with a $\pm 270\text{mV}$ + offset to obtain either full- or zero-scale digital output. If a DC common-mode offset is used, the total voltage swing allowed is $\pm 500\text{mV}$ (analog signal plus offset with respect to ground).

Reference

The ADC's reference resistor is a Kelvin-sensed, resistor string that sets the ADC's LSB size and dynamic operating range. Normally, the top and bottom of this string are driven with an external buffer amplifier. It will need to supply approximately 21mA due to the 100Ω minimum resistor string impedance. A $\pm 1.02\text{V}$ reference voltage is normally applied to inputs VART, VBRT, VARB, and VBRB. This reference voltage can be adjusted up to $\pm 1.2\text{V}$ to accommodate extended input requirements (accuracy specifications are guaranteed with $\pm 1.02\text{V}$ references). The reference inputs VARTS, VARBS, VBRTS, and VBRBS allow Kelvin sensing of the applied voltages to increase precision.

An RC network at the ADC's reference terminals is needed for best performance. This network consists of a 33Ω resistor connected in series with the buffer output that drives the reference. A $0.47\mu\text{F}$ capacitor must be connected near the resistor at the buffer's output (see *Typical Operating Circuit*). This resistor and capacitor combination should be located within 0.5 inches of the MAX101 package. Any noise on these pins will directly affect the code uncertainty and degrade the ADC's effective bits performance.

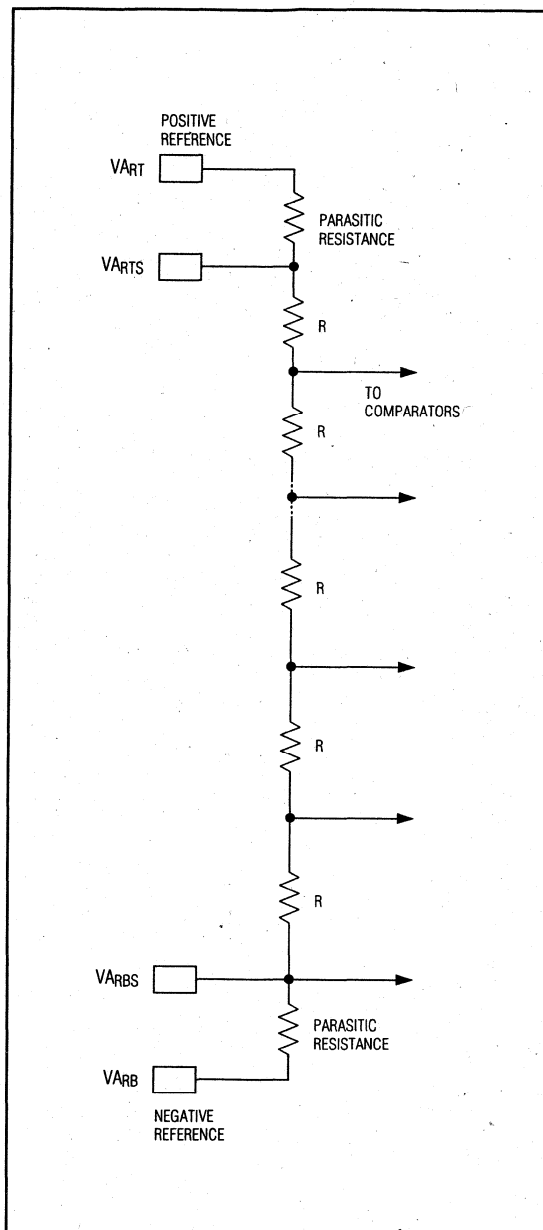


Figure 5. Reference Ladder

500Msps, 8-Bit ADC with Track/Hold

CLK and DCLK

All input and output clock signals are differential. The input clocks, CLK and $\overline{\text{CLK}}$, are the primary timing signals for the MAX101. CLK (pins 2, 62) and $\overline{\text{CLK}}$ (pins 3, 61) are fed to the internal circuitry through an internal 50 Ω transmission line. One set of CLK, $\overline{\text{CLK}}$ inputs should be driven and the other pair terminated by 50 Ω to -2V. Either set of inputs can be used as the driven inputs (input lines are balanced) for easy circuit connection. A minimum pulse width (TPWL) is required for CLK and $\overline{\text{CLK}}$ (Figures 1–3).

For best performance and consistent results, use a low-phase-jitter clock source for CLK and $\overline{\text{CLK}}$. Phase jitter larger than 2ps from the input clock source reduces the converter's effective bits performance and causes inconsistent results. The clock supplied to the MAX101 is internally divided by two, reshaped, and buffered. This divided clock becomes the internal signal used as strobes for the converters.

DCLK and $\overline{\text{DCLK}}$ are output clock signals derived from the input clocks and are used for external timing of the AData and BData outputs. (AData is valid after the rising edge of DCLK and BData is valid after the falling edge.) They are fixed at one-half the rate of the input clocks in normal mode (Table 1). The MAX101 is characterized to work with 500MHz maximum input clock frequencies. See *Typical Operating Circuit*.

Output Mode Control (DIV10)

When DIV10 is grounded, it enables the test mode, where the input incoming clock is divided by ten. This reduces the output data and clock rates by a factor of 5, allowing the output clock duty cycle to remain at 50%. The clock to output phasing remains the same and four out of every five sampled input values are discarded.

When left open, this input (DIV10) is pulled low by internal circuitry and the converter functions in its normal mode.

Layout, Grounding, and Power Supplies

A +5V $\pm 5\%$ supply as well as a -5.2V $\pm 5\%$ supply is needed for proper operation. Bypass the VEE and VCC supply pins to GND with high-quality 0.1 μF and 0.001 μF ceramic capacitors located as close to the package as possible. Connect all ground pins to a ground plane to optimize noise immunity and highest device accuracy.

Phase Adjust

This control pin affects the point in time that one-half of the converter samples the input signal relative to the other half. PHADJ is normally connected to ground (0V), but can be adjusted over a $\pm 1.25\text{V}$ range that typically provides a $\pm 18\text{ps}$ adjustment between the "A" side T/H bridge strobe and the "B" side T/H bridge strobe.

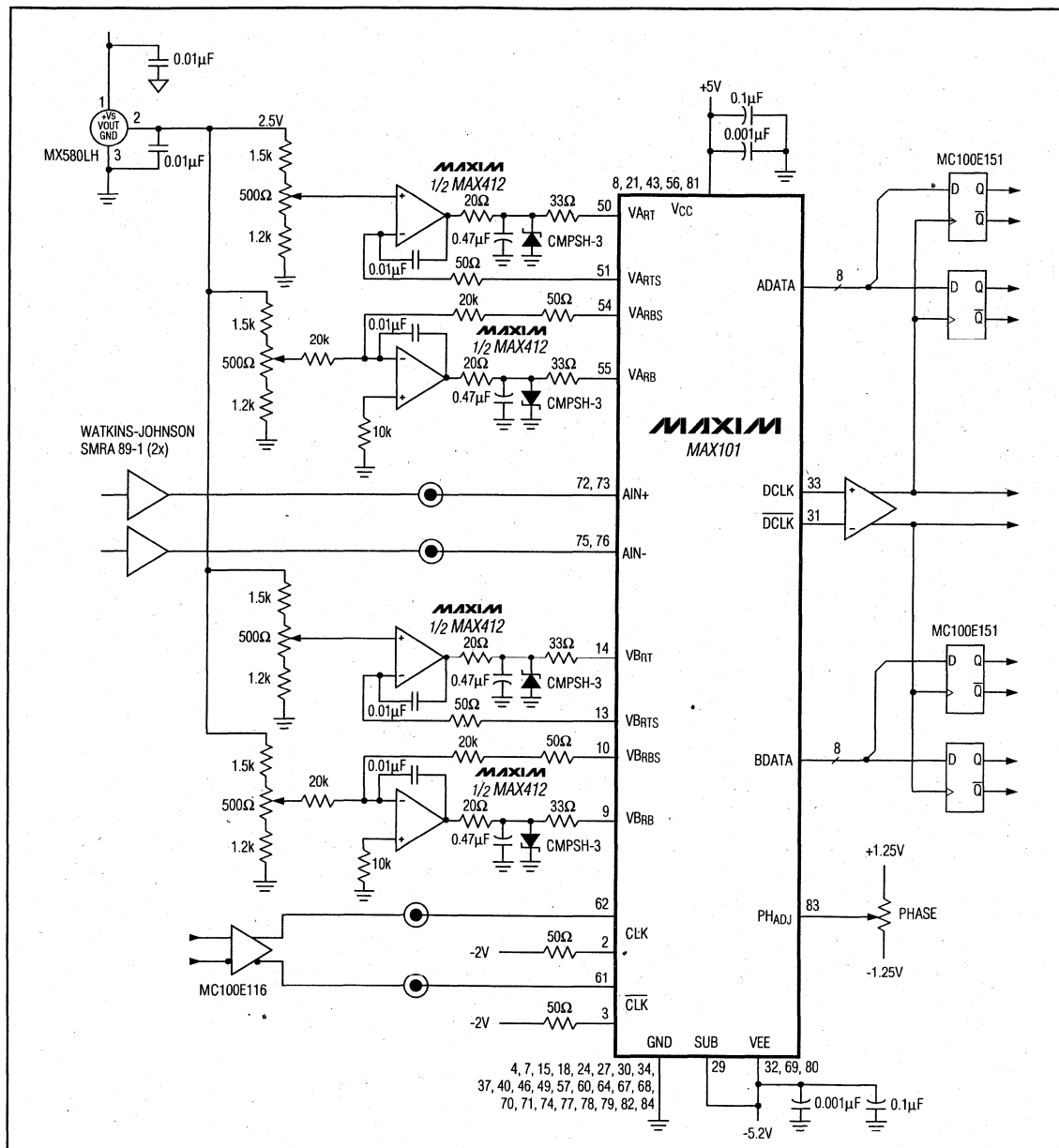
Input Clock Phasing (TRK1, $\overline{\text{TRK1}}$)

At power-up, the clock edge from which AData and BData are synchronized is undetermined. The converter can work from a specific input clock edge, as described in the following paragraph.

TRK1 and $\overline{\text{TRK1}}$ are differential inputs that are used in addition to the normal input clock (CLK) to set data phasing. A signal at one-half the input clock rate with the proper setup and hold times (setup and hold typically 300ps) is applied to these inputs. Choose AData by applying a logic "1" to TRK1 ("0" to $\overline{\text{TRK1}}$) before CLK's negative transition. Choose BData by applying a logic "0" at CLK's negative edge ("1" to $\overline{\text{TRK1}}$). In this manner, several MAX101s can be interleaved to obtain faster effective sampling rates. Voltages at the TRK1 input between $\pm 50\text{mV}$ are interpreted as logic "1" and voltages between -350mV and -500mV are interpreted as logic "0".

500MSPs, 8-Bit ADC with Track/Hold

Typical Operating Circuit



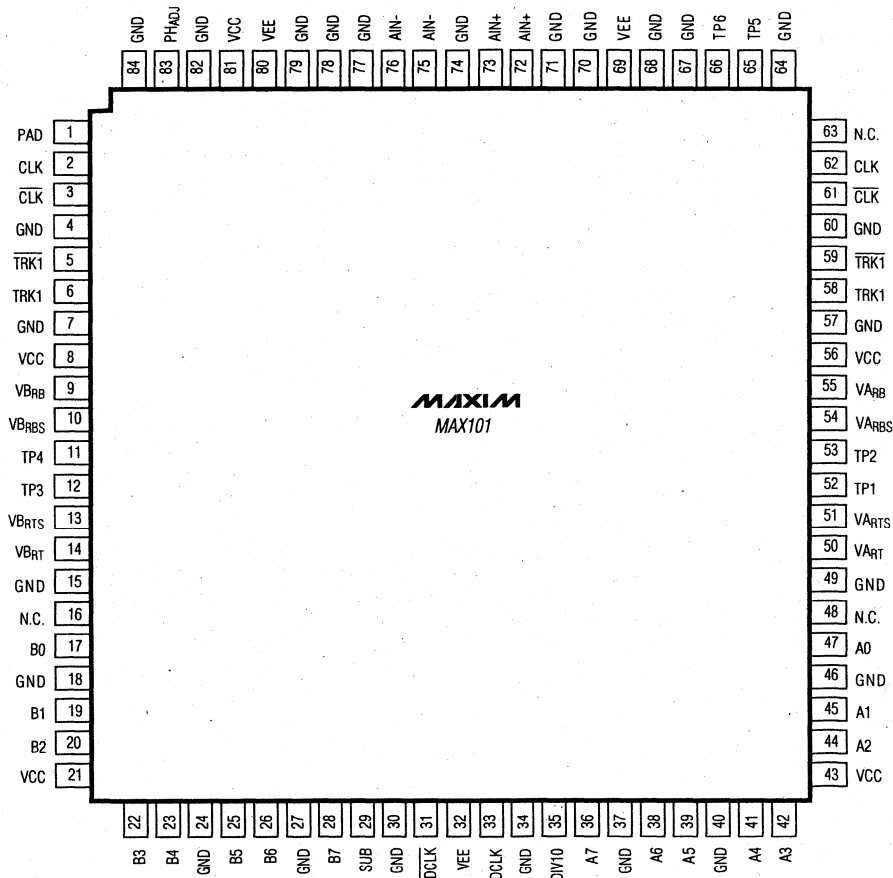
500Msps, 8-Bit ADC with Track/Hold

Pin Configuration

MAX101

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TOP VIEW



Ceramic Flat Pack

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

EVALUATION KIT WILL BE AVAILABLE

MAXIM

1Gps, 8-Bit ADC with Track/Hold

MAX104

General Description

The MAX104 ECL-compatible, 1Gps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 1.5GHz. Designed with Maxim's proprietary advanced GST-2 bipolar process, the MAX104 contains a high-performance track/hold (T/H) amplifier and a quantizer on a single monolithic die.

The innovative design of the internal T/H, which has an exceptionally wide input bandwidth of 1.5GHz, results in high, 7.3 effective bits performance at Nyquist. Special comparator design and decoding circuitry reduce out-of-sequence code errors and provide excellent metastable performance of less than one error per 10^{12} clock cycles. Unlike other ADCs, which can have errors that result in false full-scale or zero-scale outputs, the MAX104 keeps the error magnitude to 1LSB.

The analog input is designed for differential or single-ended use with a 300mV input range. Dual differential ECL-compatible output data paths provide for easy interfacing and include an 8:16 demultiplexer that reduces output data rates to one-half the clock rate. Control inputs are provided for interleaving additional MAX104 devices to increase the effective system sampling rate.

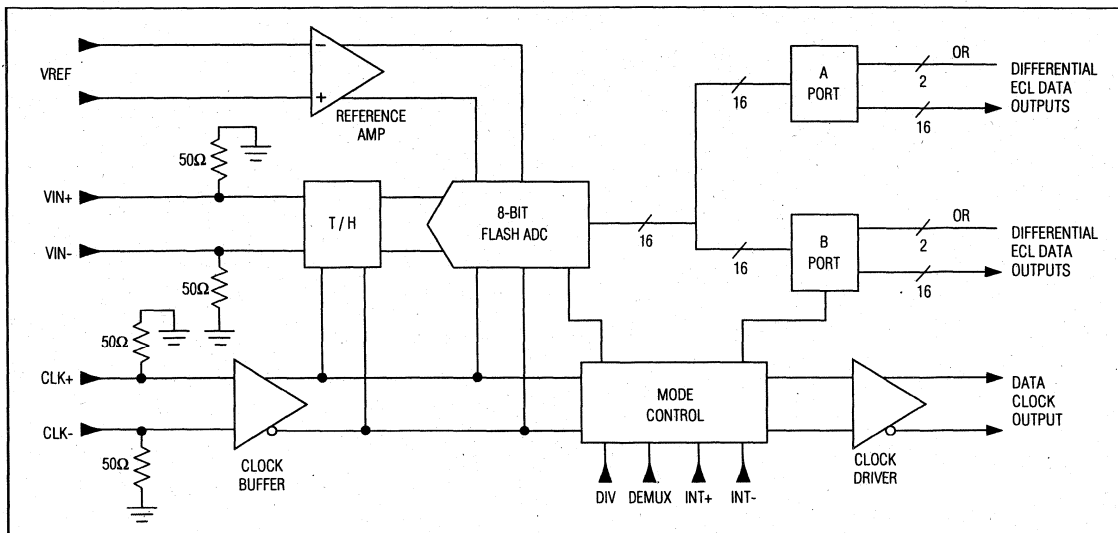
Features

- ◆ 1Gps (min) Conversion Rate
- ◆ 7.3 Effective Bits at 500MHz
- ◆ Less than $\pm 1/2$ LSB DNL and INL
- ◆ 50 Ω Differential Input
- ◆ 300mV Input Signal Range
- ◆ On-Chip Differential Reference Amplifier
- ◆ 3.5W Power Dissipation
- ◆ Latched, ECL-Compatible Differential Outputs with Overrange Bit
- ◆ Low Error Rate, Less than 10^{-12} Metastable States
- ◆ Selectable On-Chip 8:16 Demultiplexer
- ◆ Control Inputs for Interleaving
- ◆ ± 5 V Power Supplies
- ◆ 100-Pin PowerQuad-2 Plastic Package

Applications

Digital RF/IF Signal Processing
High-Speed Data Acquisition
High-Energy Physics
Medical Systems
Radar/Sonar/ECM Systems

Functional Diagram



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MAXIM

Maxim Integrated Products 7-41

Call toll free 1-800-998-8800 for free literature.

EVALUATION KIT
AVAILABLE**MAXIM**

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

General Description

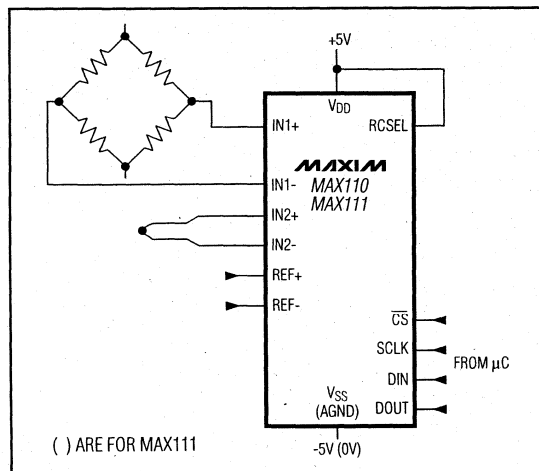
The MAX110/MAX111 analog-to-digital converters (ADCs) use an internal auto-calibration technique to achieve 14-bit resolution plus overrange, with no external components. Operating supply current is only 550 μ A (MAX110) and reduces to 4 μ A in power-down mode, making these ADCs ideal for high-resolution battery-powered or remote-sensing applications. A fast serial interface simplifies signal routing and opto-isolation, saves microcontroller pins, and offers compatibility with SPI™, QSPI™, and Microwire™. The MAX110 operates with ± 5 V supplies, and converts differential analog signals in the -3V to +3V range. The MAX111 operates with a single +5V supply and converts differential analog signals in the ± 1.5 V range, or single-ended signals in the 0V to +1.5V range.

Internal calibration allows for both offset and gain-error correction under microprocessor (μ P) control. Both devices are available in space-saving 16-pin DIP and SO packages, as well as an even smaller 20-pin SSOP package.

Applications

Process Control
Weigh Scales
Panel Meters
Data-Acquisition Systems
Temperature Measurement

Typical Operating Circuit



Features

- ♦ Single +5V Supply (MAX111)
- ♦ Two Differential Input Channels
- ♦ 14-Bit Resolution Plus Sign and Overrange
- ♦ 0.03% Linearity (MAX110)
0.05% Linearity (MAX111)
- ♦ Low Power Consumption:
550 μ A (MAX110)
640 μ A (MAX111)
4 μ A Shutdown Current
- ♦ Up to 50 Conversions/sec
- ♦ 50Hz/60Hz Rejection
- ♦ Auto-Calibration Mode
- ♦ No External Components Required
- ♦ 16-Pin DIP/SO, 20-Pin SSOP

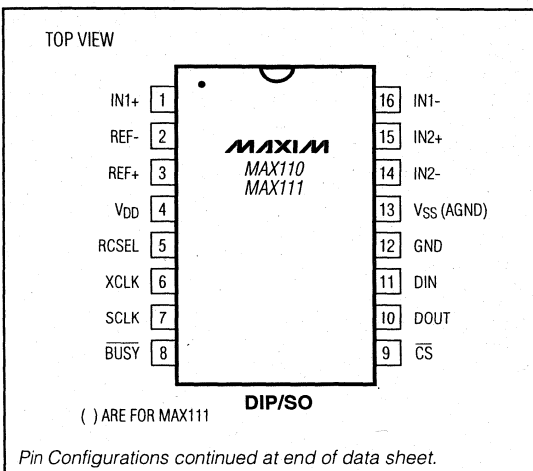
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL(%)
MAX110ACPE	0°C to +70°C	16 Plastic DIP	± 0.03
MAX110BCPE	0°C to +70°C	16 Plastic DIP	± 0.05
MAX110ACWE	0°C to +70°C	16 Wide SO	± 0.03
MAX110BCWE	0°C to +70°C	16 Wide SO	± 0.05
MAX110ACAP	0°C to +70°C	20 SSOP	± 0.03
MAX110BCAP	0°C to +70°C	20 SSOP	± 0.05
MAX110BC/D	0°C to +70°C	Dice*	± 0.05

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

Pin Configurations



Pin Configurations continued at end of data sheet.

™ SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

MAXIM

Maxim Integrated Products 7-43

Call toll free 1-800-722-8266 for free samples or literature.

MAX110/MAX111

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Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

ABSOLUTE MAXIMUM RATINGS

VDD to GND	+6V
VSS to GND (MAX110)	+0.3V to -6V
AGND to DGND	-0.3V to +0.3V
VIN1+, VIN1-	(VDD + 0.3V) to (VSS - 0.3V)
VIN2+, VIN2-	(VDD + 0.3V) to (VSS - 0.3V)
VREF+, VREF-	(VDD + 0.3V) to (VSS - 0.3V)
Digital Inputs and Outputs	(VDD + 0.3V) to -0.3V
Continuous Power Dissipation	
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)	842mW

16-Pin Wide SO (derate 9.52mW/°C above +70°C)	762mW
20-Pin SSOP (derate 8.00mW/°C above +70°C)	640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C)	800mW
Operating Temperature Ranges	
MAX11__C_	0°C to +70°C
MAX11__E_	-40°C to +85°C
MAX11__BMJE	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX110

(VDD = 5V $\pm 5\%$, VSS = -5V $\pm 5\%$, fCLK = 1MHz, +2 mode (DV2 = 1), 81,920 CLK cycles/conv, VREF+ = 1.5V, VREF- = -1.5V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution	RES	(Note 2)		14 + POL + OFL		Bits	
Differential Nonlinearity	DNL	(Notes 3, 4)		±2		LSB	
No-Missing-Codes Resolution		(Note 3)		13 + POL + OFL		Bits	
Relative Accuracy (Notes 3–7)	INL	MAX110AC/E	-VREF ≤ VIN ≤ VREF	±0.03	±0.06	%FSR	
			-0.83 x VREF ≤ VIN ≤ 0.83 x VREF	±0.015	±0.03		
		MAX110BC/E	-VREF ≤ VIN ≤ VREF		±0.08		
			-0.83 x VREF ≤ VIN ≤ 0.83 x VREF		±0.05		
		MAX110BM	-VREF ≤ VIN ≤ VREF		±0.1		
			-0.83 x VREF ≤ VIN ≤ 0.83 x VREF		±0.05		
Offset Error		VIN+ = VIN- = 0V			±4	mV	
Offset Error		After offset null			0.003	µV/°C	
Temperature Drift		Uncalibrated			0.02		
Common-Mode Rejection Ratio	CMRR	-2.5V ≤ (VIN+ = VIN-) ≤ 2.5V			6	ppm/V	
Full-Scale Error		After gain calibration (Note 5)			±0.1	%	
		Uncalibrated		-8	0		
Full-Scale Error Temperature Drift					8	ppm/°C	
Power-Supply Rejection		VSS = -5V, VDD = 4.75V to 5.25V			15	ppm	
		VDD = 5V, VSS = -4.75V to -5.25V			30		
ANALOG INPUTS							
Differential Input Voltage Range	VIN	(Note 6)		-VREF	+VREF	V	
Absolute Input Voltage Range	VIN+, VIN-			VSS + 2.25	VDD - 2.25	V	
Input Bias Current	IIN+, IIN-				500	nA	
Input Capacitance		(Note 3)			10	pF	

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

ELECTRICAL CHARACTERISTICS—MAX110 (continued)

($V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $f_{CLK} = 1\text{MHz}$, +2 mode ($DV2 = 1$), 81,920 CLK cycles/conv, $V_{REF+} = 1.5V$, $V_{REF-} = -1.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUTS						
Differential Reference Input Voltage Range	V_{REF}		0		3.0	V
Absolute Reference Input Voltage Range	V_{REF+} , V_{REF-}		$V_{SS} + 2.25$		$V_{DD} - 2.25$	V
Reference Input Current	I_{REF+} , I_{REF-}	$V_{REF+} = 2.5V$, $V_{REF-} = 0V$			500	nA
Reference Input Capacitance		(Note 3)			10	pF
CONVERSION TIME						
Synchronous Conversion Time (Note 7)	t_{CONV}	10,240 clock-cycles/conversion		20.48		ms
		102,400 clock-cycles/conversion		204.80		
Oversampling Clock Frequency	f_{OSC}	(Note 8)	0.25		1.25	MHz
DIGITAL INPUTS ($\overline{CS}$, $SCLK$, DIN , and $XCLK$ when $RCSEL = 0V$)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Capacitance		(Note 3)			10	pF
Input Leakage Current	I_{LKG}	Digital inputs at 0V or 5V			± 1	μA
DIGITAL OUTPUTS ($DOUT$, $BUSY$, and $XCLK$ when $RCSEL = V_{DD}$)						
Output Low Voltage	V_{OL}	$DOUT$, $BUSY$, $I_{SINK} = 1.6\text{mA}$			0.4	V
		$XCLK$, $I_{SINK} = 200\mu\text{A}$			0.4	
Output High Voltage	V_{OH}	$DOUT$, $BUSY$, $V_{DD} = 4.75V$, $I_{SOURCE} = 1.0\text{mA}$	$V_{DD} - 0.5$			V
		$XCLK$, $V_{DD} = 4.75V$, $I_{SOURCE} = 200\mu\text{A}$	$V_{DD} - 0.5$			
Leakage Current	I_{LKG}	$V_{OUT} = 5V$ or $0V$			± 10	μA
Output Capacitance		(Note 3)			10	pF
POWER REQUIREMENTS (all digital inputs at 0V or 5V)						
Positive Supply Voltage	V_{DD}	Performance guaranteed by supply rejection test	4.75		5.25	V
Negative Supply Voltage	V_{SS}	Performance guaranteed by supply rejection test	-4.75		-5.25	V
Positive Supply Current	I_{DD}	$V_{DD} = 5.25V$, $V_{SS} = -5.25V$ $f_{CLK} = 500\text{kHz}$, continuous-conversion mode $XCLK$ unloaded, continuous-conversion mode, RC oscillator operational (Note 9)		550	950	μA
				780		
Negative Supply Current	I_{SS}	$V_{DD} = 5.25V$, $V_{SS} = -5.25V$ $f_{CLK} = 500\text{kHz}$, continuous-conversion mode		320	650	μA
Power-Down Current	I_{DD}	$V_{DD} = 5.25V$, $V_{SS} = -5.25V$, $V_{XCLK} = 0V$, $PD = 1$		4	10	μA
	I_{SS}			0.05	2	

MAX110/MAX111

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Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

ELECTRICAL CHARACTERISTICS—MAX111

($V_{DD} = 5V \pm 5\%$, $f_{XCLK} = 1MHz$, ± 2 mode ($DV2 = 1$), 81,920 CLK cycles/conv, $V_{REF+} = 1.5V$, $V_{REF-} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution	RES	(Note 2)		14 + POL + OFL			Bits
Differential Nonlinearity	DNL	(Notes 3, 4)		±2			LSB
No-Missing-Codes Resolution		(Note 3)		13 + POL + OFL			Bits
Relative Accuracy, Differential Input (Notes 3–7)	INL	MAX111AC/E	-VREF ≤ VIN ≤ VREF	±0.05 ±0.10		%FSR	
			-0.667 x VREF ≤ VIN ≤ 0.667 x VREF	±0.03 ±0.05			
		MAX111BC/E	-VREF ≤ VIN ≤ VREF	±0.18			
			-0.667 x VREF ≤ VIN ≤ 0.667 x VREF	±0.10			
		MAX111BM	-VREF ≤ VIN ≤ VREF	±0.25			
			-0.667 x VREF ≤ VIN ≤ 0.667 x VREF	±0.20			
Relative Accuracy, Single-Ended Input (IN- = GND)	INL	MAX111AC/E	0V ≤ VIN ≤ VREF	±0.1		%FSR	
			VIN ≤ 0.667 x VREF	±0.06			
		MAX111BC/E	0V ≤ VIN ≤ VREF	±0.18			
			VIN ≤ 0.667 x VREF	±0.10			
		MAX111BM	0V ≤ VIN ≤ VREF	±0.25			
			VIN ≤ 0.667 x VREF	±0.15			
Offset Error		VIN+ = VIN- = 0V				±4	mV
Common-Mode Rejection Ratio	CMRR	10mV ≤ (VIN+ = VIN-) ≤ 2.0V		6			ppm/V
Full-Scale Error		After gain calibration (Note 5)				±0.2	%
		Uncalibrated		-8		0	
Full-Scale Error Temperature Drift				8			ppm/°C
Power-Supply Rejection		VDD = 4.75V to 5.25V		15			ppm
ANALOG INPUTS							
Differential Input Voltage Range	VIN	(Note 6)		-VREF		+VREF	V
Absolute Input Voltage Range	VIN+, VIN-			0		VDD - 3.2	V
Input Bias Current	IIN+, IIN-					500	nA
Input Capacitance		(Note 3)				10	pF

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

ELECTRICAL CHARACTERISTICS—MAX111 (continued)

($V_{DD} = 5V \pm 5\%$, $f_{CLK} = 1MHz$, $\div 2$ mode ($DV2 = 1$), 81,920 CLK cycles/conv, $V_{REF+} = 1.5V$, $V_{REF-} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUTS						
Differential Reference Input Voltage Range	V_{REF}		0		1.5	V
Absolute Reference Input Voltage Range	V_{REF+} , V_{REF-}		0		$V_{DD} - 3.2$	V
Reference Input Current	I_{REF+} , I_{REF-}	$V_{REF+} = 2.5V$, $V_{REF-} = 0V$			500	nA
Reference Input Capacitance		(Note 3)			10	pF
CONVERSION TIME						
Synchronous Conversion Time (Note 7)	t_{CONV}	10,240 clock-cycles/conversion		20.48		ms
		102,400 clock-cycles/conversion		204.80		
Oversampling Clock Frequency	f_{OSC}	(Note 8)	0.25		1.25	MHz
DIGITAL INPUTS ($\overline{CS}$, $SCLK$, DIN , and $XCLK$ when $RCSEL = 0V$)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Capacitance		(Note 3)			10	pF
Input Leakage Current	I_{LKG}	Digital inputs at 0V or 5V			± 1	μA
DIGITAL OUTPUTS ($DOUT$, $BUSY$, and $XCLK$ when $RCSEL = V_{DD}$)						
Output Low Voltage	V_{OL}	$DOUT$, $BUSY$, $I_{SINK} = 1.6mA$			0.4	V
		$XCLK$, $I_{SINK} = 200\mu A$			0.4	
Output High Voltage	V_{OH}	$DOUT$, $BUSY$, $V_{DD} = 4.75V$, $I_{SOURCE} = 1.0mA$	$V_{DD} - 0.5$			V
		$XCLK$, $V_{DD} = 4.75V$, $I_{SOURCE} = 200\mu A$	$V_{DD} - 0.5$			
Leakage Current	I_{LKG}	$V_{OUT} = 5V$ or $0V$			± 10	μA
Output Capacitance		(Note 3)			10	pF
POWER REQUIREMENTS (all digital inputs at 0V or 5V)						
Positive Supply Voltage	V_{DD}	Performance guaranteed by supply rejection test	4.75		5.25	V
Supply Current	I_{DD}	$V_{DD} = 5.25V$	$f_{CLK} = 500kHz$, continuous-conversion mode	640	1200	μA
			$XCLK$ unloaded, continuous-conversion mode, RC oscillator operational (Note 9)	960		
Power-Down Current	I_{DD}	$V_{DD} = 5.25V$, $V_{XCLK} = 0V$, $PD = 1$		4	10	μA

MAX110/MAX111

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Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

- Note 1:** These specifications apply after auto-null and gain calibration. Performance at power-supply tolerance limits is guaranteed by power-supply rejection tests. Tests are performed at $V_{DD} = 5V$ and $V_{SS} = -5V$ (MAX1110).
- Note 2:** 32,768 LSBs cover an input voltage range of $\pm V_{REF}$ (15 bits). An additional bit (OFL) is set for $V_{IN} > V_{REF}$.
- Note 3:** Guaranteed by design. Not subject to production testing.
- Note 4:** DNL is less than ± 2 counts (LSBs) out of 2^{15} counts (± 14 bits). The major source of DNL is noise, and this can be further improved by averaging.
- Note 5:** See *3-Step Calibration* section in text.
- Note 6:** $V_{REF} = (V_{REF+} - V_{REF-})$, $V_{IN} = (V_{IN1+} - V_{IN1-})$ or $(V_{IN2+} - V_{IN2-})$. The voltage is interpreted as negative when the voltage at the negative input terminal exceeds the voltage at the positive input terminal.
- Note 7:** Conversion time is set by control bits CONV1–CONV4.
- Note 8:** Tested at clock frequency of 1MHz with the divide-by-2 mode (i.e. oversampling clock of 500kHz). See *Typical Operating Characteristics* section for the effect of other clock frequencies. Also read the *Clock Frequency* section.
- Note 9:** This current depends strongly on $CXCLK$ (see *Applications Information* section).

TIMING CHARACTERISTICS (see Figure 6)

($V_{DD} = 5V$, $V_{SS} = -5V$ (MAX110), $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

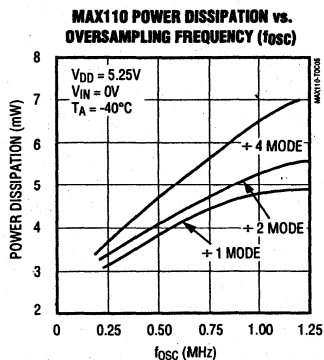
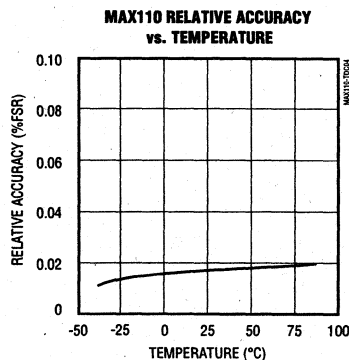
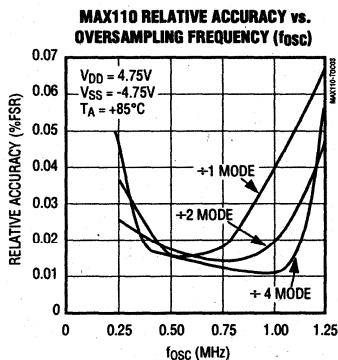
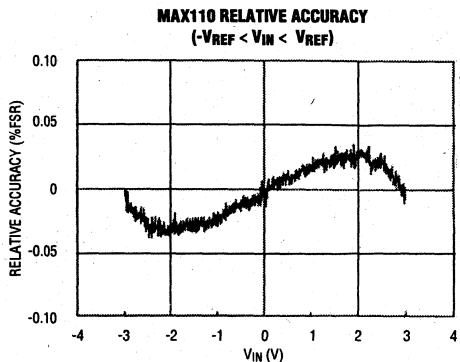
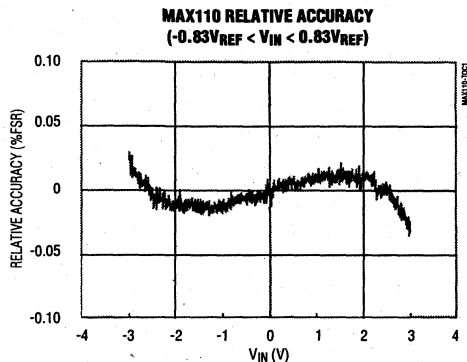
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ to SCLK Setup Time (Note 10)	t _{CS}	$T_A = +25^\circ C$		60			ns
		MAX11__C/E		80			
		MAX11__BM		100			
$\overline{CS}$ to SCLK Hold Time (Note 10)	t _{CSH}			0			ns
DIN to SCLK Setup Time (Note 10)	t _{DS}	$T_A = +25^\circ C$		60			ns
		MAX11__C/E		80			
		MAX11__BM		100			
DIN to SCLK Hold Time (Note 10)	t _{DH}			0			ns
SCLK, XCLK Pulse Width (Note 10)	t _{CK}	$T_A = +25^\circ C$		100			ns
		MAX11__C/E		120			
		MAX11__BM		160			
Data Access Time (Note 10)	t _{DA}	$C_{LOAD} = 50pF$	$T_A = +25^\circ C$	0	35	80	ns
			MAX11__C/E	0		100	
			MAX11__BM	0		120	
SCLK to DOUT Valid Delay (Note 10)	t _{DO}	$C_{LOAD} = 50pF$	$T_A = +25^\circ C$	0	60	100	ns
			MAX11__C/E	0		120	
			MAX11__BM	0		140	
Bus Relinquish Time (Note 10)	t _{DH}	$T_A = +25^\circ C$			35	80	ns
		MAX11__C/E/M				120	
RC Oscillator Frequency		$T_A = +25^\circ C$			2.0		MHz
		MAX11__C/E		1.3		2.8	
		MAX11__BM		1.1		3.0	

Note 10: Timing specifications are sample tested at $+25^\circ C$ to ensure compliance. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of $+5V$) and timed from a $+1.6V$ voltage level.

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

Typical Operating Characteristics

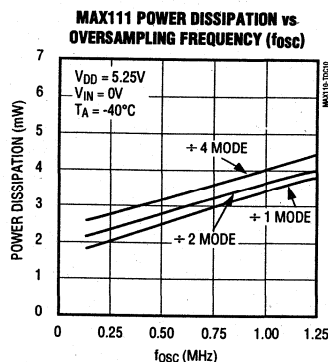
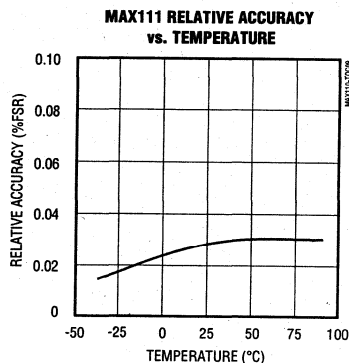
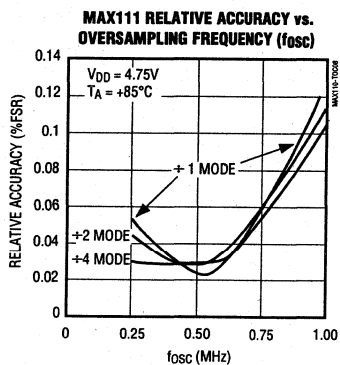
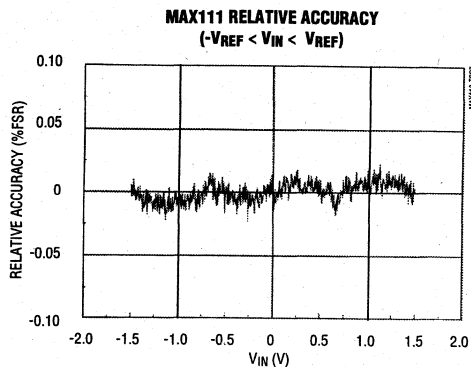
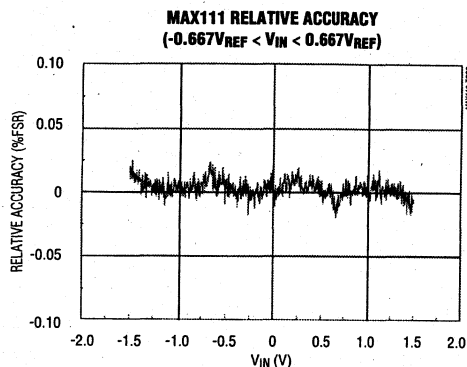
(MAX110, $V_{DD} = 5V$, $V_{SS} = -5V$, $V_{REF+} = 1.5V$, $V_{REF-} = -1.5V$, differential input ($V_{IN+} = -V_{IN-}$), $f_{CLK} = 1MHz$, $\div 2$ mode ($DV2 = 1$), 81,920 clocks/conv, $T_A = +25^\circ C$, unless otherwise noted.)



Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

Typical Operating Characteristics (continued)

(MAX1111, $V_{DD} = 5V$, $V_{REF+} = 1.5V$, $V_{REF-} = 0V$, differential input ($V_{IN+} = -V_{IN-}$), $f_{CLK} = 1MHz$, $\div 2$ mode ($DV2 = 1$), 81,920 clocks/conv, $T_A = +25^\circ C$, unless otherwise noted.)



Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

Pin Description

MAX110/MAX111

PIN		NAME	FUNCTION
DIP/SO	SSOP		
1	1	IN1+	Channel 1 Positive Analog Input
2	2	REF-	Negative Reference Input
3	3	REF+	Positive Reference Input
4	6	V _{DD}	Positive Power-Supply Input—connect to +5V
5	7	RCSEL	RC Select Input. Connect to GND to select external clock mode. Connect to V _{DD} to select RC OSC mode.
6	8	XCLK	Clock Input / RC Oscillator Output. TTL/CMOS-compatible oversampling clock input when RCSEL = GND. Connects to the internal RC oscillator when RCSEL = V _{DD} .
7	9	SCLK	Serial Clock Input. TTL/CMOS-compatible clock input for serial-interface data I/O.
8	10	BUSY	Busy Output. Goes low at conversion start, and returns high at end of conversion.
9	11	$\overline{CS}$	Chip-Select Input. Pull this input low to perform a control-word-write/data-read operation. A conversion begins when $\overline{CS}$ returns high, provided NO-OP is a 1. See the section <i>Using the MAX110/MAX111 with SPI, QSPI, and Microwire Serial Interfaces</i> .
10	12	DOUT	Serial Data Output. High-impedance when $\overline{CS}$ is high.
11	13	DIN	Serial Data Input. See <i>Control Register</i> section.
12	16	GND	Digital Ground
13	17	V _{SS}	MAX110 Negative Power-Supply Input—connect to -5V
		AGND	MAX111 Analog Ground
14	18	IN2-	Channel 2 Negative Analog Input
15	19	IN2+	Channel 2 Positive Analog Input
16	20	IN1-	Channel 1 Negative Analog Input
—	4, 5, 14, 15	N.C.	No Connect—there is no internal connection to this pin

Detailed Description

The MAX110/MAX111 ADC converts low-frequency analog signals to a 16-bit serial digital output (14 data bits, a sign bit, and an overrange bit) using a first-order sigma-delta loop (Figure 1). The differential input voltage is internally connected to a precision voltage-to-current converter. The resulting current is integrated and applied to a comparator. The comparator output then drives an up/down counter and a 1-bit DAC. When the DAC output is fed back to the integrator input, the sigma-delta loop is completed.

During a conversion, the comparator output is a V_{REF-} to V_{REF+} square wave; its duty cycle is proportional to the magnitude of the differential input voltage applied

to the ADC. The up/down counter clocks data in from the comparator at the oversampling clock rate and averages the pulse-width-modulated (PWM) square wave to produce the conversion result. A 16-bit static shift register stores the result at the end of the conversion. Figure 2 shows the ADC waveforms for a differential analog input equal to $1/2 (V_{REF+} - V_{REF-})$. The resulting comparator and 1-bit DAC outputs are high for seven cycles and low for three cycles of the oversampling clock.

Since the analog input signal is integrated over many clock cycles, much of the signal and quantization noise is attenuated. The more clock cycles allowed during each conversion, the greater the noise attenuation (see *Programming Conversion Time*).

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

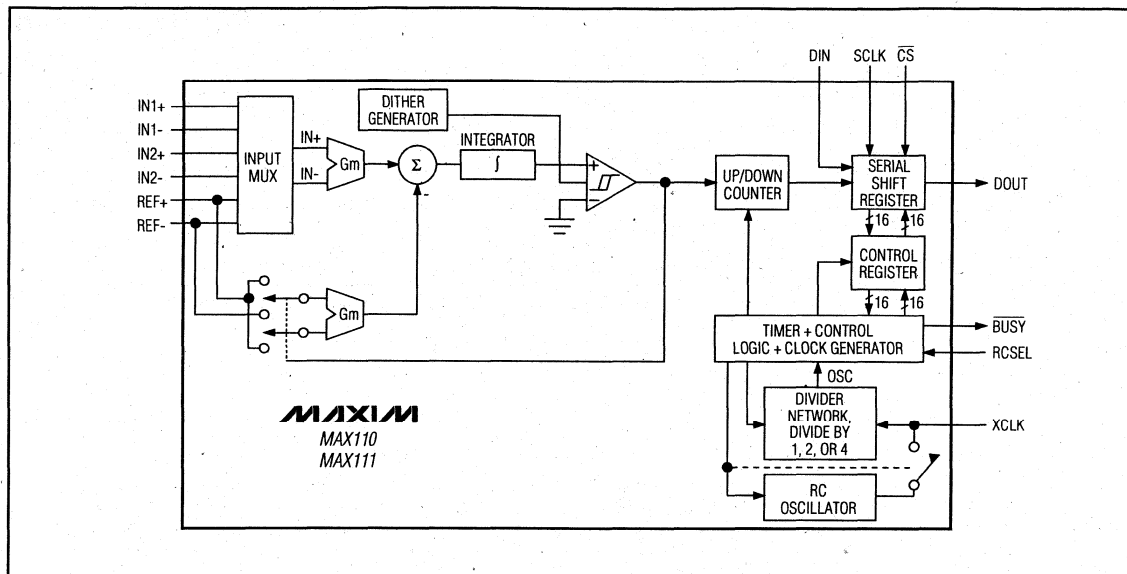


Figure 1. Functional Diagram

Oversampling Clock

XCLK internally connects to a clock-frequency divider network, whose output is the ADC oversampling clock, f_{OSC} . This allows the selected clock source (internal RC oscillator or external clock applied to XCLK) to be divided by one, two, or four (see *Clock Divider-Ratio Control Bits*).

Figure 3 shows the two methods for providing the oversampling clock to the MAX110/MAX111. In external-clock mode (Figure 3a), the internal RC oscillator is disabled and XCLK accepts a TTL/CMOS-level clock to provide the oversampling clock to the ADC.

Select external-clock mode (Figure 3a) by connecting RCSEL to GND and a TTL/CMOS-compatible clock to XCLK (see *Selecting the Oversampling Clock Frequency*).

In RC-oscillator mode (Figure 3b), the internal RC oscillator is active and its output is connected to XCLK (Figure 1). Select RC-oscillator mode by connecting RCSEL to V_{DD} . This enables the internal oscillator and connects it to XCLK for use by the ADC and external system components. Minimize the capacitive loading on XCLK when using the internal RC oscillator.

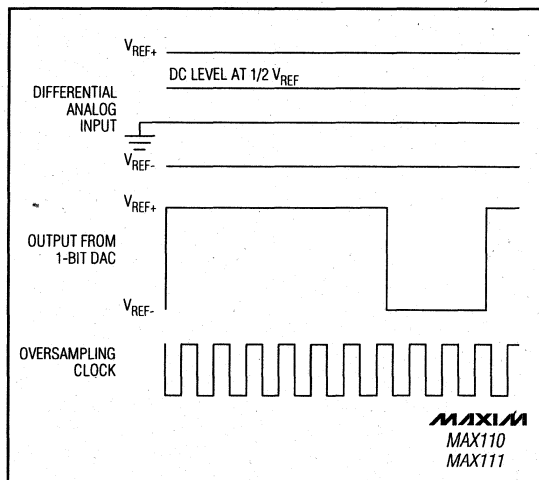


Figure 2. ADC Waveforms During a Conversion

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

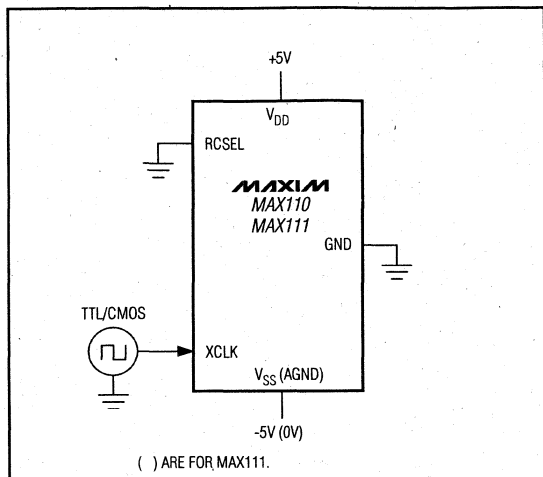


Figure 3a. Connection for External-Clock Mode

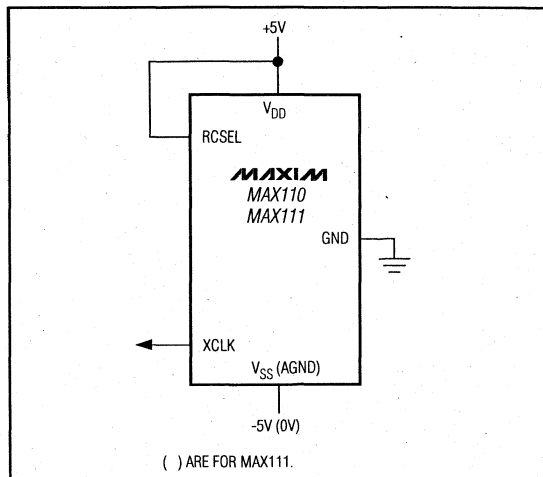


Figure 3b. Connection for Internal RC-Oscillator Mode—XCLK connects to the internal RC oscillator

ADC Operation

The output data from the MAX110/MAX111 is arranged in two's-complement format (Figures 4, 5). The sign bit (POL) is shifted out first, followed by the overrange bit (OR), and the 14 data bits (MSB first) (see Figure 6). The MAX110 operates from $\pm 5V$ power supplies and converts low-frequency analog signals in the $\pm 3V$ range when using the maximum reference voltage of $V_{REF} = 3V$ ($V_{REF} = V_{REF+} - V_{REF-}$). Within the $\pm 3V$ input range, greater accuracy is obtained within $\pm 2.5V$ (see *Electrical Characteristics* for details). Note that a negative input voltage is defined as $V_{IN-} > V_{IN+}$. For the MAX110, the absolute voltage at any analog input pin must remain within the $(V_{SS} + 2.25V)$ to $(V_{DD} - 2.25V)$ range.

The MAX111 operates from a single $+5V$ supply and converts low-frequency differential analog signals in the $\pm 1.5V$ range when using the maximum reference voltage of $V_{REF} = 1.5V$. As indicated in the *Electrical Characteristics*, greater accuracy is achieved within the $\pm 1.2V$ range. The absolute voltage at any analog input pin for the MAX111 must remain within $0V$ to $V_{DD} - 3.2V$. When $V_{IN-} > V_{IN+}$ the input is interpreted as negative.

The overrange bit (OFL) is provided to sense when the input voltage level has exceeded the reference voltage

level. The converter does not "saturate" until the input voltage is typically 20% larger. The linearity is not guaranteed in this range. Note that the overrange bit works properly if the reference voltage remains within the recommended voltage range (see *Reference Inputs*). If the reference voltage exceeds the recommended input range, the overrange bit may not operate properly.

Digital Interface—Starting a Conversion

Data is transferred into and out of the serial I/O shift register by pulling $\overline{CS}$ low and applying a serial clock at SCLK. This fully static shift register allows SCLK to range from DC to 2MHz. Output data from the ADC is clocked out on SCLK's falling edge and should be read on SCLK's rising edge. Input data to the ADC at DIN is clocked in on SCLK's rising edge. A new conversion begins when $\overline{CS}$ returns high, provided the MSB in the input control word (NO-OP) is a 1 (see *Using the MAX110/MAX111 with Microwire, SPI, and QSPI Serial Interfaces*). Figure 6 shows the detailed serial-interface timing diagram.

$\overline{CS}$ must remain high during the conversion (while $\overline{BUSY}$ remains low). Bringing $\overline{CS}$ low during the conversion causes the ADC to stop converting, and may result in erroneous output data.

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

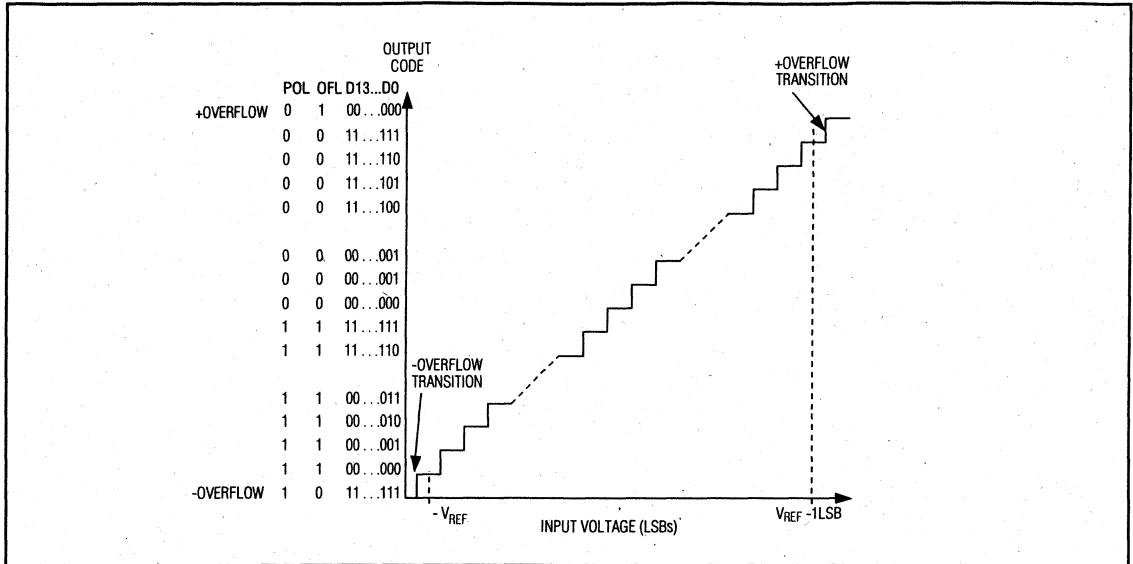


Figure 4. Differential Transfer Function

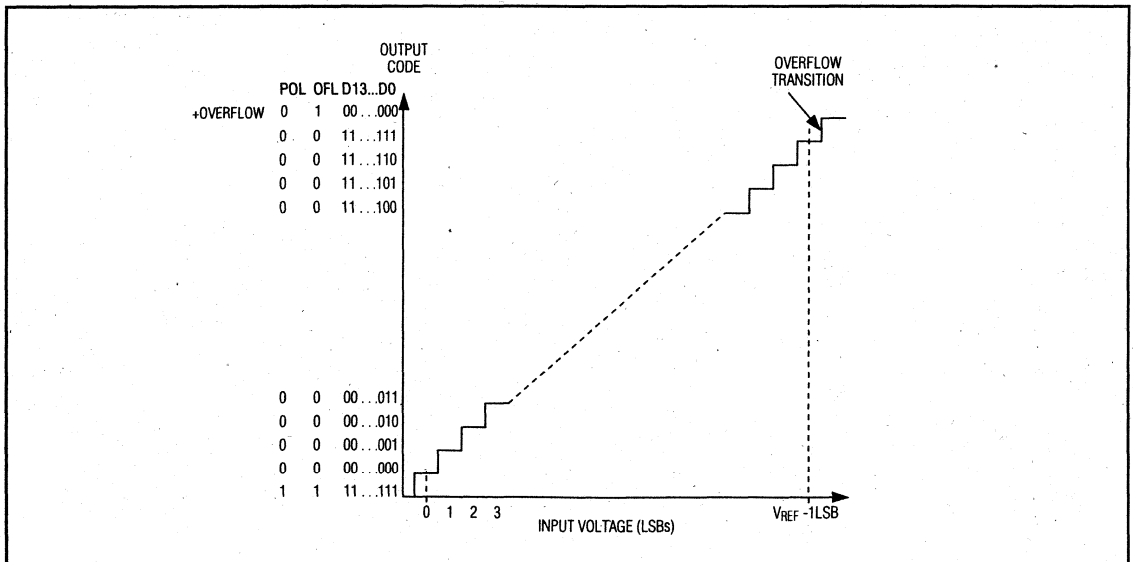


Figure 5. Unipolar Transfer Function

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

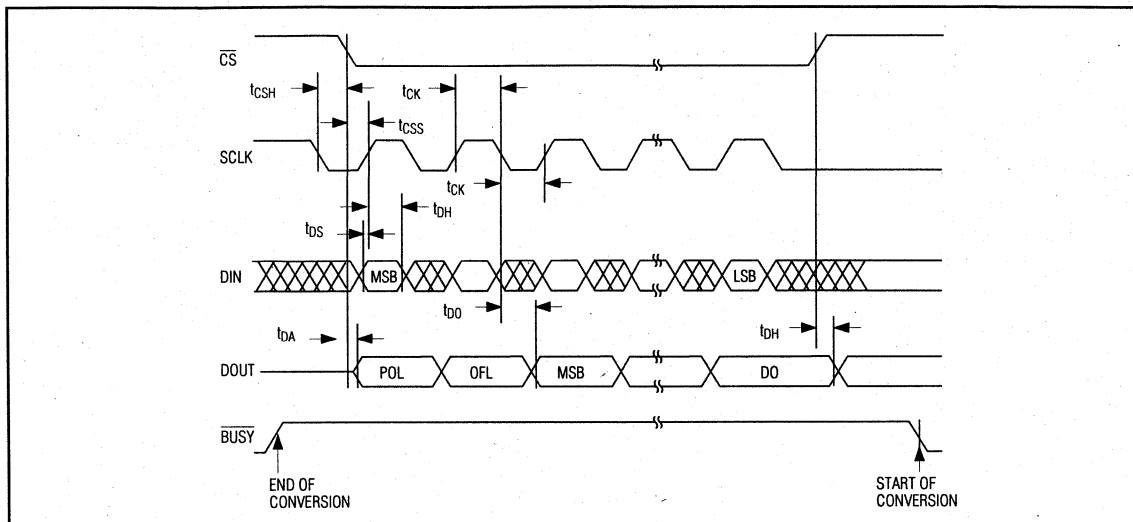


Figure 6. Detailed Serial-Interface Timing

Using the MAX110/MAX111 with SPI, QSPI, and Microwire Serial Interfaces

Figure 7 shows the most common serial-interface connections. The MAX110/MAX111 are compatible with SPI, QSPI (CPHA = 0, CPOL = 0), and Microwire serial-interface standards.

The ADC serial interface operates with just SCLK, DIN, and DOUT (allow sufficient time for the conversion to complete between read/write operations). Achieve continuous operation by connecting BUSY to an uncommitted μP I/O or interrupt, to signal the processor when the conversion results are ready. Figures 8a and 8b show the timing for SPI/Microwire and QSPI operation.

The fully static 16-bit I/O register allows infinite time between the two 8-bit read/write operations necessary to obtain the full 16 bits of data with SPI and Microwire. CS must remain low during the entire two-byte transfer (Figure 8a). QSPI allows a full 16-bit data transfer (Figure 8b).

Interfacing to the 80C32 Microcontroller Family

Figure 7c shows the general 80C32 connection to the MAX110/MAX111 using Port 1. For a more detailed discussion, see the MAX110 evaluation kit manual.

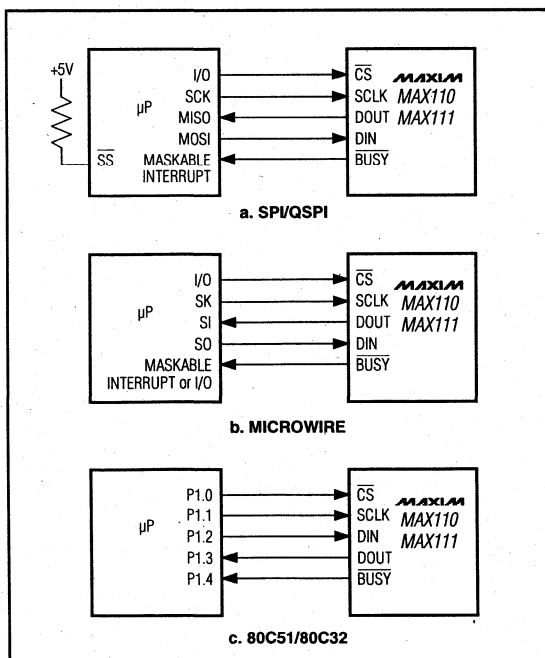


Figure 7. Common Serial-Interface Connections

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

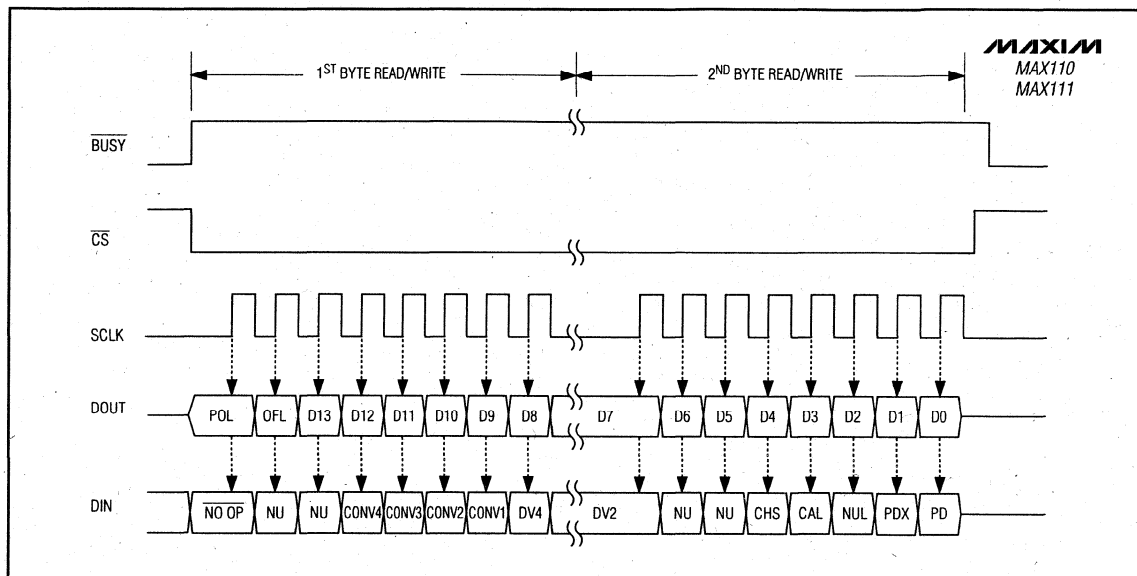


Figure 8a. SPI/Microwire-Interface Timing

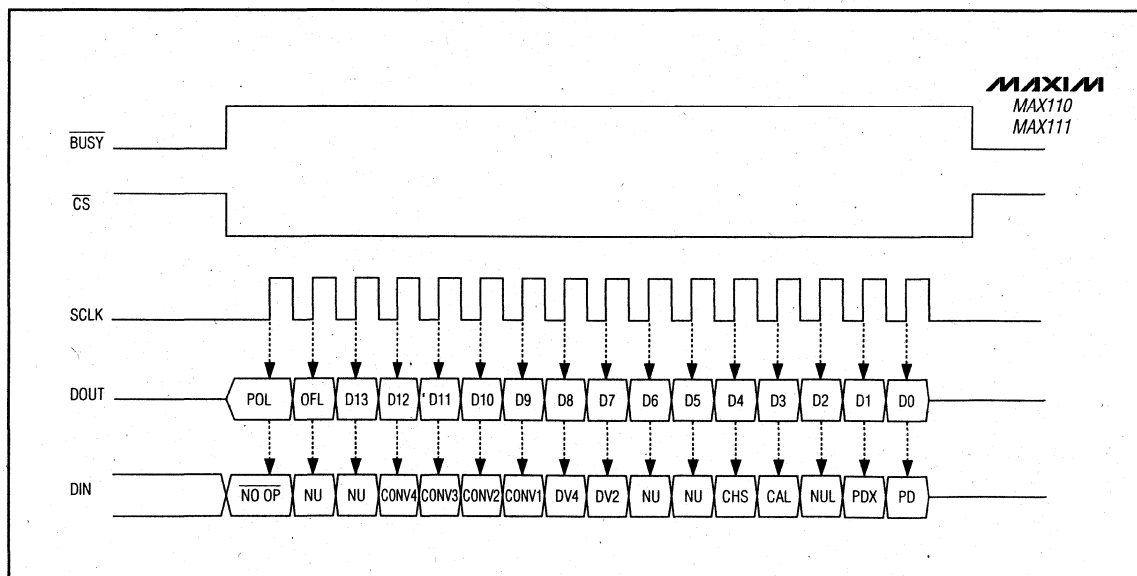


Figure 8b. QSPI Serial-Interface Timing

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Table 1. Input Control-Word Bit Map

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NO-OP	NU	NU	CONV4	CONV3	CONV2	CONV1	DV4	DV2	NU	NU	CHS	CAL	NUL	PDX	PD

↑
First bit clocked in.

BIT	NAME	DESCRIPTION
15	NO-OP	If this bit is a logic high, the remaining 15 LSBs are transferred to the control register and a new conversion begins when $\overline{CS}$ returns high. If this bit is set low, the control word is not passed to the control register, the ADC configuration remains unchanged, and no new conversion begins when $\overline{CS}$ returns high.
5, 6, 13, 14	NU	Used for test purposes only. Set these bits low.
9–12	CONV1–CONV4	Conversion Time Control Bits. See Table 4.
7, 8	DV2, DV4	XCLK to Oversampling Cock Ratio Control Bits. See Table 5.
4	CHS	Input Channel Select. A logic high selects channel 2 (IN2+ and IN2-), while a logic low selects channel 1 (IN1+ and IN1-). See Tables 2 and 3.
3	CAL	Gain-Calibration Bit. A logic high selects gain-calibration mode. See Table 3.
2	NUL	Internal Offset-Null Bit. A logic high selects offset-null mode. See Table 3.
1	PDX	Oscillator Power-Down. Set this bit high to power down the RC oscillator.
0	PD	Analog Power-Down. Set this bit high to power down the analog section.

I/O Shift Register

Serial data transfer is accomplished with a 16-bit fully static shift register. The 16-bit control word shifted into this register during a data-transfer operation controls the ADC's various functions. The MSB (NO-OP) enables/disables transfer of the control word within the ADC. A logic 1 causes the remaining 15 bits in the control word to be transferred from the I/O register into the control register when $\overline{CS}$ goes high, updating the ADC's configuration and starting a new conversion. If NO-OP is a zero, the control word is not transferred to the control register, the ADC's configuration remains unchanged, and no new conversion is initiated. This allows specific ADCs in a "daisy chain" arrangement to be reconfigured while leaving the remaining ADCs unchanged. Table 1 lists the various ADC control word functions.

Output data is shifted out of DOUT at the same time the input control word for the next conversion is shifted in (Figure 8).

On power-up, all internal registers reset to zero. Therefore, when writing the first control word to the ADC, the data simultaneously shifted out will be zeros. The first conversion begins when $\overline{CS}$ goes high (NO-OP = 1). The results are placed in the 16-bit I/O register for access on the next data-transfer operation.

Power-Down Mode

Bits 0 and 1 control the ADC's power-down mode. If bit 0 (PD) is a logic high, power is removed from all analog circuitry except the RC oscillator. A logic high at bit 1 (PDX) removes power from the RC oscillator. If both bits PD and PDX are a logic high, or if PD is high and RCSEL is low (external clock mode selected), the supply currents reduce to 4 μ A. If an external XCLK clock continues to run in power-down mode, the supply current will depend on the clock rate.

When PDX is set high, the internal RC oscillator stops shortly after $\overline{CS}$ returns high and $\overline{BUSY}$ goes low. Because the RC oscillator is stopped, $\overline{BUSY}$ remains low and does not allow a new conversion to begin. To reset $\overline{BUSY}$ high, write a "dummy" control word with NO-OP = 0 and use any combination for bits 14–0. With NO-OP = 0, bits 14–0 are ignored and $\overline{BUSY}$ will return high when $\overline{CS}$ returns high. Set NO-OP high and PDX to zero in the next control word to start the RC oscillator and perform a new conversion.

Selecting the Analog Inputs

Bit 4 (CHS) controls which of the two differential inputs connect to the internal ADC inputs (see the *Functional Diagram*). A logic high selects IN2+ and IN2- while a logic low selects IN1+ and IN1-. Table 2 shows the allowable input multiplexer configurations.

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Table 2. Allowable Input Multiplexer Configurations

CAL	NUL	CHS	NO-OP	ADC IN+	ADC IN-	DESCRIPTION
0	0	0	1	IN1+	IN1-	Channel 1 connected to ADC inputs. Conversion begins when $\overline{CS}$ returns high.
0	0	1	1	IN2+	IN2-	Channel 2 connected to ADC inputs. Conversion begins when $\overline{CS}$ returns high.
0	1	0	1	IN1-	IN1-	IN1- connected to the ADC inputs; offset-null mode selected. Autonull conversion begins when $\overline{CS}$ returns high, and the results are stored in the null register.
0	1	1	1	IN2-	IN2-	IN2- connected to the ADC inputs; offset-null mode selected. Autonull conversion begins when $\overline{CS}$ returns high, and the results are stored in the null register.
1	1	X	1	REF-	REF-	REF- connected to the ADC inputs; offset-null mode selected. Autonull conversion begins when $\overline{CS}$ returns high, and the results are stored in the null register.
1	0	X	1	REF+	REF-	REF+ and REF- connected to the ADC inputs; gain-calibration mode selected. Autocal conversion begins when $\overline{CS}$ returns high, and the results are stored in the 16-bit I/O register.
X	X	X	0	No Change	No Change	Input control word is not transferred to the control register. ADC configuration remains unchanged and no new conversion starts when $\overline{CS}$ returns high.

X = Don't Care

Table 3. Procedure to Calibrate the ADC

STEP	DESCRIPTION	CONTROL WORD									
		NO-OP	Not Used	CONV1-CONV4	DV2& DV4	Not Used	CHS	CAL	NUL	PDX	PD
1	Sets the new conversion speed (if required) and performs an offset correction conversion with the internal ADC inputs shorted to REF-. The result is stored in the null register. (This step also selects the speed/resolution for the ADC.)	1	00	New Data	XX	00	X	1	1	0	0
2	Performs a gain-calibration conversion with the null register contents as the starting value. The result is stored in the calibration register.	1	00	No Change	XX	00	X	1	0	0	0
3	Performs an offset-null conversion with the internal ADC inputs shorted to the selected input channel's negative input (IN1- or IN2-). The next operation performs the first signal conversion with the new setup.	1	00	No Change	XX	00	0 or 1	0	1	0	0

X = Don't Care

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

3-Step Calibration

The data sheet electrical specifications apply to the device after optional calibration of gain error and offset. Uncalibrated, the gain error is typically 2%.

Table 3 describes the three steps required to calibrate the ADC completely.

Once the ADC is calibrated to the selected channel, set CAL = 0 and NUL = 0 and leave CHS unchanged in the next control word to perform a signal conversion on the selected analog input channel.

Calibrate the ADC after the following operations:

- when power is first applied
- if the reference common-mode voltage changes
- if the common-mode voltage of the selected input channel varies significantly. The CMRR of the analog inputs is 0.25LSB/V.
- after changing channels (if the common-mode voltages of the two channels are different)
- after changing conversion speed/resolution.
- after significant changes in temperature. The offset drift with temperature is typically 0.003 μ V/ $^{\circ}$ C.

Automatic gain calibration is not allowed in the 102,400 cycles per conversion mode (see *Programming Conversion Time*). In this mode, calibration can be achieved by connecting the reference voltage to one input channel and performing a normal conversion. Subsequent conversion results can be corrected by software. **Do not issue a NO-OP command directly following the gain calibration, as the calibration data will be lost.**

Programming Conversion Time

The MAX110/MAX111 are specified for 12 bits of accuracy and up to ± 14 bits of resolution. The ADC's resolution depends on the number of clock cycles allowed during each conversion. Control-register bits 9–12 (CONV1–CONV4) determine the conversion time by controlling the nominal number of oversampling clock cycles required for each conversion (OSCC/CONV). Table 4 lists the available conversion times and resulting resolutions.

To program a new conversion time, perform a 3-step calibration with the appropriate CONV1–CONV4 data used in Table 3. The ADC is now calibrated at the new conversion speed/resolution.

Table 4. Available Conversion Times

CONV4	CONV3	CONV2	CONV1	CLOCK CYCLES PER CONVERSION	NOMINAL CONVERSION TIME RCSEL = GND, DV2 = DV4 = 0, XCLK = 500kHz (ms)	CONVERSION RESOLUTION (Bits)
1	0	0	1	10,240	20.48	12 + POL
0	0	1	1	20,480	40.96	13 + POL
0	1	1	0	81,920	163.84	14 + POL
0	0	0	0	102,400*	204.80	14 + POL

* Gain-calibration mode is not available with 102,400 clock cycles/conversion selected.

Table 5. Clock Divider-Ratio Control

DV2	DV4	DESCRIPTION
0	0	XCLK or internal RC oscillator connects directly to the ADC; $f_{OSC} = f_{XCLK}$.
0	1	XCLK or internal RC oscillator is divided by 4 and connects to the ADC; $f_{OSC} = f_{XCLK} \div 4$.
1	0	XCLK or internal RC oscillator is divided by 2 and connects to the ADC; $f_{OSC} = f_{XCLK} \div 2$.
1	1	Not allowed

Clock duty cycles of 50% $\pm$ 10% are recommended.

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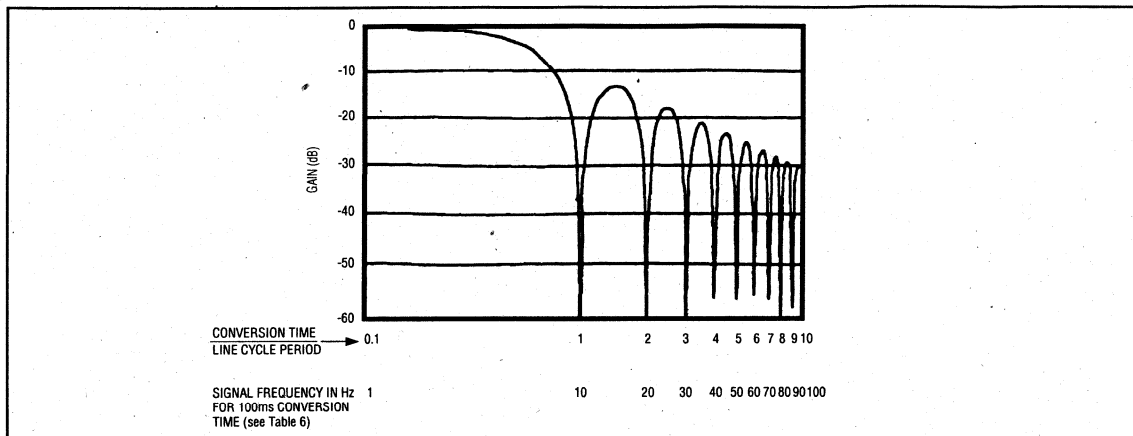


Figure 9. MAX110/MAX111 Noise Rejection Follows $\text{SIN}(X) / X$ Function

Selecting the Oversampling Clock Frequency

Choose the oversampling frequency, f_{OSC} , carefully to achieve the best relative-accuracy performance from the MAX110/MAX111 (see *Typical Operating Characteristics*).

Clock Divider-Ratio Control Bits

Bits 7 and 8 (DV2 and DV4) program the clock-frequency divider network. The divider network sets the frequency ratio between f_{XCLK} (the frequency of the external TTL/CMOS clock or internal RC oscillator) and f_{OSC} (the oversampling frequency used by the ADC). An oversampling clock frequency between 450kHz and 700kHz is optimum for the converter. **Best performance over the extended temperature range is obtained by choosing 1MHz or 1.024MHz with the divide-by-2 option (DV2 = 1) (see the section Effect of Dither on INL).** To determine the converter's accuracy at other clock frequencies, see the *Typical Operating Characteristics* and Table 5.

Effect of Dither on Relative Accuracy

First-order sigma-delta converters require dither for randomizing any systematic tone being generated in the modulator. The frequency of the dither source plays an important role in linearizing the modulator. The ratio of the dither generator's frequency to that of the modulator's oversampling clock can be changed by setting the DV2/DV4 bits. The XCLK clock is directly used by the dither generator while the DV2/DV4 bits reduce the oversampling clock by a ratio of 2 or 4. Over the commercial temperature range, any ratio (i.e., 1, 2, or 4) between the dither frequency and the oversampling

clock frequency can be used for best performance. Over the extended and military temperature ranges, the ratio of 2 or 4 gives the best performance. See the *Typical Operating Characteristics* to observe the effect of the clock divider on the converter's linearity.

50Hz/60Hz Line Frequency Rejection

High rejection of 50Hz or 60Hz is obtained by using an oversampling clock frequency and a clock-cycles/conversion setting so the conversion time equals an integral number of line cycles, as in the following equation:

$$f_{\text{OSC}} = f_{\text{LINE}} \times m / n$$

where f_{OSC} is the oversampling clock frequency, $f_{\text{LINE}} = 50\text{Hz}$ or 60Hz , m is the number of clock cycles per conversion (see Table 4), and n is the number of line cycles averaged every conversion.

This noise rejection is inherent in integrating and sigma-delta ADCs, and follows a $\text{SIN}(X) / X$ function (Figure 9). Notches in this function represent extremely high rejection, and correspond to frequencies with an integral number of cycles in the MAX110/MAX111's selected conversion time.

The shortest conversion time resulting in maximum simultaneous rejection of both 60Hz and 50Hz line frequencies is 100ms. When using the MAX111, use a 200ms conversion time for maximum 60Hz and 50Hz rejection **and** optimum performance. For either device, select the appropriate oversampling clock frequency and either an 81,240 or 102,400 clock cycles per conversion (CCPC) ratio. Table 6 suggests the possible configurations.

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MAX110/MAX111

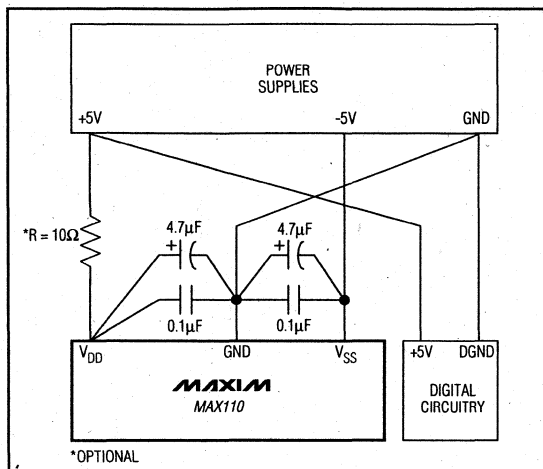


Figure 10a. MAX110 Power-Supply Grounding Connections

A 100ms conversion time cannot be achieved with either 10,240 CCPC or 20,480 CCPC modes because f_{osc} would be below the minimum 250kHz requirement.

When the gain calibration is performed, the conversion times change approximately 1% to compensate for the modulator's gain error. This slightly degrades the line-frequency rejection, because the corrected conversion time is no longer an exact multiple of the line frequency. Typically, the rejection of 50Hz/60Hz from the converter is 55dB; i.e., if there is 100mV injection at the reference or the analog input pin, it will cause an uncertainty of $\pm 0.006\%$. If the system has large 50Hz/60Hz noise, the use of internal auto gain calibration is not recommended. Instead, gain calibration should be done off-chip, using numerical computation methods.

Table 6. Suggested XCLK Frequencies to Achieve Maximum Rejection of Both 50Hz/60Hz Line Frequencies

MAX110 (t _{CONVERT} = 100ms)				
DIVIDER RATIO	81,240 CCPC		102,400 CCPC	
	f _{XCLK} (MHz)	RELATIVE ACCURACY (%)	f _{XCLK} (MHz)	RELATIVE ACCURACY (%)
1:1	0.8124	0.025	1.024	0.065
2:1	1.6248	0.018	2.048	0.045
4:1	3.2496	0.016	4.096	0.030

CCPC = Clock Cycles per Conversion

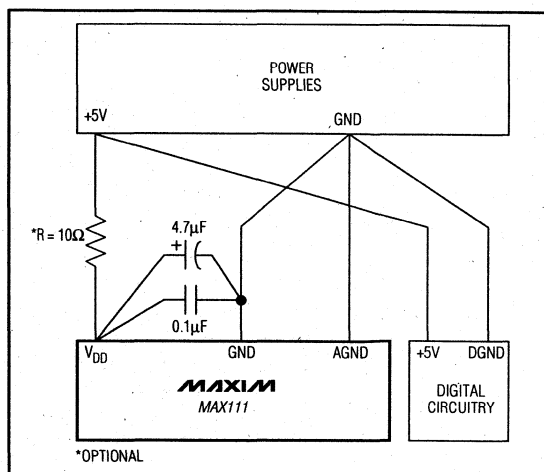


Figure 10b. MAX111 Power-Supply Grounding Connections

If you wish to use a configuration other than those suggested in Table 6, you can accomplish similar 50Hz and 60Hz line-frequency rejection off-chip by averaging several conversions.

Applications Information

Layout, Grounding, Bypassing

For minimal noise, bypass each supply to GND with a 0.1μF capacitor. A ground plane should also be placed under the analog circuitry. To minimize the coupling effects of stray capacitance, keep digital lines as far from analog components and lines as possible. Figure 10 shows the suggested power-supply and ground-plane connections.

7

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

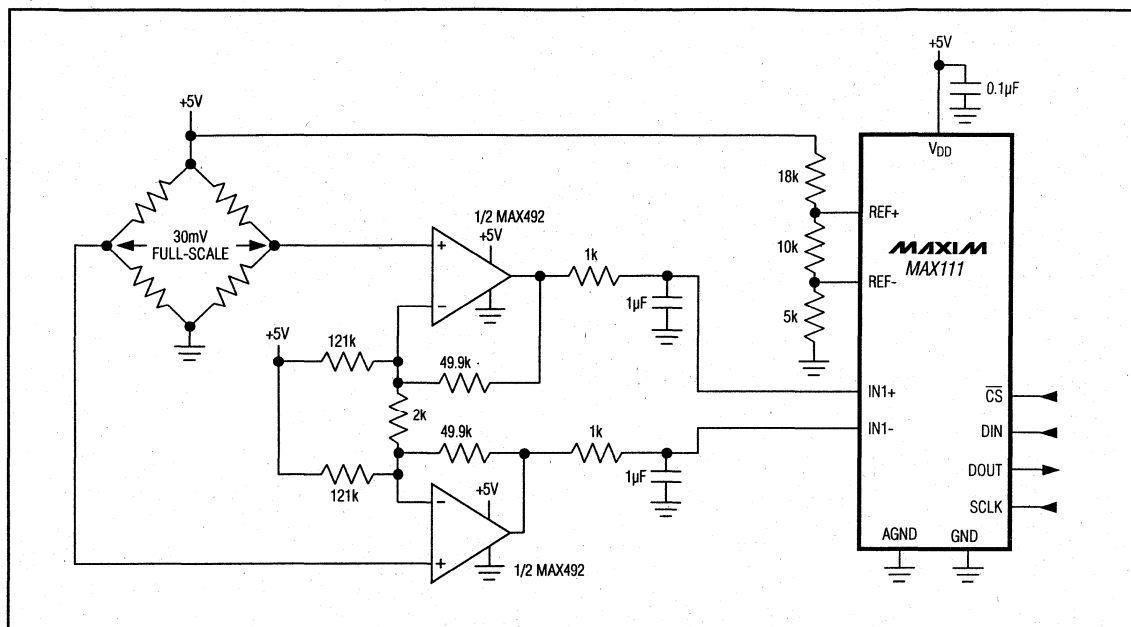


Figure 11. Weigh Scale Application

Capacitive Loading Effects of XCLK in Internal RC-Oscillator Mode

When using the internal RC oscillator, capacitive loading effects on the XCLK pin must be minimized. Stray capacitance causes the V_{DD} power consumption to increase by an amount $p = \frac{1}{2}CV^2f$, where C = stray capacitance, V is the supply voltage, and f is the frequency of the internal RC oscillator.

External Reference

The reference inputs to the ADC are high impedance, allowing both an external voltage reference and ratiometric applications without loading effects. The fully differential analog signal and reference inputs are advantageous for performing ratiometric conversions (Figures 11 and 12). For example, when measuring load cells, the bridge excitation and the ADC reference input both share the same voltage source. As the excitation changes with temperature or voltage, the output of the load cell will change. But since the differential reference voltage also changes, the conversion results remain constant, all else remaining equal.

Weigh Scale Application

The fully differential analog signal and reference inputs make the MAX111 easy to interface to transducers with differential outputs, such as the load cell in Figure 11. Because the ADC input is differential, the load cell only requires differential gain, eliminating the need for the difference amplifier (differential to single-ended converter) of the standard three op-amp instrumentation-amplifier realization.

The 30mV full-scale bridge output is amplified to 2V full-scale and applied to the MAX111 channel-one input. The reference voltage to the ADC is created by a voltage divider connected to the +5V rail. The same 5V provides excitation for the bridge; therefore, as the excitation voltage varies, the reference voltage to the ADC also varies, providing an ADC output that does not depend on the supply voltage.

The two 121k Ω resistors connected to the +5V supplies shift the common-mode voltage from 2.5V ($5V/2$) to 1.5V to ensure linearity. Match these two resistors to avoid introducing differential offset, or trim the resistor mismatch with a potentiometer. In practice, the scale is "zeroed" or "tared" by storing the average of several conversions in a memory location while the scale is

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

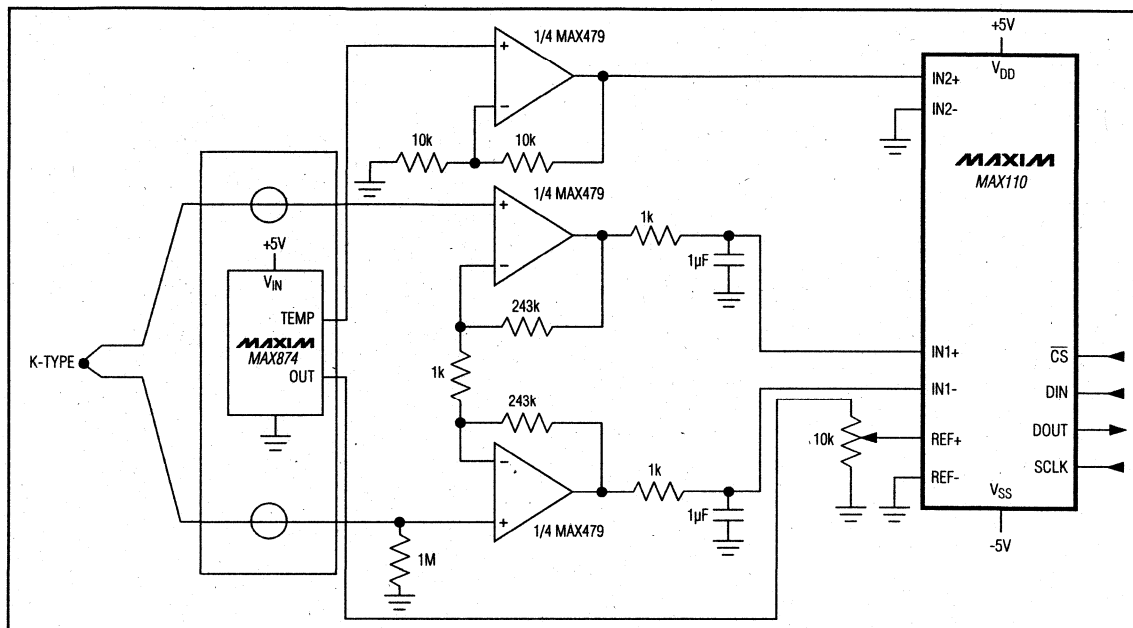


Figure 12. Thermocouple Circuit with Software Compensation

unloaded, and subtracting this value from actual weight measurements. The lowpass filtering action of the MAX111's sigma-delta converter helps minimize noise. The resolution of the weigh scale can be further increased by averaging several conversions.

Thermocouple Circuit with Software Compensation

A thermocouple is created by the junction of dissimilar metals, and generates a voltage proportional to temperature (Seebeck voltage), making it useful for temperature-measurement instruments. When a thermocouple probe is connected to a measurement instrument, other thermoelectric potentials are created between the alloys of the probe and the copper connectors of the instrument. These potentials introduce a temperature-dependent error that must be subtracted from the temperature measurement to obtain an accurate result. According to the law of intermediate metals, the junction of the thermocouple-probe alloys with the copper of the instrument junction block can be treated as another thermocouple of the same type. The voltage measured by the instrument can be expressed as:

$$V = \alpha(T1 - T_{REF})$$

where α is the Seebeck constant for the type of thermocouple, T_1 is the temperature being measured, and T_{REF} is the temperature of the junction block. Although one method to obtain T_{REF} is to force the junction block to a known temperature (0°C), a more popular approach is to measure T_{REF} directly using a thermistor or PN junction voltage.

The circuit in Figure 12 shows a k-type thermocouple going through a 54dB gain stage to channel 1 of the MAX110. A MAX874 voltage reference provides both the 3V reference voltage and reference junction temperature information to the MAX110. Armed with the temperature information provided by the MAX874, the thermocouple voltage created at the junction block can be subtracted out in software. The TEMP output of the MAX874 is nominally 690mV at room temperature, and increases with temperature at about 2.3mV/°C. Place the MAX874 as close as possible to the terminal block, and ensure good thermal contact between them. This circuit employs a common k-type thermocouple and, with the component values shown, can indicate temperatures in the range of -150°C to +125°C.

Low-Cost, 2-Channel, ± 14 -Bit Serial ADCs

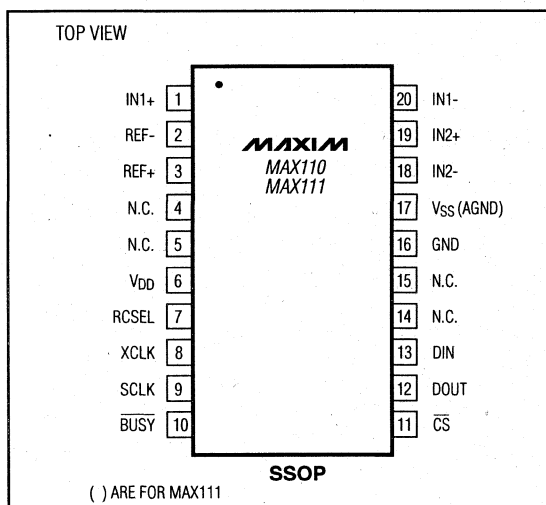
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL(%)
MAX110AEPE	-40°C to +85°C	16 Plastic DIP	± 0.03
MAX110BEPE	-40°C to +85°C	16 Plastic DIP	± 0.05
MAX110AEWE	-40°C to +85°C	16 Wide SO	± 0.03
MAX110BEWE	-40°C to +85°C	16 Wide SO	± 0.05
MAX110AEAP	-40°C to +85°C	20 SSOP	± 0.03
MAX110BEAP	-40°C to +85°C	20 SSOP	± 0.05
MAX110BMJE	-55°C to +125°C	16 CERDIP**	± 0.05
MAX111ACPE	0°C to +70°C	16 Plastic DIP	± 0.03
MAX111BCPE	0°C to +70°C	16 Plastic DIP	± 0.05
MAX111ACWE	0°C to +70°C	16 Wide SO	± 0.03
MAX111BCWE	0°C to +70°C	16 Wide SO	± 0.05
MAX111ACAP	0°C to +70°C	20 SSOP	± 0.03
MAX111BCAP	0°C to +70°C	20 SSOP	± 0.05
MAX111BC/D	0°C to +70°C	Dice*	± 0.05
MAX111AEPE	-40°C to +85°C	16 Plastic DIP	± 0.03
MAX111BEPE	-40°C to +85°C	16 Plastic DIP	± 0.05
MAX111AEWE	-40°C to +85°C	16 Wide SO	± 0.03
MAX111BEWE	-40°C to +85°C	16 Wide SO	± 0.05
MAX111AEAP	-40°C to +85°C	20 SSOP	± 0.03
MAX111BEAP	-40°C to +85°C	20 SSOP	± 0.05
MAX111BMJE	-55°C to +125°C	16 CERDIP**	± 0.05

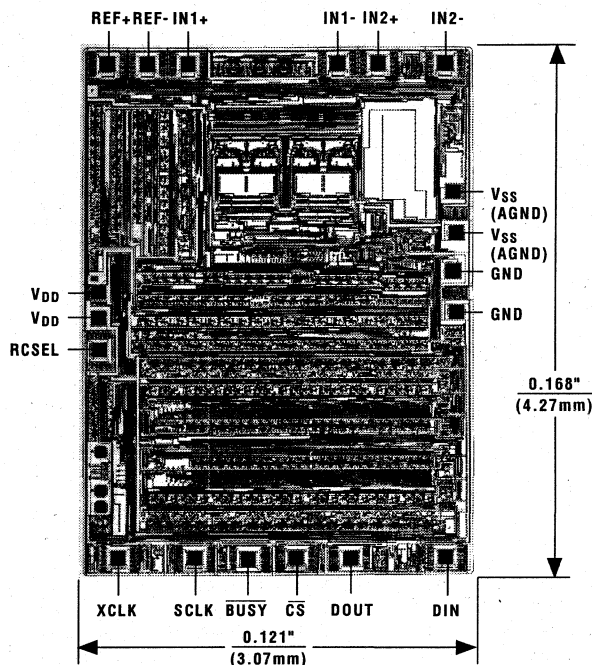
* Contact factory for dice specifications.

** Contact factory for availability.

Pin Configurations (continued)



Chip Topography



TRANSISTOR COUNT: 5849
SUBSTRATE CONNECTED TO V_{DD}

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

+3V, Low-Power, 8-Channel, Serial 12-Bit DAS

MAX146

General Description

The MAX146 is a +3V-powered, 12-bit data-acquisition system (DAS) that includes an 8-channel multiplexer, 4MHz bandwidth track/hold, 133ksps throughput, and a serial interface. Its low power dissipation (less than 5mW) makes it ideal for battery-powered applications. Its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The MAX146 has a 4-wire serial interface that operates at up to 2MHz and is compatible with SPI™, QSPI™, and Microwire™. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX146 uses either its internal clock or an external serial-interface clock to perform successive-approximation conversions.

The MAX146 has an internal 2.50V reference and a reference-buffer amplifier that simplifies gain trim. It also provides a hard-wired shutdown (SHDN) pin and two software-select power-down modes. Accessing the serial interface automatically powers up the device. By using the technique of powering down between conversions, the supply current can be reduced to under 10µA at slower sampling rates.

The MAX146 is available in 20-pin DIP and SO packages, and in a 20-pin SSOP package that occupies 50% less area than the SO package. For +5V operation, see the MAX186/MAX188 data sheet. For anti-alias filters, consult the MAX274/MAX275 data sheet.

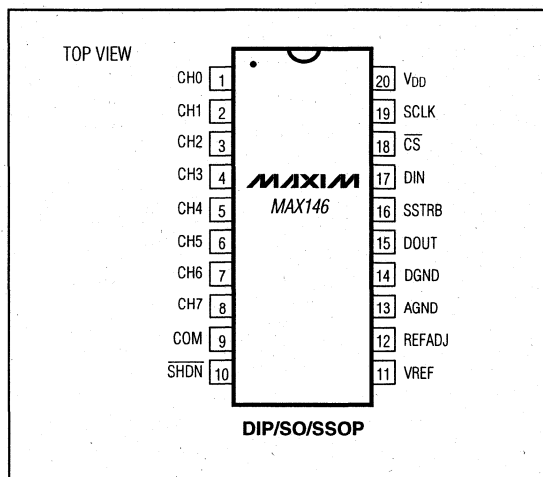
Features

- ♦ 8-Channel Single-Ended or 4-Channel Differential Inputs
- ♦ Single +2.7V to +3.6V Operation
- ♦ Low Power: 1.5mA (operating mode)
2µA (power-down mode)
- ♦ Internal Track/Hold, 133kHz Sampling Rate
- ♦ Internal 2.50V Reference
- ♦ SPI™, QSPI™, Microwire™, TMS320-Compatible 4-Wire Serial Interface
- ♦ 20-Pin DIP, SO, SSOP Packages

Applications

Portable Data Logging
Data Acquisition
High-Accuracy Process Control
Battery-Powered Instruments
Medical Instruments

Pin Configuration



Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX146ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX146BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX146ACWP	0°C to +70°C	20 SO	±1/2
MAX146BCWP	0°C to +70°C	20 SO	±1
MAX146ACAP	0°C to +70°C	20 SSOP	±1/2
MAX146BCAP	0°C to +70°C	20 SSOP	±1
MAX146BC/D	0°C to +70°C	Dice*	±1
MAX146AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX146BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX146AEWP	-40°C to +85°C	20 SO	±1/2
MAX146BEWP	-40°C to +85°C	20 SO	±1
MAX146AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX146BEAP	-40°C to +85°C	20 SSOP	±1
MAX146AMJP	-55°C to +125°C	20 CERDIP	±1/2
MAX146BMJP	-55°C to +125°C	20 CERDIP	±1

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

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ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

+3V, Low-Power, 8-Channel, Serial 10-Bit DAS

MAX149

General Description

The MAX149 is a +3V-powered, 10-bit data-acquisition system (DAS) that includes an 8-channel multiplexer, 4MHz bandwidth track/hold, 133ksps throughput, and a serial interface. Its low power dissipation (less than 5mW) makes it ideal for battery-powered applications. Its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The MAX149 has a 4-wire serial interface that operates at up to 2MHz and is compatible with SPI™, QSPI™, and Microwire™. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX149 uses either its internal clock or an external serial-interface clock to perform successive-approximation conversions.

The MAX149 has an internal 2.50V reference and a reference-buffer amplifier that simplifies gain trim. It also provides a hard-wired shutdown (SHDN) pin and two software-select power-down modes. Accessing the serial interface automatically powers up the device. By using the technique of powering down between conversions, the supply current can be reduced to under 10µA at slower sampling rates.

The MAX149 is available in 20-pin DIP and SO packages, and in a 20-pin SSOP package that occupies 50% less area than the SO package. For 12-bit applications, refer to the pin-compatible MAX146 data sheet.

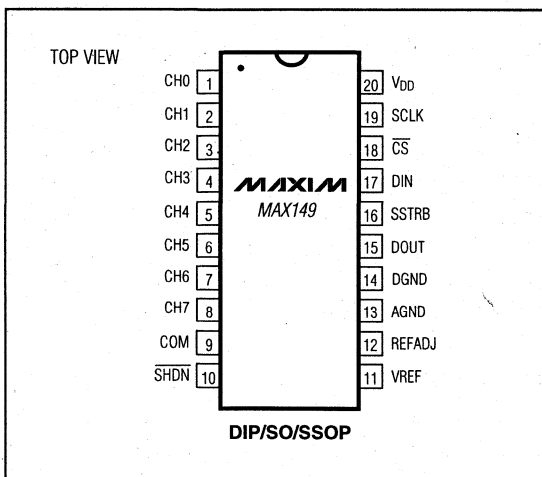
Features

- ◆ 8-Channel Single-Ended or 4-Channel Differential Inputs
- ◆ Single +2.7V to +3.6V Operation
- ◆ Low Power: 1.5mA (operating mode)
2µA (power-down mode)
- ◆ Internal Track/Hold, 133kHz Sampling Rate
- ◆ Internal 2.50V Reference
- ◆ SPI™, QSPI™, Microwire™, TMS320-Compatible 4-Wire Serial Interface
- ◆ 20-Pin DIP, SO, SSOP Packages
- ◆ Pin-Compatible 12-Bit Upgrade = MAX146

Applications

Portable Data Logging
Data Acquisition
High-Accuracy Process Control
Battery-Powered Instruments
Medical Instruments
Consumer Electronics

Pin Configuration



Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX149ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX149BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX149ACWP	0°C to +70°C	20 SO	±1/2
MAX149BCWP	0°C to +70°C	20 SO	±1
MAX149ACAP	0°C to +70°C	20 SSOP	±1/2
MAX149BCAP	0°C to +70°C	20 SSOP	±1
MAX149BC/D	0°C to +70°C	Dice*	±1
MAX149AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX149BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX149AEWP	-40°C to +85°C	20 SO	±1/2
MAX149BEWP	-40°C to +85°C	20 SO	±1
MAX149AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX149BEAP	-40°C to +85°C	20 SSOP	±1
MAX149AMJP	-55°C to +125°C	20 CERDIP	±1/2
MAX149BMJP	-55°C to +125°C	20 CERDIP	±1

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

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EVALUATION KIT
AVAILABLE**MAXIM**

14-Bit, 85ksps ADC with 10 μ A Shutdown

General Description

The MAX194 is a 14-bit successive-approximation analog-to-digital converter (ADC) that combines high speed, high accuracy, low power consumption, and a 10 μ A shutdown mode. Internal calibration circuitry corrects linearity and offset errors to maintain the full rated performance over the operating temperature range without external adjustments. The capacitive-DAC architecture provides an inherent 85ksps track/hold function.

The MAX194, with an external reference (up to +5V), offers a unipolar (0V to VREF) or bipolar (-VREF to VREF) pin-selectable input range. Separate analog and digital supplies minimize digital-noise coupling.

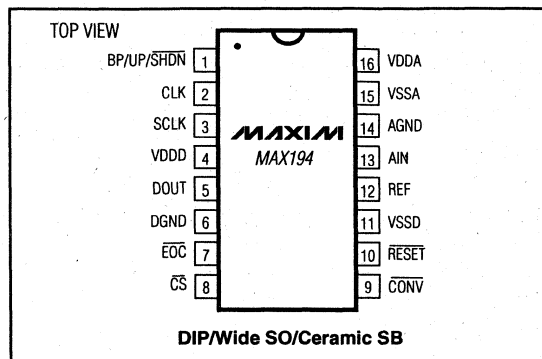
The chip select ($\overline{CS}$) input controls the three-state serial-data output. The output can be read either during conversion as the bits are determined, or following conversion at up to 5Mbps using the serial clock (SCLK). The end-of-conversion (EOC) output can be used to interrupt a processor, or can be connected directly to the convert input (CONV) for continuous, full-speed conversions.

The MAX194 is available in 16-pin DIP, wide SO, and ceramic sidebrazed packages. The output data format provides pin-for-pin and functional compatibility with the 16-bit MAX195 ADC.

Applications

Portable Instruments Audio
Industrial Controls Robotics
Multiple Transducer Measurements
Medical Signal Acquisition
Vibrations Analysis
Digital Signal Processing

Pin Configuration



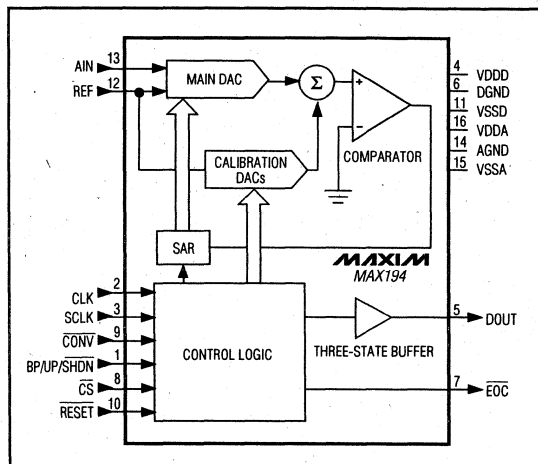
Features

- ♦ True 14-Bit Accuracy: $\frac{1}{2}$ LSB INL, 82dB SINAD
- ♦ 9.4 μ s Conversion Time
- ♦ 10 μ A Shutdown Mode
- ♦ Built-In Track/Hold
- ♦ AC and DC Specified
- ♦ Unipolar (0V to VREF) and Bipolar (-VREF to VREF) Input Range
- ♦ Three-State Serial-Data Output
- ♦ Small 16-Pin DIP and SO Packages
- ♦ Pin-Compatible 16-Bit Upgrade (MAX195)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX194ACPE	0°C to +70°C	16 Plastic DIP
MAX194BCPE	0°C to +70°C	16 Plastic DIP
MAX194ACWE	0°C to +70°C	16 Wide SO
MAX194BCWE	0°C to +70°C	16 Wide SO
MAX194AEPE	-40°C to +85°C	16 Plastic DIP
MAX194BEPE	-40°C to +85°C	16 Plastic DIP
MAX194AEWE	-40°C to +85°C	16 Wide SO
MAX194BEWE	-40°C to +85°C	16 Wide SO
MAX194AMDE	-55°C to +125°C	16 Ceramic SB
MAX194BMDE	-55°C to +125°C	16 Ceramic SB

Functional Diagram

**MAXIM**

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MAX194

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14-Bit, 85ksps ADC with 10 μ A Shutdown

ABSOLUTE MAXIMUM RATINGS

VDDD to DGND	+7V
VDDA to AGND	+7V
VSSD to DGND	+0.3V to -6V
VSSA to AGND	+0.3V to -6V
VDDD to VDDA, VSSD to VSSA	$\pm 0.3V$
AIN, REF	(VSSA - 0.3V) to (VDDA + 0.3V)
AGND to DGND	$\pm 0.3V$
Digital Inputs to DGND	-0.3V, (VDDA + 0.3V)
Digital Outputs to DGND	-0.3V, (VDDA + 0.3V)

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
Plastic DIP (derate 10.53mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	842mW
Wide SO (derate 9.52mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	762mW
Ceramic SB (derate 10.53mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	842mW
Operating Temperature Ranges	
MAX194_C_E	0°C to $+70^\circ\text{C}$
MAX194_E_E	-40°C to $+85^\circ\text{C}$
MAX194_MDE	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+160^\circ\text{C}$
Lead Temperature (soldering, 10sec)	$+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VDDD = VDDA = +5V, VSSD = VSSA = -5V, fCLK = 1.7MHz, VREF = 5V, $T_A = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	RES		14			Bits
Differential Nonlinearity	DNL				±1	LSB
Integral Nonlinearity	INL	MAX194A			±1/2	LSB
		MAX194B			±1	
Unipolar/Bipolar Offset Error		MAX194A, VREF = 4.75V			±1	LSB
		MAX194B, VREF = 4.75V			±2	
Unipolar/Bipolar Offset Tempco				0.4		ppm/°C
Unipolar Full-Scale Error		MAX194A, VREF = 4.75V			±1	LSB
		MAX194B, VREF = 4.75V			±2	
Bipolar Full-Scale Error		MAX194A, VREF = 4.75V			±2	LSB
		MAX194B, VREF = 4.75V			±4	
Full-Scale Tempco				0.1		ppm/°C
Power-Supply Rejection Ratio (VDDA and VSSA only)		VDDA = 4.75V to 5.25V, VREF = 4.75V	65			dB
		VSSA = -5.25V to -4.75V, VREF = 4.75V	65			
ANALOG INPUT						
Input Range		Unipolar		0	VREF	V
		Bipolar		-VREF	VREF	
Input Capacitance		Unipolar		250		pF
		Bipolar		125		
DYNAMIC PERFORMANCE (fs = 85kHz, bipolar range AIN = -5V to +5V, 1kHz) (Note 1)						
Signal-to-Noise plus Distortion Ratio	SINAD			82		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD				-90	dB
Peak Spurious Noise					-90	dB
Conversion Time	tCONV	16 x tCLK		9.4		µs
Clock Frequency (Notes 2, 3)	fCLK				1.7	MHz
Serial Clock Frequency	fsCLK				5	MHz

14-Bit, 85ksps ADC with 10 μ A Shutdown

ELECTRICAL CHARACTERISTICS (continued)

(VDDD = VDDA = +5V, VSSD = VSSA = -5V, fCLK = 1.7MHz, VREF = 5V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CLK, $\overline{\text{CS}}$, CONV, RESET, SCLK, BP/UP/SHDN)						
CLK, $\overline{\text{CS}}$, CONV, RESET, SCLK Input High Voltage	VIH	VDDD = 5.25V	2.4			V
CLK, $\overline{\text{CS}}$, CONV, RESET, SCLK Input Low Voltage	VIL	VDDD = 4.75V			0.8	V
CLK, $\overline{\text{CS}}$, CONV, RESET, SCLK Input Capacitance (Note 2)					10	pF
CLK, $\overline{\text{CS}}$, CONV, RESET, SCLK Input Current		Digital inputs = 0V or 5V			± 10	μ A
BP/UP/SHDN Input High Voltage	VIH		VDDD - 0.5			V
BP/UP/SHDN Input Low Voltage	VIL				0.5	V
BP/UP/SHDN Input Current, High	IIH	BP/UP/SHDN = VDDD			4.0	μ A
BP/UP/SHDN Input Current, Low	IIL	BP/UP/SHDN = 0V	-4.0			μ A
BP/UP/SHDN Mid Input Voltage	VIM		1.5	VDDD - 1.5		V
BP/UP/SHDN Voltage, Floating	VFLT	BP/UP/SHDN = open		2.75		V
BP/UP/SHDN Max Allowed Leakage, Mid Input		BP/UP/SHDN = open	-100		+100	nA
DIGITAL OUTPUTS (DOUT, EOC)						
Output Low Voltage	VOL	VDDD = 4.75V, ISINK = 1.6mA			0.4	V
Output High Voltage	VOH	VDDD = 4.75V, ISOURCE = 1mA	VDDD - 0.5			V
DOUT Leakage Current	ILKG	DOUT = 0V or 5V			± 10	μ A
Output Capacitance (Note 4)					10	pF
POWER REQUIREMENTS						
VDDD			4.75		5.25	V
VSSD			-5.25		-4.75	V
VDDA		By supply-rejection test	4.75		5.25	V
VSSA		By supply-rejection test	-5.25		-4.75	V
VDDD Supply Current	IDDD	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		2.5	4	mA
VSSD Supply Current	ISSD	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		0.9	2	mA
VDDA Supply Current	IDDA	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		3.8	5	mA
VSSA Supply Current	ISSA	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		3.8	5	mA

14-Bit, 85ksps ADC with 10 μ A Shutdown

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDD} = V_{DDA} = +5V, V_{SSD} = V_{VSSA} = -5V, f_{CLK} = 1.7MHz, V_{REF} = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS (cont.)						
Power Dissipation		V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V			80	mW
V _{DDD} Shutdown Supply Current (Note 5)	I _{DDD}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		1.6	5	μ A
V _{SSD} Shutdown Supply Current	I _{SSD}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		0.1	5	μ A
V _{DDA} Shutdown Supply Current	I _{DDA}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		0.1	5	μ A
V _{VSSA} Shutdown Supply Current	I _{VSSA}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		0.1	5	μ A

Note 1: Accuracy and dynamic performance tests performed after calibration.

Note 2: Tested with 50% duty cycle. Duty cycles from 25% to 75% at 1.7MHz are acceptable.

Note 3: See *External Clock* section.

Note 4: Guaranteed by design, not tested.

Note 5: Measured in shutdown mode with CLK and SCLK low.

TIMING CHARACTERISTICS

(V_{DDD} = V_{DDA} = +5V, V_{SSD} = V_{VSSA} = -5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T _A = +25°C		T _A = 0°C to +70°C		T _A = -40°C to +85°C		T _A = -55°C to +125°C		UNITS
			TYP		MIN	MAX	MIN	MAX	MIN	MAX	
CONV Pulse Width	t _{CW}				20		30		35		ns
CONV to CLK Falling Synchronization (Note 4)	t _{CC1}					10		10		10	ns
CONV to CLK Rising Synchronization (Note 4)	t _{CC2}					40		40		40	ns
Data Access Time	t _{DV}	C _L = 50pF				80		80		90	ns
Bus Relinquish Time	t _{DH}	C _L = 10pF				40		40		40	ns
CLK to EOC High	t _{CEH}	C _L = 50pF				300		300		350	ns
CLK to EOC Low	t _{CEL}	C _L = 50pF				300		300		350	ns
CLK to DOUT Valid	t _{CD}	C _L = 50pF			100	350	100	375	100	400	ns
SCLK to DOUT Valid	t _{SD}	C _L = 50pF			20	140	20	160	20	160	ns
$\overline{\text{CS}}$ to SCLK Setup Time	t _{CSS}				75		75		75		ns
$\overline{\text{CS}}$ to SCLK Hold Time	t _{CSH}				-10		-10		-10		ns
Acquisition Time	t _{AQ}				2.4		2.4		2.4		μ s
Calibration Time	t _{CAL}	14,000 $\times$ t _{CLK}			8.2		8.2		8.2		ms
RESET to CLK Setup Time	t _{RCS}				-40		-40		-40		ns
RESET to CLK Hold Time	t _{RCH}				120		120		120		ns
Start-Up Time (Note 6)	t _{SU}	Exiting shutdown	3.2								μ s

Note 6: Settling time required after deasserting shutdown to achieve less than 0.1LSB additional error.

14-Bit, 85ksps ADC with 10 μ A Shutdown

Pin Description

MAX194

PIN	NAME	FUNCTION
1	BP/UP/SHDN	Bipolar/Unipolar/Shutdown Input. Three-state input selects bipolar or unipolar input range, or shutdown. 0V = shutdown, +5V = unipolar, floating = bipolar.
2	CLK	Conversion Clock Input
3	SCLK	Serial Clock Input is used to shift data out between conversions. May be asynchronous to CLK.
4	VDDD	+5V Digital Power Supply
5	DOUT	Serial Data Output, MSB first
6	DGND	Digital Ground
7	EOC	End-of-Conversion/Calibration Output—normally low. Rises at beginning of conversion or calibration and falls at the end of either. May be used as an output framing signal.
8	CS	Chip-Select Input—active low. Enables the serial interface and the three-state data output (DOUT).
9	CONV	Convert-Start Input—active low. Conversion begins on the falling edge after $\overline{\text{CONV}}$ goes low if input signal has been acquired; otherwise, on the falling clock edge after acquisition.
10	RESET	Reset Input. Pulling $\overline{\text{RESET}}$ low places ADC in inactive state. Rising edge resets control logic and begins calibration.
11	VSSD	-5V Digital Power Supply
12	REF	Reference Input, 0V to 5V
13	AIN	Analog Input, 0V to VREF unipolar or $\pm V_{\text{REF}}$ bipolar range
14	AGND	Analog Ground
15	VSSA	-5V Analog Power Supply
16	VDDA	+5V Analog Power Supply

Detailed Description

The MAX194 uses a successive-approximation register (SAR) to convert an analog input to a 14-bit digital code, which is output as a serial data stream. The data bits can be read either during the conversion, at the CLK clock rate, or between conversions asynchronous with CLK, at the SCLK rate (up to 5Mbps).

The MAX194 includes a capacitive digital-to-analog converter (DAC) that provides an inherent track/hold input. The interface and control logic are designed for easy connection to most microprocessors (μ Ps), limiting the need for external components. In addition to the SAR and DAC, the MAX194 includes a serial interface, a sampling comparator used by the SAR, ten calibration DACs, and control logic for calibration and conversion.

The DAC consists of an array of capacitors with binary weighted values plus one "dummy sub-LSB" capacitor (Figure 1). During input acquisition in unipolar mode, the array's common terminal is connected to AGND and all free terminals are connected to the input signal (AIN). After acquisition, the common terminal is disconnected from AGND and the free terminals are disconnected

from AIN, trapping a charge proportional to the input voltage on the capacitor array.

The free terminal of the MSB (largest) capacitor is connected to the reference (REF), which pulls the common terminal (connected to the comparator) positive. Simultaneously, the free terminals of all other capacitors in the array are connected to AGND, which drives the comparator input negative. If the analog input is near VREF, connecting the MSB's free terminal to REF only pulls the comparator input slightly positive. However, connecting the remaining capacitor's free terminals to ground drives the comparator input well below ground, so that the comparator input is negative, the comparator output is low, and the MSB is set high. If the analog input is near ground, the comparator output is high and the MSB is low.

Following this, the next largest capacitor is disconnected from AGND and connected to REF, and the comparator determines the next bit. This continues until all bits have been determined. For a bipolar input range, the MSB capacitor is connected to REF rather than AIN during input acquisition, which results in an input range of VREF to -VREF.

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14-Bit, 85ksps ADC with 10 μ A Shutdown

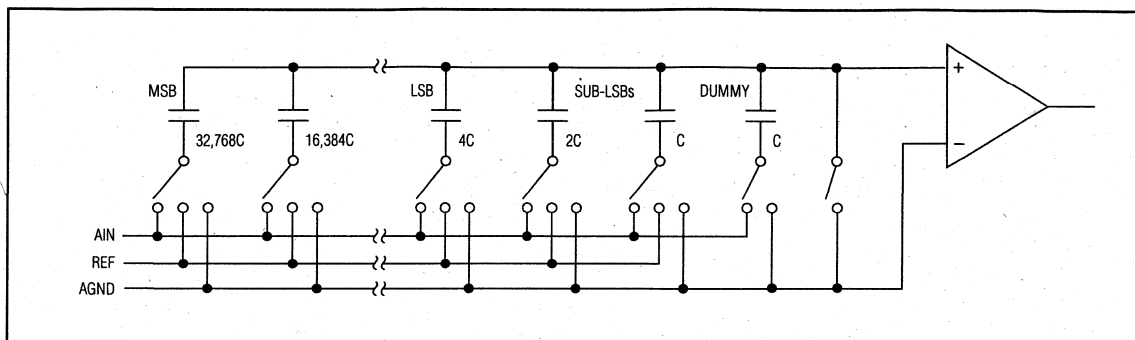


Figure 1. Capacitor DAC Functional Diagram

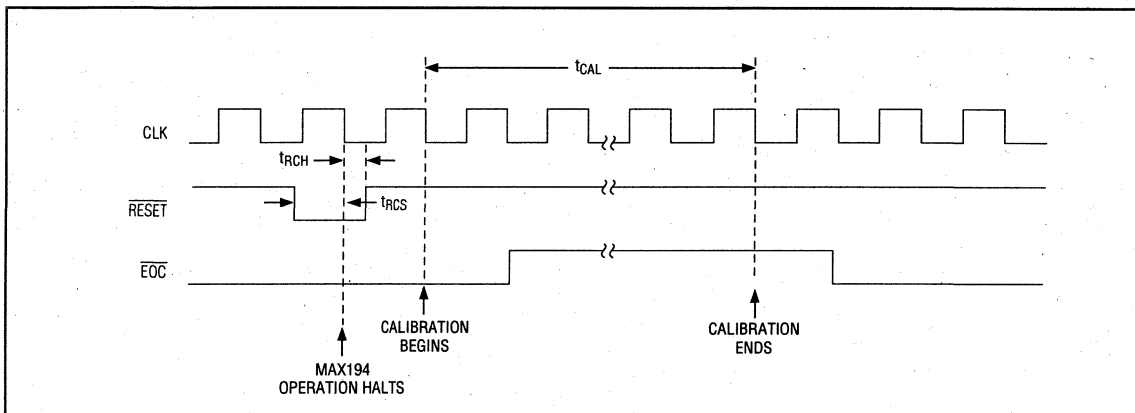


Figure 2. Initiating Calibration

Calibration

In an ideal DAC, each of the capacitors associated with the data bits would be exactly twice the value of the next smaller capacitor. In practice, this results in a range of values too wide to be realized in an economically feasible size. The capacitor array actually consists of two arrays, which are capacitively coupled to reduce the LSB array's effective value. The capacitors in the MSB array are production trimmed to reduce errors. Small variations in the LSB capacitors contribute insignificant errors to the 14-bit result.

Unfortunately, trimming alone does not yield 14-bit performance or compensate for changes in performance due to changes in temperature, supply voltage, and other parameters. For this reason, the MAX194 includes a calibration DAC for each capacitor in the MSB array. These DACs are capacitively coupled to the main DAC

output and offset the main DAC's output according to the value on their digital inputs. During calibration, the correct digital code to compensate for the error in each MSB capacitor is determined and stored. Thereafter, the stored code is input to the appropriate calibration DAC whenever the corresponding bit in the main DAC is high, compensating for errors in the associated capacitor.

The MAX194 calibrates automatically on power-up. To reduce the effects of noise, each calibration experiment is performed many times and the results are averaged. Calibration requires about 14,000 clock cycles, or 8.2ms at the highest clock (CLK) speed (1.7MHz). In addition to the power-up calibration, bringing RESET low halts MAX194 operation, and bringing it high again initiates a calibration (Figure 2).

14-Bit, 85ksps ADC with 10 μ A Shutdown

MAX194

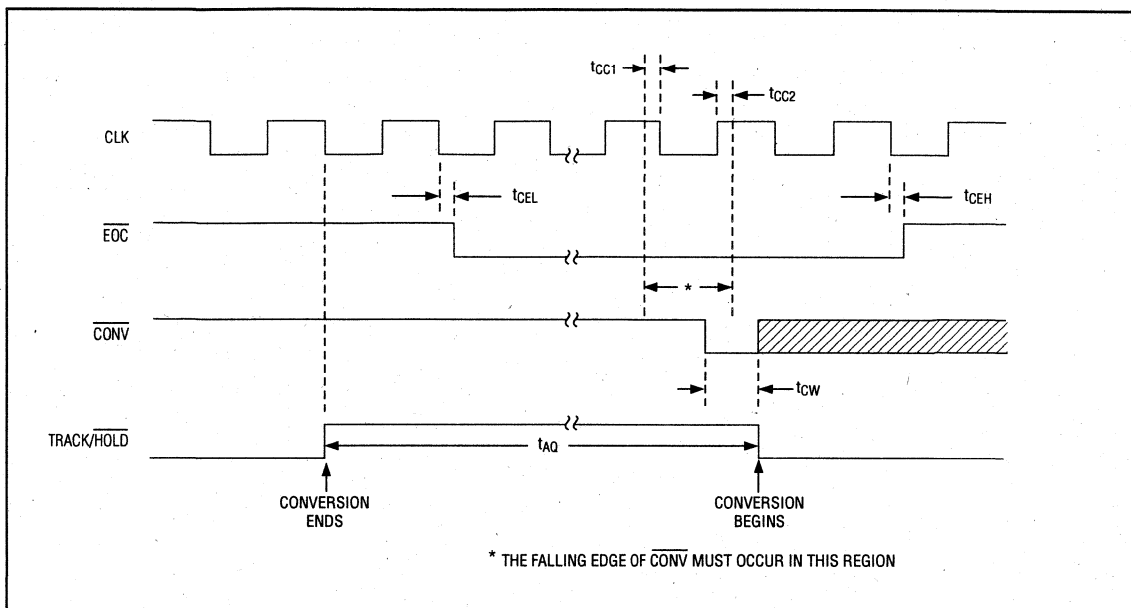


Figure 3. Initiating Conversions—At least 3 CLK cycles since end of previous conversion.

If the power supplies do not settle within the MAX194's power-on delay (500ns minimum), power-up calibration may begin with supply voltages that differ from the final values and the converter may not be properly calibrated. If so, recalibrate the converter (pulse RESET low) before use. For best DC accuracy, calibrate the MAX194 any time there is a significant change in supply voltages, temperature, reference voltage, or clock characteristics (see *External Clock* section) because these parameters affect the DC offset. If linearity is the only concern, much larger changes in these parameters can be tolerated.

Because the calibration data is stored digitally, there is no need either to perform frequent conversions to maintain accuracy or to recalibrate if the MAX194 has been held in shutdown for long periods. However, recalibration is recommended if it is likely that supply voltages or ambient temperature has significantly changed since the previous calibration.

Digital Interface

The digital interface pins consist of BP/UP/SHDN, CLK, SCLK, EOC, CS, CONV, and RESET.

BP/UP/SHDN is a three-level input. Leave it floating to configure the MAX194's analog input in bipolar mode ($A_{IN} = -V_{REF}$ to V_{REF}) or connect it high for a unipolar

input ($A_{IN} = 0V$ to V_{REF}). Bringing BP/UP/SHDN low places the MAX194 in its 10 μ A shutdown mode.

A logic low on RESET halts MAX194 operation. The rising edge of RESET initiates calibration as described in the *Calibration* section above.

Begin a conversion by bringing CONV low. The convert signal must be synchronized with CLK. The falling edge of CONV must occur during the period shown in Figures 3 and 4. When CLK is not directly controlled by your processor, two methods of ensuring synchronization are to drive CONV from EOC (continuous conversions) or to gate the conversion-start signal with the conversion clock so that CONV can go low only while CLK is low (Figure 5). Ensure that the maximum propagation delay through the gate is less than 40ns.

The MAX194 automatically ensures four CLK periods for track/hold acquisition. If, when CONV is asserted, at least three clock (CLK) cycles have passed since the end of the previous conversion, a conversion will begin on CLK's next falling edge and EOC will go high on the following falling CLK edge (Figure 3). After conversion begins, additional convert start pulses are ignored. If, when convert is asserted, less than three clock cycles have passed, a conversion will begin on the fourth falling clock edge after the end of the previous conver-

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14-Bit, 85ksps ADC with 10 μ A Shutdown

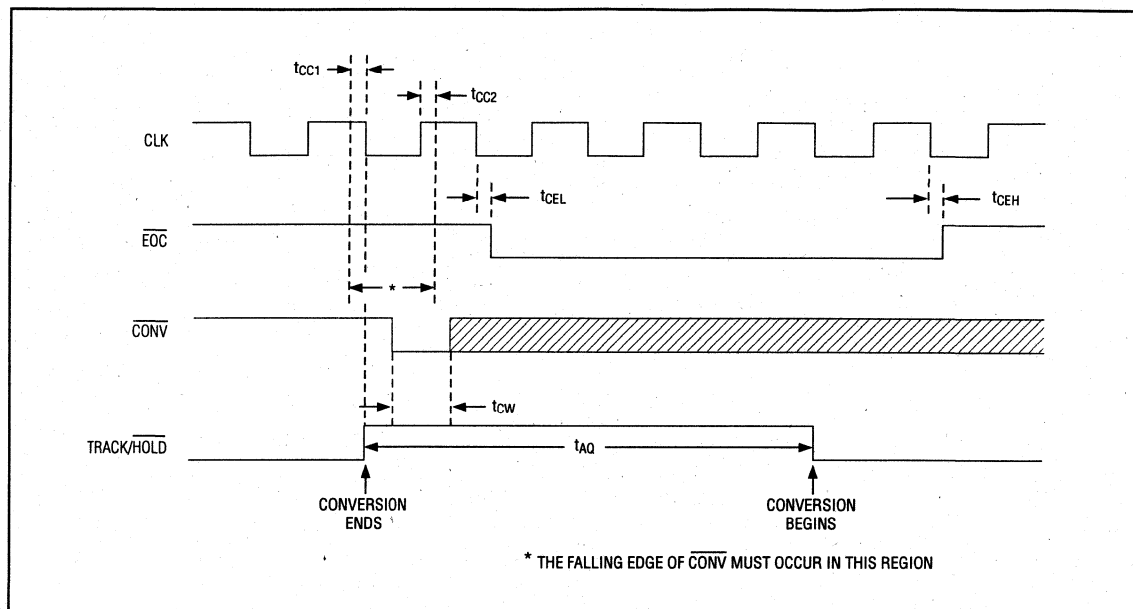


Figure 4. Initiating Conversions—Less than 3 CLK cycles since end of previous conversion.

sion and $\overline{\text{EOC}}$ will go high on the following CLK falling edge (Figure 4). $\overline{\text{CONV}}$ is ignored during conversions.

External Clock

The conversion clock (CLK) should have a duty cycle between 25% and 75% at 1.7MHz (the maximum clock frequency). For lower frequency clocks, ensure the minimum high and low times exceed 150ns. The minimum clock rate for accurate conversion is 125Hz for temperatures up to +70°C or 1kHz at +125°C due to leakage of the sampling capacitor array. In addition, CLK should not remain high longer than 50ms at temperatures up to +70°C or 500 μ s at +125°C. If CLK is held high longer than this, RESET must be pulsed low to initiate a recalibration because it is possible that state information stored in internal dynamic memory may be lost. The MAX194's clock can be stopped indefinitely if it is held low.

If the frequency, duty cycle, or other aspects of the clock signal's shape change, the offset created by coupling between CLK and the analog inputs (AIN and REF) changes. Recalibration corrects for this offset and restores DC accuracy.

Output Data

The conversion result is clocked out MSB first, formatted as 14 data bits plus two sub-LSBs. Serial data is available on DOUT only when $\overline{\text{CS}}$ is held low. Otherwise, DOUT is in a high-impedance state. There are two ways to read the data on DOUT. To read the data bits as they are determined (at the CLK clock rate), hold $\overline{\text{CS}}$ low during the conversion. To read results between conversions, hold $\overline{\text{CS}}$ low and clock SCLK at up to 5MHz.

If you read the serial data bits as they are determined (at the conversion-clock rate), $\overline{\text{EOC}}$ frames the data bits (Figure 6). Conversion begins with the first falling CLK edge, after $\overline{\text{CONV}}$ goes low and the input signal has been acquired. Data bits are shifted out of DOUT on subsequent falling CLK edges. Clock data in on CLK's rising edge or, if the clock speed is greater than 1MHz, on the following falling edge of CLK to meet the maximum CLK-to-DOUT timing specification. See the *Operating Modes and SPI/QSPI Interfaces* section for additional information. Reading the serial data during the conversion results in the maximum conversion throughput, because a new conversion can begin immediately after the input acquisition period following the previous conversion.

14-Bit, 85ksps ADC with 10 μ A Shutdown

MAX194

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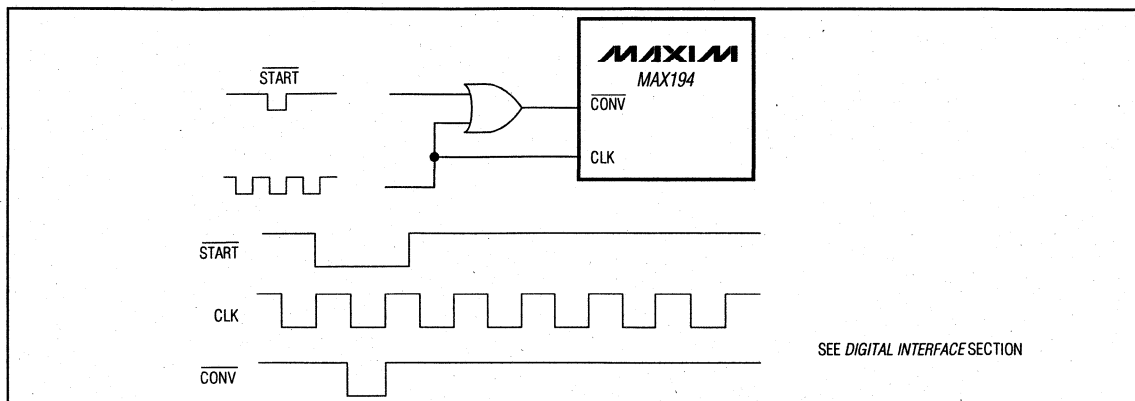


Figure 5. Gating $\overline{\text{CONV}}$ to Synchronize with CLK

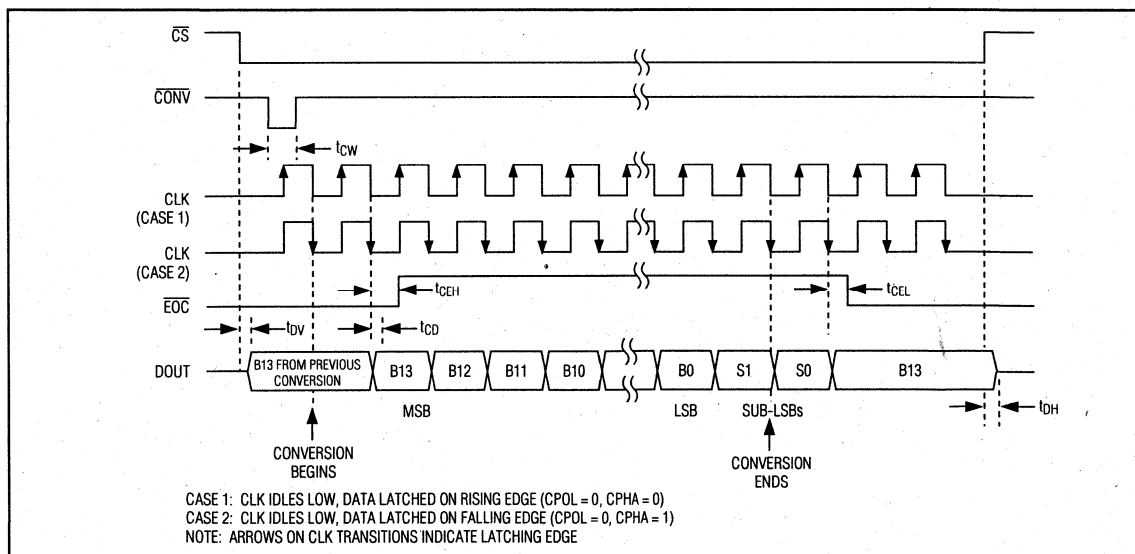


Figure 6. Output Data Format, Reading Data During Conversion (Mode 1)

- If you read the data bits between conversions, you can
- 1) count CLK cycles until the end of the conversion, or
 - 2) poll $\overline{\text{EOC}}$ to determine when the conversion is finished, or
 - 3) generate an interrupt on $\overline{\text{EOC}}$'s falling edge.

Note that the MSB conversion result appears at DOUT after $\overline{\text{CS}}$ goes low but **before** the first SCLK pulse. Each subsequent SCLK pulse shifts out the next conversion

bit. The 15th SCLK pulse shifts out the sub-LSB (S0). Additional clock pulses shift out zeros.

Data is clocked out on SCLK's falling edge. Clock data in on SCLK's rising edge or, for clock speeds above 2.5MHz, on the following falling edge to meet the maximum SCLK-to-DOUT timing specification (Figure 7). The maximum SCLK speed is 5MHz. See the *Operating Modes and SPI/QSPI Interfaces* section for additional information. When the conversion clock is near its maxi-

14-Bit, 85ksps ADC with 10 μ A Shutdown

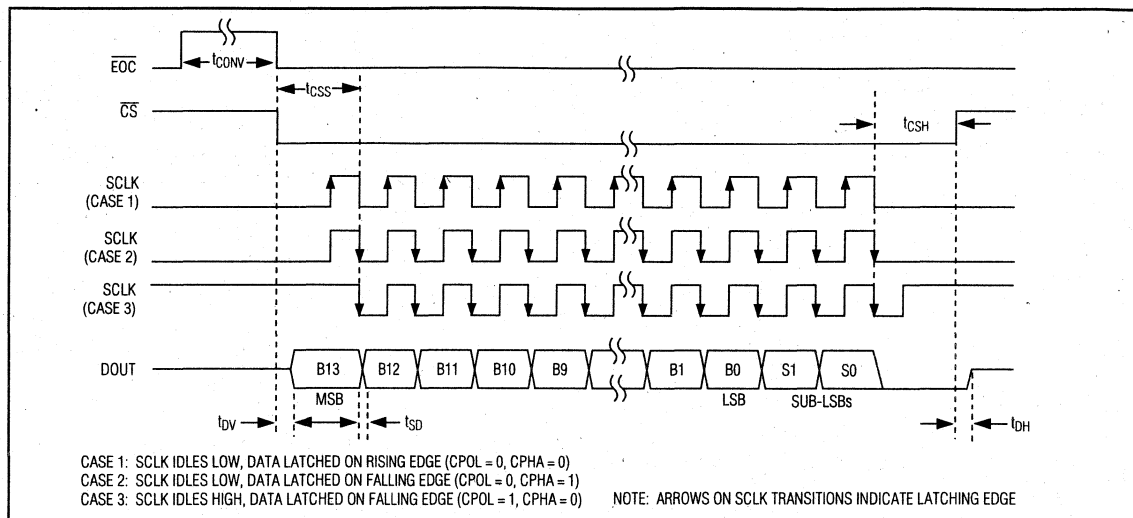


Figure 7. Output Data Format, Reading Data Between Conversions (Mode 2)

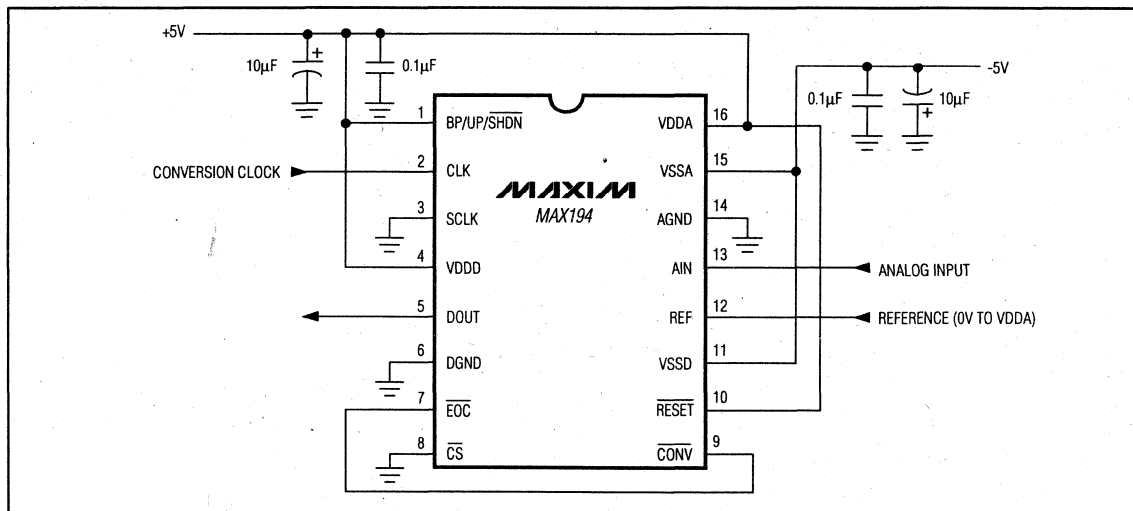


Figure 8. MAX194 in the Simplest Operating Configuration

imum (1.7MHz), reading the data after each conversion (during the acquisition time) results in lower throughput (about 70ksps max) than reading the data during conversions, because it takes longer than the minimum input acquisition time (four cycles at 1.7MHz) to clock 16 data bits at 5Mbps. After the data has been clocked

in, leave some time (about 1 μ s) for any coupled noise on AIN to settle before beginning the next conversion.

Whichever method is chosen for reading the data, conversions can be individually initiated by bringing CONV low, or they can occur continuously by connecting EOC to CONV. Figure 8 shows the MAX194 in its simplest operational configuration.

14-Bit, 85ksps ADC with 10 μ A Shutdown

MAX194

Table 1. Low-ESR Capacitor Suppliers

COMPANY	CAPACITOR	FACTORY FAX [COUNTRY CODE]	USA TELEPHONE
Sprague	595D series, 592D series	[1] (603) 224-1430	(603) 224-1961
AVX	TPS series	[1] (207) 283-1941	(800) 282-4975
Sanyo	OS-CON series, MV-GX series	[81] 7-2070-1174	(619) 661-6835
Nichicon	PL series	[1] (708) 843-2798	(708) 843-7500

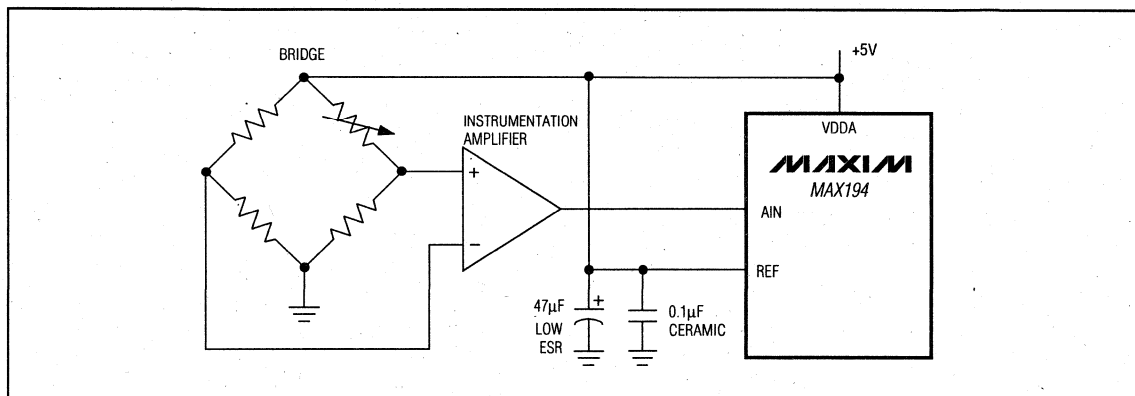


Figure 9. Ratiometric Measurement Without an Accurate Reference

Applications Information

Reference

The MAX194 reference voltage range is 0V to VDDA. When choosing the reference voltage, the MAX194's equivalent input noise (40 μ V_{RMS} in unipolar mode, 80 μ V_{RMS} in bipolar mode) should be considered. Also, if VREF exceeds VDDA, errors will occur due to the internal protection diodes that will begin to conduct, so use caution when using a reference near VDDA (unless VREF and VDDA are virtually identical). VREF must never exceed its absolute maximum rating (VDDA + 0.3V).

The MAX194 needs a good reference to achieve its rated performance. The most important requirement is that the reference must present a low impedance to the REF input. This is often achieved by buffering the reference through an op amp and bypassing the REF input with a large (1 μ F to 47 μ F), low-ESR capacitor in parallel with a 0.1 μ F ceramic capacitor. Low-ESR capacitors are available from the manufacturers listed in Table 1.

The reference must drive the main conversion DAC capacitors as well as the capacitors in the calibration

DACs, all of which may be switching between GND and REF at the conversion clock frequency. The total capacitive load presented can exceed 1000pF and, unlike the analog input (AIN), REF is sampled continuously throughout the conversion.

The first step in choosing a reference circuit is to decide what kind of performance is required. This often suggests compromises made in the interests of cost and size. It is possible that a system may not require an accurate reference at all. If a system makes a ratiometric measurement such as Figure 9's bridge circuit, any relatively noise-free voltage that presents a low impedance at the REF input will serve as a reference. The +5V analog supply suffices if you use a large, low-impedance bypass capacitor to keep REF stable during switching of the capacitor arrays. Do not place a resistance between the +5V supply and the bypass capacitor, because it will cause linearity errors due to the dynamic REF input current, which typically ranges from 300 μ A to 400 μ A.

Figure 10 shows a more typical scheme that provides good AC accuracy. The MAX874's initial accuracy can

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14-Bit, 85ksps ADC with 10 μ A Shutdown

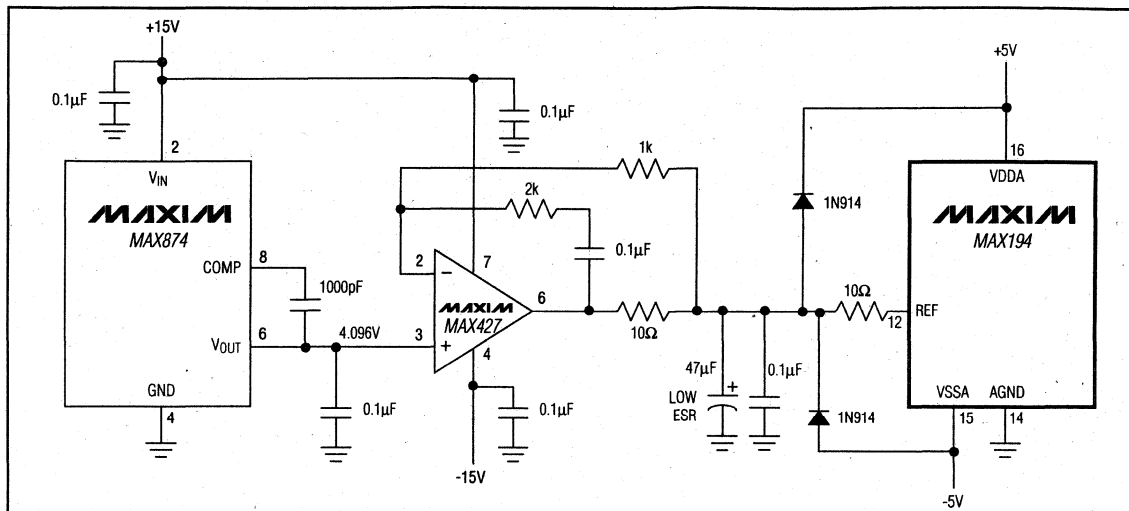


Figure 10. Typical Reference Circuit for AC Accuracy

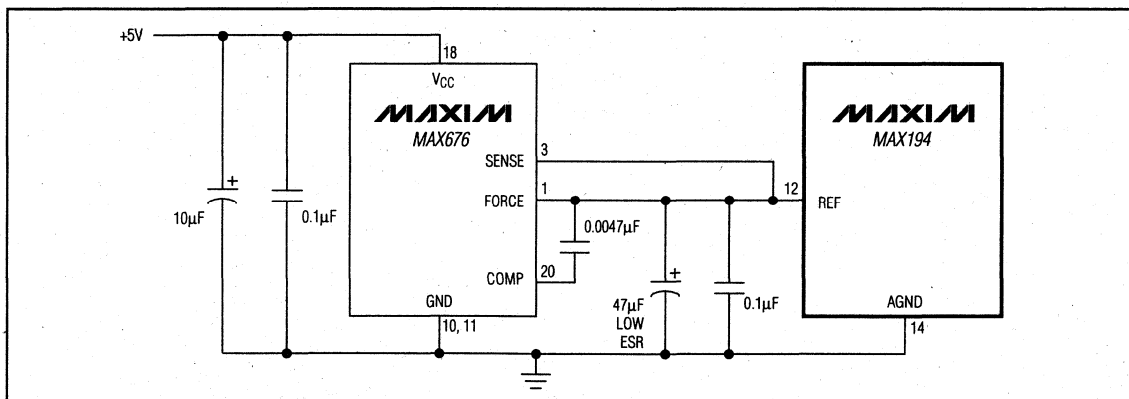


Figure 11. MAX676 Provides High-Accuracy +4.096V Reference

be improved by trimming, but the drift is too great to provide good stability over temperature. The MAX427 buffer provides the necessary drive current to stabilize the REF input quickly after capacitance changes.

The reference inaccuracies contribute additional full-scale error. A reference with less than $1/2^{14}$ total error (61 parts per million) over the operating temperature range is required to maintain full 14-bit accuracy. The MAX676, which utilizes an on-chip ROM to calibrate for drift, achieves a drift specification of 1ppm/°C and easi-

ly drives the REF input directly. This allows large temperature changes with less than 1LSB error. While the MAX676's initial-accuracy specification (0.01%) results in a maximum error of about ± 2 LSB, the reference voltage can be trimmed or the offset can be corrected in software if absolute DC accuracy is essential. Figure 11's circuit provides outstanding temperature stability as well as excellent DC accuracy if the initial error is corrected.

14-Bit, 85ksps ADC with 10 μ A Shutdown

MAX194

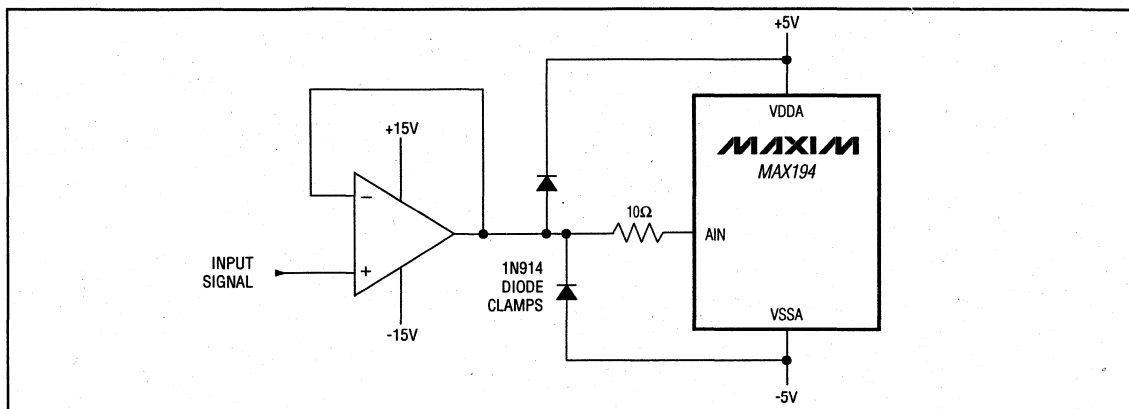


Figure 12. Analog Input Protection for Overvoltage or Improper Supply Sequence

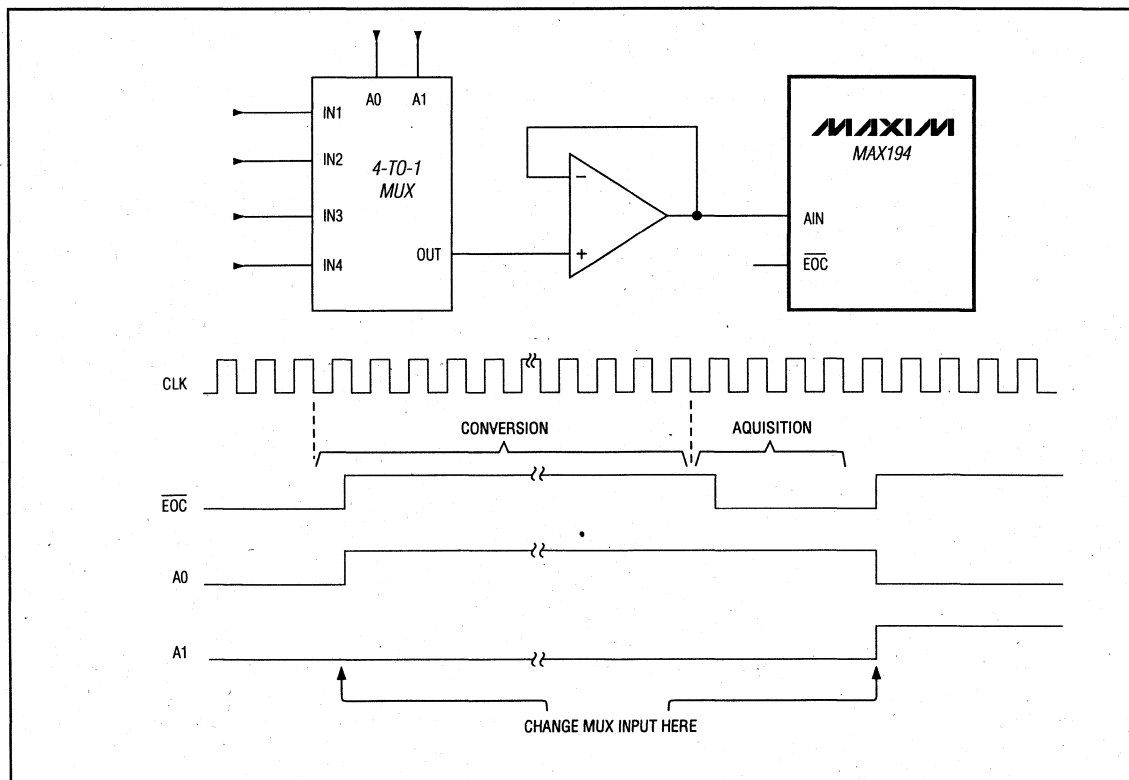


Figure 13. Change multiplexer input near beginning of conversion to allow time for slewing and settling.

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14-Bit, 85ksps ADC with 10 μ A Shutdown

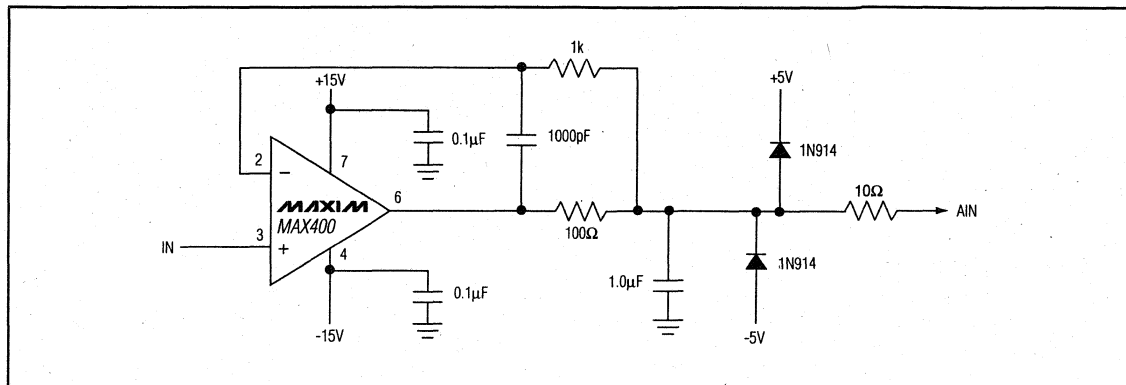


Figure 14. MAX400 Drives AIN for Low-Frequency Use

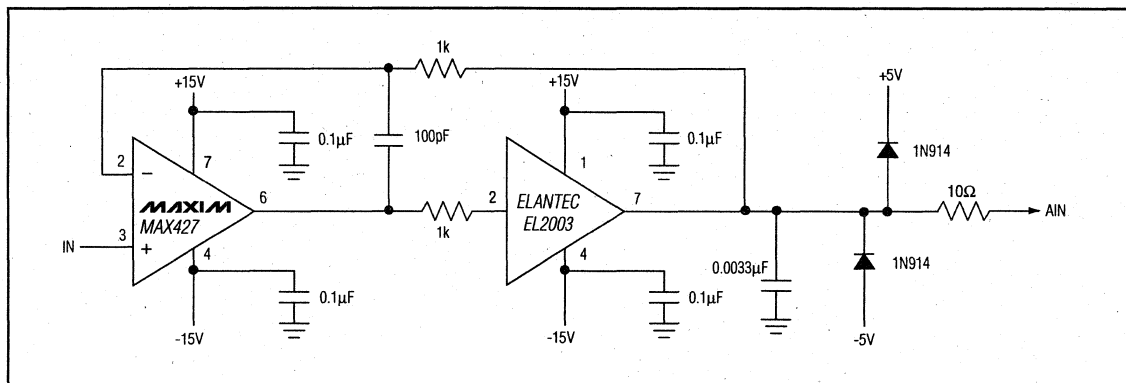


Figure 15. AIN Buffer for AC/DC Use

REF and AIN Input Protection

The REF and AIN signals should not exceed the MAX194 supply rails. If this can occur, diode clamp the signal to the supply rails. Use silicon diodes and a 10 Ω current-limiting resistor (Figures 10 and 12) or Schottky diodes without the resistor.

When using the current-limiting resistor, place the resistor between the appropriate input (AIN or REF) and any bypass capacitor. While this results in AC transients at the input due to dynamic input currents, the transients settle quickly and do not affect conversion results. Improperly placing the bypass capacitor directly at the input forms an RC lowpass filter with the current-limiting resistor, which averages the dynamic input current and causes linearity errors.

Analog Input

The MAX194 uses a capacitive DAC that provides an inherent track/hold function. The input impedance is typically 30 Ω in series with 250pF in unipolar mode and 50 Ω in series with 125pF in bipolar mode.

Input Range

The analog input range can be either unipolar (0V to VREF) or bipolar (-VREF to VREF), depending on the state of the BP/UP/SHDN pin (see *Digital Interface* section). The reference range is 0V to VDDA. When choosing the reference voltage, the equivalent MAX194 input noise (40 μ V_{RMS} in unipolar mode, 80 μ V_{RMS} in bipolar mode) should be considered.

14-Bit, 85ksps ADC with 10 μ A Shutdown

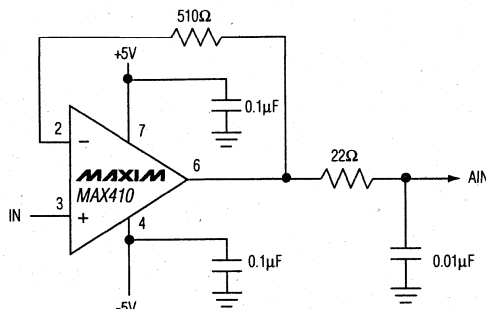


Figure 16. ± 5 V Buffer for AC/DC Use Has ± 3.5 V Swing

Input Acquisition and Settling

Four conversion-clock periods are allocated for acquiring the input signal. At the highest conversion rate, four clock periods is 2.4 μ s. If more than three clock cycles have occurred since the end of the previous conversion, conversion begins on the next falling clock edge after CONV goes low. Otherwise, bringing CONV low begins a conversion on the fourth falling clock edge after the previous conversion. This scheme ensures the minimum input acquisition time is four clock periods.

Most applications require an input buffer amplifier. If the input signal is multiplexed, the input channel should be switched near the beginning of a conversion, rather than near the end of or after a conversion (Figure 13). This allows time for the input buffer amplifier to respond to a large step change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change *before* the beginning of the acquisition time.

At the beginning of acquisition, the capacitive DAC is connected to the amplifier output, causing some output disturbance. Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the capacitive DAC with very little change in voltage (Figure 14). However, for AC use, AIN must be driven by a wideband buffer (at least 10MHz), which must be stable with the DAC's capacitive load (in parallel with any AIN bypass capacitor used) and also must settle quickly (Figure 15 or 16).

Digital Noise

Digital noise can easily be coupled to AIN and REF. The conversion clock (CLK) and other digital signals

that are active during input acquisition contribute noise to the conversion result. If the noise signal is synchronous to the sampling interval, an effective input offset is produced. Asynchronous signals produce random noise on the input, whose high-frequency components may be aliased into the frequency band of interest. Minimize noise by presenting a low impedance (at the frequencies contained in the noise signal) at the inputs. This requires bypassing AIN to AGND, or buffering the input with an amplifier that has a small-signal bandwidth of several megahertz, or preferably both. AIN has a bandwidth of about 16MHz.

Offsets resulting from synchronous noise (such as the conversion clock) are canceled by the MAX194's calibration scheme. However, because the magnitude of the offset produced by a synchronous signal depends on the signal's shape, recalibration may be appropriate if the shape or relative timing of the clock or other digital signals change, as might occur if more than one clock signal or frequency is used.

Distortion

Avoid degrading dynamic performance by choosing an amplifier with distortion much less than the MAX194's THD (-90dB, or 0.0032%) at frequencies of interest. If the chosen amplifier has insufficient common-mode rejection, which results in degraded THD performance, use the inverting configuration (positive input grounded) to eliminate errors from this source. Low temperature-coefficient, gain-setting resistors reduce linearity errors caused by resistance changes due to self-heating. Also, to reduce linearity errors due to finite amplifier gain, use an amplifier circuit with sufficient loop gain at the frequencies of interest (Figures 14, 15, 16).

14-Bit, 85ksps ADC with 10 μ A Shutdown

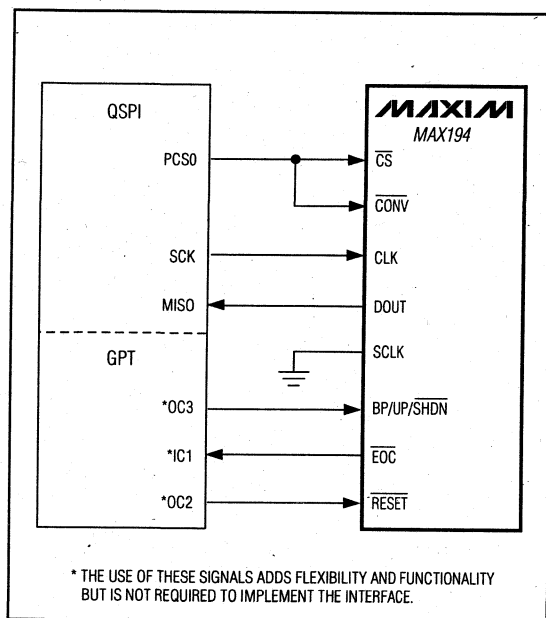


Figure 17. MAX194 Connection to QSPI Processor Clocking Data Out During Conversions

DC Accuracy

If DC accuracy is important, choose a buffer with an offset much less than the MAX194's maximum offset (± 1 LSB = $\pm 488\mu\text{V}$ for a $\pm 4\text{V}$ input range), or whose offset can be trimmed while maintaining good stability over the required temperature range.

Recommended Circuits

Figure 14 shows a good circuit for DC and low-frequency use. The MAX400 has very low offset ($10\mu\text{V}$) and drift ($0.2\mu\text{V}/^\circ\text{C}$), and low voltage noise ($10\text{nV}/\sqrt{\text{Hz}}$) as well. However, its gain-bandwidth product (GBW) is much too low to drive AIN directly, so the analog input is bypassed to present a low impedance at high frequencies. The large bypass capacitor is isolated from the amplifier output by a 100Ω resistor, which provides additional noise filtering. Since the $\pm 15\text{V}$ supplies exceed the AIN range, add protection diodes at AIN.

Figure 15 shows a wide-bandwidth amplifier (MAX427) driving a wideband video buffer, which is capable of driving AIN and a small bypass capacitor (for noise reduction) directly. The video buffer is inside the MAX427's feedback loop, providing good DC accuracy, while the buffer's low output impedance and high current capabil-

ity provide good AC performance. AIN is diode-clamped to the $\pm 5\text{V}$ rails to prevent overvoltage. The MAX427's $15\mu\text{V}$ maximum offset voltage, $0.8\mu\text{V}/^\circ\text{C}$ maximum drift, and less than $5\text{nV}/\sqrt{\text{Hz}}$ noise specifications make this an excellent choice for AC/DC use.

If $\pm 15\text{V}$ supplies are unavailable, Figure 16's circuit works very well with the $\pm 5\text{V}$ analog supplies used by the MAX194. The MAX410 has a minimum $\pm 3.5\text{V}$ common-mode input range, with a similar output voltage swing, which allows use of a reference voltage to 3.5V . The offset voltage ($250\mu\text{V}$), drift ($1\mu\text{V}/^\circ\text{C}$), unity-gain bandwidth (28MHz), and low voltage noise ($2.4\text{nV}/\sqrt{\text{Hz}}$) are appropriate for 14-bit performance. The $0.01\mu\text{F}$ bypass capacitor improves the noise performance.

Operating Modes and SPI/QSPI Interfaces

The two basic interface modes are defined according to whether serial data is received during the conversion (clocked with CLK, SCLK unused) or in bursts between conversions (clocked with SCLK). Each mode is presented interfaced to a QSPI processor, but is also compatible with SPI.

Mode 1 (Simultaneous Conversion and Data Transfer)

In this mode, each data bit is read from the MAX194 during the conversion as it is determined. SCLK is grounded and CLK is used as both the conversion clock and the serial data clock. Figure 17 shows a QSPI processor connected to the MAX194 for use in this mode and Figure 18 is the associated timing diagram.

In addition to the standard QSPI interface signals, general I/O lines are used to monitor $\overline{\text{EOC}}$ and to drive BP/UP/SHDN and RESET. The two general output pins may not be necessary for a given application and, if I/O lines are unavailable, the $\overline{\text{EOC}}$ connection can be omitted as well.

The $\overline{\text{EOC}}$ signal is monitored during calibration to determine when calibration is finished and before beginning a conversion to ensure the MAX194 is not in mid-conversion, but it is possible for a system to ignore $\overline{\text{EOC}}$ completely. On power-up or after pulsing RESET low, the μP must provide 14,000 CLK cycles to complete the calibration sequence (Figure 2). One way to do this is to toggle CLK and monitor $\overline{\text{EOC}}$ until it goes low, but it is possible to simply count 14,000 CLK cycles to complete the calibration. Similarly, it is unnecessary to check the status of $\overline{\text{EOC}}$ before beginning a conversion if you are sure the last conversion is complete. This can be done by ensuring that every conversion consists of at least 20 CLK cycles.

14-Bit, 85ksps ADC with 10µA Shutdown

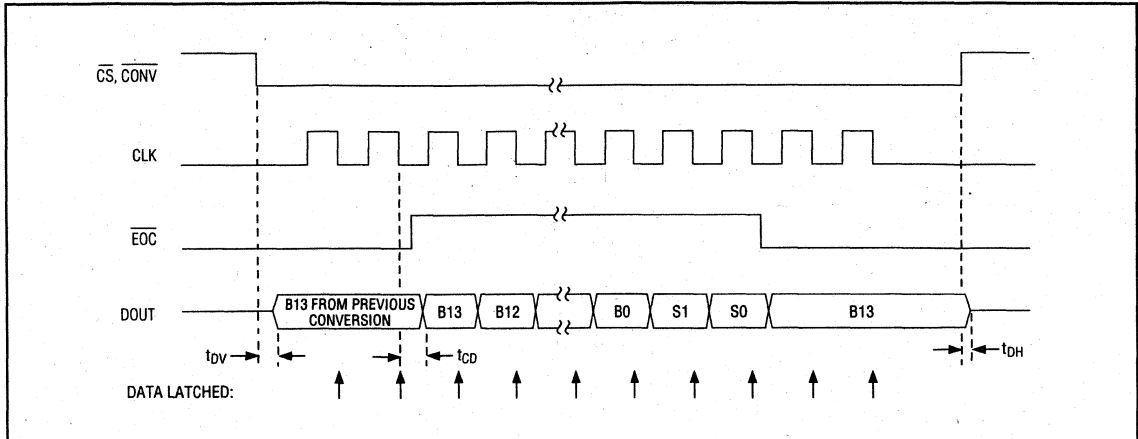


Figure 18. Timing Diagram for Circuit of Figure 17

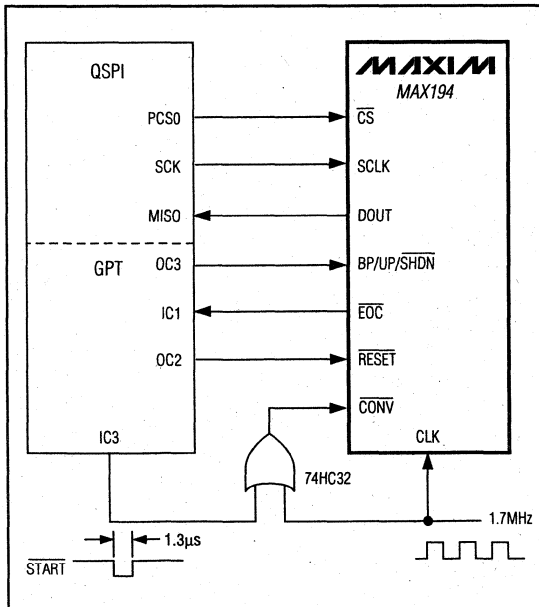


Figure 19. MAX194 Connection to QSPI Processor Clocking Data Out with SCLK Between Conversions

Data is clocked out of the MAX194 on CLK's falling edge and can be clocked into the μP on the rising edge or the following falling edge. If you clock data in on the rising edge (SPI/QSPI with CPOL = 0 and CPHA = 0; standard Microwire: Hitachi H8), the maximum CLK rate is given by:

$$f_{\text{CLK}}(\text{max}) = \frac{1}{2} \times \frac{1}{t_{\text{CD}} + t_{\text{SD}}}$$

where t_{CD} is the MAX194's CLK-to-DOUT valid delay and t_{SD} is the data setup time for your μP .

If clocking data in on the falling edge (CPOL = 0, CPHA = 1), the maximum CLK rate is given by:

$$f_{\text{CLK}}(\text{max}) = \frac{1}{t_{\text{CD}} + t_{\text{SD}}}$$

Do not exceed the maximum CLK frequency given in the *Electrical Characteristics* table. To clock data in on the falling edge, your processor hold time must not exceed t_{CD} minimum (100ns).

While QSPI can provide the required 20 CLK cycles as two continuous 10-bit transfers, SPI is limited to 8-bit transfers. This means that with SPI, a conversion must consist of three 8-bit transfers. Ensure that the pauses between 8-bit operations at your selected clock rate are short enough to maintain a 20ms or shorter conversion time, or the leakage of the capacitive DAC may cause errors.

14-Bit, 85ksps ADC with 10 μ A Shutdown

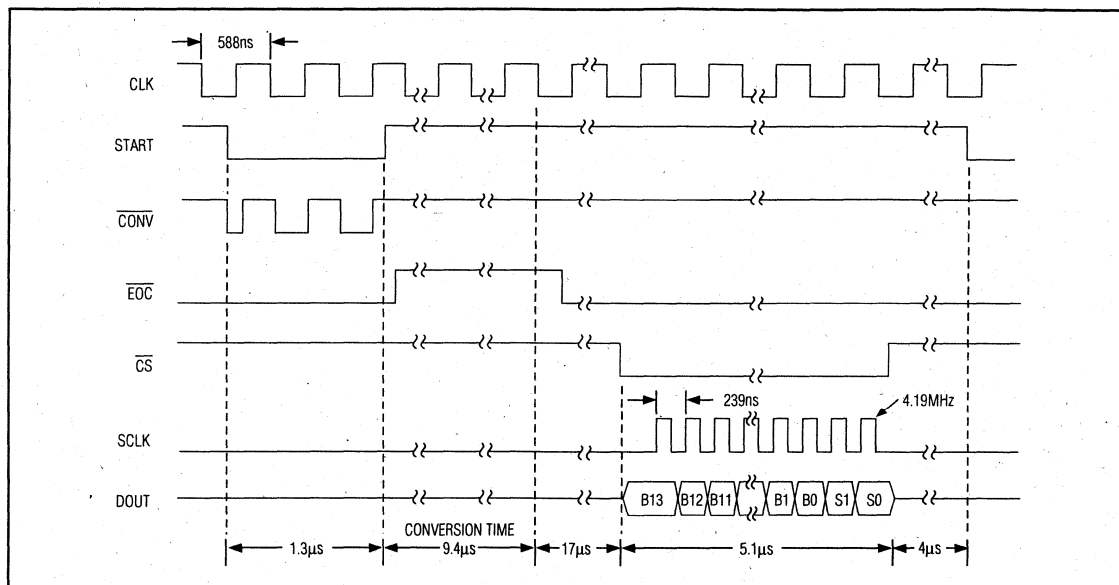


Figure 20. Timing Diagram for Circuit of Figure 19

Complete source code for the Motorola 68HC16 and the MAX194 evaluation kit (EV kit) using this mode is available in the MAX194 EV kit manual.

Mode 2 (Asynchronous Data Transfer)

This mode uses a conversion clock (CLK) and a serial clock (SCLK). The serial data is clocked out between conversions, which reduces the maximum throughput for high CLK rates, but may be more convenient for some applications. Figure 19 is a block diagram with a QSPI processor (Motorola 68HC16) connected to the MAX194. Figure 20 shows the associated timing diagram. Figure 21 gives an assembly language listing for this arrangement.

An OR gate is used to synchronize the "start" signal to the asynchronous CLK, as described in the *External Clock* section. As with Mode 1, the QSPI processor must run CLK during calibration and either count CLK cycles or, as is done here, monitor $\overline{EOC}$ to determine when calibration is complete. Also, $\overline{EOC}$ is polled by the μP to determine when a conversion result is available. When $\overline{EOC}$ goes low, data is clocked out at the highest QSPI data rate (4.19Mbps). After the data is transferred, a new conversion can be initiated whenever desired.

The timing specification for SCLK-to-DOUT valid (t_{SD}) imposes some constraints on the serial interface. At SCLK rates up to 2.5Mbps, data is clocked out of the MAX194 by a falling edge of SCLK and may be clocked into the μP by the next rising edge (CPOL = 0, CPHA = 0). For data rates greater than 2.5Mbps (or for lower rates, if desired) it is necessary to clock data out of the MAX194 on SCLK's falling edge and to clock it into the μP on SCLK's next falling edge (CPOL = 0, CPHA = 1). Also, your processor hold time must not exceed t_{SD} minimum (20ns). As with CLK in mode 1, maximum SCLK rates may not be possible with some interface specifications that are subsets of SPI.

Supplies, Layout, Grounding and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source and at the MAX194, as shown in Figure 22. If the analog and digital supplies come from the same source, isolate the digital supply from the analog supply with a low-value resistor (10 Ω).

14-Bit, 85ksps ADC with 10µA Shutdown

MAX194

7

```
*****
* MAX194 code listing for 68HC16 module and circuit of Figure 19      *
* (C) 1994 Maxim Integrated Products                                  *
*                                                                       *
* Written for use with the Motorola 68HC Macro Assembler - Vers. 4.1 *
* Uses the QSPI in Master mode to read the MAX194.                    *
*****

*****
*
* Pin assignment for MAX194
*
ShdnPin    EQU $20      ; BP/UP = OC3
ResetPin    EQU $10      ; RESET = OC2
EOCPin      EQU $01      ; /EOC/ = IC1
DoutFrom194 EQU $01      ; DOUT  = MISO
SCKto194    EQU $04      ; SCLK  = SCK
CSto194     EQU $08      ; /CS/  = PCS0/\SS\
Start       EQU $04      ; Start = IC3

*****

*
* QSPI initialization parameters
*
SPBR    EQU $2 ; QSPI baud rate = (16.78MHz/(2*SPBR)) = 4.19 MHz
CPOL    EQU $0 ; serial clock is low when idle
CPHA    EQU $0 ; CPOL=CPHA, so data is valid on rising edge of clock
BITS    EQU $10 ; bits per transfer field = 16
DSCKL   EQU $2 ; delay before SCK = (DSCKL/16.78MHz) = 119 nsec
DTL     EQU $1 ; delay after transfer = (DTL*32/16.78MHz) = 1.19 usec
NEWQP   EQU $0 ; pointer to first valid queue entry
ENDQP   EQU $1 ; pointer to last valid queue entry

***
* Start of main program
***

MAIN:

* Initialize the GPT module as a general purpose I/O port
*
    ; GPT pins that are initially high
    ;
    LDAA #(ResetPin)!(ShdnPin)!(Start)
    STAA GPTPDR ; general purpose timer register

    ; GPT pins that are outputs
    ;
    LDAA #(ResetPin)!(ShdnPin)!(Start)
    STAA PDDR ; pin data direction register

* Initialize the QSM / QSPI
*
    ; list of QSM pins that are high by default
    ;
```

Figure 21. MAX194 Code Listing for 68HC16 Module and Circuit of Figure 19

14-Bit, 85ksps ADC with 10 μ A Shutdown

```

LDAA #(CSto194)!(SCKto194)
STAA QPDR                                ; QSPI port data register

; list of pins that are assigned to the QSPI
;
LDAA #(CSto194)!(SCKto194)!(DoutFrom194)
STAA QPAR                                ; QSPI pin assignment register

; list of QSM pins that are outputs
;
LDAA #(CSto194)!(SCKto194)
STAA QDDR                                ; QSPI data direction register

; QSPI Setup - Master Mode
CLR SPCR3                                ; disable halt mode interrupt

LDD #(((BITS)&$0F)*$0400)!(((SPBR)&$FF)!($8000)!((CPOL)*$200)!((CPHA)*$100)
STD SPCR0                                ; QSPI in master mode, 16 bits per transfer, 4Mhz baud rate
; SCK inactive low, data captured on leading edge of SCK

LDD #((DSCKL&$7F)*$100)!(DTL&$FF)
STD SPCR1                                ; delay before SCK = 119ns, delay after transfer = 1.19us

; QSPI Setup - No Wrap
LDD #((ENDQP&$0F)*$100)!(NEWQP&$0F)
STD SPCR2                                ; new queue pointer = 0, end queue pointer =1

*****
*
* Reset the MAX194.
*

BCLR GPTPDR,#ResetPin                    ; take MAX194 RESET pin low

WaitHigh1:
BRCLR GPTPDR,#EOCPin,WaitHigh1            ; wait until EOC goes high

BSET GPTPDR,#ResetPin                    ; take MAX194 RESET pin high

WaitLow1:
BRSET GPTPDR,#EOCPin,WaitLow1             ; wait until EOC goes low

; prime the ReadMAX194 routine by starting a conversion
; pulse start pin(IC3), conversion start command; must be externally sync'd with CLK

BCLR GPTPDR,#Start                        ; clear Start, Start is low
LDAA #2                                    ; loop count (delay >= 2/Fclk)
PulseWidth1:
DECA                                      ; decrement loop count
BNE PulseWidth1
BSET GPTPDR,#Start                        ; set Start, start is high

*****
*
* ReadMAX194:
*

```

Figure 21. MAX194 Code Listing for 68HC16 Module and Circuit of Figure 19 (continued)

14-Bit, 85ksps ADC with 10 μ A Shutdown

```

Loop1:
    BRSET GPTPDR,#EOCPin,Loop1 ; wait until EOC is low

; QSPI Setup - No Wrap
    LDD  #((ENDQP&$0F)*$100)!(NEWQP&$0F)
    STD  SPCR2

; QSPI enable
    BSETW SPCR1,#$8000
    BCLR SPSR,#$80                                ; clear QSPI finished flag (SPIF)

WaitForQSPI:                                ; wait until the QSPI finishes
    BRCLR SPSR,#SPSRSPIF,WaitForQSPI

; start the next conversion
; pulse Start pin (IC3)

    BCLR GPTPDR,#Start                            ; clear Start, Start is low
    LDAA #2                                        ; loop count (delay >= 2/Fclk)
    PulseWidth2:
    DECA                                           ; decrement loop count
    BNE PulseWidth2
    BSET GPTPDR,#Start                            ; set Start, Start is high

    LBRA ReadMAX194                                ; long branch to ReadMAX194

```

Figure 21. MAX194 Code Listing for 68HC16 Module and Circuit of Figure 19 (continued)

Constraints on sequencing the four power supplies are as follows.

- Apply VDDA before VDDD.
- Apply VSSA before VSSD.
- Apply AIN and REF after VDDA and VSSA are present.
- The power supplies should settle within the MAX194's power-on delay (minimum 500ns) or you should recalibrate the converter (pulse RESET low) before use.

Be sure that digital return currents do not pass through the analog ground and that return-current paths are low impedance. A 5mA current flowing through a PC board ground trace impedance of only 0.1 Ω creates an error voltage of about 500 μ V, or about 1LSB error with a ± 4 V full-scale system.

The board layout should ensure as much as possible that digital and analog signal lines are kept separate. Do not run analog and digital (especially clock) lines parallel to one another. If you must cross one with the other, do so at right angles.

The ADC's high-speed comparator is sensitive to high-frequency noise on the VDDA and VSSA power supplies. Bypass these supplies to the analog ground plane with 0.1 μ F in parallel with 1 μ F or 10 μ F low-ESR capacitors. Keep capacitor leads short for best supply-noise rejection.

Shutdown

The MAX194 may be shut down by pulling BP/UP/SHDN low. In addition to lowering power dissipation to 10 μ W (100 μ W max) when the device is not in use, considerable power savings is possible by shutting the converter down for short periods between conversions. There is no need to perform a reset (calibration) after the converter has been shut down unless the time in shutdown is long enough that the supply voltages or ambient temperature may have changed.

The time required for the converter to "wake up" and settle depends heavily on the amount of additional error acceptable. For 0.1LSB additional error, 3.2 μ s is sufficient settling time and also allows enough time for reacquisition of the analog input signal. 20 μ s settling is required for less than 0.05LSB error. Figure 23 is a

14-Bit, 85ksps ADC with 10 μ A Shutdown

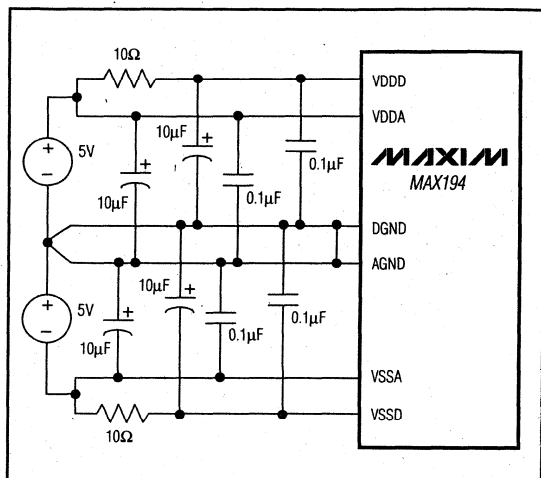


Figure 22. Supply Bypassing and Grounding

graph of theoretical power consumption vs. conversions per second for the MAX194 that assumes the conversion clock is 1.7MHz and the converter is shut down as much as possible between conversions.

Stop CLK before shutting down the MAX194. CLK must be stopped without generating short clock pulses. Short CLK pulses (less than 150ns), or shutting down the MAX194 without stopping CLK, may adversely affect the MAX194's internal calibration data. In applications where CLK is free-running and asynchronous, use the circuit of Figure 24 to stop CLK cleanly.

To minimize the time required to settle and perform a conversion, shut the converter down only after a conversion is finished and the desired mode (unipolar or bipolar) has been set. This ensures that the sampling capacitor array is properly connected to the input signal. If shut down in mid-conversion, when awakened, the MAX194 finishes the old conversion, allows four clock (CLK) cycles for input acquisition, then begins the new conversion.

Dynamic Performance

High-speed sampling capability, 85ksps throughput, and wide dynamic range make the MAX194 ideal for AC applications and signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves

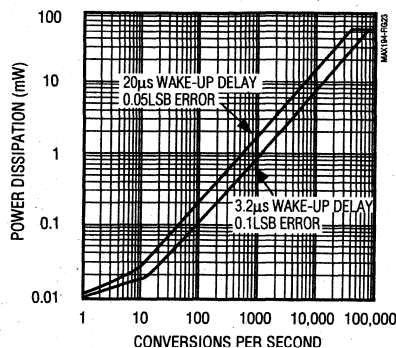


Figure 23. Power Dissipation vs. Conversions/sec When Shutting the MAX194 Down Between Conversions

applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements other than the fundamental input frequency.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample rate. This usually (but not always) includes distortion as well as noise components. For this reason, the ratio is sometimes referred to as Signal-to-Noise + Distortion (SINAD).

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: $SNR = (6.02N + 1.76)dB$, where N is the number of bits of resolution. A perfect 14-bit ADC can, therefore, do no better than 86dB. An FFT plot of the output shows the output level in various spectral bands. Figure 25 shows the result of sampling a pure 1kHz sinusoid at 85ksps with the MAX194.

By transposing the equation that converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "effective number of bits" the ADC provides: $N = (SNR - 1.76) / 6.02$. Substituting SINAD for SNR in this formula results in a better mea-

14-Bit, 85ksps ADC with 10μA Shutdown

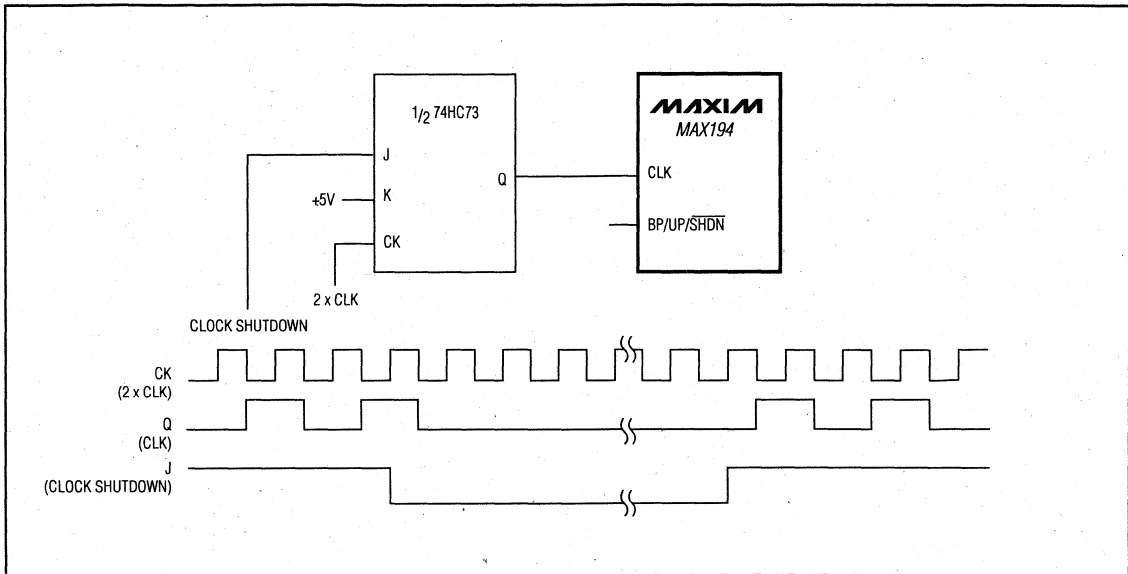


Figure 24. Circuit to Stop Free-Running Asynchronous CLK

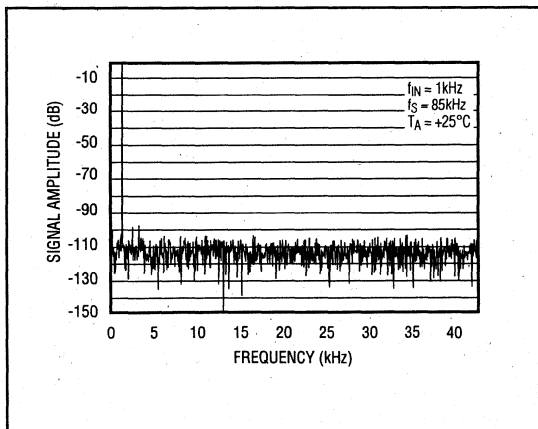


Figure 25. MAX194 FFT Plot

sure of the ADC's usefulness. Figure 26 shows the effective number of bits as a function of the MAX194's input frequency calculated from the SINAD.

Total Harmonic Distortion

If a pure sine wave is input to an ADC, AC integral non-linearity (INL) of an ADC's transfer function results in harmonics of the input frequency being present in the sampled output data.

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* includes the 2nd through 5th harmonics. In the MAX194, this distortion is caused primarily by the changes in on-resistance of the AIN sampling switches with changing input voltage. These resistance changes, together with the DAC's capacitance (which can also vary with input voltage), cause a varying time delay for AC signals, which causes significant distortion at moderately high frequencies (Figure 27).

14-Bit, 85ksps ADC with 10 μ A Shutdown

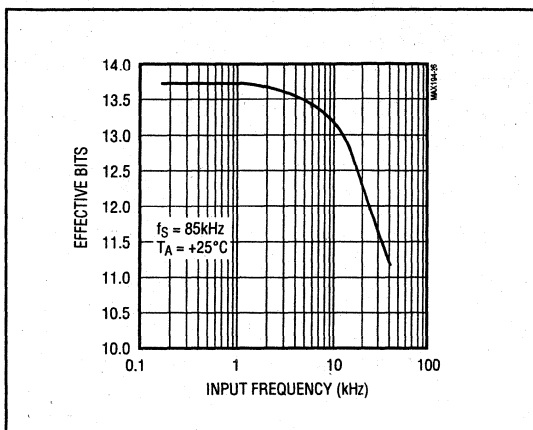


Figure 26. Effective Bits vs. Input Frequency

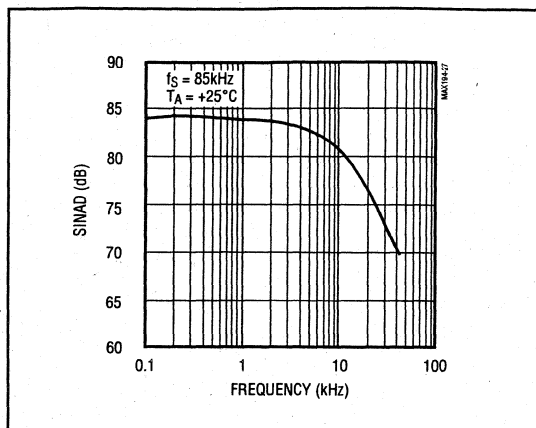


Figure 27. Signal-to-Noise + Distortion vs. Frequency

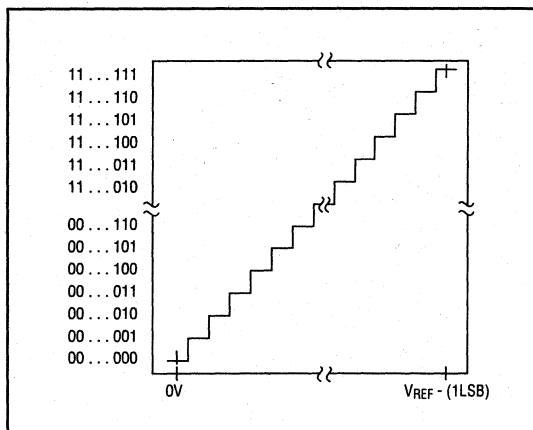


Figure 28. MAX194 Unipolar Transfer Function

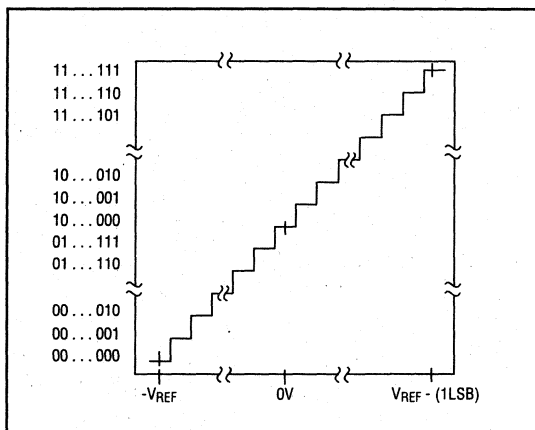


Figure 29. MAX194 Bipolar Transfer Function

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually, this peak occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Transfer Function

Figures 28 and 29 show the MAX194's transfer functions. In unipolar mode, the output data is in binary format and in bipolar mode it is offset binary.

16-Bit, 85ksps ADC with 10 μ A Shutdown

General Description

The MAX195 is a 16-bit successive-approximation analog-to-digital converter (ADC) that combines high speed, high accuracy, low power consumption, and a 10 μ A shutdown mode. Internal calibration circuitry corrects linearity and offset errors to maintain the full rated performance over the operating temperature range without external adjustments. The capacitive-DAC architecture provides an inherent 85ksps track/hold function.

The MAX195, with an external reference (up to +5V), offers a unipolar (0V to VREF) or bipolar (-VREF to VREF) pin-selectable input range. Separate analog and digital supplies minimize digital-noise coupling.

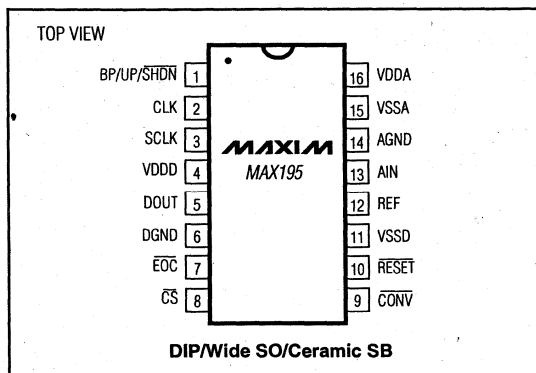
The chip select ($\overline{CS}$) input controls the three-state serial-data output. The output can be read either during conversion as the bits are determined, or following conversion at up to 5Mbps using the serial clock (SCLK). The end-of-conversion (EOC) output can be used to interrupt a processor, or can be connected directly to the convert input (CONV) for continuous, full-speed conversions.

The MAX195 is available in 16-pin DIP, wide SO, and ceramic sidebrazed packages.

Applications

Portable Instruments
Audio
Industrial Controls
Robotics
Multiple Transducer Measurements
Medical Signal Acquisition
Vibrations Analysis
Digital Signal Processing

Pin Configuration



Features

- ◆ 16 Bits, No Missing Codes
- ◆ 90dB SINAD
- ◆ 9.4 μ s Conversion Time
- ◆ 10 μ A (max) Shutdown Mode
- ◆ Built-In Track/Hold
- ◆ AC and DC Specified
- ◆ Unipolar (0V to VREF) and Bipolar (-VREF to VREF) Input Range
- ◆ Three-State Serial-Data Output
- ◆ Small 16-Pin DIP and SO Packages

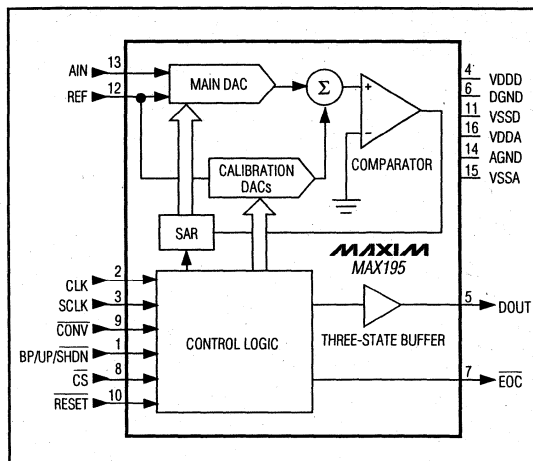
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX195BCPE	0°C to +70°C	16 Plastic DIP
MAX195BCWE	0°C to +70°C	16 Wide SO
MAX195ACDE	0°C to +70°C	16 Ceramic SB
MAX195BC/D	0°C to +70°C	Dice*
MAX195BEPE	-40°C to +85°C	16 Plastic DIP
MAX195BEWE	-40°C to +85°C	16 Wide SO
MAX195AEDE	-40°C to +85°C	16 Ceramic SB
MAX195AMDE	-55°C to +125°C	16 Ceramic SB**
MAX195BMDE	-55°C to +125°C	16 Ceramic SB**

* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

** Contact factory for availability and processing to MIL-STD-883.

Functional Diagram



16-Bit, 85ksps ADC with 10 μ A Shutdown

ABSOLUTE MAXIMUM RATINGS

VDDD to DGND	+7V
VDDA to AGND	+7V
VSSD to DGND	+0.3V to -6V
VSSA to AGND	+0.3V to -6V
VDDD to VDDA, VSSD to VSSA	 $\pm$ 0.3V
AIN, REF	(VSSA - 0.3V) to (VDDA + 0.3V)
AGND to DGND	 $\pm$ 0.3V
Digital Inputs to DGND	-0.3V, (VDDA + 0.3V)
Digital Outputs to DGND	-0.3V, (VDDA + 0.3V)

Continuous Power Dissipation (TA = +70°C)	
Plastic DIP (derate 10.53mW/°C above +70°C)	842mW
Wide SO (derate 9.52mW/°C above +70°C)	762mW
Ceramic SB (derate 10.53mW/°C above +70°C)	842mW
Operating Temperature Ranges	
MAX195_C_E	0°C to +70°C
MAX195_E_E	-40°C to +85°C
MAX195_MDE	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VDDD = VDDA = +5V, VSSD = VSSA = -5V, fCLK = 1.7MHz, VREF = 5V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	RES		16			Bits
Differential Nonlinearity	DNL	MAX195A		$\pm$ 1		LSB
		MAX195B		$\pm$ 2		
Integral Nonlinearity	INL	MAX195A		$\pm$ 0.003		%FSR
		MAX195B		$\pm$ 0.004		
Unipolar/Bipolar Offset Error		MAX195A, VREF = 4.75V		$\pm$ 3		LSB
		MAX195B, VREF = 4.75V		$\pm$ 4		
Unipolar/Bipolar Offset Tempco				0.4		ppm/°C
Unipolar Full-Scale Error		VREF = 4.75V		$\pm$ 0.0075		%FSR
Bipolar Full-Scale Error		VREF = 4.75V		$\pm$ 0.018		%FSR
Full-Scale Tempco				0.1		ppm/°C
Power-Supply Rejection Ratio (VDDA and VSSA only)		VDDA = 4.75V to 5.25V, VREF = 4.75V	65			dB
		VSSA = -5.25V to -4.75V, VREF = 4.75V	65			
ANALOG INPUT						
Input Range		Unipolar	0		VREF	V
		Bipolar	-VREF		VREF	
Input Capacitance		Unipolar		250		pF
		Bipolar		125		
DYNAMIC PERFORMANCE (fs = 85kHz, bipolar range AIN = -5V to +5V, 1kHz) (Note 1)						
Signal-to-Noise plus Distortion Ratio (Note 2)	SINAD	TA = +25°C	87	90		dB
Total Harmonic Distortion (up to the 5th harmonic) (Note 2)	THD	TA = +25°C		-97	-90	dB
Peak Spurious Noise (Note 2)		TA = +25°C			-90	dB
Conversion Time	tCONV	16 x tCLK	9.4			μ s
Clock Frequency (Notes 3, 4)	fCLK			1.7		MHz
Serial Clock Frequency	fSCLK			5		MHz

16-Bit, 85ksps ADC with 10 μ A Shutdown

ELECTRICAL CHARACTERISTICS (continued)

(VDDD = VDDA = +5V, VSSD = VSSA = -5V, fCLK = 1.7MHz, VREF = 5V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CLK, CS, CONV, RESET, SCLK, BP/UP/SHDN)						
CLK, CS, CONV, RESET, SCLK Input High Voltage	VIH	VDDD = 5.25V	2.4			V
CLK, CS, CONV, RESET, SCLK Input Low Voltage	VIL	VDDD = 4.75V			0.8	V
CLK, CS, CONV, RESET, SCLK Input Capacitance (Note 3)					10	pF
CLK, CS, CONV, RESET, SCLK Input Current		Digital inputs = 0V or 5V			± 10	μ A
BP/UP/SHDN Input High Voltage	VIH		VDDD - 0.5			V
BP/UP/SHDN Input Low Voltage	VIL				0.5	V
BP/UP/SHDN Input Current, High	IiH	BP/UP/SHDN = VDDD			4.0	μ A
BP/UP/SHDN Input Current, Low	IiL	BP/UP/SHDN = 0V	-4.0			μ A
BP/UP/SHDN Mid Input Voltage	VIM		1.5	VDDD - 1.5		V
BP/UP/SHDN Voltage, Floating	VFLT	BP/UP/SHDN = open		2.75		V
BP/UP/SHDN Max Allowed Leakage, Mid Input		BP/UP/SHDN = open	-100		+100	nA
DIGITAL OUTPUTS (DOUT, EOC)						
Output Low Voltage	VOL	VDDD = 4.75V, ISINK = 1.6mA			0.4	V
Output High Voltage	VOH	VDDD = 4.75V, ISOURCE = 1mA	VDDD - 0.5			V
DOUT Leakage Current	ILKG	DOUT = 0V or 5V			± 10	μ A
Output Capacitance (Note 2)					10	pF
POWER REQUIREMENTS						
VDDD			4.75		5.25	V
VSSD			-5.25		-4.75	V
VDDA		By supply-rejection test	4.75		5.25	V
VSSA		By supply-rejection test	-5.25		-4.75	V
VDDD Supply Current	IDD	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		2.5	4	mA
VSSD Supply Current	ISSD	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		0.9	2	mA
VDDA Supply Current	IDDA	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		3.8	5	mA
VSSA Supply Current	ISSA	VDDD = VDDA = 5.25V, VSSD = VSSA = -5.25V		3.8	5	mA

MAX195

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16-Bit, 85ksps ADC with 10 μ A Shutdown

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDD} = V_{DDA} = +5V, V_{SSD} = V_{VSSA} = -5V, f_{CLK} = 1.7MHz, V_{REF} = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS (cont.)						
Power Dissipation		V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V			80	mW
V _{DDD} Shutdown Supply Current (Note 5)	I _{DDD}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		1.6	5	μ A
V _{SSD} Shutdown Supply Current	I _{SSD}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		0.1	5	μ A
V _{DDA} Shutdown Supply Current	I _{DDA}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		0.1	5	μ A
V _{VSSA} Shutdown Supply Current	I _{VSSA}	V _{DDD} = V _{DDA} = 5.25V, V _{SSD} = V _{VSSA} = -5.25V, BP/UP/SHDN = 0V		0.1	5	μ A

Note 1: Accuracy and dynamic performance tests performed after calibration.

Note 2: Guaranteed by design, not tested.

Note 3: Tested with 50% duty cycle. Duty cycles from 25% to 75% at 1.7MHz are acceptable.

Note 4: See *External Clock* section.

Note 5: Measured in shutdown mode with CLK and SCLK low.

TIMING CHARACTERISTICS

(V_{DDD} = V_{DDA} = +5V, V_{SSD} = V_{VSSA} = -5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T _A = +25°C TYP	T _A = 0°C to +70°C		T _A = -40°C to +85°C		T _A = -55°C to +125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
CONV Pulse Width	t _{CW}			20		30		35		ns
CONV to CLK Falling Synchronization (Note 2)	t _{CC1}				10		10		10	ns
CONV to CLK Rising Synchronization (Note 2)	t _{CC2}				40		40		40	ns
Data Access Time	t _{DV}	C _L = 50pF			80		80		90	ns
Bus Relinquish Time	t _{DH}	C _L = 10pF			40		40		40	ns
CLK to EOC High	t _{CEH}	C _L = 50pF			300		300		350	ns
CLK to EOC Low	t _{CEL}	C _L = 50pF			300		300		350	ns
CLK to DOUT Valid	t _{CD}	C _L = 50pF		100	350	100	375	100	400	ns
SCLK to DOUT Valid	t _{SD}	C _L = 50pF		20	140	20	160	20	160	ns
$\overline{\text{CS}}$ to SCLK Setup Time	t _{CSS}			75		75		75		ns
$\overline{\text{CS}}$ to SCLK Hold Time	t _{CSH}			-10		-10		-10		ns
Acquisition Time	t _{AQ}			2.4		2.4		2.4		μ s
Calibration Time	t _{CAL}	14,000 $\times$ t _{CLK}		8.2		8.2		8.2		ms
RESET to CLK Setup Time	t _{RCS}			-40		-40		-40		ns
RESET to CLK Hold Time	t _{RCH}			120		120		120		ns
Start-Up Time (Note 6)	t _{SU}	Exiting shutdown	50							μ s

Note 6: Settling time required after deasserting shutdown to achieve less than 0.1LSB additional error.

16-Bit, 85ksps ADC with 10 μ A Shutdown

Pin Description

MAX195

PIN	NAME	FUNCTION
1	BP/UP/SHDN	Bipolar/Unipolar/Shutdown Input. Three-state input selects bipolar or unipolar input range, or shutdown. 0V = shutdown, +5V = unipolar, floating = bipolar.
2	CLK	Conversion Clock Input
3	SCLK	Serial Clock Input is used to shift data out between conversions. May be asynchronous to CLK.
4	VDDD	+5V Digital Power Supply
5	DOUT	Serial Data Output, MSB first
6	DGND	Digital Ground
7	EOC	End-of-Conversion/Calibration Output—normally low. Rises one clock cycle after the beginning of conversion or calibration and falls one clock cycle after the end of either. May be used as an output framing signal.
8	$\overline{CS}$	Chip-Select Input—active low. Enables the serial interface and the three-state data output (DOUT).
9	$\overline{CONV}$	Convert-Start Input—active low. Conversion begins on the falling edge after $\overline{CONV}$ goes low if the input signal has been acquired; otherwise, on the falling clock edge after acquisition.
10	RESET	Reset Input. Pulling RESET low places the ADC in an inactive state. Rising edge resets control logic and begins calibration.
11	VSSD	-5V Digital Power Supply
12	REF	Reference Input, 0V to 5V
13	AIN	Analog Input, 0V to VREF unipolar or $\pm VREF$ bipolar range
14	AGND	Analog Ground
15	VSSA	-5V Analog Power Supply
16	VDDA	+5V Analog Power Supply

Detailed Description

The MAX195 uses a successive-approximation register (SAR) to convert an analog input to a 16-bit digital code, which is output as a serial data stream. The data bits can be read either during the conversion, at the CLK clock rate, or between conversions asynchronous with CLK at the SCLK rate (up to 5Mbps).

The MAX195 includes a capacitive digital-to-analog converter (DAC) that provides an inherent track/hold input. The interface and control logic are designed for easy connection to most microprocessors (μ Ps), limiting the need for external components. In addition to the SAR and DAC, the MAX195 includes a serial interface, a sampling comparator used by the SAR, ten calibration DACs, and control logic for calibration and conversion.

The DAC consists of an array of 16 capacitors with binary weighted values plus one "dummy LSB" capacitor (Figure 1). During input acquisition in unipolar mode, the array's common terminal is connected to AGND and all free terminals are connected to the input signal (AIN). After acquisition, the common terminal is disconnected from AGND and the free terminals are

disconnected from AIN, trapping a charge proportional to the input voltage on the capacitor array.

The free terminal of the MSB (largest) capacitor is connected to the reference (REF), which pulls the common terminal (connected to the comparator) positive. Simultaneously, the free terminals of all other capacitors in the array are connected to AGND, which drives the comparator input negative. If the analog input is near VREF, connecting the MSB's free terminal to REF only pulls the comparator input slightly positive. However, connecting the remaining capacitor's free terminals to ground drives the comparator input well below ground, so the comparator input is negative, the comparator output is low, and the MSB is set high. If the analog input is near ground, the comparator output is high and the MSB is low.

Following this, the next largest capacitor is disconnected from AGND and connected to REF, and the comparator determines the next bit. This continues until all bits have been determined. For a bipolar input range, the MSB capacitor is connected to REF rather than AIN during input acquisition, which results in an input range of VREF to -VREF.

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16-Bit, 85ksps ADC with 10 μ A Shutdown

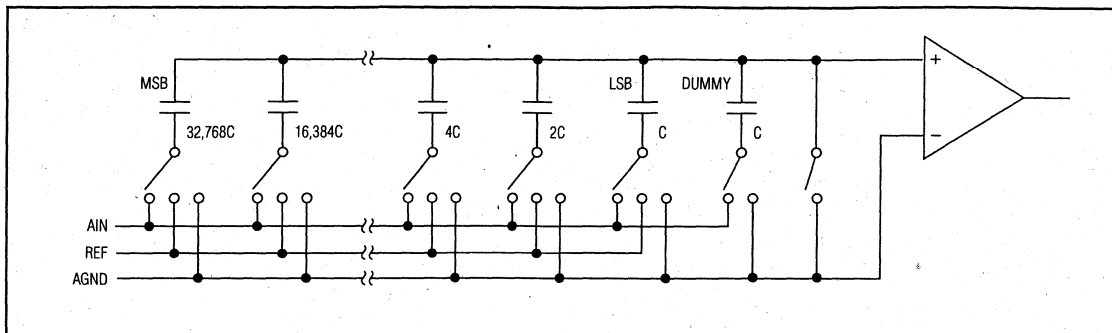


Figure 1. Capacitor DAC Functional Diagram

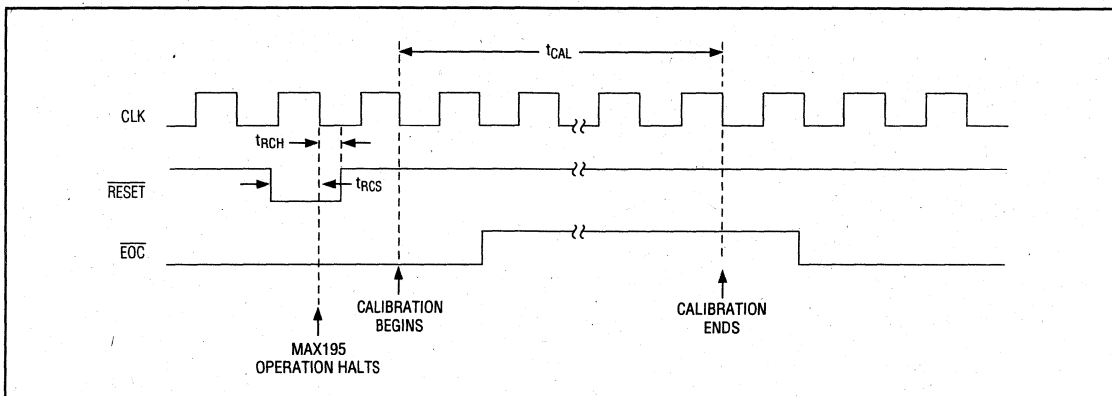


Figure 2. Initiating Calibration

Calibration

In an ideal DAC, each of the capacitors associated with the data bits would be exactly twice the value of the next smaller capacitor. In practice, this results in a range of values too wide to be realized in an economically feasible size. The capacitor array actually consists of two arrays, which are capacitively coupled to reduce the LSB array's effective value. The capacitors in the MSB array are production trimmed to reduce errors. Small variations in the LSB capacitors contribute insignificant errors to the 16-bit result.

Unfortunately, trimming alone does not yield 16-bit performance or compensate for changes in performance due to changes in temperature, supply voltage, and other parameters. For this reason, the MAX195 includes a calibration DAC for each capacitor in the MSB array. These DACs are capacitively coupled to the main DAC

output and offset the main DAC's output according to the value on their digital inputs. During calibration, the correct digital code to compensate for the error in each MSB capacitor is determined and stored. Thereafter, the stored code is input to the appropriate calibration DAC whenever the corresponding bit in the main DAC is high, compensating for errors in the associated capacitor.

The MAX195 calibrates automatically on power-up. To reduce the effects of noise, each calibration experiment is performed many times and the results are averaged. Calibration requires about 14,000 clock cycles, or 8.2ms at the highest clock (CLK) speed (1.7MHz). In addition to the power-up calibration, bringing RESET low halts MAX195 operation, and bringing it high again initiates a calibration (Figure 2).

16-Bit, 85ksps ADC with 10 μ A Shutdown

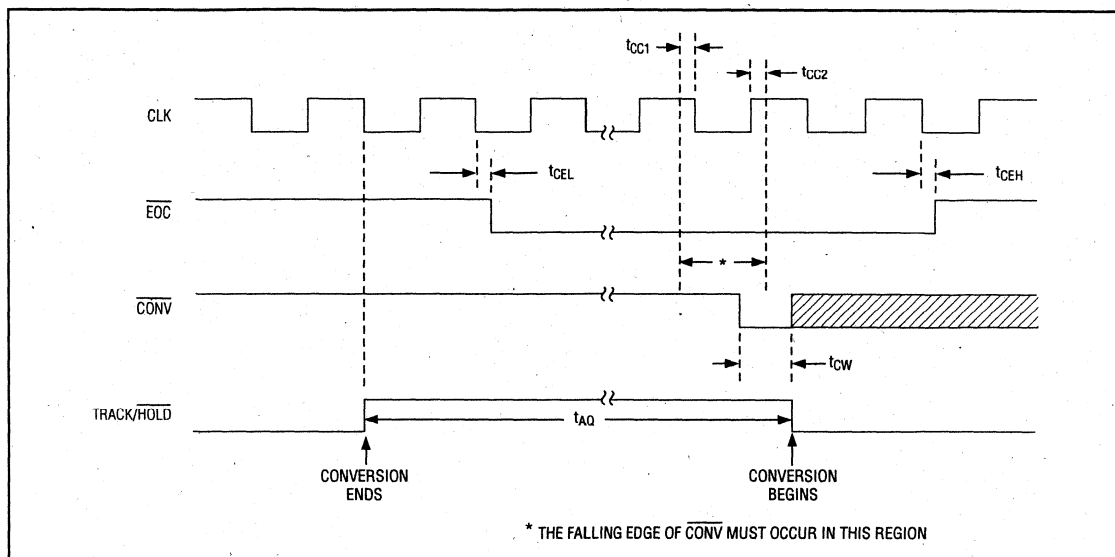


Figure 3. Initiating Conversions—At least 3 CLK cycles since end of previous conversion.

If the power supplies do not settle within the MAX195's power-on delay (500ns minimum), power-up calibration may begin with supply voltages that differ from the final values and the converter may not be properly calibrated. If so, recalibrate the converter (pulse $\overline{\text{RESET}}$ low) before use. For best DC accuracy, calibrate the MAX195 any time there is a significant change in supply voltages, temperature, reference voltage, or clock characteristics (see *External Clock* section) because these parameters affect the DC offset. If linearity is the only concern, much larger changes in these parameters can be tolerated.

Because the calibration data is stored digitally, there is no need either to perform frequent conversions to maintain accuracy or to recalibrate if the MAX195 has been held in shutdown for long periods. However, recalibration is recommended if it is likely that ambient temperature or supply voltages have significantly changed since the previous calibration.

Digital Interface

The digital interface pins consist of $\overline{\text{BP/UP/SHDN}}$, CLK, SCLK, EOC, CS, CONV, and RESET.

$\overline{\text{BP/UP/SHDN}}$ is a three-level input. Leave it floating to configure the MAX195's analog input in bipolar mode ($\text{AIN} = -V_{\text{REF}}$ to V_{REF}) or connect it high for a unipolar

input ($\text{AIN} = 0V$ to V_{REF}). Bringing $\overline{\text{BP/UP/SHDN}}$ low places the MAX195 in its 10 μ A shutdown mode.

A logic low on $\overline{\text{RESET}}$ halts MAX195 operation. The rising edge of $\overline{\text{RESET}}$ initiates calibration as described in the *Calibration* section above.

Begin a conversion by bringing $\overline{\text{CONV}}$ low. After conversion begins, additional convert start pulses are ignored. The convert signal must be synchronized with CLK. The falling edge of $\overline{\text{CONV}}$ must occur during the period shown in Figures 3 and 4. When CLK is not directly controlled by your processor, two methods of ensuring synchronization are to drive $\overline{\text{CONV}}$ from EOC (continuous conversions) or to gate the conversion-start signal with the conversion clock so that $\overline{\text{CONV}}$ can go low only while CLK is low (Figure 5). Ensure that the maximum propagation delay through the gate is less than 40ns.

The MAX195 automatically ensures four CLK periods for track/hold acquisition. If, when $\overline{\text{CONV}}$ is asserted, at least three clock (CLK) cycles have passed since the end of the previous conversion, a conversion will begin on CLK's next falling edge and EOC will go high on the following falling CLK edge (Figure 3). If, when convert is asserted, less than three clock cycles have passed, a conversion will begin on the fourth falling clock edge

16-Bit, 85ksps ADC with 10 μ A Shutdown

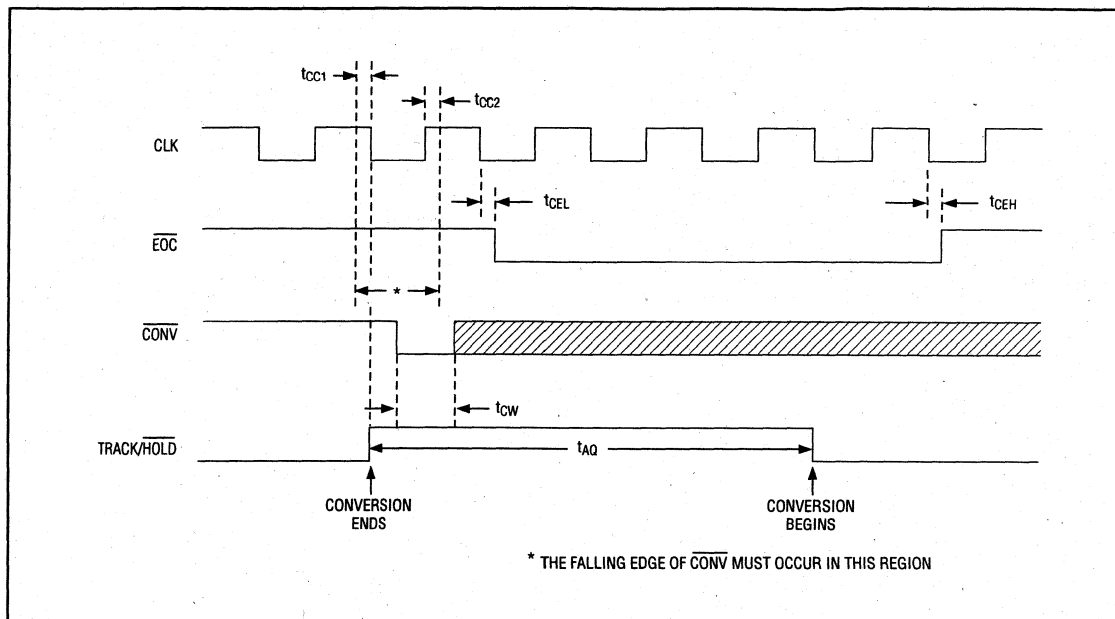


Figure 4. Initiating Conversions—Less than 3 CLK cycles since end of previous conversion.

after the end of the previous conversion and $\overline{EOC}$ will go high on the following CLK falling edge (Figure 4).

External Clock

The conversion clock (CLK) should have a duty cycle between 25% and 75% at 1.7MHz (the maximum clock frequency). For lower frequency clocks, ensure the minimum high and low times exceed 150ns. The minimum clock rate for accurate conversion is 125Hz for temperatures up to +70°C or 1kHz at +125°C due to leakage of the sampling capacitor array. In addition, CLK should not remain high longer than 50ms at temperatures up to +70°C or 500 μ s at +125°C. If CLK is held high longer than this, RESET must be pulsed low to initiate a recalibration because it is possible that state information stored in internal dynamic memory may be lost. The MAX195's clock can be stopped indefinitely if it is held low.

If the frequency, duty cycle, or other aspects of the clock signal's shape change, the offset created by coupling between CLK and the analog inputs (AIN and REF) changes. Recalibration corrects for this offset and restores DC accuracy.

Output Data

The conversion result, clocked out MSB first, is available on DOUT only when $\overline{CS}$ is held low. Otherwise, DOUT is in a high-impedance state. There are two ways to read the data on DOUT. To read the data bits as they are determined (at the CLK clock rate), hold $\overline{CS}$ low during the conversion. To read results between conversions, hold $\overline{CS}$ low and clock SCLK at up to 5MHz.

If you read the serial data bits as they are determined, $\overline{EOC}$ frames the data bits (Figure 6). Conversion begins with the first falling CLK edge, after CONV goes low and the input signal has been acquired. Data bits are shifted out of DOUT on subsequent falling CLK edges. Clock data in on CLK's rising edge or, if the clock speed is greater than 1MHz, on the following falling edge of CLK to meet the maximum CLK-to-DOUT timing specification. See the *Operating Modes and SPI/QSPI Interfaces* section for additional information. Reading the serial data during the conversion results in the maximum conversion throughput, because a new conversion can begin immediately after the input acquisition period following the previous conversion.

16-Bit, 85ksps ADC with 10 μ A Shutdown

MAX195

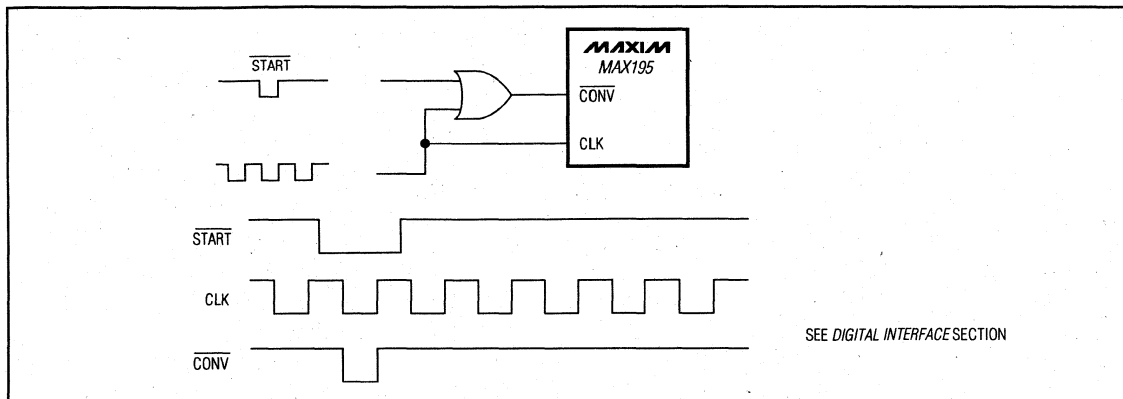


Figure 5. Gating $\overline{\text{CONV}}$ to Synchronize with CLK

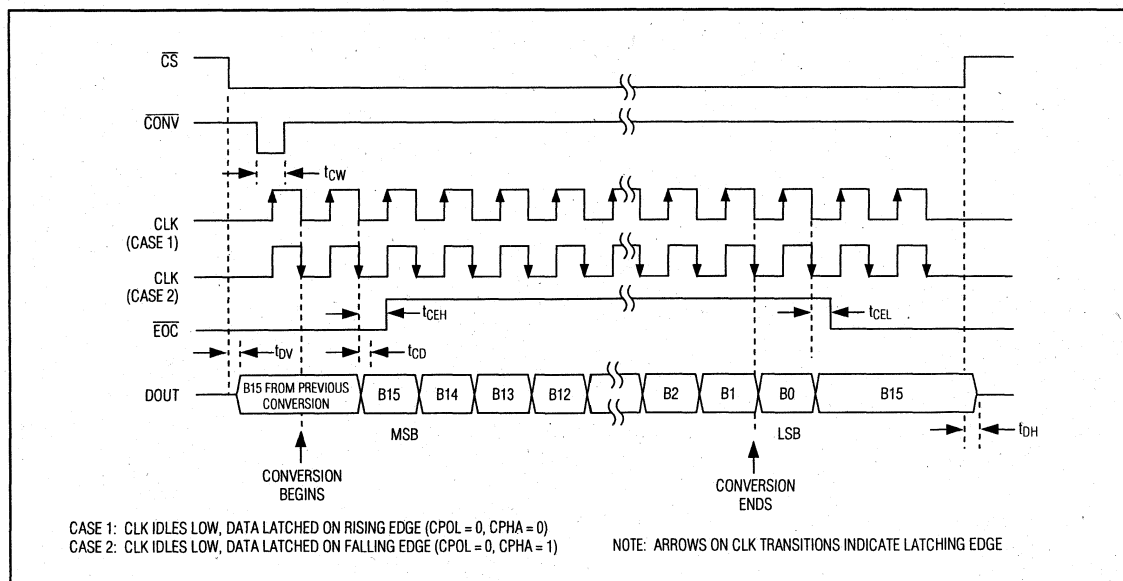


Figure 6. Output Data Format, Reading Data During Conversion (Mode 1)

If you read the data bits between conversions, you can:

- 1) count CLK cycles until the end of the conversion, or
- 2) poll $\overline{\text{EOC}}$ to determine when the conversion is finished, or
- 3) generate an interrupt on $\overline{\text{EOC}}$'s falling edge.

Note that the MSB conversion result appears at DOUT after CS goes low, but **before** the first SCLK pulse. Each subsequent SCLK pulse shifts out the next conversion bit. The 15th SCLK pulse shifts out the LSB. Additional clock pulses shift out zeros.

16-Bit, 85ksps ADC with 10 μ A Shutdown

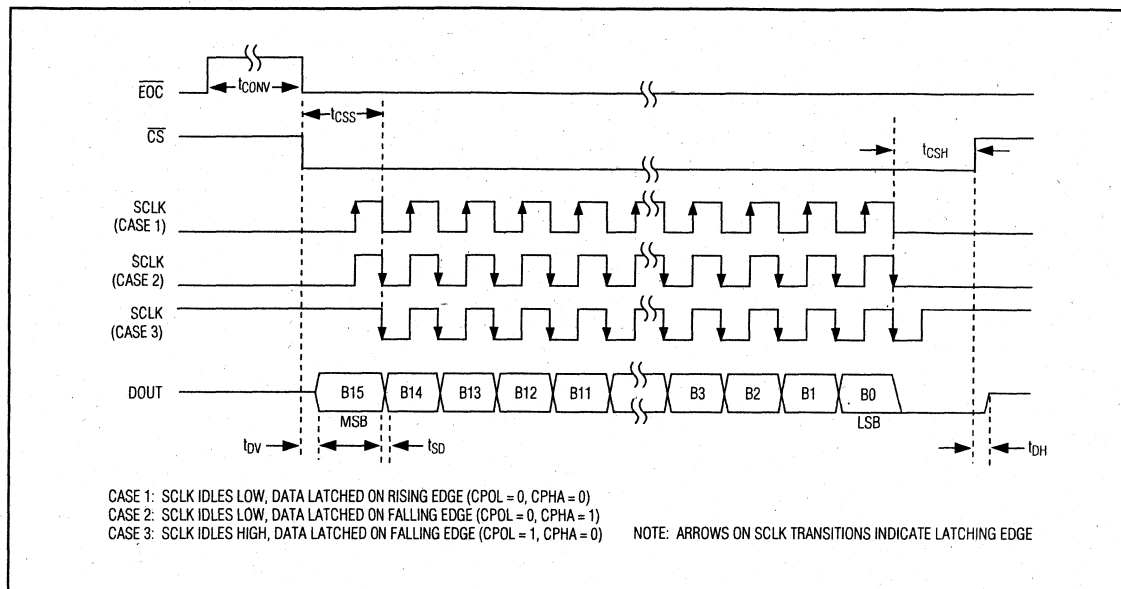


Figure 7. Output Data Format, Reading Data Between Conversions (Mode 2)

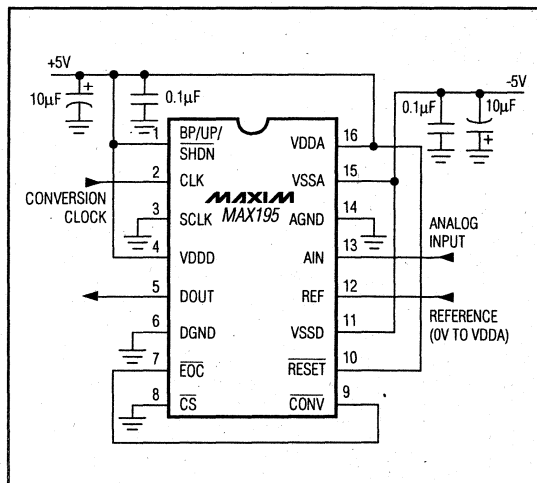


Figure 8. MAX195 in the Simplest Operating Configuration

Data is clocked out on SCLK's falling edge. Clock data in on SCLK's rising edge or, for clock speeds above 2.5MHz, on the following falling edge to meet the maximum SCLK-to-DOUT timing specification (Figure 7). The maximum SCLK speed is 5MHz. See the *Operating Modes and SPI/QSPI Interfaces* section for additional information. When the conversion clock is near its maximum (1.7MHz), reading the data after each conversion (during the acquisition time) results in lower throughput (about 70ksps max) than reading the data during conversions, because it takes longer than the minimum input acquisition time (four cycles at 1.7MHz) to clock 16 data bits at 5Mbps. After the data has been clocked in, leave some time (about 1 μ s) for any coupled noise on AIN to settle before beginning the next conversion.

Whichever method is chosen for reading the data, conversions can be individually initiated by bringing CONV low, or they can occur continuously by connecting EOC to CONV. Figure 8 shows the MAX195 in its simplest operational configuration.

16-Bit, 85ksps ADC with 10 μ A Shutdown

Table 1. Low-ESR Capacitor Suppliers

COMPANY	CAPACITOR	FACTORY FAX [COUNTRY CODE]	USA TELEPHONE
Sprague	595D series, 592D series	[1] (603) 224-1430	(603) 224-1961
AVX	TPS series	[1] (207) 283-1941	(800) 282-4975
Sanyo	OS-CON series, MVGX series	[81] 7-2070-1174	(619) 661-6835
Nichicon	PL series	[1] (708) 843-2798	(708) 843-7500

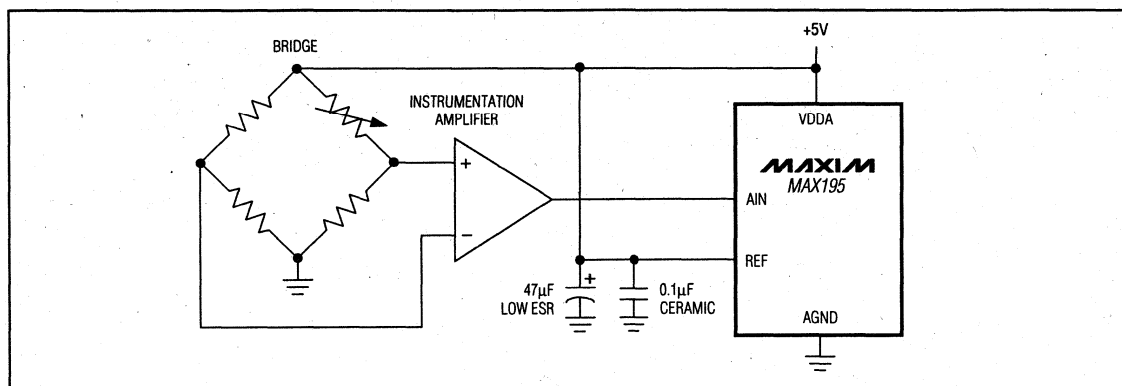


Figure 9. Ratiometric Measurement Without an Accurate Reference

Applications Information

Reference

The MAX195 reference voltage range is 0V to VDDA. When choosing the reference voltage, the MAX195's equivalent input noise (40 μ V_{RMS} in unipolar mode, 80 μ V_{RMS} in bipolar mode) should be considered. Also, if VREF exceeds VDDA, errors will occur due to the internal protection diodes that will begin to conduct, so use caution when using a reference near VDDA (unless VREF and VDDA are virtually identical). VREF must never exceed its absolute maximum rating (VDDA + 0.3V).

The MAX195 needs a good reference to achieve its rated performance. The most important requirement is that the reference must present a low impedance to the REF input. This is often achieved by buffering the reference through an op amp and bypassing the REF input with a large (1 μ F to 47 μ F), low-ESR capacitor in parallel with a 0.1 μ F ceramic capacitor. Low-ESR capacitors are available from the manufacturers listed in Table 1.

The reference must drive the main conversion DAC capacitors as well as the capacitors in the calibration

DACs, all of which may be switching between GND and REF at the conversion clock frequency. The total capacitive load presented can exceed 1000pF and, unlike the analog input (AIN), REF is sampled continuously throughout the conversion.

The first step in choosing a reference circuit is to decide what kind of performance is required. This often suggests compromises made in the interests of cost and size. It is possible that a system may not require an accurate reference at all. If a system makes a ratiometric measurement such as Figure 9's bridge circuit, any relatively noise-free voltage that presents a low impedance at the REF input will serve as a reference. The +5V analog supply suffices if you use a large, low-impedance bypass capacitor to keep REF stable during switching of the capacitor arrays. Do not place a resistance between the +5V supply and the bypass capacitor, because it will cause linearity errors due to the dynamic REF input current, which typically ranges from 300 μ A to 400 μ A.

Figure 10 shows a more typical scheme that provides good AC accuracy. The MAX874's initial accuracy can

16-Bit, 85ksps ADC with 10 μ A Shutdown

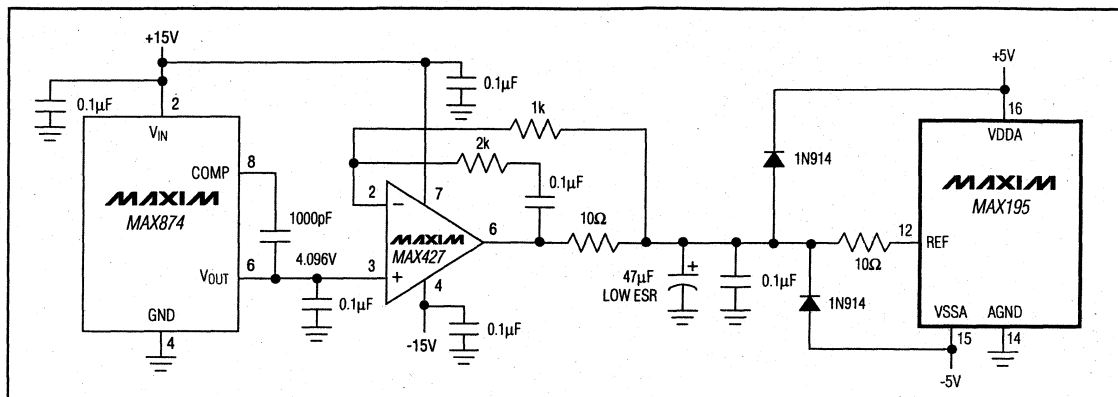


Figure 10. Typical Reference Circuit for AC Accuracy

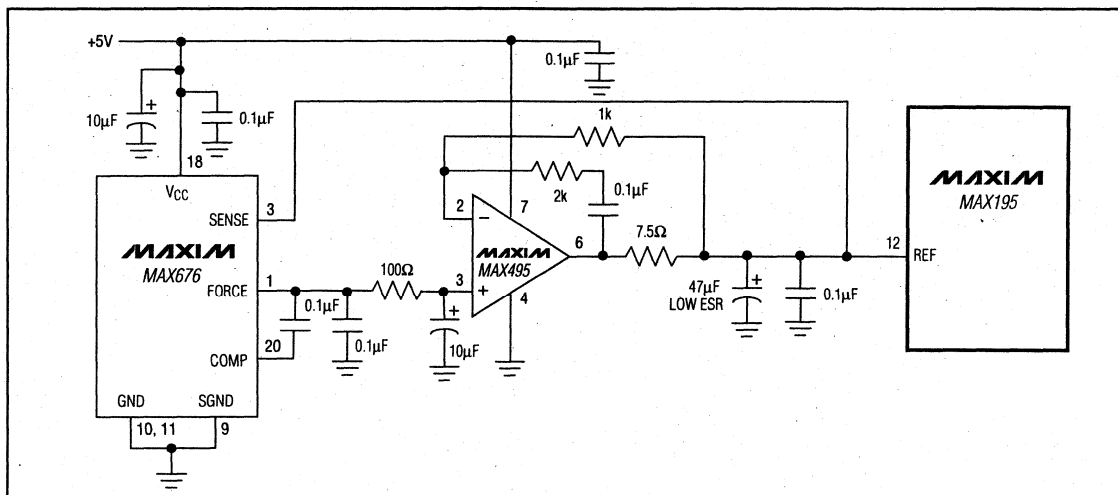


Figure 11. High-Accuracy Reference Runs from Single +5V Supply

be improved by trimming, but the drift is too great to provide good stability over temperature. The MAX427 buffer provides the necessary drive current to stabilize the REF input quickly after capacitance changes.

The reference inaccuracies contribute additional full-scale error. A reference with less than $1/2^{16}$ total error (15 parts per million) over the operating temperature range is required to limit the additional error to less than 1LSB. The MAX676, which utilizes an on-chip ROM to calibrate for drift, achieves a drift specification

of 1ppm/°C. This allows reasonable temperature changes with less than 1LSB error. While the MAX676's initial-accuracy specification (0.01%) results in an offset error of about ± 7 LSB, the reference voltage can be trimmed or the offset can be corrected in software if absolute DC accuracy is essential. Figure 11's circuit provides outstanding temperature stability as well as excellent DC accuracy if the initial error is corrected. The MAX495 buffer is placed inside the MAX676's feedback loop so the buffer's offset does not cause additional error.

16-Bit, 85ksps ADC with 10 μ A Shutdown

MAX195

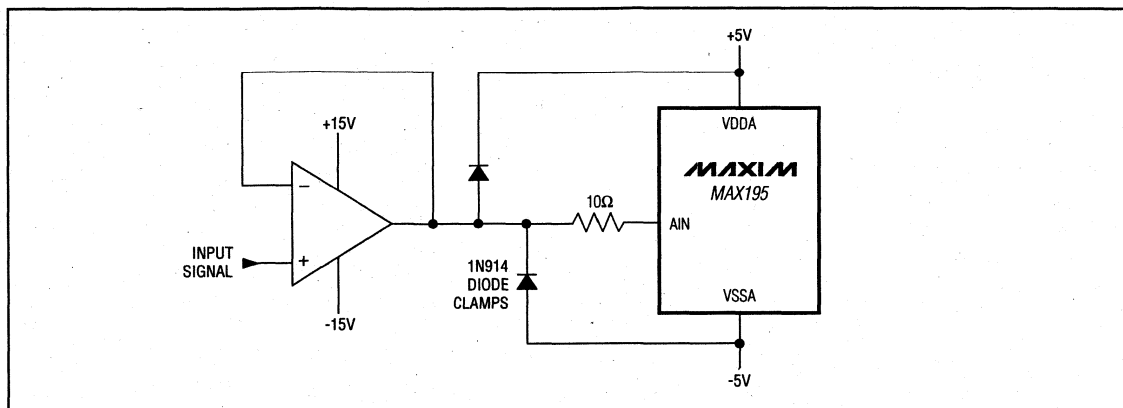


Figure 12. Analog Input Protection for Overvoltage or Improper Supply Sequence

REF and AIN Input Protection

The REF and AIN signals should not exceed the MAX195 supply rails. If this can occur, diode clamp the signal to the supply rails. Use silicon diodes and a 10 Ω current-limiting resistor (Figures 10 and 12) or Schottky diodes without the resistor.

When using the current-limiting resistor, place the resistor between the appropriate input (AIN or REF) and any bypass capacitor. While this results in AC transients at the input due to dynamic input currents, the transients settle quickly and do not affect conversion results. Improperly placing the bypass capacitor directly at the input forms an RC lowpass filter with the current-limiting resistor, which averages the dynamic input current and causes linearity errors.

Analog Input

The MAX195 uses a capacitive DAC that provides an inherent track/hold function. The input impedance is typically 30 Ω in series with 250pF in unipolar mode and 50 Ω in series with 125pF in bipolar mode.

Input Range

The analog input range can be either unipolar (0V to VREF) or bipolar (-VREF to VREF), depending on the state of the BP/UP/SHDN pin (see *Digital Interface* section). The reference range is 0V to VDDA. When choosing the reference voltage, the equivalent MAX195 input noise (40 μ V_{RMS} in unipolar mode, 80 μ V_{RMS} in bipolar mode) should be considered.

Input Acquisition and Settling

Four conversion-clock periods are allocated for acquiring the input signal. At the highest conversion rate, four clock periods is 2.4 μ s. If more than three clock cycles have occurred since the end of the previous conversion, conversion begins on the next falling clock edge after $\overline{\text{CONV}}$ goes low. Otherwise, bringing $\overline{\text{CONV}}$ low begins a conversion on the fourth falling clock edge after the previous conversion. This scheme ensures the minimum input acquisition time is four clock periods.

Most applications require an input buffer amplifier. If the input signal is multiplexed, the input channel should be switched near the beginning of a conversion, rather than near the end of or after a conversion (Figure 13). This allows time for the input buffer amplifier to respond to a large step change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change *before* the beginning of the acquisition time.

At the beginning of acquisition, the capacitive DAC is connected to the amplifier output, causing some output disturbance. Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the capacitive DAC with very little change in voltage (Figure 14). However, for AC use, AIN must be driven by a wideband buffer (at least 10MHz), which must be stable with the DAC's capacitive load (in parallel with any AIN bypass capacitor used) and also must settle quickly (Figure 15 or 16).

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16-Bit, 85ksps ADC with 10 μ A Shutdown

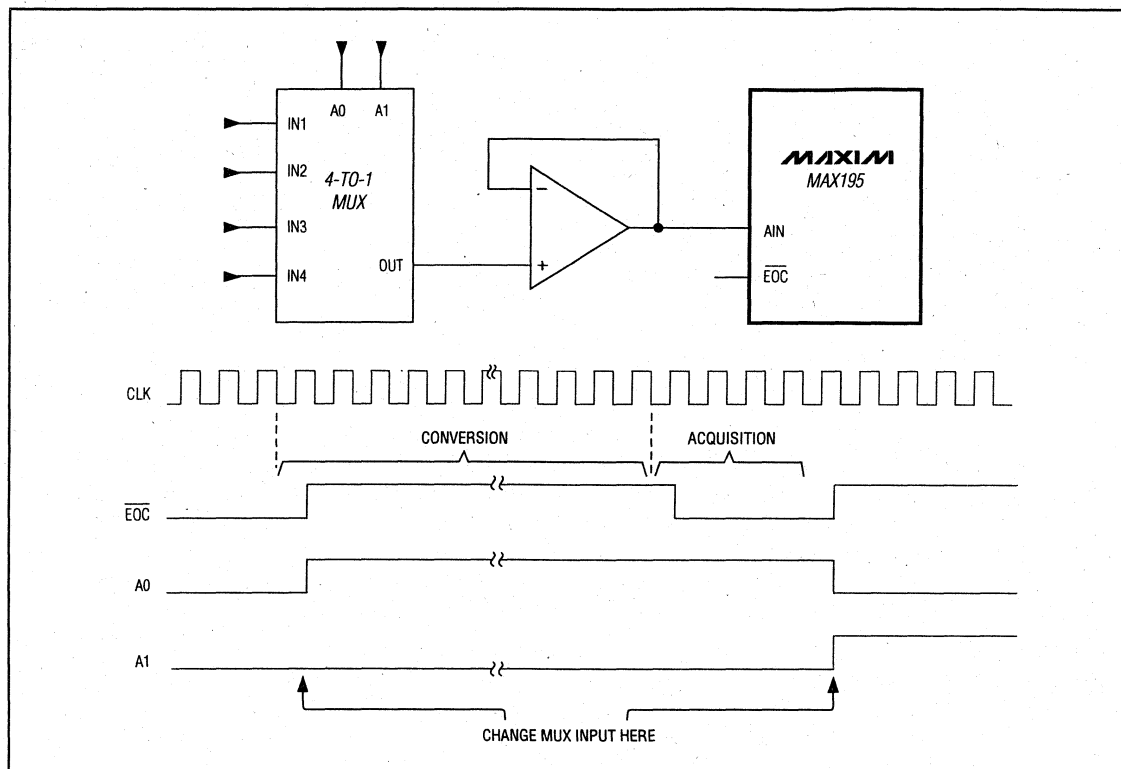


Figure 13. Change multiplexer input near beginning of conversion to allow time for slewing and settling.

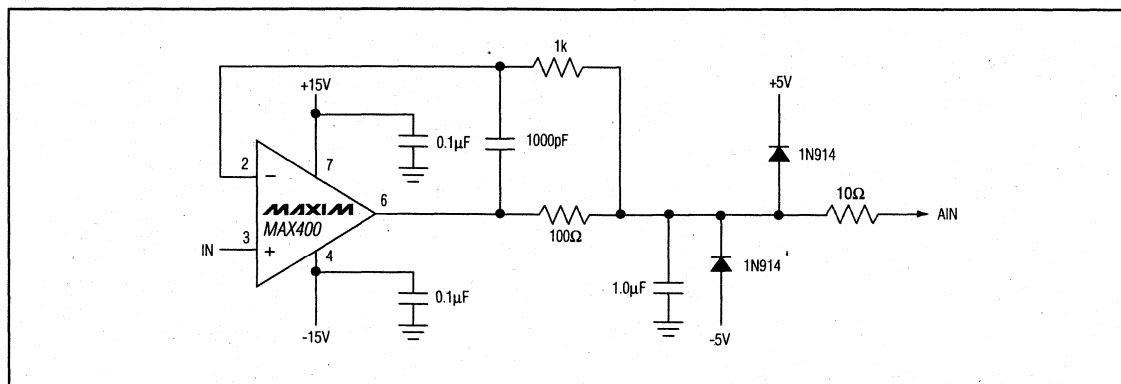


Figure 14. MAX400 Drives AIN for Low-Frequency Use

16-Bit, 85ksps ADC with 10 μ A Shutdown

Digital Noise

Digital noise can easily be coupled to AIN and REF. The conversion clock (CLK) and other digital signals that are active during input acquisition contribute noise to the conversion result. If the noise signal is synchronous to the sampling interval, an effective input offset is produced. Asynchronous signals produce random noise on the input, whose high-frequency components may be aliased into the frequency band of interest. Minimize noise by presenting a low impedance (at the frequencies contained in the noise signal) at the inputs. This requires bypassing AIN to AGND, or buffering the input with an amplifier that has a small-signal bandwidth of several megahertz, or preferably both. AIN has a bandwidth of about 16MHz.

Offsets resulting from synchronous noise (such as the conversion clock) are canceled by the MAX195's calibration scheme. However, because the magnitude of the offset produced by a synchronous signal depends on the signal's shape, recalibration may be appropriate if the shape or relative timing of the clock or other digital signals change, as might occur if more than one clock signal or frequency is used.

Distortion

Avoid degrading dynamic performance by choosing an amplifier with distortion much less than the MAX195's THD (-97dB, or 0.0014%) at frequencies of interest. If the chosen amplifier has insufficient common-mode rejection, which results in degraded THD performance, use the inverting configuration (positive input grounded) to eliminate errors from this source. Low temperature-coefficient, gain-setting resistors reduce linearity errors caused by resistance changes due to self-heat-

ing. Also, to reduce linearity errors due to finite amplifier gain, use an amplifier circuit with sufficient loop gain at the frequencies of interest (Figures 14, 15, 16).

DC Accuracy

If DC accuracy is important, choose a buffer with an offset much less than the MAX195's maximum offset ($\pm 3\text{LSB} = \pm 366\mu\text{V}$ for a $\pm 4\text{V}$ input range), or whose offset can be trimmed while maintaining good stability over the required temperature range.

Recommended Circuits

Figure 14 shows a good circuit for DC and low-frequency use. The MAX400 has very low offset ($10\mu\text{V}$) and drift ($0.2\mu\text{V}/^\circ\text{C}$), and low voltage noise ($10\text{nV}/\sqrt{\text{Hz}}$) as well. However, its gain-bandwidth product (GBW) is much too low to drive AIN directly, so the analog input is bypassed to present a low impedance at high frequencies. The large bypass capacitor is isolated from the amplifier output by a 100Ω resistor, which provides additional noise filtering. Since the $\pm 15\text{V}$ supplies exceed the AIN range, add protection diodes at AIN (see *REF and AIN Input Protection* section).

Figure 15 shows a wide-bandwidth amplifier (MAX427) driving a wideband video buffer, which is capable of driving AIN and a small bypass capacitor (for noise reduction) directly. The video buffer is inside the MAX427's feedback loop, providing good DC accuracy, while the buffer's low output impedance and high-current capability provide good AC performance. AIN is diode-clamped to the $\pm 5\text{V}$ rails to prevent overvoltage. The MAX427's $15\mu\text{V}$ maximum offset voltage, $0.8\mu\text{V}/^\circ\text{C}$ maximum drift, and less than $5\text{nV}/\sqrt{\text{Hz}}$ noise specifications make this an excellent choice for AC/DC use.

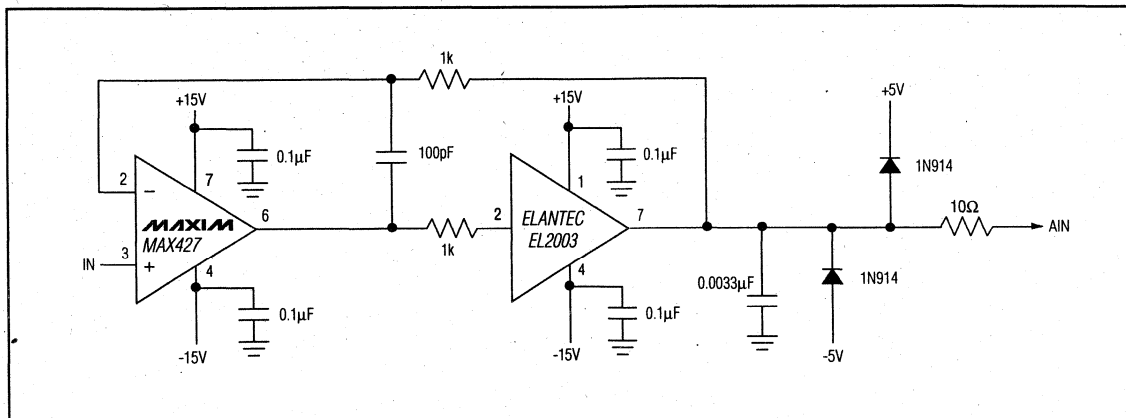


Figure 15. AIN Buffer for AC/DC Use

16-Bit, 85ksps ADC with 10μA Shutdown

If $\pm 15\text{V}$ supplies are unavailable, Figure 16's circuit works very well with the $\pm 5\text{V}$ analog supplies used by the MAX195. The MAX410 has a minimum $\pm 3.5\text{V}$ common-mode input range, with a similar output voltage swing, which allows use of a reference voltage up to 3.5V . The offset voltage ($250\mu\text{V}$) is about 2LSB. The drift ($1\mu\text{V}/^\circ\text{C}$), unity-gain bandwidth (28MHz), and low voltage noise ($2.4\text{nV}/\sqrt{\text{Hz}}$) are appropriate for 16-bit performance.

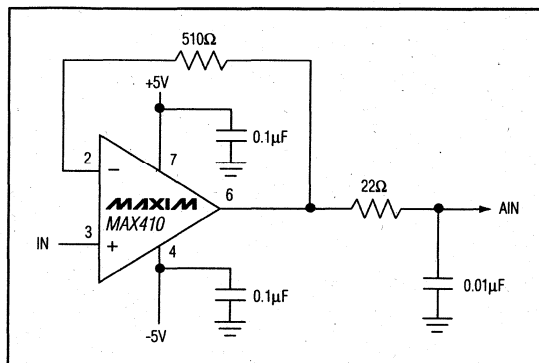


Figure 16. $\pm 5\text{V}$ Buffer for AC/DC Use Has $\pm 3.5\text{V}$ Swing

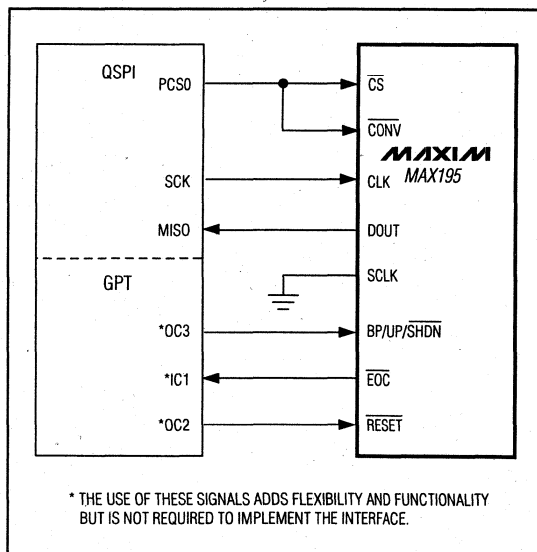


Figure 17. MAX195 Connection to QSPI Processor Clocking Data Out During Conversions

Operating Modes and SPI/QSPI Interfaces

The two basic interface modes are defined according to whether serial data is received during the conversion (clocked with CLK, SCLK unused) or in bursts between conversions (clocked with SCLK). Each mode is presented interfaced to a QSPI processor, but is also compatible with SPI.

Mode 1 (Simultaneous Conversion and Data Transfer)

In this mode, each data bit is read from the MAX195 during the conversion as it is determined. SCLK is grounded and CLK is used as both the conversion clock and the serial data clock. Figure 17 shows a QSPI processor connected to the MAX195 for use in this mode and Figure 18 is the associated timing diagram.

In addition to the standard QSPI interface signals, general I/O lines are used to monitor EOC and to drive BP/UP/SHDN and RESET. The two general output pins may not be necessary for a given application and, if I/O lines are unavailable, the EOC connection can be omitted as well.

The $\overline{\text{EOC}}$ signal is monitored during calibration to determine when calibration is finished and before beginning a conversion to ensure the MAX195 is not in mid-conversion, but it is possible for a system to ignore $\overline{\text{EOC}}$ completely. On power-up or after pulsing RESET low, the μP must provide 14,000 CLK cycles to complete the calibration sequence (Figure 2). One way to do this is to toggle CLK and monitor $\overline{\text{EOC}}$ until it goes low, but it is possible to simply count 14,000 CLK cycles to complete the calibration. Similarly, it is unnecessary to check the status of $\overline{\text{EOC}}$ before beginning a conversion if you are sure the last conversion is complete. This can be done by ensuring that every conversion consists of at least 20 CLK cycles.

Data is clocked out of the MAX195 on CLK's falling edge and can be clocked into the μP on the rising edge or the following falling edge. If you clock data in on the rising edge (SPI/QSPI with CPOL = 0 and CPHA = 0; standard Microwire: Hitachi H8), the maximum CLK rate is given by:

$$f_{\text{CLK}}(\text{max}) = \frac{1}{\frac{1}{2} \times (t_{\text{CD}} + t_{\text{SD}})}$$

where t_{CD} is the MAX195's CLK-to-DOUT valid delay* and t_{SD} is the data setup time for your μP .

16-Bit, 85ksps ADC with 10µA Shutdown

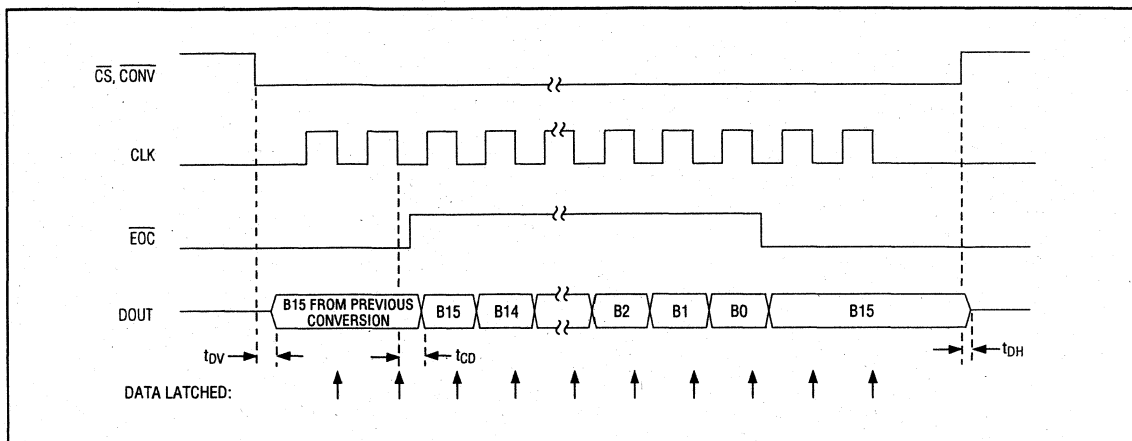


Figure 18. Timing Diagram for Circuit of Figure 17 (Mode 1)

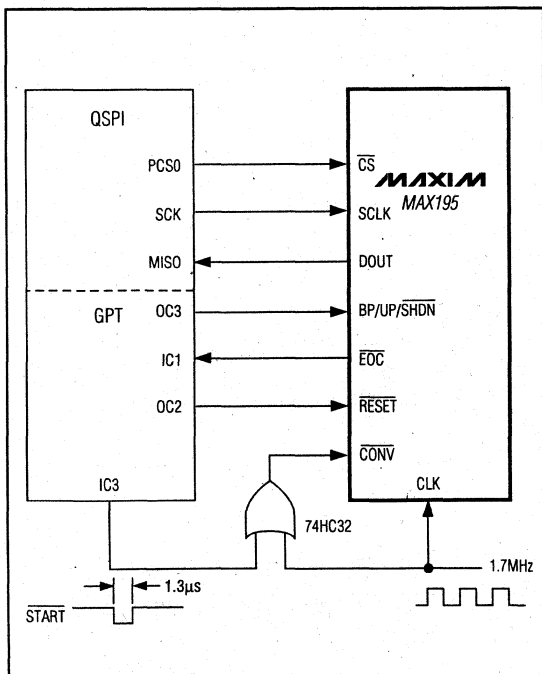


Figure 19. MAX195 Connection to QSPI Processor Clocking Data Out with SCLK Between Conversions

If clocking data in on the falling edge (CPOL = 0, CPHA = 1), the maximum CLK rate is given by:

$$f_{CLK}(\max) = \frac{1}{t_{CD} + t_{SD}}$$

Do not exceed the maximum CLK frequency given in the *Electrical Characteristics* table. To clock data in on the falling edge, your processor hold time must not exceed t_{CD} minimum (100ns).

While QSPI can provide the required 20 CLK cycles as two continuous 10-bit transfers, SPI is limited to 8-bit transfers. This means that with SPI, a conversion must consist of three 8-bit transfers. Ensure that the pauses between 8-bit operations at your selected clock rate are short enough to maintain a 20ms or shorter conversion time, or the leakage of the capacitive DAC may cause errors.

Complete source code for the Motorola 68HC16 and the MAX195 evaluation kit (EV kit) using this mode is available with the MAX195 EV kit.

Mode 2 (Asynchronous Data Transfer)

This mode uses a conversion clock (CLK) and a serial clock (SCLK). The serial data is clocked out between conversions, which reduces the maximum throughput for high CLK rates, but may be more convenient for some applications. Figure 19 is a block diagram with a QSPI processor (Motorola 68HC16) connected to the MAX195. Figure 20 shows the associated timing diagram. Figure 21 gives an assembly language listing for this arrangement.

16-Bit, 85ksps ADC with 10 μ A Shutdown

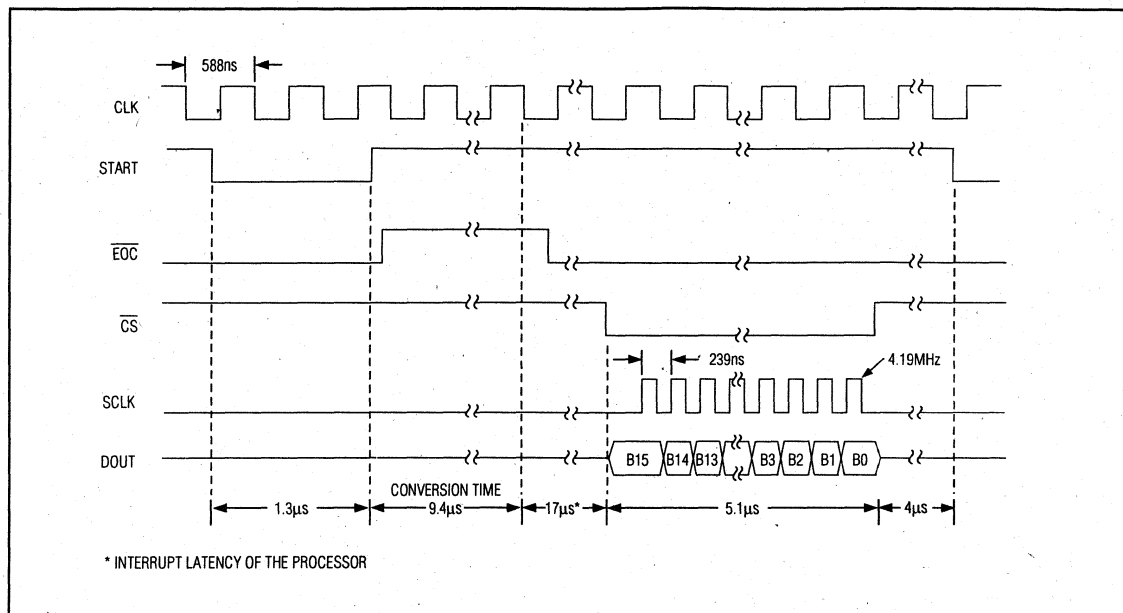


Figure 20. Timing Diagram for Circuit of Figure 19 (Mode 2)

An OR gate is used to synchronize the "start" signal to the asynchronous CLK, as described in the *External Clock* section. As with Mode 1, the QSPI processor must run CLK during calibration and either count CLK cycles or, as is done here, monitor $\overline{\text{EOC}}$ to determine when calibration is complete. Also, $\overline{\text{EOC}}$ is polled by the μP to determine when a conversion result is available. When $\overline{\text{EOC}}$ goes low, data is clocked out at the highest QSPI data rate (4.19Mbps). After the data is transferred, a new conversion can be initiated whenever desired.

The timing specification for SCLK-to-DOUT valid (t_{SD}) imposes some constraints on the serial interface. At SCLK rates up to 2.5Mbps, data is clocked out of the MAX195 by a falling edge of SCLK and may be clocked into the μP by the next rising edge (CPOL = 0, CPHA = 0). For data rates greater than 2.5Mbps (or for lower rates, if desired) it is necessary to clock data out of the MAX195 on SCLK's falling edge and to clock it into the μP on SCLK's next falling edge (CPOL = 0, CPHA = 1). Also, your processor hold time must not exceed t_{SD} minimum (20ns). As with CLK in mode 1, maximum SCLK rates may not be possible with some interface specifications that are subsets of SPI.

Supplies, Layout, Grounding and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source and at the MAX195, as shown in Figure 22. If the analog and digital supplies come from the same source, isolate the digital supply from the analog supply with a low-value resistor (10 Ω).

Constraints on sequencing the four power supplies are as follows.

- Apply VDDA before VDDD.
- Apply VSSA before VSSD.
- Apply AIN and REF after VDDA and VSSA are present.
- The power supplies should settle within the MAX195's power-on delay (minimum 500ns) or you should recalibrate the converter (pulse RESET low) before use.

16-Bit, 85ksps ADC with 10 μ A Shutdown

```
*****
* MAX195 code listing for 68HC16 module and circuit of Figure ____ *
* (C) 1994 Maxim Integrated Products *
* *
* Written for use with the Motorola 68HC Macro Assembler - Vers. 4.1 *
* Uses the QSPI in Master mode to read the MAX195. *
*****

*****
*
* Pin assignment for MAX195
*
ShdnPin EQU $20 ; BP/UP = OC3
ResetPin EQU $10 ; RESET = OC2
EOCPin EQU $01 ; /EOC/ = IC1
DoutFrom195 EQU $01 ; DOUT = MISO
SCKto195 EQU $04 ; SCLK = SCK
CSto195 EQU $08 ; /CS/ = PCS0/\SS\
Start EQU $04 ; Start = IC3

*****
*
* QSPI initialization parameters
*
SPBR EQU $2 ; QSPI baud rate = (16.78MHz/(2*SPBR)) = 4.19 MHz
CPOL EQU $0 ; serial clock is low when idle
CPHA EQU $0 ; CPOL=CPHA, so data is valid on rising edge of clock
BITS EQU $10 ; bits per transfer field = 16
DSCKL EQU $2 ; delay before SCK = (DSCKL/16.78MHz) = 119 nsec
DTL EQU $1 ; delay after transfer = (DTL*32/16.78MHz) = 1.19 usec
NEWQP EQU $0 ; pointer to first valid queue entry
ENDQP EQU $1 ; pointer to last valid queue entry

***
* Start of main program
***

MAIN:

* Initialize the GPT module as a general purpose I/O port
*
; GPT pins that are initially high
;
LDAA #(ResetPin)!(ShdnPin)!(Start)
STAA GPTPDR ; general purpose timer register

; GPT pins that are outputs
;
LDAA #(ResetPin)!(ShdnPin)!(Start)
STAA PDDR ; pin data direction register

* Initialize the QSM / QSPI
*
; list of QSM pins that are high by default
;
```

Figure 21. MAX195 Code Listing for 68HC16 Module and Circuit of Figure 19

16-Bit, 85ksps ADC with 10 μ A Shutdown

```

LDAA #(CSto195)!(SCKto195)
STAA QPDR                                ; QSPI port data register

; list of pins that are assigned to the QSPI
;
LDAA #(CSto195)!(SCKto195)!(DoutFrom195)
STAA QPAR                                ; QSPI pin assignment register

; list of QSM pins that are outputs
;
LDAA #(CSto195)!(SCKto195)
STAA QDDR                                ; QSPI data direction register

; QSPI Setup - Master Mode
CLR  SPCR3                                ; disable halt mode interrupt

LDD  #(((BITS)&$0F)*$0400)!(((SPBR)&$FF)!($B000)!((CPOL)*$200)!((CPHA)*$100)
STD  SPCR0                                ; QSPI in master mode, 16 bits per transfer, 4Mhz baud rate
                                           ; SCK inactive low, data captured on leading edge of SCK

LDD  #((DSCKL&$7F)*$100)!(DTL&$FF)
STD  SPCR1                                ; delay before SCK = 119ns, delay after transfer = 1.19us

; QSPI Setup - No Wrap
LDD  #((ENDQP&$0F)*$100)!(NEWQP&$0F)
STD  SPCR2                                ; new queue pointer = 0, end queue pointer = 1

*****
*
* Reset the MAX195.
*

BCLR GPTPDR,#ResetPin                    ; take MAX195 RESET pin low

WaitHigh1:
BRCLR GPTPDR,#EOCPin,WaitHigh1           ; wait until EOC goes high

BSET GPTPDR,#ResetPin                    ; take MAX195 RESET pin high

WaitLow1:
BRSET GPTPDR,#EOCPin,WaitLow1            ; wait until EOC goes low

; prime the ReadMAX195 routine by starting a conversion
; pulse Start pin(IC3), conversion start command; must be externally sync'd with CLK

BCLR GPTPDR,#Start                        ; clear Start, Start is low
LDAA #2                                  ; loop count (delay >= 2/Fclk)
PulseWidth1:
DECA                                     ; decrement loop count
BNE PulseWidth1
BSET GPTPDR,#Start                        ; set Start, start is high

*****
*
* ReadMAX195:
*

```

Figure 21. MAX195 Code Listing for 68HC16 Module and Circuit of Figure 19 (continued)

16-Bit, 85ksps ADC with 10 μ A Shutdown

```

Loop1:
    BRSET GPTPDR,#EOCPin,Loop1 ; wait until EOC is low

; QSPI Setup - No Wrap
    LDD #((ENDQP&$0F)*$100)!(NEWQP&$0F)
    STD SPCR2

; QSPI enable
    BSETW SPCR1,#$8000
    BCLR SPSR,#$80 ; clear QSPI finished flag (SPIF)

WaitForQSPI: ; wait until the QSPI finishes
    BRCLR SPSR,#SPSRSPIF,WaitForQSPI

; start the next conversion
; pulse Start pin (IC3)

    BCLR GPTPDR,#Start ; clear Start, Start is low
    LDAA #2 ; loop count (delay >= 2/Fclk)
PulseWidth2:
    DECA ; decrement loop count
    BNE PulseWidth2
    BSET GPTPDR,#Start ; set Start, Start is high

    LBRA ReadMAX195 ; long branch to ReadMAX195

```

Figure 21. MAX195 Code Listing for 68HC16 Module and Circuit of Figure 19 (continued)

Be sure that digital return currents do not pass through the analog ground and that return-current paths are low impedance. A 5mA current flowing through a PC board ground trace impedance of only 0.05 Ω creates an error voltage of about 250 μ V, or about 2LSBs error with a $\pm$ 4V full-scale system.

The board layout should ensure as much as possible that digital and analog signal lines are kept separate. Do not run analog and digital (especially clock) lines parallel to one another. If you must cross one with the other, do so at right angles.

The ADC's high-speed comparator is sensitive to high-frequency noise on the VDDA and VSSA power supplies. Bypass these supplies to the analog ground plane with 0.1 μ F in parallel with 1 μ F or 10 μ F low-ESR capacitors. Keep capacitor leads short for best supply-noise rejection.

Shutdown

The MAX195 may be shut down by pulling BP/UP/SHDN low. In addition to lowering power dissipation to 10 μ W (100 μ W max) when the device is not in use, you can save considerable power by shutting the converter down for short periods between conversions. There is no need to perform a reset (calibration) after the converter has been shut down unless the time in shutdown

is long enough that the supply voltages or ambient temperature may have changed.

The time required for the converter to "wake up" and settle depends heavily on the amount of additional error acceptable. For 0.5LSB additional error, 3.2 μ s is sufficient settling time and also allows enough time for reacquisition of the analog input signal. 50 μ s settling is required for less than 0.1LSB error. Figure 23 is a graph of theoretical power consumption vs. conversions per second for the MAX195 that assumes the conversion clock is 1.7MHz and the converter is shut down as much as possible between conversions.

Stop CLK before shutting down the MAX195. CLK must be stopped without generating short clock pulses. Short CLK pulses (less than 150ns), or shutting down the MAX195 without stopping CLK, may adversely affect the MAX195's internal calibration data. In applications where CLK is free-running and asynchronous, use the circuit of Figure 24 to stop CLK cleanly.

To minimize the time required to settle and perform a conversion, shut the converter down only after a conversion is finished and the desired mode (unipolar or bipolar) has been set. This ensures that the sampling capacitor array is properly connected to the input signal. If shut down in mid-conversion, when awakened,

16-Bit, 85ksps ADC with 10 μ A Shutdown

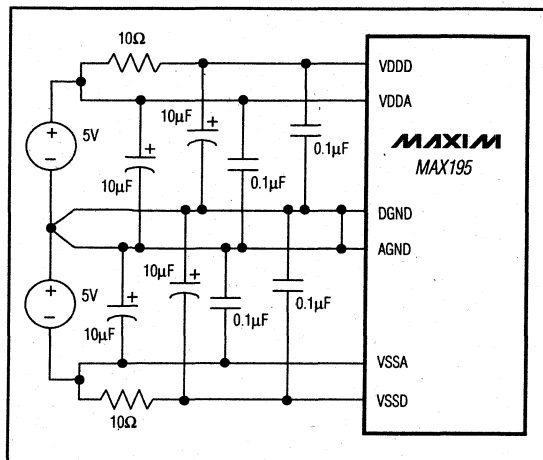


Figure 22. Supply Bypassing and Grounding

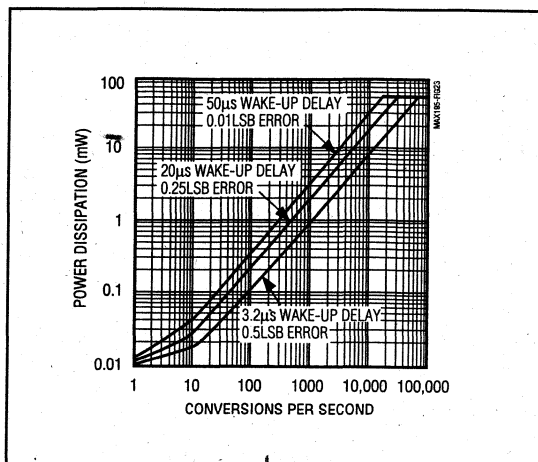


Figure 23. Power Dissipation vs. Conversions/sec When Shutting the MAX195 Down Between Conversions

the MAX195 finishes the old conversion, allows four clock (CLK) cycles for input acquisition, then begins the new conversion.

Dynamic Performance

High-speed sampling capability, 85ksps throughput, and wide dynamic range make the MAX195 ideal for AC applications and signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements other than the fundamental input frequency.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample rate. This usually (but not always) includes distortion as well as noise components. For this reason, the ratio is sometimes referred to as Signal-to-Noise + Distortion (SINAD).

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: $SNR = (6.02N + 1.76)dB$, where N is the number of bits of resolution. A perfect 16-bit ADC can, therefore, do no better than 98dB. An FFT plot of the output shows the output level in various spectral bands. Figure 25 shows the result of sampling a pure 1kHz sinusoid at 85ksps with the MAX195.

By transposing the equation that converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "effective number of bits" the ADC provides: $N = (SNR - 1.76) / 6.02$. Substituting SINAD for SNR in this formula results in a better measure of the ADC's usefulness. Figure 26 shows the effective number of bits as a function of the MAX195's input frequency calculated from the SINAD.

If your intended sample rate is much lower than the MAX195's maximum of 85ksps, you can improve your noise performance by taking more samples than necessary (oversampling) and averaging them in software. Figure 27 is a histogram showing 16,384 samples for the MAX195 without averaging, with an ideal "noiseless conversion," and with a running average of five samples. The standard deviation is 0.621LSB without averaging and 0.382LSB with the running average. If fewer data points are needed, normal averaging (e.g., five data points averaged to produce one data point) can be used instead of a running average, with similar results.

16-Bit, 85ksps ADC with 10 μ A Shutdown

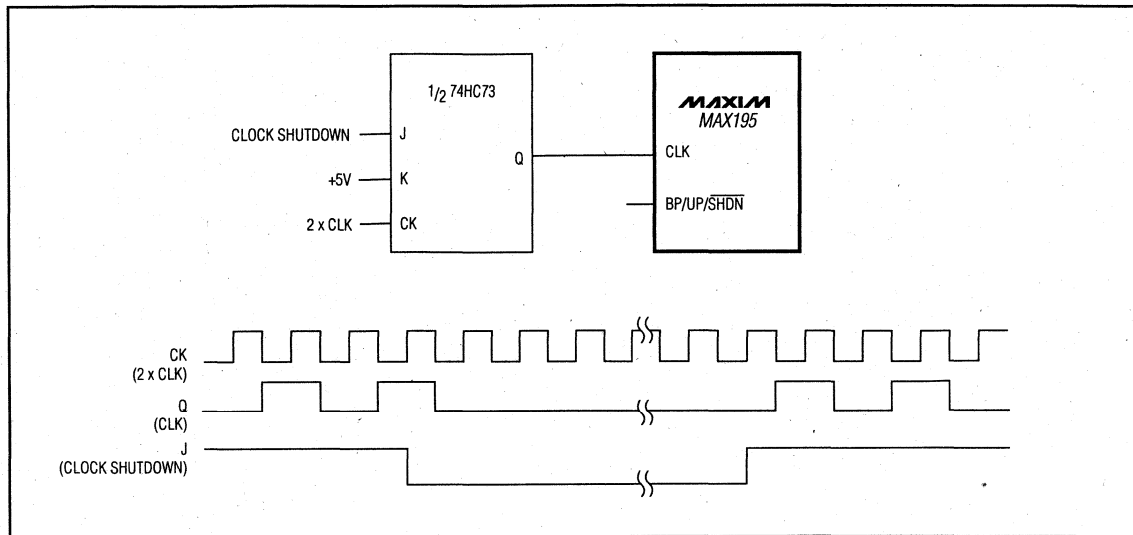


Figure 24. Circuit to Stop Free-Running Asynchronous CLK

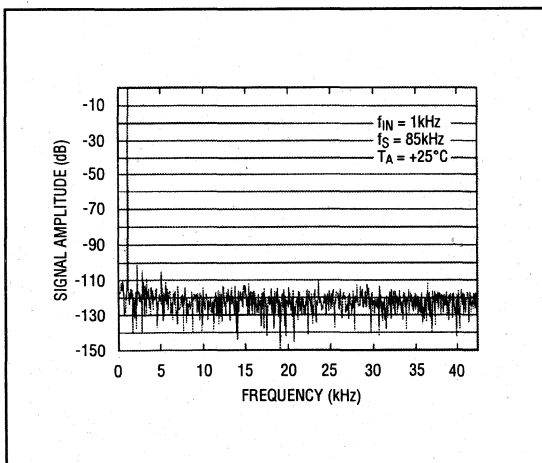


Figure 25. MAX195 FFT Plot

Even better than oversampling and averaging is oversampling and digital filtering. Averaging is just a rough (but computationally simple) type of digital filter. Finite impulse response (and other) digital filter algorithms are readily available, and are useful even with slow processors if the data rate is low or the data does not need to be processed in real-time. When using averaging, be sure to average an odd number of samples to avoid small offset errors caused by asymmetrical rounding.

Whether simple averaging or more complex digital filtering is used, the effect of oversampling is to spread the noise across a wider bandwidth. Digital filtering or averaging then eliminates the portion of this noise that lies above the filter's passband, leaving less noise in the passband than if oversampling was not used. An additional benefit of oversampling is that it simplifies the design or choice of an anti-aliasing pre-filter for the input. You can use a filter with a more gradual rolloff, because the sample rate is much higher than the frequency of interest.

16-Bit, 85ksps ADC with 10μA Shutdown

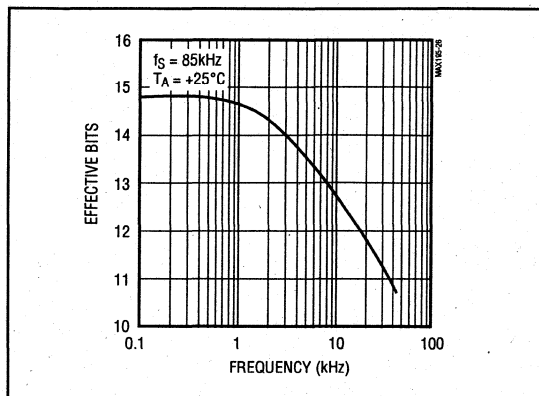


Figure 26. Effective Bits vs. Input Frequency

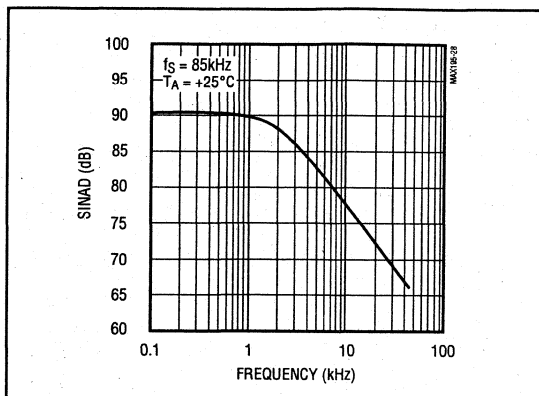


Figure 28. Signal-to-Noise + Distortion vs. Frequency

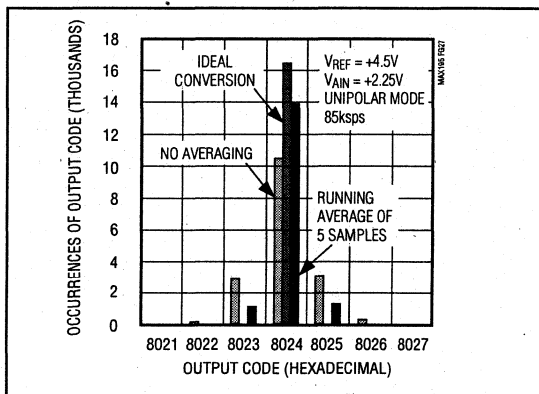


Figure 27. Histogram of 16,384 Conversions Shows Effects of Noise and Averaging

Total Harmonic Distortion

If a pure sine wave is input to an ADC, AC integral non-linearity (INL) of an ADC's transfer function results in harmonics of the input frequency being present in the sampled output data.

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* includes the 2nd through 5th harmonics. In the MAX195, this distortion is caused primarily by the changes in on-resistance of the AIN sampling switches with changing input voltage. These resistance changes, together with the DAC's capacitance (which can also vary with input voltage), cause a varying time delay for AC signals, which causes significant distortion at moderately high frequencies (Figure 28).

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually, this peak occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Transfer Function

Figures 29 and 30 show the MAX195's transfer functions. In unipolar mode, the output data is in binary format and in bipolar mode it is offset binary.

16-Bit, 85ksps ADC with 10 μ A Shutdown

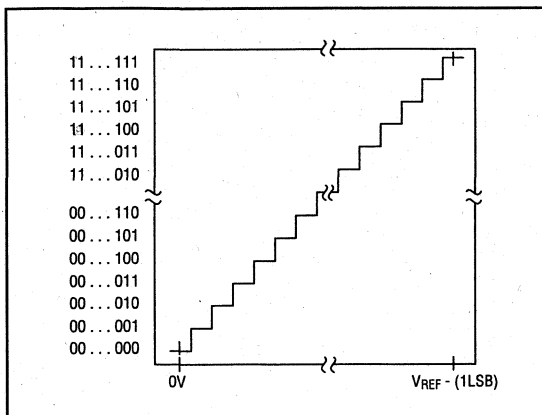


Figure 29. MAX195 Unipolar Transfer Function

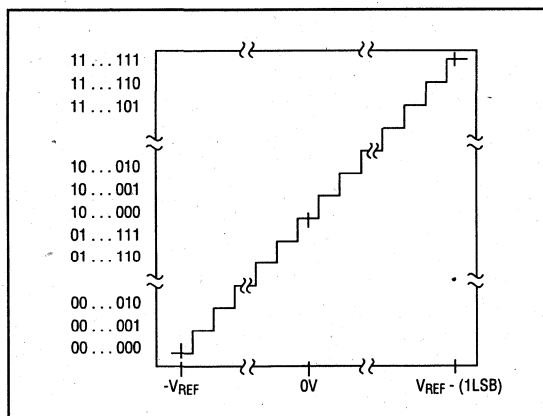
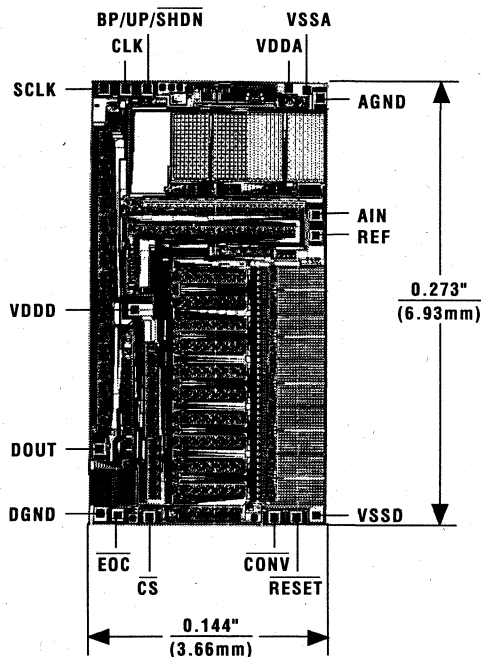


Figure 30. MAX195 Bipolar Transfer Function

Chip Topography



TRANSISTOR COUNT: 7966
SUBSTRATE CONNECTED TO VDDA

MAX195

7

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

Multi-Range, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

General Description

The MAX196/MAX198 multi-range, 12-bit data-acquisition systems (DAS) operate with only a single +5V supply, yet convert analog signals at their inputs up to $\pm 10V$ (MAX196) and $\pm 4V$ (MAX198). These devices provide six analog input channels that are independently software programmable for a variety of ranges: $\pm 10V$, $\pm 5V$, $0V$ to $+10V$, or $0V$ to $+5V$ for the MAX196; and $\pm VREF$, $\pm VREF/2$, $0V$ to $+VREF$, or $0V$ to $+VREF/2$ for the MAX198. This range-switching feature increases the effective dynamic range to 14 bits, providing the flexibility to interface $4mA$ -to- $20mA$, $\pm 12V$ and $\pm 15V$ -powered sensors to a single +5V system. In addition, these converters are fault-protected to $\pm 16.5V$; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 12-bit parallel interface, 5MHz bandwidth track/hold, 100ksps throughput rate, internal/external clock, internal/external acquisition timing, and an internal 4.096V or external reference.

Two programmable power-down modes (STBYPD, FULLPD) provide low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX196/MAX198 employ a standard microprocessor (μP) interface, and have data-access and bus-relinquish timing specifications that are compatible with most popular μPs . Their bidirectional, 12-bit, three-state I/O interface directly connects to 16-bit μP busses.

The MAX196/MAX198 are available in 28-pin DIP, wide SO, SSOP (shrink small-outline package) and ceramic sidebrake packages. For 8+4 bus interfaces, see the MAX197 and the MAX199 data sheets.

Applications

Industrial-Control Systems
Robotics
Data-Acquisition Systems
Automatic Testing Systems
Medical Instruments
Telecommunications

Features

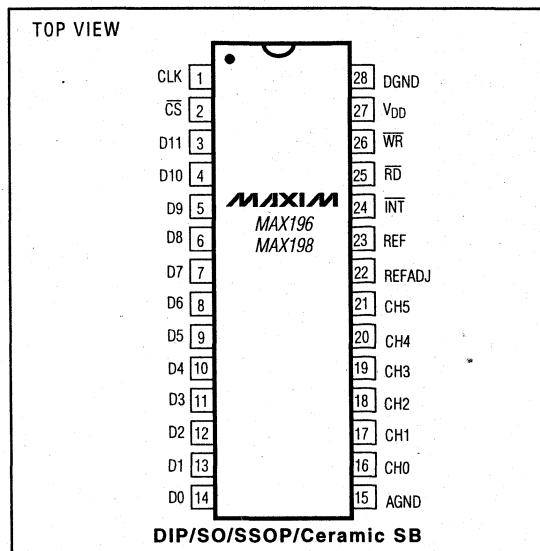
- ◆ 12-Bit Resolution, 1/2LSB Linearity
- ◆ Single +5V Operation
- ◆ Software-Selectable Input Ranges:
 $\pm 10V$, $\pm 5V$, $0V$ to $+10V$, $0V$ to $+5V$ (MAX196)
 $\pm VREF$, $\pm VREF/2$, $0V$ to $+VREF$, $0V$ to $+VREF/2$ (MAX198)
- ◆ Internal 4.096V or External Reference
- ◆ Fault-Protected Input Multiplexer ($\pm 16.5V$)
- ◆ Six Analog Input Channels
- ◆ $6\mu s$ Conversion Time, 100ksps Sampling Rate
- ◆ Internal or External Acquisition Control
- ◆ Two Power-Down Modes
- ◆ Internal or External Clock

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX196ACNI	$0^{\circ}C$ to $+70^{\circ}C$	28 Narrow Plastic DIP	$\pm 1/2$
MAX196BCNI	$0^{\circ}C$ to $+70^{\circ}C$	28 Narrow Plastic DIP	± 1
MAX196ACWI	$0^{\circ}C$ to $+70^{\circ}C$	28 Wide SO	$\pm 1/2$

Ordering Information continued on next page.

Pin Configuration



MAXIM

Maxim Integrated Products 7-119

Call toll free 1-800-998-8800 for free samples or literature.

Multi-Range, Single +5V, 12-Bit DAS with 12-Bit Bus Interface

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX196BCWI	0°C to +70°C	28 Wide SO	±1
MAX196ACAI	0°C to +70°C	28 SSOP	±1/2
MAX196BCAI	0°C to +70°C	28 SSOP	±1
MAX196BC/D	0°C to +70°C	Dice*	±1
MAX196AENI	-40°C to +85°C	28 Narrow Plastic DIP	±1/2
MAX196BENI	-40°C to +85°C	28 Narrow Plastic DIP	±1
MAX196AEWI	-40°C to +85°C	28 Wide SO	±1/2
MAX196BEWI	-40°C to +85°C	28 Wide SO	±1
MAX196AEAI	-40°C to +85°C	28 SSOP	±1/2
MAX196BEAI	-40°C to +85°C	28 SSOP	±1
MAX196AMYI	-55°C to +125°C	28 Narrow Ceramic SB**	±1/2
MAX196BMYI	-55°C to +125°C	28 Narrow Ceramic SB**	±1
MAX198ACNI	0°C to +70°C	28 Narrow Plastic DIP	±1/2
MAX198BCNI	0°C to +70°C	28 Narrow Plastic DIP	±1
MAX198ACWI	0°C to +70°C	28 Wide SO	±1/2
MAX198BCWI	0°C to +70°C	28 Wide SO	±1
MAX198ACAI	0°C to +70°C	28 SSOP	±1/2
MAX198BCAI	0°C to +70°C	28 SSOP	±1
MAX198BC/D	0°C to +70°C	Dice*	±1
MAX198AENI	-40°C to +85°C	28 Narrow Plastic DIP	±1/2
MAX198BENI	-40°C to +85°C	28 Narrow Plastic DIP	±1
MAX198AEWI	-40°C to +85°C	28 Wide SO	±1/2
MAX198BEWI	-40°C to +85°C	28 Wide SO	±1
MAX198AEAI	-40°C to +85°C	28 SSOP	±1/2
MAX198BEAI	-40°C to +85°C	28 SSOP	±1
MAX198AMYI	-55°C to +125°C	28 Narrow Ceramic SB**	±1/2
MAX198BMYI	-55°C to +125°C	28 Narrow Ceramic SB**	±1

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

EVALUATION KIT
AVAILABLE**MAXIM****Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$),
Single $+5V$, 12-Bit DAS with 8+4 Bus Interface****General Description**

The MAX197 multi-range, 12-bit data-acquisition system (DAS) requires only a single $+5V$ supply for operation, yet accepts signals at its analog inputs that may span both above the power-supply rail and below ground. This system provides 8 analog input channels that are independently software programmable for a variety of ranges: $\pm 10V$, $\pm 5V$, $0V$ to $+10V$, or $0V$ to $+5V$. This increases effective dynamic range to 14 bits, and provides the user flexibility to interface $4mA$ -to- $20mA$, $\pm 12V$, and $\pm 15V$ powered sensors to a single $+5V$ system. In addition, the converter is overvoltage tolerant to $\pm 16.5V$; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a $5MHz$ bandwidth track/hold, a $100ksps$ throughput rate, software-selectable internal or external clock and acquisition, 8+4 parallel interface, and an internal $4.096V$ or an external reference.

A hardware SHDN pin and two programmable power-down modes (STBYPD, FULLPD) are provided for low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX197 employs a standard microprocessor (μP) interface. A three-state data I/O port is configured to operate with 8-bit data buses, and data-access and bus-release timing specifications are compatible with most popular μPs . All logic inputs and outputs are TTL/CMOS compatible.

The MAX197 is available in 28-pin DIP, wide SO, SSOP, and ceramic SB packages.

For a different combination of ranges ($\pm 4V$, $\pm 2V$, $0V$ to $4V$, $0V$ to $2V$), see the MAX199 data sheet. For 12-bit bus interface, see the MAX196 and MAX198 data sheets.

Applications

Industrial-Control Systems
Robotics
Data-Acquisition Systems
Automatic Testing Systems
Medical Instruments
Telecommunications

Functional Diagram appears at end of data sheet.

Features

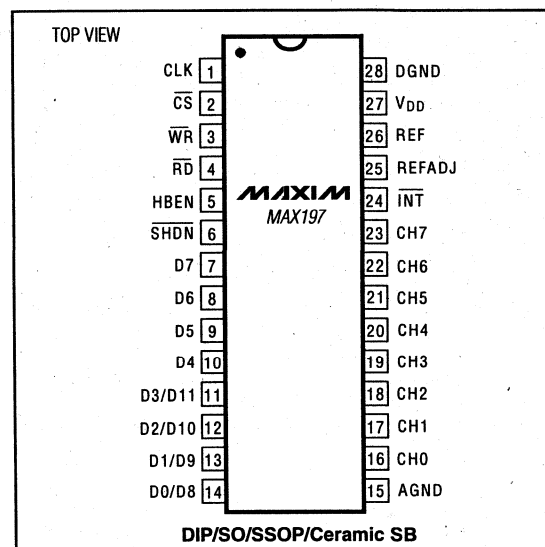
- ◆ 12-Bit Resolution, $1/2LSB$ Linearity
- ◆ Single $+5V$ Operation
- ◆ Software-Selectable Input Ranges:
 $\pm 10V$, $\pm 5V$, $0V$ to $10V$, $0V$ to $5V$
- ◆ Fault-Protected Input Multiplexer ($\pm 16.5V$)
- ◆ 8 Analog Input Channels
- ◆ $6\mu s$ Conversion Time, $100ksps$ Sampling Rate
- ◆ Internal or External Acquisition Control
- ◆ Internal $4.096V$ or External Reference
- ◆ Two Power-Down Modes
- ◆ Internal or External Clock

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX197ACNI	$0^{\circ}C$ to $+70^{\circ}C$	28 Narrow Plastic DIP
MAX197BCNI	$0^{\circ}C$ to $+70^{\circ}C$	28 Narrow Plastic DIP
MAX197ACWI	$0^{\circ}C$ to $+70^{\circ}C$	28 Wide SO
MAX197BCWI	$0^{\circ}C$ to $+70^{\circ}C$	28 Wide SO
MAX197ACAI	$0^{\circ}C$ to $+70^{\circ}C$	28 SSOP
MAX197BCAI	$0^{\circ}C$ to $+70^{\circ}C$	28 SSOP
MAX197BC/D	$0^{\circ}C$ to $+70^{\circ}C$	Dice*

Ordering Information continued at end of data sheet.

*Dice are specified at $T_A = +25^{\circ}C$, DC parameters only.

Pin Configuration

MAX197

7

MAXIM

Maxim Integrated Products 7-121

Call toll free 1-800-722-8266 for free samples or literature.

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

ABSOLUTE MAXIMUM RATINGS

V _{DD} to AGND	-0.3V to +7V
AGND to DGND	-0.3V to +0.3V
REF to AGND	-0.3V to (V _{DD} + 0.3V)
REFADJ to AGND	-0.3V to (V _{DD} + 0.3V)
Digital Inputs to DGND	-0.3V to (V _{DD} + 0.3V)
Digital Outputs to DGND	-0.3V to (V _{DD} + 0.3V)
CH0-CH7 to AGND	 $\pm 16.5V$
Continuous Power Dissipation (T _A = +70°C)	
Narrow Plastic DIP (derate 14.29mW/°C above +70°C)	1143mW
Wide SO (derate 12.50mW/°C above +70°C)	1000mW
SSOP (derate 9.52mW/°C above +70°C)	762mW
Narrow Ceramic SB (derate 20.00mW/°C above +70°C)	1600mW

Operating Temperature Ranges

MAX197_C_	0°C to +70°C
MAX197_E_	-40°C to +85°C
MAX197_M_	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V $\pm 5\%$; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7 μ F at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX197A				±1/2	LSB
		MAX197B				±1	
Differential Nonlinearity	DNL					±1	LSB
Offset Error		Unipolar	MAX197A			±3	LSB
			MAX197B			±5	
		Bipolar	MAX197A			±5	
			MAX197B			±10	
Channel-to-Channel Offset Error Matching		Unipolar				±0.1	LSB
		Bipolar				±0.5	
Gain Error (Note 2)		Unipolar	MAX197A			±7	LSB
			MAX197B			±10	
		Bipolar	MAX197A			±7	
			MAX197B			±10	
Gain Temperature Coefficient (Note 2)		Unipolar				3	ppm/°C
		Bipolar				5	
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±10Vp-p, fSAMPLE = 100ksps)							
Signal-to-Noise + Distortion Ratio	SINAD		MAX197A	70			dB
			MAX197B	69			
Total Harmonic Distortion	THD	Up to the 5th harmonic		-85		-78	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		50kHz, VIN = ±5V (Note 3)		-86			dB
Aperture Delay		External CLK mode/external acquisition control		15			ns
Aperture Jitter		External CLK mode/external acquisition control		<50			ps
		Internal CLK mode/internal acquisition control (Note 4)		10			ns

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Track/Hold Acquisition Time		$f_{CLK} = 2.0MHz$			3	μs
Small-Signal Bandwidth		-3dB rolloff	$\pm 10V$ range	5		MHz
			$\pm 5V$ range	2.5		
			0V to 10V range	2.5		
			0V to 5V range	1.25		
Input Voltage Range (See Table 1)		Unipolar		0	10	V
				0	5	
		Bipolar		-10	10	
				-5	5	
Input Current		Unipolar	0V to 10V range		720	μA
			0V to 5V range		360	
		Bipolar	-10V to 10V range	-1200	720	
			-5V to 5V range	-600	360	
Input Dynamic Resistance		Unipolar		21		$k\Omega$
		Bipolar		16		
Input Capacitance		(Note 5)			40	pF
INTERNAL REFERENCE						
REF Output Voltage	V_{REF}	$T_A = +25^\circ C$	4.076	4.096	4.116	V
REF Output Tempco	$TC V_{REF}$			40		ppm/ $^\circ C$
Output Short-Circuit Current					30	mA
Load Regulation		0mA to 0.5mA output current (Note 6)			7.5	mV
Capacitive Bypass at REF			4.7			μF
REFADJ Output Voltage			2.465	2.500	2.535	V
REFADJ Adjustment Range		With recommended circuit (Figure 1)		± 1.5		%
Buffer Voltage Gain				1.6384		V/V
REFERENCE INPUT (Buffer disabled, reference input applied to REF pin)						
Input Voltage Range			2.4		4.18	V
Input Current		$V_{REF} = 4.18V$	Normal or STANDBY power-down mode		400	μA
			FULL power-down mode		1	
Input Resistance		Normal or STANDBY power-down mode	10			$k\Omega$
		FULL power-down mode	5			M Ω
REFADJ Threshold for Buffer Disable			$V_{DD} - 50mV$			V

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage	V _{DD}			4.75		5.25	V
Supply Current	I _{DD}	Normal mode, bipolar ranges				18	mA
		Normal mode, unipolar ranges			6	10	
		Standby power-down (STBYPD)			700	850	μA
		Full power-down mode (FULLPD) (Note 7)				120	
Power-Supply Rejection Ratio (Note 8)	PSRR	External reference = 4.096V				±1/2	LSB
		Internal reference				±1/2	
TIMING							
Internal Clock Frequency	f _{CLK}	C _{CLK} = 100pF		1.25	1.56	2.00	MHz
External Clock Frequency Range	f _{CLK}			0.1		2.0	MHz
Acquisition Time	t _{ACQI}	Internal acquisition	External CLK	3.0			μs
			Internal CLK	3.0		5.0	
	t _{ACQE}	External acquisition (Note 9)		3.0			
		After FULLPD or STBYPD			5		
Conversion Time	t _{CONV}	External CLK		6.0			μs
		Internal CLK, C _{CLK} = 100pF		6.0	7.7	10.0	
Throughput Rate		External CLK				100	ksps
		Internal CLK, C _{CLK} = 100pF		62			
Bandgap Reference Start-Up Time		Power-up (Note 10)			200		μs
Reference Buffer Settling		To 0.1mV REF bypass capacitor fully discharged	C _{REF} = 4.7μF		8		ms
			C _{REF} = 33μF		60		
DIGITAL INPUTS (D7–D0, CLK, RD, WR, CS, HBEN, SHDN) (Note 11)							
Input High Voltage	V _{INH}			2.4			V
Input Low Voltage	V _{INL}					0.8	V
Input Leakage Current	I _{IN}	V _{IN} = 0V or V _{DD}				±10	μA
Input Capacitance	C _{IN}	(Note 5)				15	pF
DIGITAL OUTPUTS (D7–D4, D3/D11, D2/D10, D1/D9, D0/D8, INT)							
Output Low Voltage	V _{OL}	V _{DD} = 4.75V, I _{SINK} = 1.6mA				0.4	V
Output High Voltage	V _{OH}	V _{DD} = 4.75V, I _{SOURCE} = 1mA		V _{DD} - 1			V
Three-State Output Capacitance	C _{OUT}	(Note 5)				15	pF

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

TIMING CHARACTERISTICS

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}		80			ns
$\overline{WR}$ Pulse Width	t_{WR}		80			ns
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CSWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CSWH}		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CSRS}		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CSRH}		0			ns
CLK to $\overline{WR}$ Setup Time	t_{CWS}				100	ns
CLK to $\overline{WR}$ Hold Time	t_{CWH}				50	ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		60			ns
Data Valid to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{RD}$ Low to Output Data Valid	t_{DO}	Figure 2, $C_L = 100pF$ (Note 12)			120	ns
HBEN High or HBEN Low to Output Valid	t_{DO1}	Figure 2, $C_L = 100pF$ (Note 12)			120	ns
$\overline{RD}$ High to Output Disable	t_{TR}	(Note 13)			70	ns
$\overline{RD}$ Low to $\overline{INT}$ High Delay	t_{INT1}				120	ns

Note 1: Accuracy specifications tested at $V_{DD} = 5.0V$. Performance at power-supply tolerance limits guaranteed by Power-Supply Rejection test. Tested for the $\pm 10V$ input range.

Note 2: External reference: $V_{REF} = 4.096V$, offset error nulled, ideal last code transition = $FS - 3/2LSB$.

Note 3: Ground "on" channel; sine wave applied to all "off" channels.

Note 4: Maximum full-power input frequency for 1LSB error with 10ns jitter = 3kHz.

Note 5: Guaranteed by design. Not tested.

Note 6: Use static loads only.

Note 7: Tested using internal reference.

Note 8: PSRR measured at full-scale.

Note 9: External acquisition timing: starts at data valid at $ACQMOD = \text{low control byte}$; ends at rising edge of $\overline{WR}$ with $ACQMOD = \text{high control byte}$.

Note 10: Not subject to production testing. Provided for design guidance only.

Note 11: All input control signals specified with $t_r = t_f = 5ns$ from a voltage level of 0.8V to 2.4V.

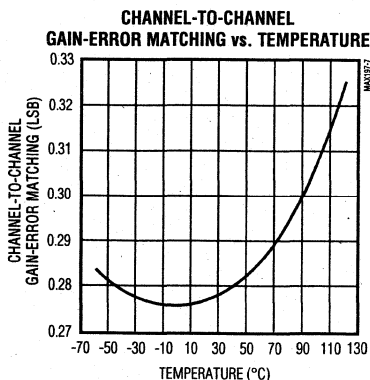
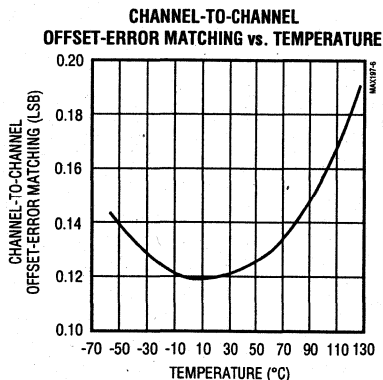
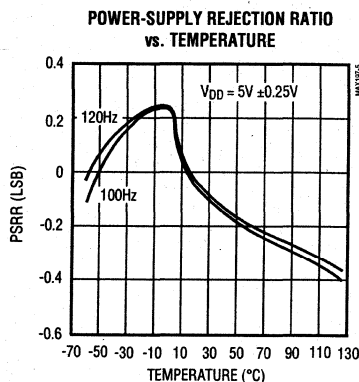
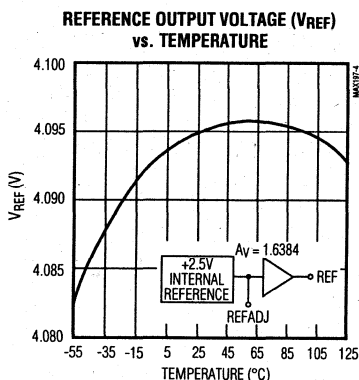
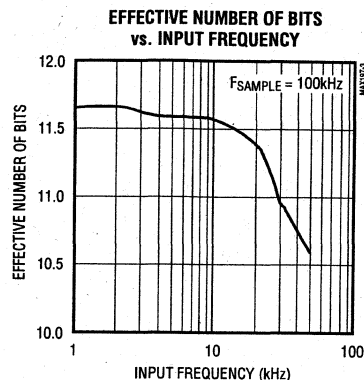
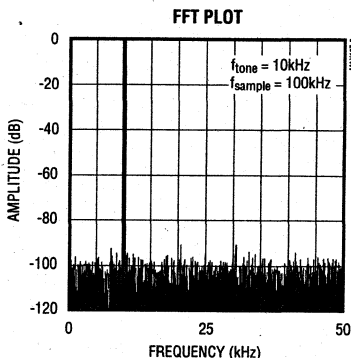
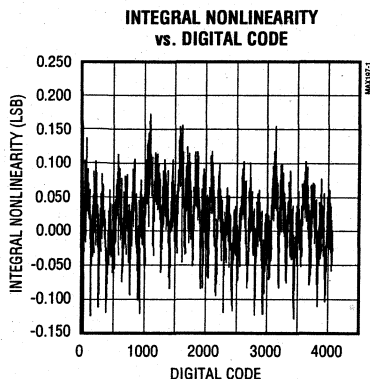
Note 12: t_{DO} and t_{DO1} are measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 13: t_{TR} is defined as the time required for the data lines to change by 0.5V.

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Input. In external clock mode, drive CLK with a TTL/CMOS compatible clock. In internal clock mode, place a capacitor from this pin to ground to set the internal clock frequency; $f_{CLK} = 1.56\text{MHz}$ typical with $C_{CLK} = 100\text{pF}$.
2	$\overline{CS}$	Chip Select, active low.
3	$\overline{WR}$	When $\overline{CS}$ is low, in the internal acquisition mode, a rising edge on $\overline{WR}$ latches in configuration data and starts an acquisition plus a conversion cycle. When $\overline{CS}$ is low, in the external acquisition mode, the first rising edge on $\overline{WR}$ starts an acquisition and a second rising edge on $\overline{WR}$ ends acquisition and starts a conversion cycle.
4	$\overline{RD}$	If $\overline{CS}$ is low, a falling edge on $\overline{RD}$ will enable a read operation on the data bus.
5	HBEN	Used to multiplex the 12-bit conversion result. When high, the 4 MSBs are multiplexed on the data bus; when low, the 8 LSBs are available on the bus.
6	$\overline{SHDN}$	Shutdown. Puts the device into full power-down (FULLPD) mode when pulled low.
7–10	D7–D4	Three-State Digital I/O
11	D3/D11	Three-State Digital I/O. D3 output (HBEN = low), D11 output (HBEN = high).
12	D2/D10	Three-State Digital I/O. D2 output (HBEN = low), D10 output (HBEN = high).
13	D1/D9	Three-State Digital I/O. D1 output (HBEN = low), D9 output (HBEN = high).
14	D0/D8	Three-State Digital I/O. D0 output (HBEN = low), D8 output (HBEN = high). D0 = LSB.
15	AGND	Analog Ground
16–23	CH0–CH7	Analog Input Channels
24	$\overline{INT}$	$\overline{INT}$ goes low when conversion is complete and output data is ready.
25	REFADJ	Bandgap Voltage-Reference Output/External Adjust Pin. Bypass with a $0.01\mu\text{F}$ capacitor to AGND. Connect to V_{DD} when using an external reference at the REF pin.
26	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a $4.096V$ nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD} .
27	V_{DD}	$+5V$ Supply. Bypass with $0.1\mu\text{F}$ capacitor to AGND.
28	DGND	Digital Ground

7

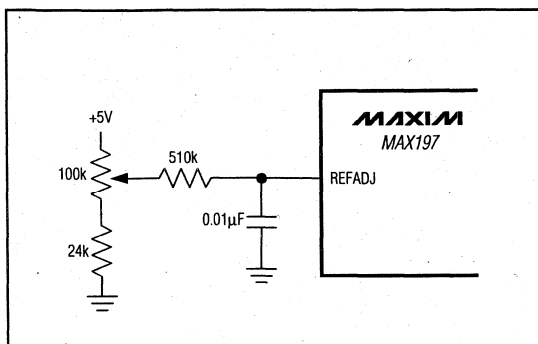


Figure 1. Reference-Adjust Circuit

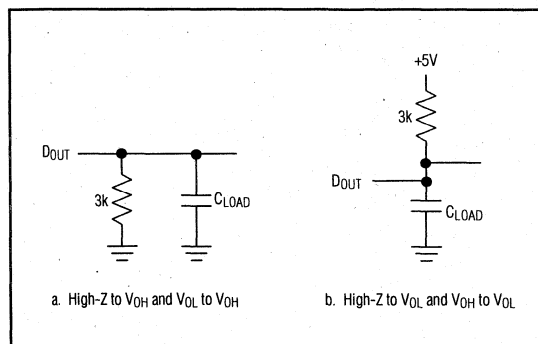


Figure 2. Load Circuits for Enable Time

Multi-Range ($\pm 10\text{V}$, $\pm 5\text{V}$, $+10\text{V}$, $+5\text{V}$), Single $+5\text{V}$, 12-Bit DAS with 8+4 Bus Interface

Detailed Description

Converter Operation

The MAX197, a multi-range, fault-tolerant ADC, uses successive approximation and internal input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. The parallel-output format provides easy interface to microprocessors (μPs). Figure 3 shows the MAX197 in its simplest operational configuration.

Analog-Input Track/Hold

In the internal acquisition control mode (control bit D5 set to 0), the T/H enters its tracking mode on $\overline{\text{WR}}$'s rising edge, and enters its hold mode when the internally timed (6 clock cycles) acquisition interval ends. A low impedance input source, which settles in less than $1.5\mu\text{s}$, is required to maintain conversion accuracy at the maximum conversion rate.

In the external acquisition control mode (D5 = 1), the T/H enters its tracking mode on the first $\overline{\text{WR}}$ rising edge and enters its hold mode when it detects the second $\overline{\text{WR}}$ rising edge with D5 = 0. See the *External Acquisition* section.

Input Bandwidth

The ADC's input tracking circuitry has a 5MHz small-signal bandwidth. When using the internal acquisition

mode with an external clock frequency of 2MHz, a 100kps throughput rate can be achieved. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended (MAX274/MAX275 continuous-time filters).

Input Range and Protection

Figure 4 shows the equivalent input circuit. With $\text{VREF} = 4.096\text{V}$, the MAX197 can be programmed for input ranges of $\pm 10\text{V}$, $\pm 5\text{V}$, 0V to 10V , or 0V to 5V by setting the appropriate control bits (D3, D4) in the control byte (see Tables 2 and 3). The full-scale input voltage depends on the voltage at REF (Table 1). When an external reference is applied at REFADJ, the voltage at REF is given by $\text{VREF} = 1.6384 \times \text{VREFADJ}$ ($2.4\text{V} < \text{VREF} < 4.18\text{V}$).

Table 1. Full Scale and Zero Scale

RANGE (V)	ZERO SCALE (V)	-FULL SCALE	+FULL SCALE
0 to 5	0	—	$\text{VREF} \times 1.2207$
0 to 10	0	—	$\text{VREF} \times 2.4414$
± 5	—	$-\text{VREF} \times 1.2207$	$\text{VREF} \times 1.2207$
± 10	—	$-\text{VREF} \times 2.4414$	$\text{VREF} \times 2.4414$

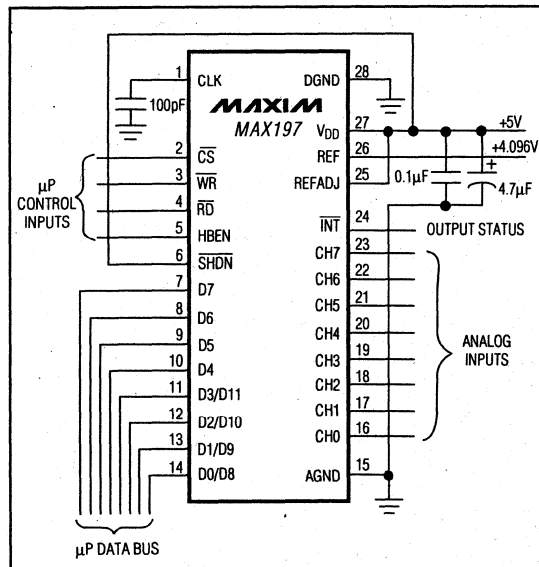


Figure 3. Operational Diagram

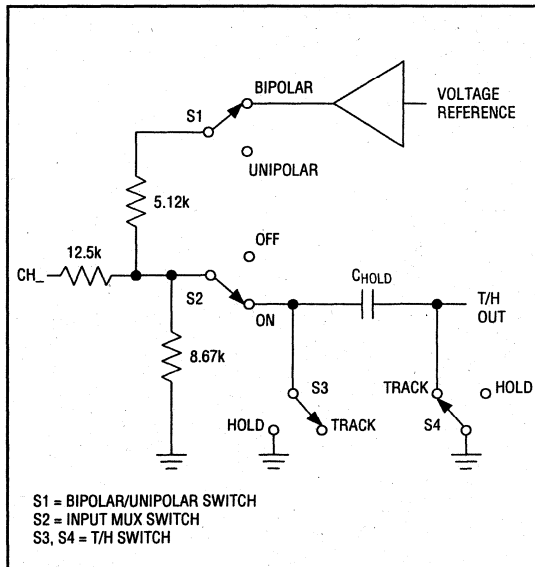


Figure 4. Equivalent Input Circuit

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

The input channels are overvoltage protected to $\pm 16.5V$. This protection is active even if the device is in power-down mode.

Even with $V_{DD} = 0V$, the input resistive network provides current-limiting that adequately protects the device.

Digital Interface

Input data (control byte) and output data are multiplexed on a three-state parallel interface. This parallel I/O can easily be interfaced with a μP . $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ control the write and read operations. $\overline{CS}$ is the standard chip-select signal, which enables a μP to address the MAX197 as an I/O port. When high, it disables the $\overline{WR}$ and $\overline{RD}$ inputs and forces the interface into a high-Z state.

Input Format

The control byte is latched into the device, on pins D7–D0, during a write cycle. Table 2 shows the control-byte format.

Output Data Format

The output data format is binary in unipolar mode and two's-complement binary in bipolar mode. When reading the output data, $\overline{CS}$, and $\overline{RD}$ must be low. When $\overline{HBEN}$ is low, the lower eight bits are read. When $\overline{HBEN}$ is high, the upper four MSBs are available and the output data bits D4–D7 are either set low (in unipolar mode) or set to the value of the MSB (in bipolar mode) (Table 6).

Table 2. Control-Byte Format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7, 6	PD1, PD0	These two bits select the clock and power-down modes (Table 4).
5	ACQMOD	0 = internally controlled acquisition (6 clock cycles), 1 = externally controlled acquisition
4	RNG	Selects the full-scale voltage magnitude at the input (Table 3).
3	BIP	Selects unipolar or bipolar conversion mode (Table 3).
2, 1, 0	A2, A1, A0	These are address bits for the input mux to select the "on" channel (Table 5).

Table 3. Range and Polarity Selection

BIP	RNG	INPUT RANGE (V)
0	0	0 to 5
0	1	0 to 10
1	0	± 5
1	1	± 10

Table 4. Clock and Power-Down Selection

PD1	PD0	DEVICE MODE
0	0	Normal Operation / External Clock Mode
0	1	Normal Operation / Internal Clock Mode
1	0	Standby Power-Down (STBYPD); clock mode is unaffected
1	1	Full Power-Down (FULLPD); clock mode is unaffected

Table 5. Channel Selection

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	*							
0	0	1		*						
0	1	0			*					
0	1	1				*				
1	0	0					*			
1	0	1						*		
1	1	0							*	
1	1	1								*

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

Table 6. Data-Bus Output

PIN	HBEN = LOW	HBEN = HIGH
D0	B0 (LSB)	B8
D1	B1	B9
D2	B2	B10
D3	B3	B11 (MSB)
D4	B4	B11 (BIP = 1) / 0 (BIP = 0)
D5	B5	B11 (BIP = 1) / 0 (BIP = 0)
D6	B6	B11 (BIP = 1) / 0 (BIP = 0)
D7	B7	B11 (BIP = 1) / 0 (BIP = 0)

How to Start a Conversion

Conversions are initiated with a write operation, which selects the mux channel and configures the MAX197 for either unipolar or bipolar input range. A write pulse ($\overline{WR}$ + $\overline{CS}$) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode.

Writing a new control byte during conversion cycle will abort conversion and start a new acquisition interval.

Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared ($ACQMOD = 0$). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval ($3\mu s$ with $f_{CLK} = 2MHz$) ends. See Figure 5.

External Acquisition

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with $ACQMOD = 1$, starts an acquisition interval of indeterminate length. The second write pulse, written with $ACQMOD = 0$, terminates acquisition and starts conversion on $\overline{WR}$'s rising edge (Figure 6). However, if the second control byte contains $ACQMOD = 1$, an indefinite acquisition interval is restarted.

The address bits for the input mux must have the same values on the first and second write pulses. Power-down mode bits ($PD0$, $PD1$) can assume new values on the second write pulse (see *Power-Down Mode*).

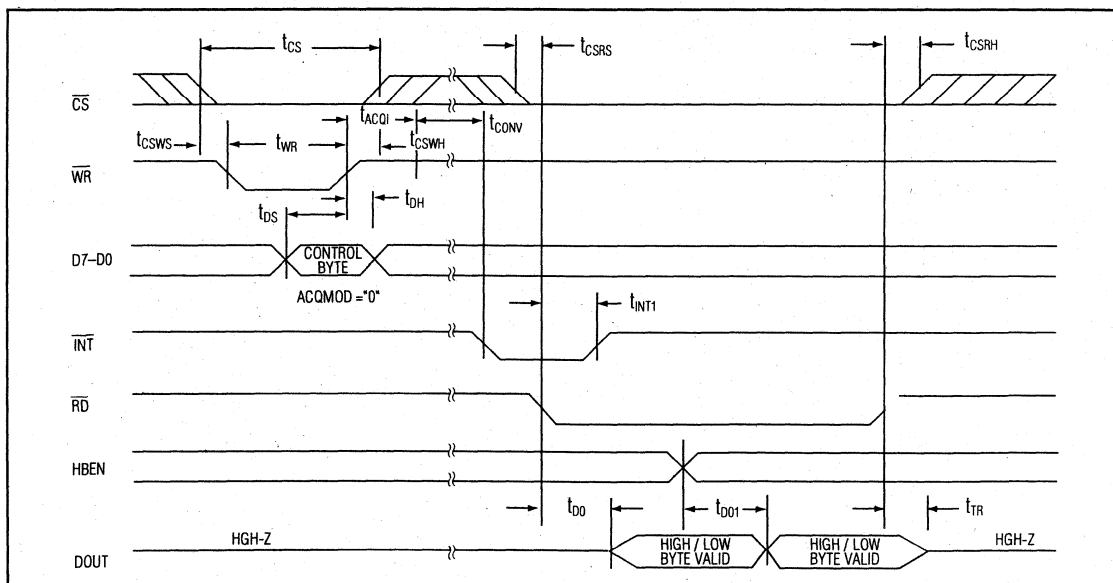


Figure 5. Conversion Timing Using Internal Acquisition Mode

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

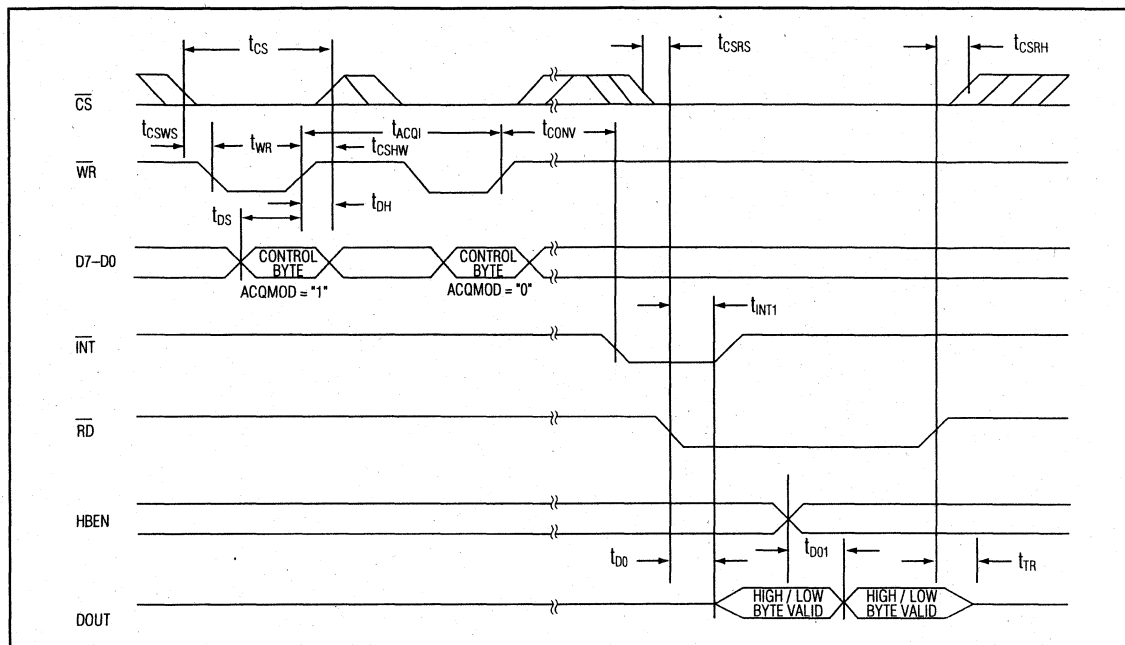


Figure 6. Conversion Timing Using External Acquisition Mode

How to Read a Conversion

A standard interrupt signal, $\overline{INT}$, is provided to allow the device to flag the μP when the conversion has ended and a valid result is available. $\overline{INT}$ goes low when conversion is complete and the output data is ready (Figures 5 and 6). It returns high on the first read cycle or if a new control byte is written.

Clock Modes

The MAX197 operates with either an internal or an external clock. Control bits (D6, D7) select either internal or external clock mode. Once the desired clock mode is selected, changing these bits to program power-down will not affect the clock mode. In each mode, internal or external acquisition can be used. At power-up, external clock mode is selected.

Internal Clock Mode

Select internal clock mode to free the μP from the burden of running the SAR conversion clock. To select this mode, write the control byte with D7 = 0 and D6 = 1. A 100pF capacitor between the CLK pin and ground sets this frequency to 1.56MHz nominal. Figure 7

shows a linear relationship between the internal clock period and the value of the external capacitor used.

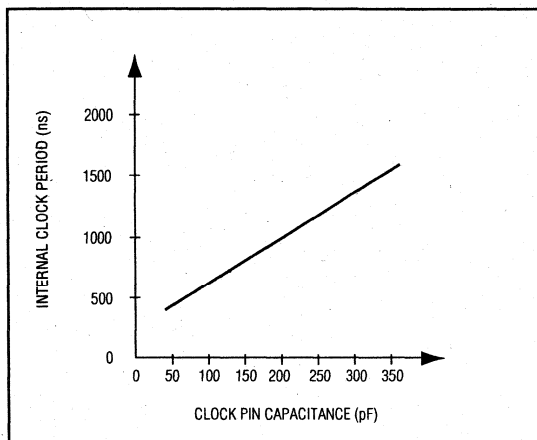


Figure 7. Internal Clock Period vs. Clock Pin Capacitance

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

External Clock Mode

Select external clock mode by writing the control byte with D7 = 0 and D6 = 0. Figure 8 shows CLK and $\overline{WR}$ timing relationships in internal and external acquisition modes, with an external clock. A 100kHz to 2.0MHz

external clock with 45% to 55% duty cycle is required for proper operation. Operating at clock frequencies lower than 100kHz will cause a voltage droop across the hold capacitor, and subsequently degrade performance.

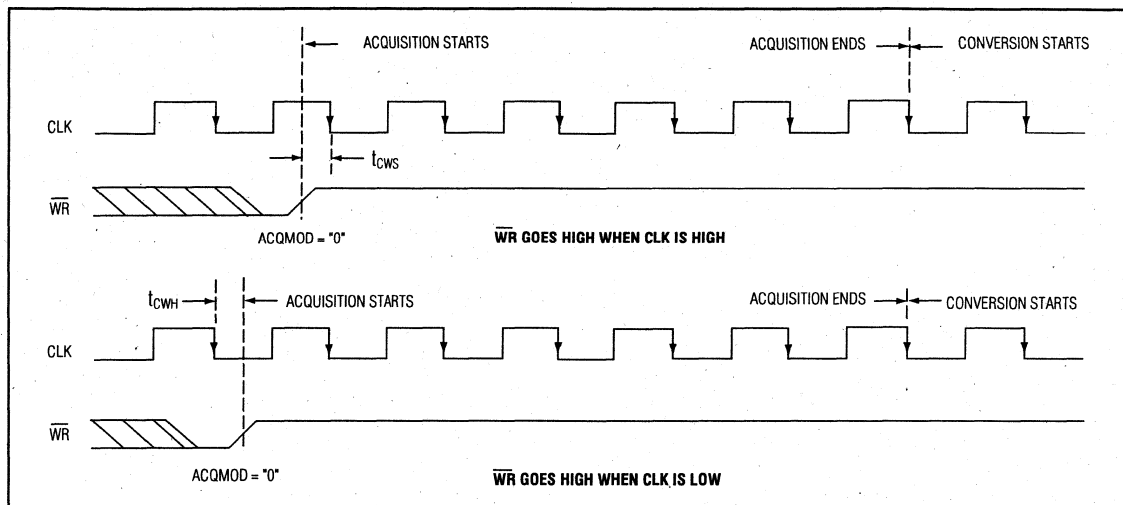


Figure 8a. External Clock and $\overline{WR}$ Timing (Internal Acquisition Mode)

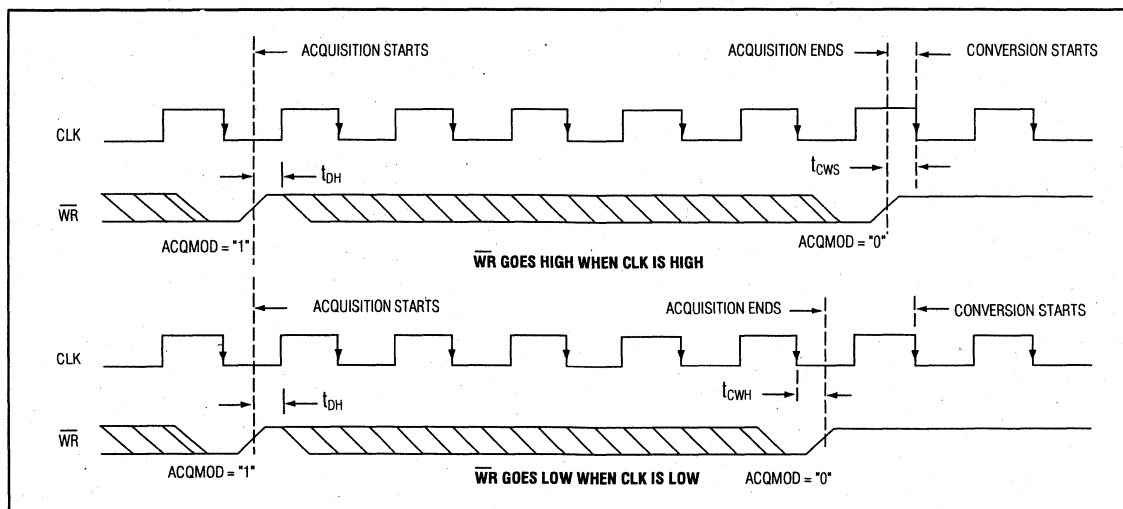


Figure 8b. External Clock and $\overline{WR}$ Timing (External Acquisition Mode)

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

Applications Information

Power-On Reset

At power-up, the internal power-supply circuitry sets INT high and puts the device in normal operation/external clock mode. This state is selected to keep the internal clock from loading the external clock driver when the part is used in external clock mode.

Internal or External Reference

The MAX197 can operate with either an internal or an external reference. An external reference can be connected to either the REF pin or to the REFADJ pin (Figure 9).

To use the REF input directly, disable the internal buffer by tying REFADJ to V_{DD} . Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a $0.01\mu F$ capacitor to AGND.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at the REF pin from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a $4.7\mu F$ capacitor to AGND and the REFADJ pin with a $0.01\mu F$ capacitor to AGND. The internal reference voltage is adjustable to $\pm 1.5\%$ (± 65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

At REF and REFADJ, the input impedance is a minimum of $10k\Omega$ for DC currents. During conversions, an

external reference at REF must be able to deliver $400\mu A$ DC load currents, and must have an output impedance of 10Ω or less. If the reference has higher input impedance or is noisy, bypass it close to the REF pin with a $4.7\mu F$ capacitor to AGND.

With an external reference voltage of less than 4.096V at the REF pin or less than 2.5V at the REFADJ pin, the increase in the ratio of the RMS noise to the LSB value ($FS / 4096$) results in performance degradation (loss of effective bits).

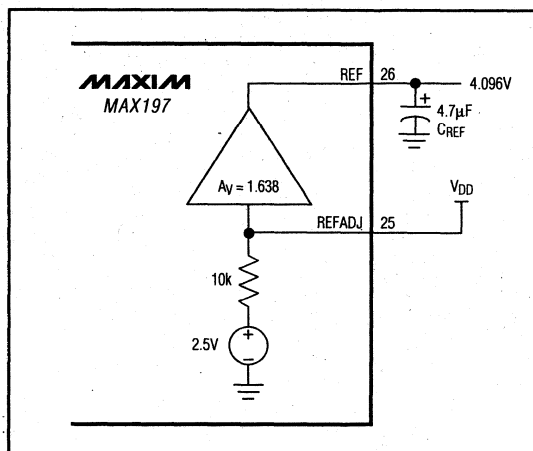


Figure 9b. External Reference, Reference at REF

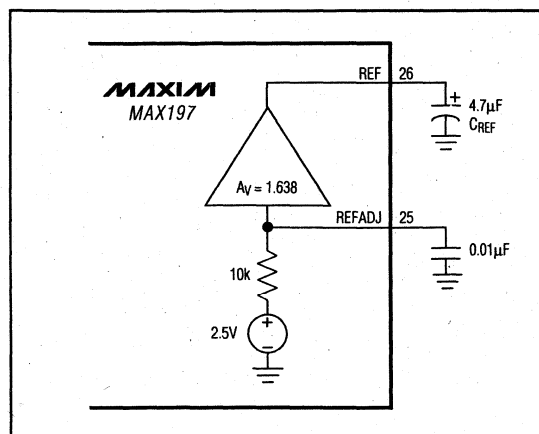


Figure 9a. Internal Reference

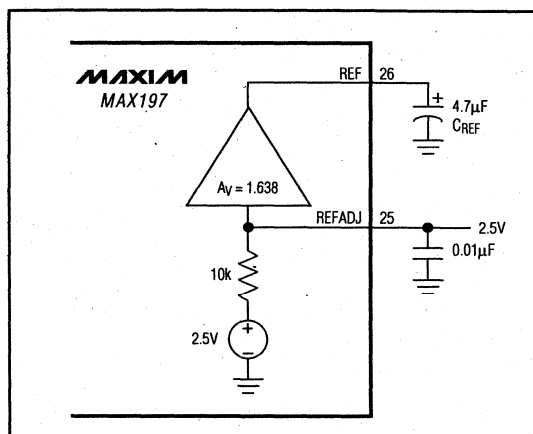


Figure 9c. External Reference, Reference at REFADJ

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

Power-Down Mode

To save power, you can put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available, in addition to a hardware shutdown. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte. When software power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion results may be read. Input overvoltage protection is active in all power-down modes. The device returns to normal operation on the first $\overline{WR}$ falling edge during write operation.

For hardware-controlled (FULLPD) power-down, pull the $\overline{SHDN}$ pin low. When hardware shutdown is asserted, it becomes effective immediately and the conversion is aborted.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the $4.7\mu F$ capacitor at the REF pin. This is a "DC" state that does not degrade after power-down of any duration. Therefore, you can use any sampling rate with this mode, without regard to start-up delays.

However, in FULLPD mode, only the bandgap reference is active. Connect a $33\mu F$ capacitor between REF and AGND to maintain the reference voltage between conversion and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate and add $50\mu s$ for settling time. Throughput rates of 10ksps offer typical supply currents of $470\mu A$, using the recommended $33\mu F$ capacitor value.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX197 down after each conversion without requiring any start-up time on the next conversion.

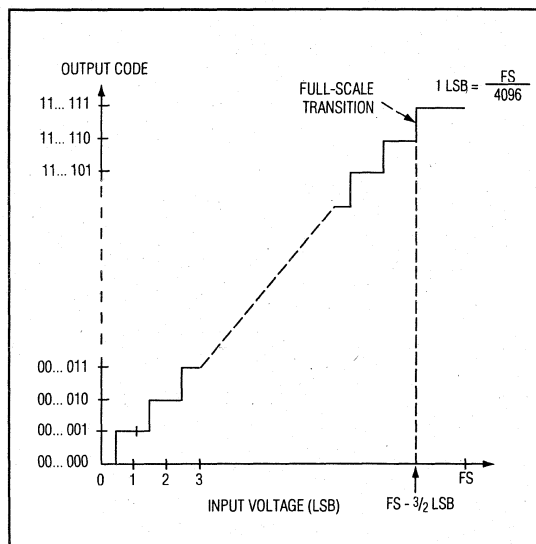


Figure 10. Unipolar Transfer Function

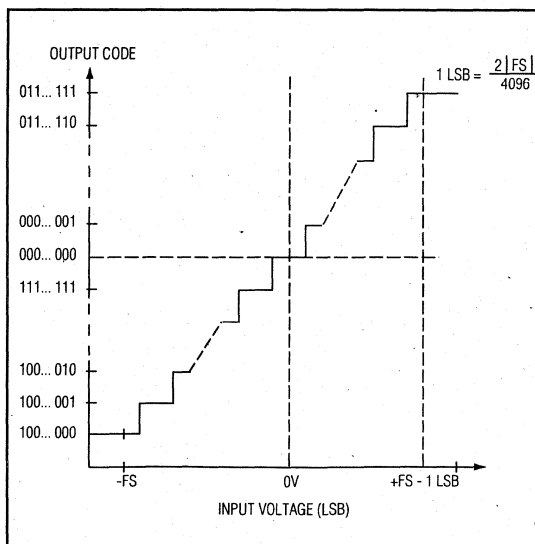


Figure 11. Bipolar Transfer Function

Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

Transfer Function

Output data coding for the MAX197 is binary in unipolar mode with $1\text{LSB} = (\text{FS} / 4096)$ and twos-complement binary in bipolar mode with $1\text{LSB} = ((2 \times |\text{FS}|) / 4096)$. Code transitions occur halfway between successive-integer LSB values. Figures 10 and 11 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively. For full-scale (FS) values, refer to Table 1.

Layout, Grounding, and Bypassing

Careful printed circuit board layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Digital ground lines can run between digital signal lines to minimize interference. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass V_{DD} with $0.1\mu\text{F}$ and $4.7\mu\text{F}$ capacitors to AGND to minimize high- and low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and V_{DD} , as shown in Figure 12.

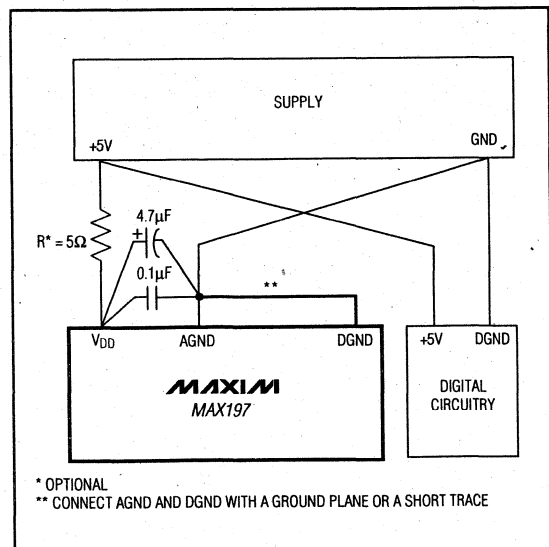


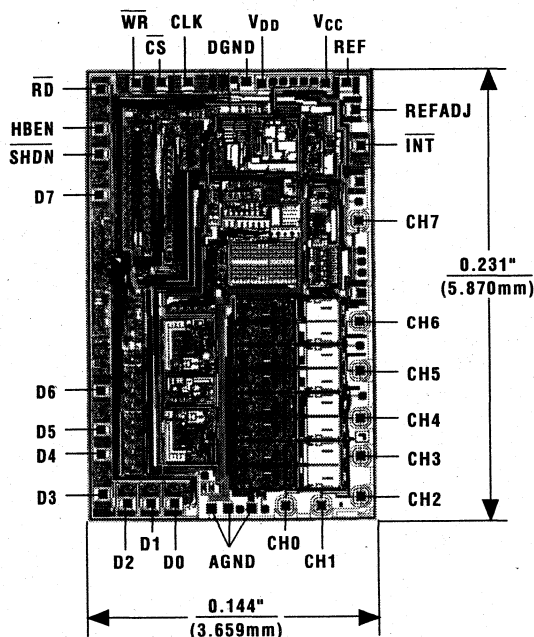
Figure 12. Power-Supply Grounding Connection

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX197AENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX197BENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX197AEWI	-40°C to +85°C	28 Wide SO
MAX197BEWI	-40°C to +85°C	28 Wide SO
MAX197AEAI	-40°C to +85°C	28 SSOP
MAX197BEAI	-40°C to +85°C	28 SSOP
MAX197AMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX197BMYI	-55°C to +125°C	28 Narrow Ceramic SB**

** Contact factory for availability and processing to MIL-STD-883.

Chip Topography



TRANSISTOR COUNT: 2956

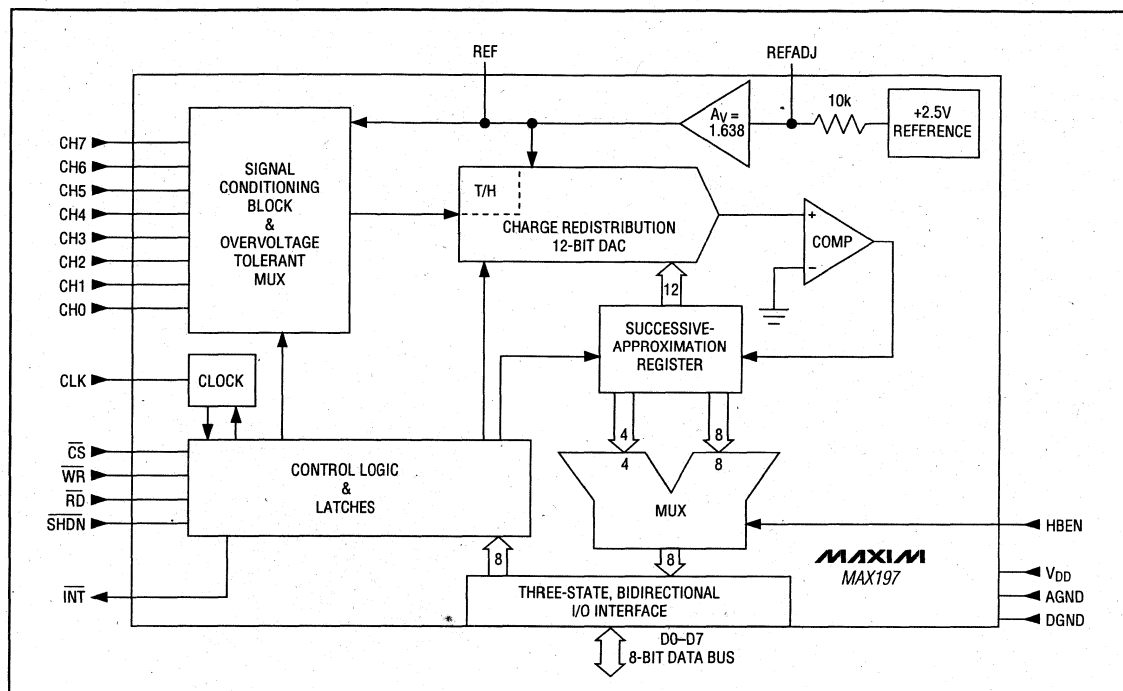
SUBSTRATE CONNECTED TO GND

MAX197

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Multi-Range ($\pm 10V$, $\pm 5V$, $+10V$, $+5V$), Single $+5V$, 12-Bit DAS with 8+4 Bus Interface

Functional Diagram



EVALUATION KIT AVAILABLE

MAXIM

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

General Description

The MAX199 multi-range, 12-bit data-acquisition system (DAS) requires only a single +5V supply for operation, and converts analog signals up to $\pm 4V$ at its inputs. This system provides eight analog input channels that are independently software programmable for a variety of ranges: $\pm V_{REF}$, $\pm V_{REF}/2$, $0V$ to V_{REF} , or $0V$ to $V_{REF}/2$. This increases effective dynamic range to 14 bits, and provides the user flexibility to interface 4mA-to-20mA, $\pm 12V$, and $\pm 15V$ powered sensors to a single +5V system. In addition, the converter is fault-protected to $\pm 16.5V$; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, 100ksps throughput rate, internal/external clock, internal/external acquisition control, 8+4 parallel interface, and operation with an internal 4.096V or external reference.

A hardware SHDN pin and two programmable power-down modes (STBYPD, FULLPD) provide low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX199 employs a standard microprocessor (μP) interface. Its three-state data I/O interface is configured to operate with 8-bit data buses, and data-access and bus-release timing specifications are compatible with most popular μPs . All logic inputs and outputs are TTL/CMOS compatible.

The MAX199 is available in 28-pin DIP, wide SO, SSOP, and ceramic SB packages.

For a different combination of input ranges ($\pm 10V$, $\pm 5V$, $0V$ to $10V$, $0V$ to $5V$), see the MAX197 data sheet. For 12-bit bus interfaces, see the MAX196/MAX198 data sheet.

Applications

Industrial-Control Systems
Robotics
Data-Acquisition Systems
Automatic Testing Systems
Medical Instruments
Telecommunications

Features

- ♦ 12-Bit Resolution, 1/2LSB Linearity
- ♦ Single +5V Operation
- ♦ Software-Selectable Input Ranges:
 $\pm V_{REF}$, $\pm V_{REF}/2$, $0V$ to V_{REF} , $0V$ to $V_{REF}/2$
- ♦ Internal 4.096V or External Reference
- ♦ Fault-Protected Input Multiplexer ($\pm 16.5V$)
- ♦ 8 Analog Input Channels
- ♦ 6 μs Conversion Time, 100ksps Sampling Rate
- ♦ Internal or External Acquisition Control
- ♦ Two Power-Down Modes
- ♦ Internal or External Clock

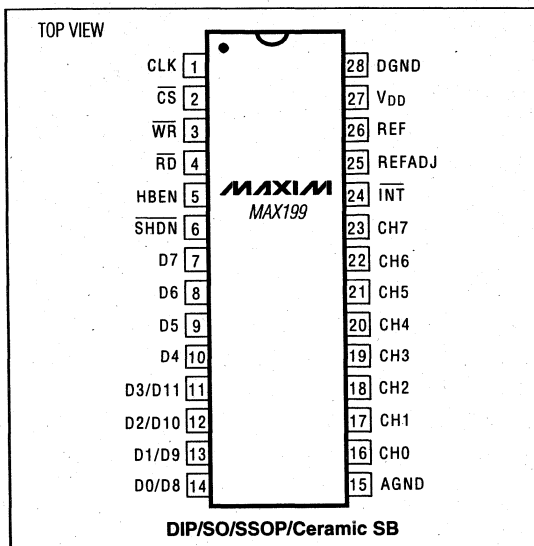
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX199ACNI	0°C to +70°C	28 Narrow Plastic DIP
MAX199BCNI	0°C to +70°C	28 Narrow Plastic DIP
MAX199ACWI	0°C to +70°C	28 Wide SO
MAX199BCWI	0°C to +70°C	28 Wide SO
MAX199ACAI	0°C to +70°C	28 SSOP
MAX199BCAI	0°C to +70°C	28 SSOP
MAX199BC/D	0°C to +70°C	Dice*

Ordering information continued at end of data sheet.

*Dice are specified at $T_A = +25^\circ C$, DC parameters only.

Pin Configuration



Functional Diagram appears at end of data sheet.

MAXIM

Maxim Integrated Products 7-137

Call toll free 1-800-722-8266 for free samples or literature.

MAX199

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Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

ABSOLUTE MAXIMUM RATINGS

V _{DD} to AGND	-0.3V to +7V
AGND to DGND	-0.3V to +0.3V
REF to AGND	-0.3V to (V _{DD} + 0.3V)
REFADJ to AGND	-0.3V to (V _{DD} + 0.3V)
Digital Inputs to DGND	-0.3V to (V _{DD} + 0.3V)
Digital Outputs to DGND	-0.3V to (V _{DD} + 0.3V)
CH0-CH7 to AGND	 $\pm 16.5V$
Continuous Power Dissipation (T _A = +70°C)	
Narrow Plastic DIP (derate 14.29mW/°C above +70°C)	1143mW

Wide SO (derate 12.50mW/°C above +70°C)	1000mW
SSOP (derate 9.52mW/°C above +70°C)	762mW
Narrow Ceramic SB (derate 20.00mW/°C above +70°C)	1600mW
Operating Temperature Ranges	
MAX199_C_	0°C to +70°C
MAX199_E_	-40°C to +85°C
MAX199_M_	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V $\pm 5\%$; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7 μ F at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX199A				±1/2	LSB
		MAX199B				±1	
Differential Nonlinearity	DNL					±1	LSB
Offset Error		Unipolar	MAX199A			±3	LSB
			MAX199B			±5	
		Bipolar	MAX199A			±5	
			MAX199B			±10	
Channel-to-Channel Offset Error Matching		Unipolar				±0.1	LSB
		Bipolar				±0.5	
Gain Error (Note 2)		Unipolar	MAX199A			±7	LSB
			MAX199B			±10	
		Bipolar	MAX199A			±7	
			MAX199B			±10	
Gain Temperature Coefficient (Note 2)		Unipolar				3	ppm/°C
		Bipolar				5	
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±4.096Vp-p, fSAMPLE = 100ksps)							
Signal-to-Noise + Distortion Ratio	SINAD		MAX199A		70		dB
			MAX199B		69		
Total Harmonic Distortion	THD	Up to the 5th harmonic			-85	-78	dB
Spurious-Free Dynamic Range	SFDR				80		dB
Channel-to-Channel Crosstalk		50kHz, VIN = ±4V (Note 3)			-86		dB
Aperture Delay		External CLK mode/external acquisition control			15		ns
Aperture Jitter		External CLK mode/external acquisition control			<50		ps
		Internal CLK mode/internal acquisition control (Note 4)			10		ns

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
ANALOG INPUT								
Track/Hold Acquisition Time		fCLK = 2.0MHz		3			μs	
Small-Signal Bandwidth		-3dB rolloff	±VREF range	5			MHz	
			±VREF/2 range	2.5				
			0V to VREF range	2.5				
			0V to VREF/2 range	1.25				
Input Voltage Range		Unipolar (see Table 2)		0	VREF		V	
				0	VREF/2			
		Bipolar (see Table 2)		-VREF	VREF			
				-VREF/2	VREF/2			
Input Current		Unipolar range		0.1	10		μA	
		Bipolar	±VREF range	-1200	10			
			±VREF/2 range	-600	10			
Input Dynamic Resistance		Unipolar		40		MΩ		
		Bipolar		10		kΩ		
Input Capacitance		(Note 5)		40		pF		
INTERNAL REFERENCE								
REF Output Voltage	VREF	TA = +25°C		4.076	4.096	4.116	V	
REF Output Tempco (Contact Maxim Applications for guaranteed temperature drift specifications)	TC VREF	MAX199_C		±15			ppm/°C	
		MAX199_E		±30				
		MAX199_M		±40				
Output Short-Circuit Current				30			mA	
Load Regulation		0mA to 0.5mA output current (Note 6)		7.5			mV	
		0mA to 0.1mA output current (Note 6)		0.8				
Capacitive Bypass at REF				4.7			μF	
REFADJ Output Voltage				2.465	2.500	2.535	V	
REFADJ Adjustment Range		With recommended circuit (Figure 1)		±1.5			%	
Buffer Voltage Gain				1.6384			V/V	
REFERENCE INPUT (Buffer disabled, reference input applied to REF pin)								
Input Voltage Range				2.4			4.18	V
Input Current		VREF = 4.18V	Normal, or STANDBY power-down mode	400			μA	
			FULL power-down mode	1				
Input Resistance		Normal, or STANDBY power-down mode		10			kΩ	
		FULL power-down mode		5			MΩ	
REFADJ Threshold for Buffer Disable				VDD - 50mV			V	

MAX199

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Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage	VDD			4.75		5.25	V
Supply Current	IDD	Normal mode, bipolar ranges				18	mA
		Normal mode, unipolar ranges			6	10	
		Standby power-down (STBYPD)			700	850	μA
		Full power-down mode (FULLPD) (Note 7)			60	120	
Power-Supply Rejection Ratio (Note 8)	PSRR	External reference = 4.096V				±1/2	LSB
		Internal reference				±1/2	
TIMING							
Internal Clock Frequency	fCLK	CCLK = 100pF		1.25	1.56	2.00	MHz
External Clock Frequency Range	fCLK			0.1		2.0	MHz
Acquisition Time	tACQI	Internal acquisition	External CLK	3.0			μs
			Internal CLK	3.0		5.0	
	tACQE	External acquisition (Note 9)		3.0			
		After FULLPD or STBYPD			5		
Conversion Time	tCONV	External CLK		6.0			μs
		Internal CLK, CCLK = 100pF		6.0	7.7	10.0	
Throughput Rate		External CLK				100	ksps
		Internal CLK, CCLK = 100pF		62			
Bandgap Reference Start-Up Time		Power-up (Note 10)			200		μs
Reference Buffer Settling		To 0.1mV, REF bypass capacitor fully discharged	CREF = 4.7μF		8		ms
			CREF = 33μF		60		
DIGITAL INPUTS (D7–D0, CLK, RD, WR, CS, HBEN, SHDN) (Note 11)							
Input High Voltage	VINH			2.4			V
Input Low Voltage	VINL					0.8	V
Input Leakage Current	IIN	VIN = 0V or VDD				±10	μA
Input Capacitance	CIN	(Note 5)				15	pF
DIGITAL OUTPUTS (D7–D4, D3/D11, D2/D10, D1/D9, D0/D8, INT)							
Output Low Voltage	VOL	VDD = 4.75V, ISINK = 1.6mA				0.4	V
Output High Voltage	VOH	VDD = 4.75V, ISOURCE = 1mA		VDD - 1			V
Three-State Output Capacitance	COUT	(Note 5)				15	pF

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

TIMING CHARACTERISTICS

($V_{DD} = 5V \pm 5\%$; unipolar/bipolar range; external reference mode, $V_{REF} = 4.096V$; $4.7\mu F$ at REF pin; external clock, $f_{CLK} = 2.0MHz$ with 50% duty cycle; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CS Pulse Width	t_{CS}		80			ns
$\overline{WR}$ Pulse Width	t_{WR}		80			ns
CS to $\overline{WR}$ Setup Time	t_{CSWS}		0			ns
CS to $\overline{WR}$ Hold Time	t_{CSWH}		0			ns
CS to $\overline{RD}$ Setup Time	t_{CSRS}		0			ns
CS to $\overline{RD}$ Hold Time	t_{CSRH}		0			ns
CLK to $\overline{WR}$ Setup Time	t_{CWS}				100	ns
CLK to $\overline{WR}$ Hold Time	t_{CWH}				50	ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		60			ns
Data Valid to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{RD}$ Low to Output Data Valid	t_{DO}	Figure 2, $C_L = 100pF$ (Note 12)			120	ns
HBEN High or HBEN Low to Output Valid	t_{DO1}	Figure 2, $C_L = 100pF$ (Note 12)			120	ns
$\overline{RD}$ High to Output Disable	t_{TR}	(Note 13)			70	ns
$\overline{RD}$ Low to $\overline{INT}$ High Delay	t_{INT1}				120	ns

Note 1: Accuracy specifications tested at $V_{DD} = 5.0V$. Performance at power-supply tolerance limits guaranteed by Power-Supply Rejection test. Tested for the $\pm 4.096V$ input range.

Note 2: External reference: $V_{REF} = 4.096V$, offset error nulled, ideal last code transition = $FS - 3/2LSB$.

Note 3: Ground "on" channel; sine wave applied to all "off" channels.

Note 4: Maximum full-power input frequency for 1LSB error with 10ns jitter = 3kHz.

Note 5: Guaranteed by design. Not tested.

Note 6: Use static loads only.

Note 7: Tested using internal reference.

Note 8: PSRR measured at full-scale. $V_{DD} = 4.75V$ to $5.25V$.

Note 9: External acquisition timing: starts at rising edge of $\overline{WR}$ with control bit ACQMOD = low; ends at rising edge of $\overline{WR}$ with ACQMOD = high.

Note 10: Not subject to production testing. Provided for design guidance only.

Note 11: All input control signals specified with $t_R = t_F = 5ns$ from a voltage level of 0.8V to 2.4V.

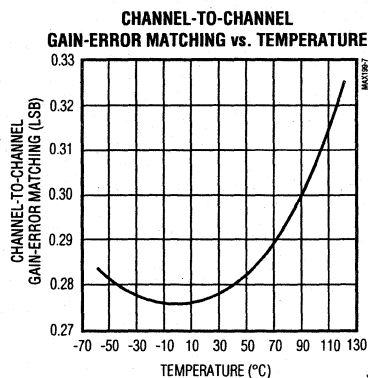
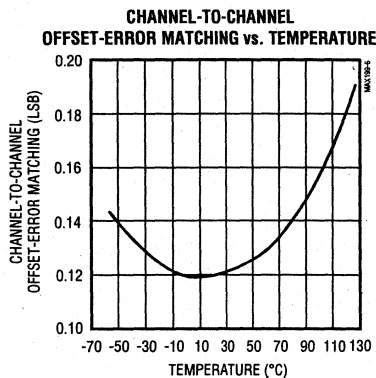
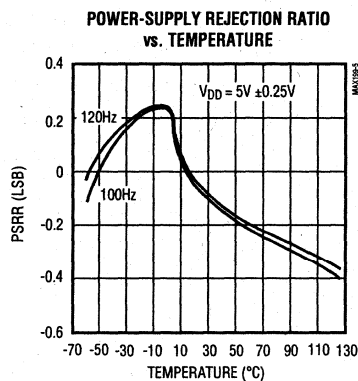
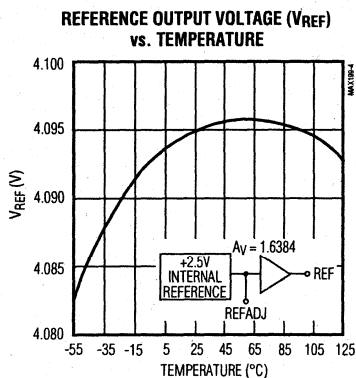
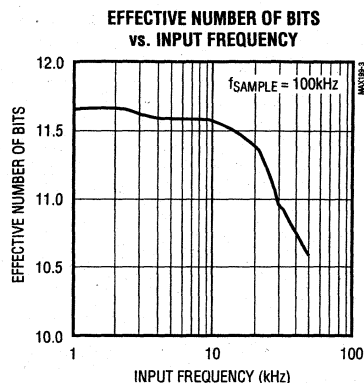
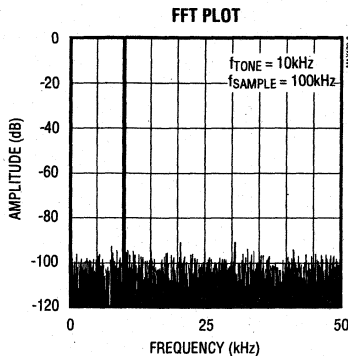
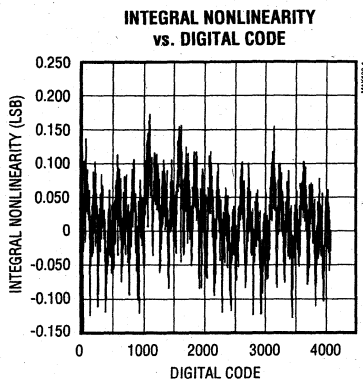
Note 12: t_{DO} and t_{DO1} are measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 13: t_{TR} is defined as the time required for the data lines to change by 0.5V.

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Input. In external clock mode, drive CLK with a TTL/CMOS compatible clock. In internal clock mode, place a capacitor (C_{CLK}) from this pin to ground to set the internal clock frequency; $f_{CLK} = 1.56\text{MHz}$ typical with $C_{CLK} = 100\text{pF}$.
2	$\overline{CS}$	Chip Select, active low.
3	$\overline{WR}$	When $\overline{CS}$ is low, in the internal acquisition mode, a rising edge on $\overline{WR}$ latches in configuration data and starts an acquisition plus a conversion cycle. When $\overline{CS}$ is low, in the external acquisition mode, the first rising edge on $\overline{WR}$ starts an acquisition and a second rising edge on $\overline{WR}$ ends acquisition and starts a conversion cycle.
4	$\overline{RD}$	When $\overline{CS}$ is low, a falling edge on $\overline{RD}$ will enable a read operation on the data bus.
5	HBEN	Used to multiplex the 12-bit conversion result. When high, the 4 MSBs are multiplexed on the data bus; when low, the 8 LSBs are available on the bus.
6	$\overline{SHDN}$	Shutdown. Puts the device into full power-down (FULLPD) mode when pulled low.
7–10	D7–D4	Three-State Digital I/O
11	D3/D11	Three-State Digital I/O. D3 output (HBEN = low), D11 output (HBEN = high).
12	D2/D10	Three-State Digital I/O. D2 output (HBEN = low), D10 output (HBEN = high).
13	D1/D9	Three-State Digital I/O. D1 output (HBEN = low), D9 output (HBEN = high).
14	D0/D8	Three-State Digital I/O. D0 output (HBEN = low), D8 output (HBEN = high). D0 = LSB.
15	AGND	Analog Ground
16–23	CH0–CH7	Analog Input Channels
24	$\overline{INT}$	$\overline{INT}$ goes low when conversion is complete and output data is ready.
25	REFADJ	Bandgap Voltage-Reference Output / External Adjust Pin. Bypass with a $0.01\mu\text{F}$ capacitor to AGND. Connect to V_{DD} when using an external reference at the REF pin.
26	REF	Reference Buffer Output / ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD} .
27	V_{DD}	+5V Supply. Bypass with $0.1\mu\text{F}$ capacitor to AGND.
28	DGND	Digital Ground

MAX199

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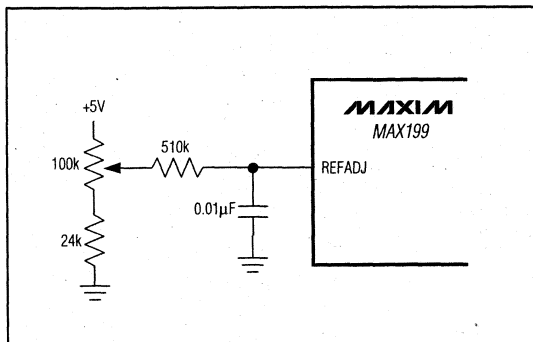


Figure 1. Reference-Adjust Circuit

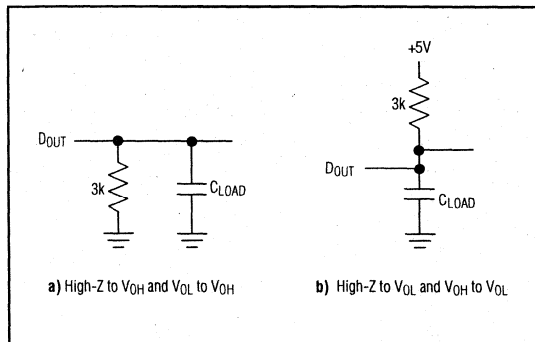


Figure 2. Load Circuits for Enable Time

**Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$),
+5V Supply, 12-Bit DAS with 8+4 Bus Interface**

Detailed Description

Converter Operation

The MAX199, a multi-range, fault-tolerant ADC, uses successive approximation and internal input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. The parallel-output format provides easy interface to microprocessors (μ Ps). Figure 3 shows the MAX199 in its simplest operational configuration.

Analog-Input Track/Hold

In the internal acquisition control mode (control bit D5 set to 0), the T/H enters its tracking mode on WR 's rising edge, and enters its hold mode when the internally timed (6 clock cycles) acquisition interval ends. In bipolar mode, a low-impedance input source, which settles in less than $1.5\mu s$, is required to maintain conversion accuracy at the maximum conversion rate.

When configured for unipolar mode, the input does not need to be driven from a low-impedance source. The acquisition time (tAZ) is a function of the source output resistance (Rs), the channel input resistance (RIN), and the T/H capacitance.

Acquisition time is calculated by:

For 0V to V_{REF} : $t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF$

For 0V to $V_{REF}/2$: $t_{AZ} = 9 \times (R_S + R_{IN}) \times 32pF$

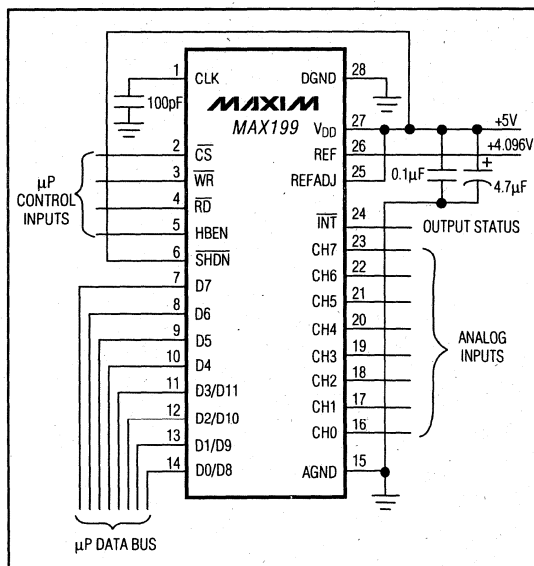


Figure 3. Operational Diagram

where $R_{IN} = 7k\Omega$, and t_{AZ} is never less than $2\mu s$ (0V to V_{REF} range) or $3\mu s$ (0V to $V_{REF}/2$ range).

In the external acquisition control mode ($D5 = 1$), the T/H enters its tracking mode on the first $\overline{WR}$ rising edge and enters its hold mode when it detects the second $\overline{WR}$ rising edge with $D5 = 0$. See the *External Acquisition* section.

Input Bandwidth

The ADC's input tracking circuitry has a 5MHz small-signal bandwidth. When using the internal acquisition mode with an external clock frequency of 2MHz, a 100ksp/s throughput rate can be achieved. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended (MAX274/MAX275 continuous-time filters).

Input Range and Protection

Figure 4 shows the equivalent input circuit. The MAX199 can be programmed for input ranges of $\pm V_{REF}$, $\pm V_{REF}/2$, $0V$ to V_{REF} , or $0V$ to $V_{REF}/2$ by setting the appropriate control bits (D3, D4) in the control byte (see Tables 1 and 2). When an external reference is applied at REFADJ, the voltage at REF is given by $V_{REF} = 1.6384 \times V_{REFADJ}$ ($2.4V < V_{REF} < 4.18V$).

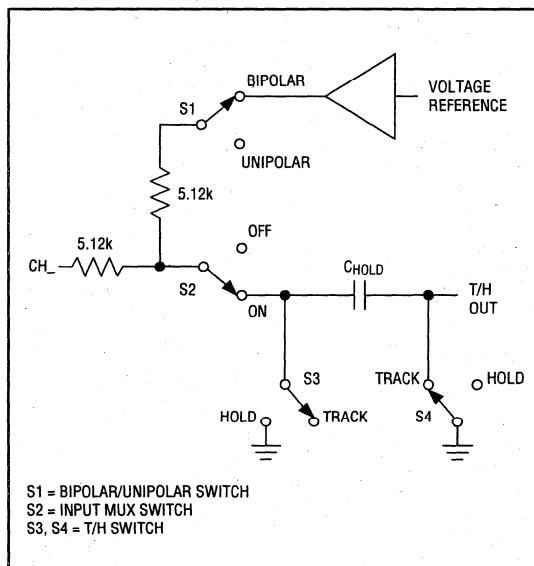


Figure 4. Equivalent Input Circuit

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

MAX199

The input channels are overvoltage protected to $\pm 16.5V$. This protection is active even if the device is in power-down mode.

Even with $V_{DD} = 0V$, the input resistive network provides current-limiting that adequately protects the device.

Digital Interface

Input data (control byte) and output data are multiplexed on a three-state parallel interface. This parallel I/O can easily be interfaced with a μP . $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ control the write and read operations. $\overline{CS}$ is the standard chip-select signal, which enables a μP to address the MAX199 as an I/O port. When high, it disables the $\overline{WR}$ and $\overline{RD}$ inputs and forces the interface into a high-Z state.

Input Format

The control byte is latched into the device, on pins D7–D0, during a write cycle. Table 1 shows the control-byte format.

Output Data Format

The output data format is binary in unipolar mode and two's-complement binary in bipolar mode. When reading the output data, $\overline{CS}$ and $\overline{RD}$ must be low. When $\overline{HBEN}$ is low, the lower eight bits are read. When $\overline{HBEN}$ is high, the upper four MSBs are available and the output data bits D4–D7 are either set low (in unipolar mode) or set to the value of the MSB (in bipolar mode) (Table 5).

Table 1. Control-Byte Format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7, 6	PD1, PD0	These two bits select the clock and power-down modes (Table 3).
5	ACQMOD	0 = internally controlled acquisition (6 clock cycles), 1 = externally controlled acquisition
4	RNG	Selects the full-scale voltage magnitude at the input (Table 2).
3	BIP	Selects unipolar or bipolar conversion mode (Table 2).
2, 1, 0	A2, A1, A0	These are address bits for the input mux to select the "on" channel (Table 4).

Table 2. Range and Polarity Selection

BIP	RNG	INPUT RANGE (V)
0	0	0 to $V_{REF}/2$
0	1	0 to V_{REF}
1	0	$\pm V_{REF}/2$
1	1	$\pm V_{REF}$

Table 3. Clock and Power-Down Selection

PD1	PD0	DEVICE MODE
0	0	Normal Operation / External Clock Mode
0	1	Normal Operation / Internal Clock Mode
1	0	Standby Power-Down (STBYPD); clock mode is unaffected
1	1	Full Power-Down (FULLPD); clock mode is unaffected

Table 4. Channel Selection

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	*							
0	0	1		*						
0	1	0			*					
0	1	1				*				
1	0	0					*			
1	0	1						*		
1	1	0							*	
1	1	1								*

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Table 5. Data-Bus Output

PIN	HBEN = LOW	HBEN = HIGH
D0	B0 (LSB)	B8
D1	B1	B9
D2	B2	B10
D3	B3	B11 (MSB)
D4	B4	B11 (BIP = 1) / 0 (BIP = 0)
D5	B5	B11 (BIP = 1) / 0 (BIP = 0)
D6	B6	B11 (BIP = 1) / 0 (BIP = 0)
D7	B7	B11 (BIP = 1) / 0 (BIP = 0)

How to Start a Conversion

Conversions are initiated with a write operation, which selects the mux channel and configures the MAX199 for either unipolar or bipolar input range. A write pulse ($\overline{WR}$ + $\overline{CS}$) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode.

Writing a new control byte during the conversion cycle will abort the conversion in progress and start a new acquisition interval.

Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3 μ s with fCLK = 2MHz) ends. See Figure 5.

External Acquisition

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0, terminates acquisition and starts conversion on $\overline{WR}$'s rising edge (Figure 6). However, if the second control byte contains ACQMOD = 1, an indefinite acquisition interval is restarted.

The address bits for the input mux must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see *Power-Down Mode*).

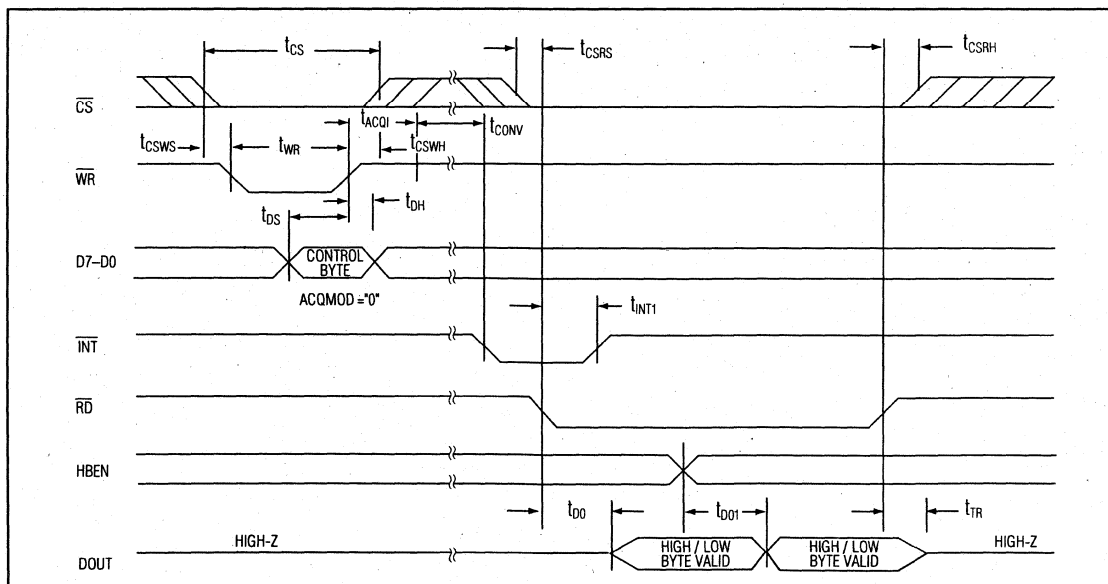


Figure 5. Conversion Timing Using Internal Acquisition Mode

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

MAX199

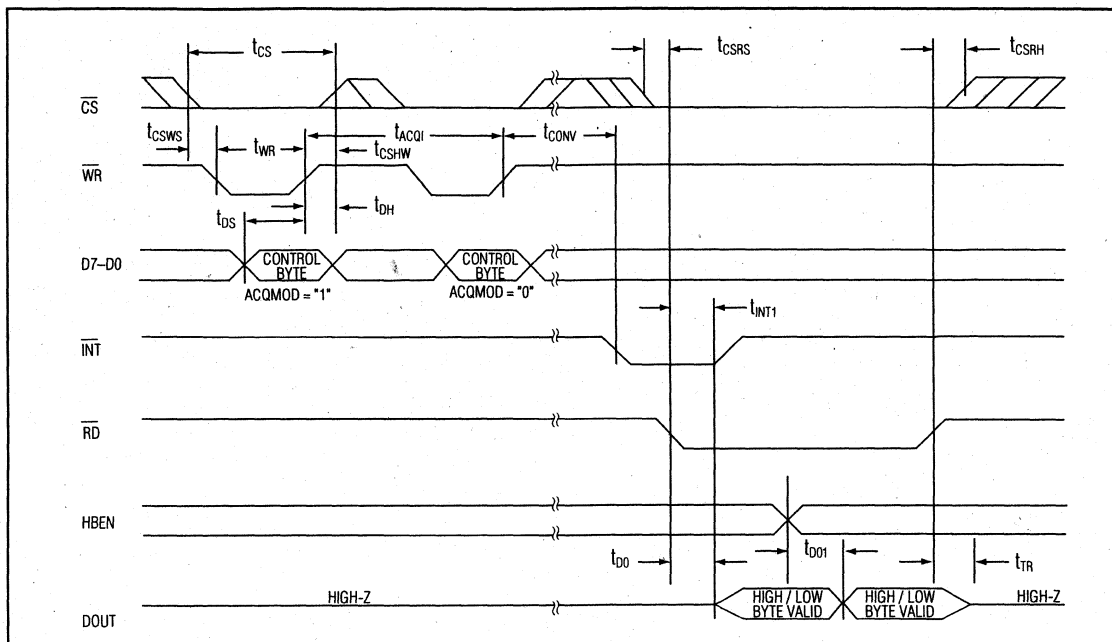


Figure 6. Conversion Timing Using External Acquisition Mode

How to Read a Conversion

A standard interrupt signal, $\overline{INT}$, is provided to allow the device to flag the μP when the conversion has ended and a valid result is available. $\overline{INT}$ goes low when the conversion is complete and the output data is ready (Figures 5 and 6). It returns high on the first read cycle or if a new control byte is written.

Clock Modes

The MAX199 operates with either an internal or an external clock. Control bits (D6, D7) select either internal or external clock mode. Once the desired clock mode is selected, changing these bits to program power-down will not affect the clock mode. In each mode, internal or external acquisition can be used. At power-up, the MAX199 defaults to external clock mode.

Internal Clock Mode

Select internal clock mode to free the μP from the burden of running the SAR conversion clock. To select this mode, write the control byte with D7 = 0 and D6 = 1. A 100pF capacitor between the CLK pin and ground sets this frequency to 1.56MHz nominal. Figure 7

shows a linear relationship between the internal clock period and the value of the external capacitor used.

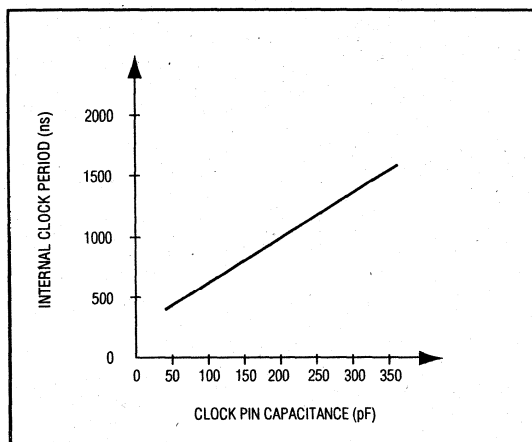


Figure 7. Internal Clock Period vs. Clock Pin Capacitance

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

External Clock Mode

Select external clock mode by writing the control byte with D7 = 0 and D6 = 0. Figure 8 shows CLK and $\overline{WR}$ timing relationships in internal and external acquisition modes, with an external clock. A 100kHz to 2.0MHz

external clock with 45% to 55% duty cycle is required for proper operation. Operating at clock frequencies lower than 100kHz will cause a voltage droop across the hold capacitor, and subsequently degrade performance.

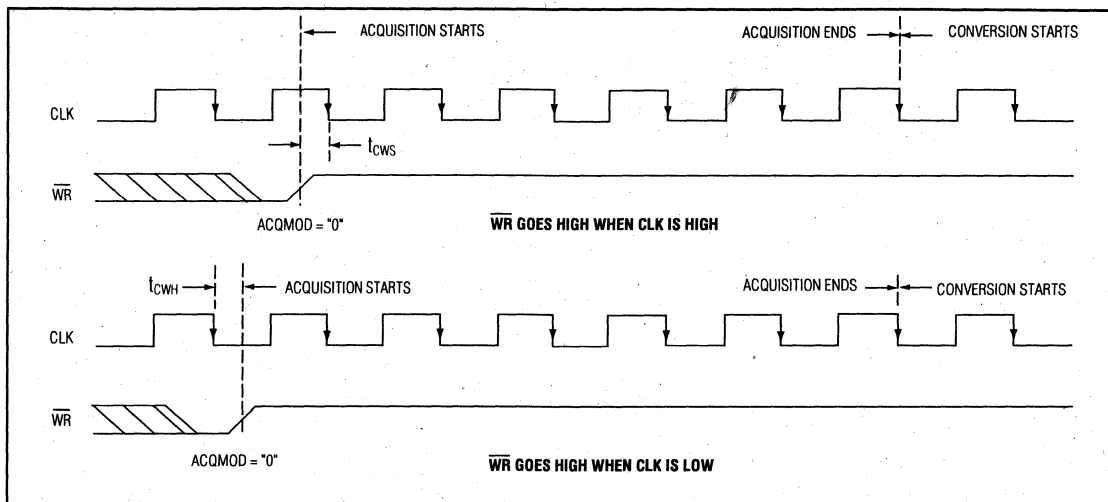


Figure 8a. External Clock and $\overline{WR}$ Timing (Internal Acquisition Mode)

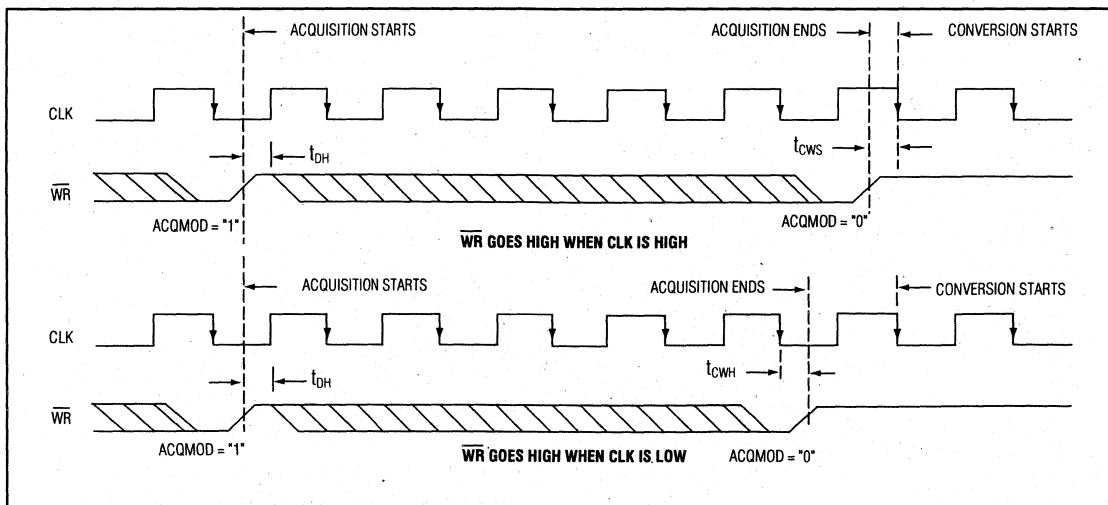


Figure 8b. External Clock and $\overline{WR}$ Timing (External Acquisition Mode)

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Applications Information

Power-On Reset

At power-up, the internal power-supply circuitry sets $\overline{INT}$ high and puts the device in normal operation / external clock mode. This state is selected to keep the internal clock from loading the external clock driver when the part is used in external clock mode.

Internal or External Reference

The MAX199 can operate with either an internal or external reference. An external reference can be connected to either the REF pin or to the REFADJ pin (Figure 9).

To use the REF input directly, disable the internal buffer by tying REFADJ to V_{DD} . Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a $0.01\mu F$ capacitor to AGND.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at the REF pin from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a $4.7\mu F$ capacitor to AGND and the REFADJ pin with a $0.01\mu F$ capacitor to AGND. The internal reference voltage is adjustable to $\pm 1.5\%$ (± 65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

At REF and REFADJ, the input impedance is a minimum of $10k\Omega$ for DC currents. During conversions, an

external reference at REF must be able to deliver $400\mu A$ DC load currents, and must have an output impedance of 10Ω or less. If the reference has higher input impedance or is noisy, bypass it close to the REF pin with a $4.7\mu F$ capacitor to AGND.

With an external reference voltage of less than 4.096V at the REF pin or less than 2.5V at the REFADJ pin, the increase in the ratio of the RMS noise to the LSB value (FS / 4096) results in performance degradation (loss of effective bits).

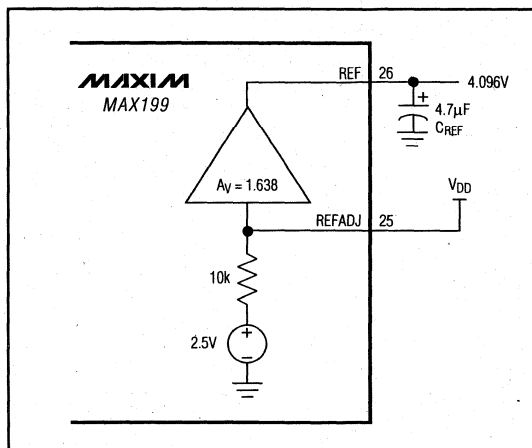


Figure 9b. External Reference at REF

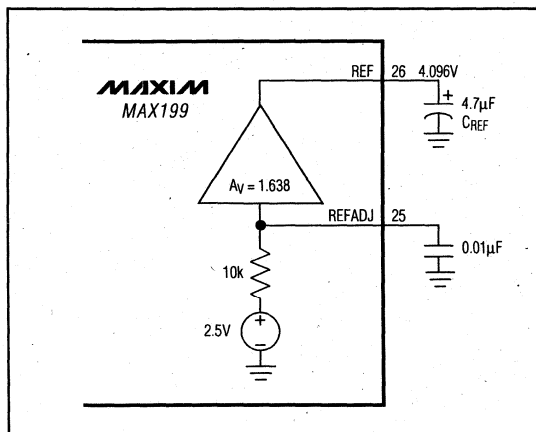


Figure 9a. Internal Reference

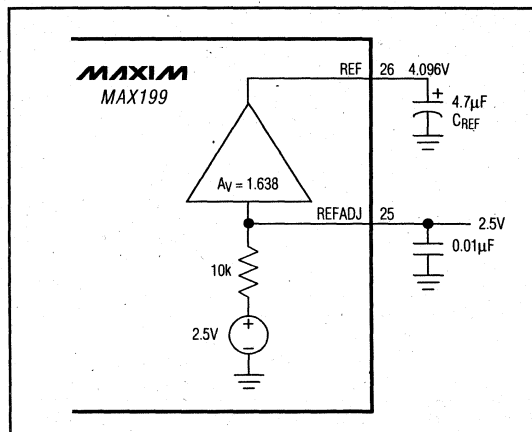


Figure 9c. The external reference at REFADJ overdrives the internal reference.

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Power-Down Mode

To save power, you can put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available, in addition to a hardware shutdown. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte. When software power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion results may be read. Input overvoltage protection is active in all power-down modes. The device returns to normal operation on the first $\overline{WR}$ falling edge during a write operation.

For hardware-controlled (FULLPD) power-down, pull the $\overline{SHDN}$ pin low. When hardware shutdown is asserted, it becomes effective immediately and the conversion is aborted.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the $4.7\mu F$ capacitor at the REF pin. This is a "DC" state that does not degrade after power-down of any duration. Therefore, you can use any sampling rate with this mode, without regard to start-up delays.

However, in FULLPD mode, only the bandgap reference is active. Connect a $33\mu F$ capacitor between REF and AGND to maintain the reference voltage between conversion and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksp/s can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows a conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate and add $50\mu s$ for settling time. Throughput rates of 10ksp/s offer typical supply currents of $470\mu A$, using the recommended $33\mu F$ capacitor value.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX199 down after each conversion without requiring any start-up time on the next conversion.

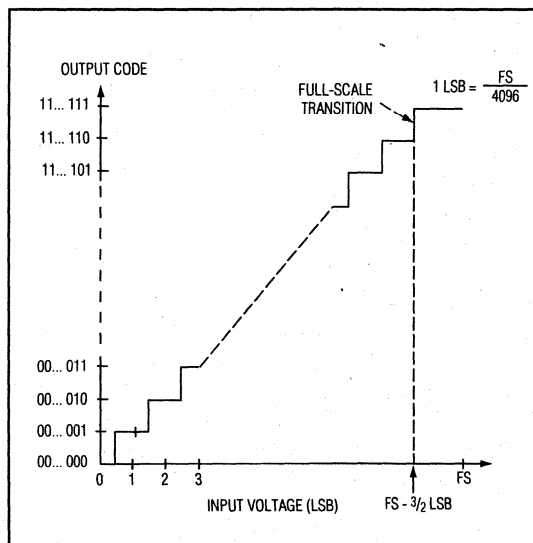


Figure 10. Unipolar Transfer Function

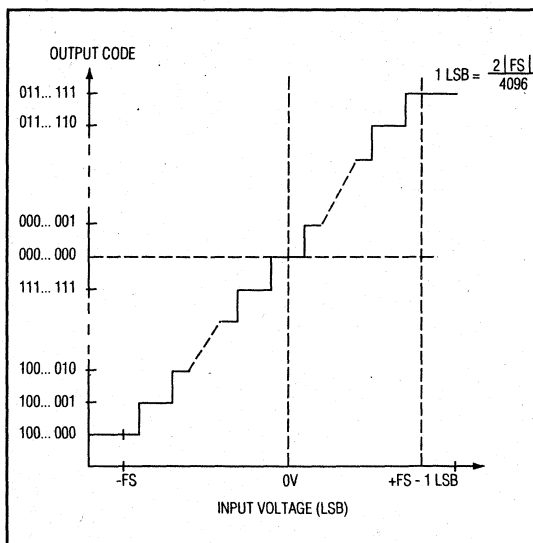


Figure 11. Bipolar Transfer Function

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Transfer Function

Output data coding for the MAX199 is binary in unipolar mode with $1\text{LSB} = (\text{FS} / 4096)$ and two's-complement binary in bipolar mode with $1\text{LSB} = [(2 \times |\text{FS}|) / 4096]$. Code transitions occur halfway between successive-integer LSB values. Figures 10 and 11 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively.

Layout, Grounding, and Bypassing

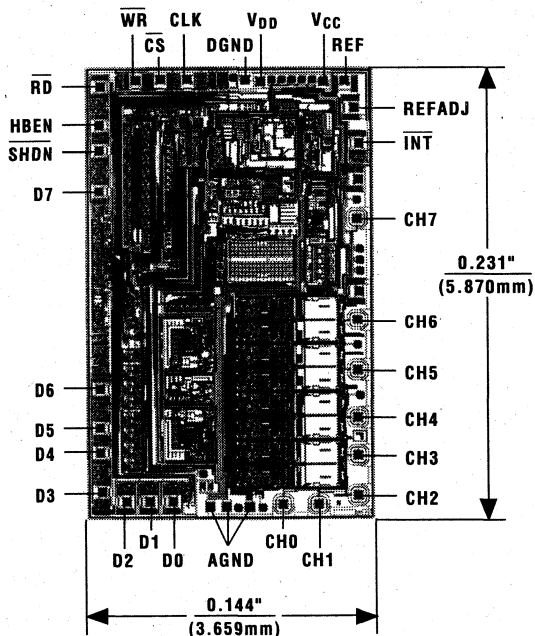
Careful printed circuit board layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Digital ground lines can run between digital signal lines to minimize interference. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass VDD with $0.1\mu\text{F}$ and $4.7\mu\text{F}$ capacitors to AGND to minimize high- and low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and VDD, as shown in Figure 12.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX199AENI	-40°C to $+85^{\circ}\text{C}$	28 Narrow Plastic DIP
MAX199BENI	-40°C to $+85^{\circ}\text{C}$	28 Narrow Plastic DIP
MAX199AEWI	-40°C to $+85^{\circ}\text{C}$	28 Wide SO
MAX199BEWI	-40°C to $+85^{\circ}\text{C}$	28 Wide SO
MAX199AEAI	-40°C to $+85^{\circ}\text{C}$	28 SSOP
MAX199BEAI	-40°C to $+85^{\circ}\text{C}$	28 SSOP
MAX199AMYI	-55°C to $+125^{\circ}\text{C}$	28 Narrow Ceramic SB**
MAX199BMYI	-55°C to $+125^{\circ}\text{C}$	28 Narrow Ceramic SB**

** Contact factory for availability and processing to MIL-STD-883.

Chip Topography



TRANSISTOR COUNT: 2956

SUBSTRATE CONNECTED TO GND

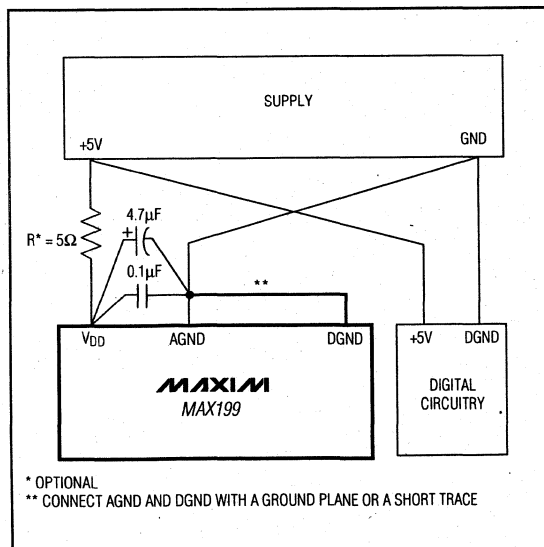
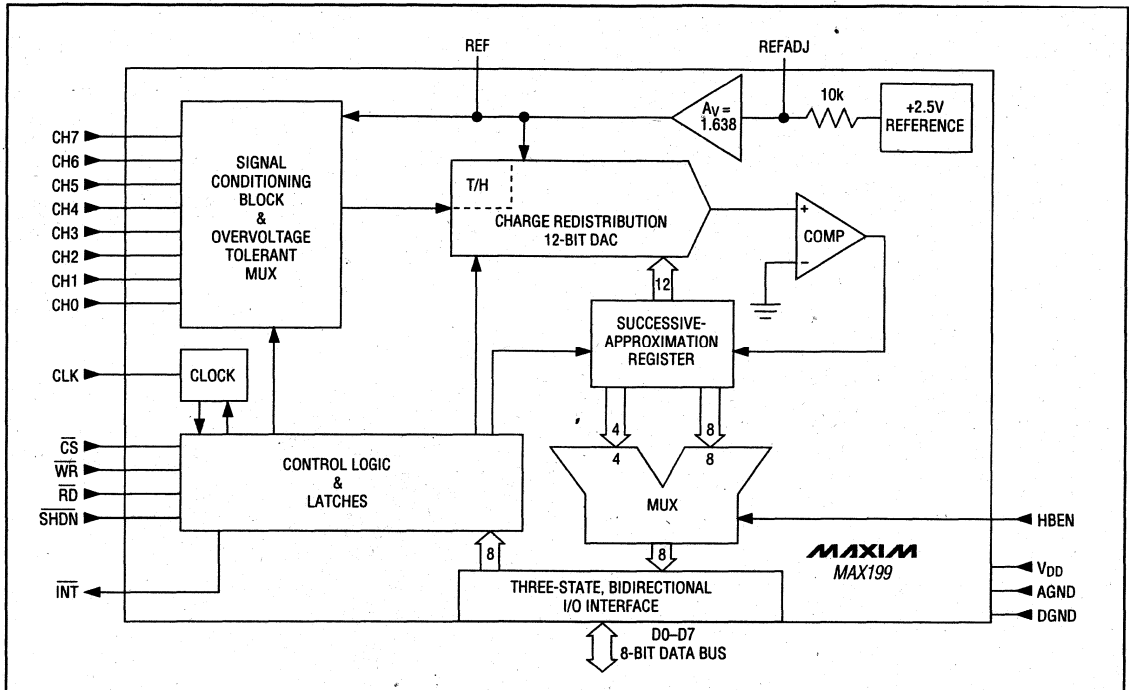


Figure 12. Power-Supply Grounding Connection

Multi-Range ($\pm 4V$, $\pm 2V$, $+4V$, $+2V$), +5V Supply, 12-Bit DAS with 8+4 Bus Interface

Functional Diagram





Video/High-Speed Amplifiers

Video/High-Speed Amplifiers, Product Tables and Trees	8-2
MAX4005 950MHz FET-Input Buffer w/ 75 Ω Output.....	8-5
MAX4100 600MHz High-Speed, Low-Power Op Amp*	8-9
MAX4101 750MHz High-Speed, Low-Power Op Amp*	8-9
MAX4102 300MHz High-Speed, Low-Power Video Op Amp*	8-11
MAX4103 450MHz High-Speed, Low-Power Video Op Amp*	8-11
MAX4104 750MHz Ultra-High-Speed, Low-Noise Op Amp*	8-13
MAX4105 750MHz Ultra-High-Speed, Low-Noise Op Amp*	8-13
MAX4106 550MHz High-Speed, Ultra-Low-Noise Op Amp*	8-15
MAX4107 500MHz High-Speed, Ultra-Low-Noise Op Amp*	8-15
MAX4108 550MHz High-Speed, Low-Distortion Op Amp*	8-17
MAX4109 500MHz High-Speed, Low-Distortion Op Amp*	8-17
MAX4111 330MHz Buffered Video Switch/Crosspoint Building Block	8-19
MAX4112 500MHz High-Speed, Current-Mode Feedback Op Amp*	8-31
MAX4113 375MHz High-Speed, Current-Mode Feedback Op Amp*	8-31
MAX4121 330MHz Buffered Video Switch/Crosspoint Building Block	8-19
MAX4141 330MHz Buffered Video Switch/Crosspoint Building Block	8-33
MAX4177 380MHz, Gain of +1, High-Speed Buffer*	8-41
MAX4221 330MHz Buffered Video Switch/Crosspoint Building Block	8-19
MAX4277 350MHz, Gain of +2, High-Speed Buffer*	8-41
MAX476 325MHz High-Speed Op Amp*	8-43
MAX496 430MHz Quad Video Buffer*	8-45
MAX497 375MHz Quad Video Buffer*	8-45
MAX498 Two-Channel, Quad RGB Video Switch w/ Gain of +2 Buffers*	8-47
MAX499 Two-Channel, Triple RGB Video Switch w/ Gain of +2 Buffers*	8-47

*Advance Information—first page of data sheet in preparation.

VIDEO & HIGH-SPEED AMPLIFIERS

BUFFERS	CROSSPOINT SWITCHES	MULTIPLEXERS	AMPLIFIERS	CRT DRIVER
★ MAX4005 (950MHz, JFET)	★ ☆ MAX4111 (330MHz 1x1)	★ ☆ MAX4111 (330MHz 1x1)	MAX404 (80MHz, AV ≥ 2V/V)	★ MAX445 (200MHz, 2.5ns t _{r/f} , high-voltage output)
MAX405 (160MHz, 0.998V/V gain)	★ ☆ MAX4121 (330MHz 2x1)	★ ☆ MAX4121 (330MHz 2x1)	MAX408 (100MHz, AV ≥ 3V/V)	
† MAX4177 (430MHz, AV = +1)	★ ☆ MAX4221 (330MHz dual 2x1)	★ ☆ MAX4221 (330MHz dual 2x1)	† MAX4100 (600MHz, low power)	
† MAX4277 (390MHz, AV = +2)	★ ☆ MAX4141 (330MHz 4x1)	★ ☆ MAX4141 (330MHz 4x1)	† MAX4101 (750MHz, AV ≥ 2V/V)	
MAX460 (140MHz, JFET input)	MAX456 (8x8)	MAX440 (160MHz, 8-ch mux + output amp)	† MAX4102 (325MHz, lowest DP/DG)	
MAX467 (100MHz, triple buffer)	★ MAX458 (100MHz 8x4, output drivers)	MAX441 (160MHz, 4-ch mux + output amp)	† MAX4103 (450MHz, AV ≥ 2V/V)	
MAX468 (100MHz, quad buffer)	★ MAX459 (90MHz 8x4, AV = +2 output drivers)	MAX442 (160MHz, 2-ch mux + output amp)	† MAX4104 (800MHz, 2nV/√Hz)	
MAX469 (90MHz, AV = +2, triple buffer)	† ☆ MAX499 (310MHz, AV = +2, output drivers)		† MAX4105 (800MHz, AV ≥ 2V/V)	
MAX470 (90MHz, AV = +2, quad buffer)		MAX453 (50MHz, 2-ch mux + output amp)	† MAX4106 (550MHz, 0.65nV/√Hz)	
† MAX496 (430MHz, AV = +1, quad buffer)		MAX454 (50MHz, 4-ch mux + output amp)	† MAX4107 (500MHz, AV ≥ 10V/V)	
† MAX497 (390MHz, AV = +2, quad buffer)		MAX455 (50MHz, 8-ch mux + output amp)	† MAX4108 (550MHz, 1300V/μs)	
			† MAX4109 (500MHz, AV ≥ 2V/V)	MAX452 (50MHz)
			† MAX4112 (500MHz, 1500V/μs)	MAX453 (50MHz, 2-ch mux + amp)
			† MAX4113 (375MHz, AV ≥ 10V/V)	MAX454 (50MHz, 4-ch mux + amp)
			MAX428 (dual MAX408)	MAX455 (50MHz, 8-ch mux + amp)
			MAX435 (275MHz, diff in/diff out)	MAX457 (70MHz dual)
			MAX436 (200MHz, diff in/single out)	† MAX476 (350MHz, 1800V/μs)
			MAX448 (quad MAX408)	

★ New product

† Future product

☆ Evaluation kit available

Video/High-Speed Amplifiers

Part Number	Unity GBW (MHz)	Slew Rate (V/μs)	DP/DG (degrees/°)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Channel (mA)	Features	Price† 1000-up (\$)
VIDEO AMPLIFIERS								
MAX404	80 (A _v ≥2)	500	0.01/0.05	50	±5	30	Broadcast-quality video op amp, 0.01°/0.05% diff phase/gain, symmetrical inputs, 70dB CMRR, 66dB A _{vol}	2.68
MAX408/428/448	100 (A _v ≥3)	90	N/A	50/op amp	±5	7	Single/dual/quad op amp, high-output drive	3.02/4.06/6.74
MAX435/436	275	800	N/A	10	±5	35	Ultra high-speed differential input/output transconductance amp, no feedback required	2.75
MAX445	200	2.5ms t _{rlt}	N/A	140	±10V, +75V	70 (V+)	CKT video display driver for ultra-high resolution monitors, single IC pre-amp and high-voltage (+75V) output stage	6.83
MAX452	50	300	0.2/0.5	14	±5	25	Unity-gain stable, drives 75Ω coax cable	2.40
MAX457	70	300	0.2/0.5	15	±5	35	Dual, unity-gain stable, drives 75Ω coax cable	4.45
MAX476	350	1800	0.01/0.01	100	±5	8	400μA shutdown, 0/01°/0.01% diff phase/gain error	††
MAX4100/MAX4101	600/	250/300	0.02/0.05	70	±5	5	Low power, voltage feedback, 65dB open-loop gain, 2mV V _{os}	††
MAX4102/MAX4103	750 (A _v ≥2V/V)	300/375	0.008/0.008	70	±5	5	Lowest diff phase/gain error	††
MAX4104/MAX4105	800/	250/450	0.01/0.01	70	±5	15	2nV/√Hz, low noise, low distortion	††
MAX4106/MAX4107	800 (A _v ≥2V/V)	325/700	0.01/0.01	70	±5	16	0.65nV/√Hz, ultra-low noise, low distortion	††
MAX4108/MAX4109	550/	1300/1500	0.01/0.01	70	±5	20	85dB SFDR (at 20MHz), ultra-low distortion	††
MAX4112/MAX4113	500/	1500/1800	0.02/0.02	70	±5	5	Current-mode feedback, low power	††

Part Number	Unity GBW (MHz)	Slew Rate (V/μs)	DP/DG (degrees/°)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Channel (mA)	Features	Price† 1000-up (\$)
MAX4005	950	1000	N/A	75Ω output	±5	25	FET input buffer with 75Ω output to minimize reflections, 0.03°/0.11% diff phase/gain, 60MHz gain flatness (0.1dB), 28dBm IP ₃ (100MHz)	2.75
MAX405	180	650	0.01/0.03	60	±5	35	Broadcast quality, 0.99V gain guaranteed over temp, 0.01°/0.03% diff phase/gain error	4.25
MAX4177	430	1800	0.01/0.01	100	±5	8	Gain of +1 buffer, 180MHz gain flatness to 0.1dB, 400μA shutdown/high-Z state, 0.01°/0.01% diff phase/gain error	††
MAX4277	390	1500	0.01/0.01	100	±5	8	Gain of +2 buffer, 150MHz gain flatness to 0.1dB, 400μA shutdown/high-Z state, 0.01°/0.01% diff phase/gain error	††
MAX460	140	1500	N/A	100	±15	19	FET input, EL2005/LH0033 upgrade	19.78
MAX467	100	200	0.03/0.01	20	±5	50	Triple (RGB) video buffer, 0.03°/0.01% diff phase/gain error	3.70
MAX468	100	200	0.03/0.01	20	±5	65	Quad, unity-gain video buffer, 0.03°/0.01% diff phase/gain error	4.20
MAX469	90	300	0.14/0.12	20	±5	50	Triple (RGB), gain of +2 video buffer, 0.03°/0.01% diff phase/gain error	3.70
MAX470	90	300	0.14/0.12	20	±5	65	Quad, gain of +2 (6dB) video buffer, 0.03°/0.01% diff phase/gain error	4.20
MAX496	430	2800	0.01/0.01	100	±5	7.5	Quad gain of +1 (0dB) closed-loop buffer, 0.01°/0.01% diff phase/gain error	††
MAX497	390	2400	0.01/0.01	100	±5	7.5	Quad gain of +2 (6dB) closed-loop buffer, 0.01°/0.01% diff phase/gain error	††

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
 †† Future product—contact factory for pricing and availability. Specifications are preliminary.

Video/High-Speed Amplifiers (continued)

Part Number	Unity GBW (MHz)	Slew Rate (V/ μ s)	DP/DG (degrees/ μ s)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Channel (mA)	Features	Price [†] 1000-up (\$)
VIDEO MULTIPLEXERS/AMPLIFIERS								
MAX4111	330	700	0.01/0.01	500 μ A	$\pm$ 5	5	1x1 video crosspoint building block, 0.1dB gain flatness of 150MHz, 0.01°/0.01% diff phase/gain error	1.70
MAX4121	330	700	0.01/0.01	500 μ A	$\pm$ 5	5	2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz, 0.01°/0.01% diff phase/gain error	2.10
MAX4221	330	700	0.01/0.01	500 μ A	$\pm$ 5	5	Dual 2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz, 0.01°/0.01% diff phase/gain error	4.50
MAX4141	330	700	0.01/0.01	500 μ A	$\pm$ 5	5	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz, 0.01°/0.01% diff phase/gain error	4.50
MAX440	160 (A _V ≥2)	370	0.03/0.04	35	$\pm$ 5	40	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain error, 15ns switch time, high-Z output state	8.95
MAX441	160	370	0.03/0.04	35	$\pm$ 5	40	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain error, 15ns switch time	5.90
MAX442	140	250	0.03/0.04	35	$\pm$ 5	40	Video amp with 2-channel mux, 15ns switch time, 8-pin DIP/SO	4.45
MAX453	50	300	1.2/0.5	14	$\pm$ 5	25	Video amp with 2-channel video mux	3.94
MAX454	50	300	1.2/0.5	14	$\pm$ 5	25	Video amp with 4-channel video mux	5.25
MAX455	50	300	1.2/0.5	14	$\pm$ 5	25	Video amp with 8-channel video mux	8.75
RGB VIDEO SWITCHES								
Part Number	Unity GBW (MHz)	Slew Rate (V/ μ s)	Switching Time (ns)	Number of Inputs	Number of Outputs	Buffer Amp Gain (V/V)	Output Current (mA)	Price [†] 1000-up (\$)
MAX463/465	100	300	20	6 (RGBA, RGBB)	3 (RGB)	+1/+2	20	6.97
MAX464/466	100	300	20	8 (RGBA + Sync, RGBB + Sync)	4 (RGB + Sync)	+1/+2	20	7.97
MAX498	310	1500	3	8 (RGBA + Sync, RGBB + Sync)	4	+2	40	††
MAX499	310	1500	3	6 (RGBA + RGBB)	3	+2	40	††
VIDEO CROSSPOINT SWITCHES								
Part Number	Unity GBW (MHz)	Slew Rate (V/ μ s)	DP/DG (degrees/ μ s)	Off Isolation (dB typ)	Crosstalk (dB typ)	EV Kit	Features	Price [†] 1000-up (\$)
MAX4111	330	700	0.01/0.01	74 (30MHz)	N/A	Yes	1x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	1.70
MAX4121	330	700	0.01/0.01	74 (30MHz)	66	Yes	2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.10
MAX4221	330	700	0.01/0.01	74 (30MHz)	66	Yes	Dual 2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50
MAX4141	330	700	0.01/0.01	74 (30MHz)	66	Yes	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50
MAX456	35	250	1/0.5	80 (5MHz)	70 (5MHz)	Yes	8x8 crosspoint switch array with eight output buffers, high-Z output capability	19.98
MAX458/459	100/90	300	0.05/0.01	60 (10MHz)	55 (10MHz)	Yes	8x4 crosspoint switch array with four 75 Ω cable drivers, high-Z output capability	21.85

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.



950MHz FET-Input Buffer with 75Ω Output

General Description

The MAX4005 is a $\pm 5\text{V}$, single-ended unity-gain buffer with a high-impedance JFET input, intended to drive a 75Ω load. A 75Ω thin-film output resistor is included on-board to minimize reflections when driving a 75Ω load through a transmission line of arbitrary length. Gain in this configuration is 0.5.

Features

- ◆ 950MHz Bandwidth
- ◆ 350ps Rise/Fall Times
- ◆ 0.11%/0.03° Differential Gain/Phase Error
- ◆ 1000V/ μs Slew Rate
- ◆ 10pA Input Bias Current
- ◆ 75Ω Output Impedance

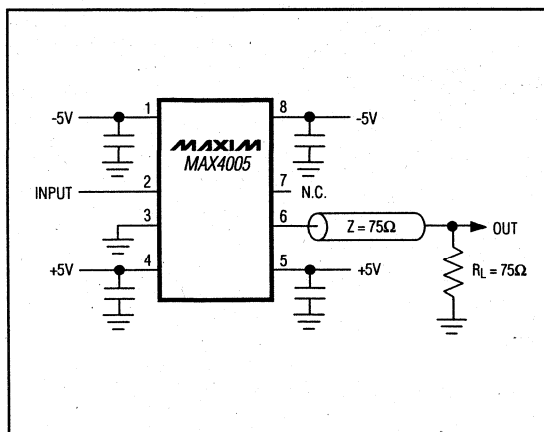
Applications

Video Buffer / Line Driver
Isolation Between High-Impedance Node
and Low-Impedance Instrument
Remote Signal Sensing
Impedance Transformation
Fanout Multiplier for 75Ω Distribution Systems

Ordering Information

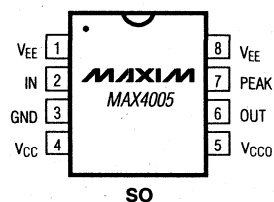
PART	TEMP. RANGE	PIN-PACKAGE
MAX4005CSA	0°C to +70°C	8 SO

Typical Operating Circuit



Pin Configuration

TOP VIEW



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Maxim Integrated Products 8-5

Call toll free 1-800-998-8800 for free samples or literature.

950MHz FET-Input Buffer with 75Ω Output

ABSOLUTE MAXIMUM RATINGS

Input Voltage.....	±2.5V	Ground Voltage.....	0.0V
VCC Supply Voltage.....	+5.5V	Continuous Power Dissipation (T _A = +70°C).....	471mW
Output-Stage Supply.....	+5.5V	Operating Temperature Range.....	0°C to +70°C
VEE Supply Voltage.....	-5.5V	Lead Temperature (soldering, 10sec).....	+300°C
Peaking Pad Voltage.....	0.0V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = 4.75V to 5.25V, VEE = -4.75V to -5.25V, T_A = +25°C, stated performance characterized for T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+5V VCC Current	I _{VCC1}	V _{IN} = 0V, R _L = 75Ω	9	14	19	mA
+5V Output Stage Quiescent Current	I _{VCC2}	V _{IN} = 0V, R _L = 75Ω	9	11	14	mA
-5V VEE Current	I _{VEE}	V _{IN} = 0V, R _L = 75Ω	17	24	31	mA
Output Offset Voltage		R _L = 75Ω, gain = 0.5	-3		3	mV
Output Resistance	R _{OUT}		74.0	75.0	76.5	Ω
Input Current	I _B	V _{IN} = 0V	-1	0.01	1	nA
Gain		R _L = 75Ω	0.49	0.50	0.51	
Linearity		R _L = 75Ω, measured over input dynamic range		0.50	1	%
Input Dynamic Range		R _L = 75Ω, gain = 0.5	-1.3		1.6	V
+5V VCC Power-Supply Rejection Ratio		V _{IN} = 0V, R _L = 75Ω	40	55		dB
+5V Output Stage Power-Supply Rejection Ratio		V _{IN} = 0V, R _L = 75Ω	50	75		dB
-5V VEE Power-Supply Rejection Ratio		V _{IN} = 0V, R _L = 75Ω	40	60		dB

TYPICAL OPERATING PERFORMANCE (VCC = 5.0V, VEE = -5.0V, R_L = 75Ω, T_A = +25°C, unless otherwise noted.)

Bandwidth	BW	-3dB	950	MHz
		-6dB	2000	
Input Capacitance	C _{IN}		2.2	pF
Settling Time to 0.1%	t _{SET}	V _{IN} = 0.25V step, V _{OUT} = 0.125V step	2	ns
Rise/Fall Times	t _{RISE} /t _{FALL}	V _{IN} = 0.25V step with < 30ps rise time	350	ps
Gain Flatness	GF	At 30MHz	±0.01	dB
Gain Flatness ±0.1dB	GF1		60	MHz
Gain Flatness ±0.2dB	GF2		80	MHz
Slew Rate	SR	V _{IN} = 2.5V step with 200ps rise time	1000	V/μs
Overdrive Recovery Time	t _{OD}	V _{IN} = 2.5V step	5	ns
2nd Harmonic Distortion	2HD	At 50MHz	-50	dBc
3rd Harmonic Distortion	3HD	At 50MHz	< -60	dBc
3rd-Order Intercept	TOI	At 100MHz	28	dBm
Differential Gain Error	DG	At 3.58MHz	0.11	%
Differential Phase Error	DP	At 3.58MHz	0.03	degrees

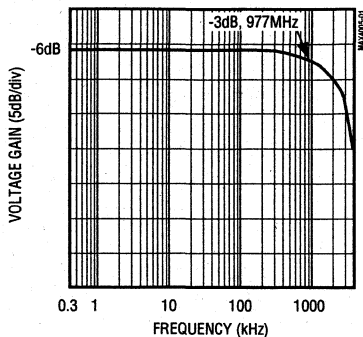
950MHz FET-Input Buffer with 75Ω Output

Typical Operating Characteristics

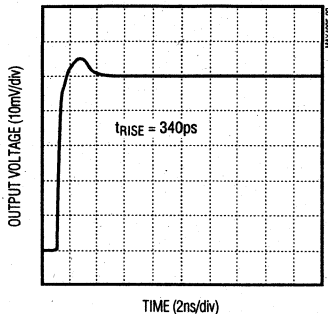
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX4005

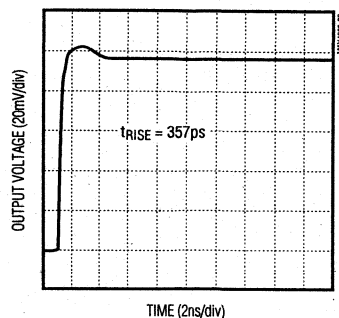
GAIN vs. FREQUENCY



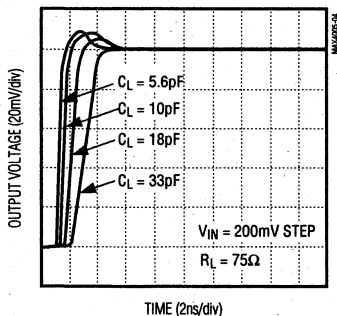
SMALL-SIGNAL STEP RESPONSE



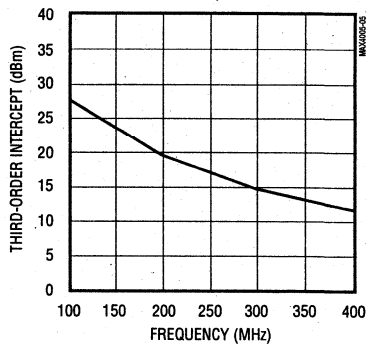
SMALL-SIGNAL STEP RESPONSE



**SMALL-SIGNAL STEP RESPONSE
vs. CAPACITIVE LOAD**



**THIRD-ORDER INTERCEPT
vs. FREQUENCY**



950MHz FET-Input Buffer with 75Ω Output

Pin Description

PIN	NAME	FUNCTION
1, 8	VEE	-5V Negative Supplies
2	IN	High-Impedance Input
3	GND	Ground
4	VCC	+5V Positive Supply
5	VCCO	Output Stage +5V Positive Supply
6	OUT	Output ($Z_{OUT} = 75\Omega$)
7	PEAK	Normally no connection. Capacitor to ground will peak frequency response.

Applications Information

Power Supply

The MAX4005 allows for two separate +5V supplies for the output stage and the rest of the MAX4005 circuit. The supplies are bonded out separately to give the option of using a different +5V supply. The output stage is a Class A type, with the output transistor fed by a current source in the emitter, so its current will vary with output signal. For best bandwidth and pulse response, solder bypass chip capacitors directly from the supply pins on the four corners of the package to a ground plane.

Input Impedance

The MAX4005 has a JFET input with an input capacitance of only 2pF. As a result, the leakage current is typically less than 10pA. This exceptionally high input impedance is important in applications that require isolation between a high source impedance and a low-impedance transmission cable. An attenuator may be used in front of the MAX4005 to increase the dynamic range and reduce input capacitance.

Output Impedance

A 75Ω precision thin-film output resistor is included on-board to provide more precise reverse termination than standard discrete resistors. This minimizes reflections caused by impedance mismatching when driving transmission cable. The MAX4005 can also drive a 50Ω load with only a slight loss in amplitude (gain drops from 0.5 to 0.4). The typical operating performance specifications shown in the *Electrical Characteristics* have been verified with a 50Ω load, as well as a 75Ω load.

Frequency Response Peaking

To peak the response to compensate for losses when driving long transmission lines, connect a chip capacitor of about 10pF to 50pF between the PEAK pin and ground. This peaking occurs in the 200MHz to 500MHz range. The PEAK pin will normally be left open for flat-test response.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

600MHz, High-Speed, Low-Power Op Amps

General Description

The MAX4100/MAX4101 op amps combine ultra-high-speed performance with low-power operation. The MAX4100 is compensated for unity-gain stability, while the MAX4101 is compensated for stability in applications with a closed-loop gain (A_{VCL}) of 2V/V or greater.

The MAX4100/MAX4101 require only 5mA of supply current while delivering a 600MHz unity-gain bandwidth with a 250V/ μ s slew rate (MAX4100) or a 750MHz gain bandwidth with a 300V/ μ s slew rate (MAX4101).

These high-speed op amps have a wide output voltage swing of $\pm 3.5V$ and a high current-drive capability of 70mA.

Applications

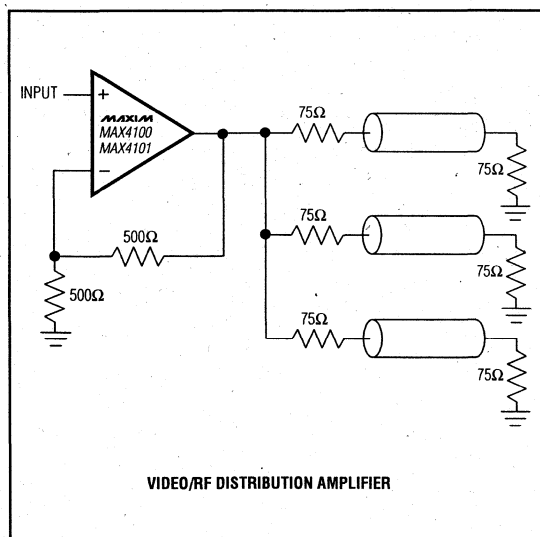
Video Cable Driver
Ultrasound
Gamma Cameras
Portable Instruments
Active Filters
ADC Buffers

Features

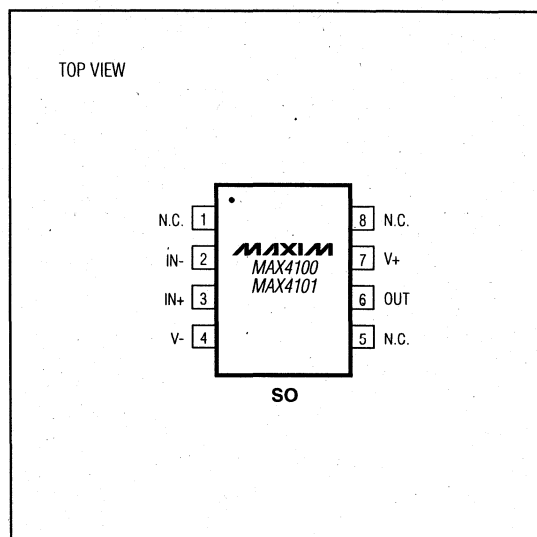
- ♦ 600MHz Unity-Gain Bandwidth (MAX4100)
750MHz Gain-Bandwidth ($A_{VCL} = 2V/V$, MAX4101)
- ♦ 250V/ μ s Slew Rate (MAX4100)
300V/ μ s Slew Rate (MAX4101)
- ♦ 0.05%/0.02° Differential Gain/Phase
- ♦ High Output Drive: 70mA
- ♦ Low Power: 5mA Supply Current

MAX4100/MAX4101

Typical Application Circuit



Pin Configuration



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MAXIM

Maxim Integrated Products 8-9

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

300MHz, High-Speed, Low-Power Video Op Amps

MAX4102/MAX4103

General Description

The MAX4102/MAX4103 op amps combine ultra-high-speed performance and ultra-low differential gain and phase with low-power operation. The MAX4102 is compensated for unity-gain stability, while the MAX4103 is compensated for stability in applications with a closed-loop gain (A_{VCL}) of 2V/V or greater.

The MAX4102/MAX4103 require only 5mA of supply current while delivering a 300MHz unity-gain bandwidth (MAX4102) or a 450MHz gain bandwidth (MAX4103). Differential gain and phase are an ultra-low 0.008%/0.008° ($R_L = 150\Omega$), making these amplifiers ideal for composite video applications.

These high-speed op amps have a wide output voltage swing of $\pm 3.3V$ and high current-drive capability of 70mA.

Applications

Broadcast and High-Definition TV Systems

Pulse/RF Amplifier

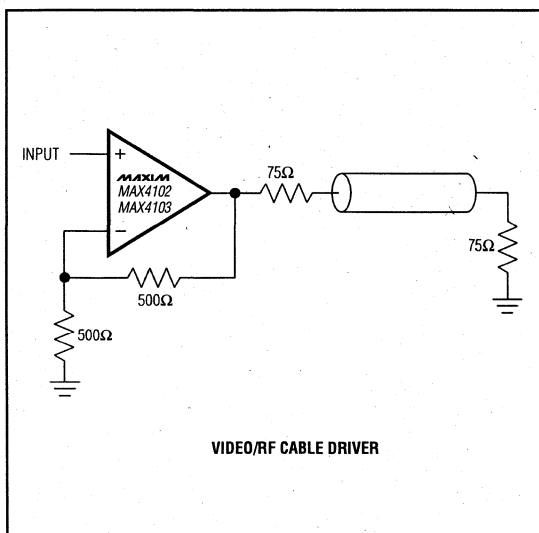
Ultrasound

ADC/DAC Amplifier

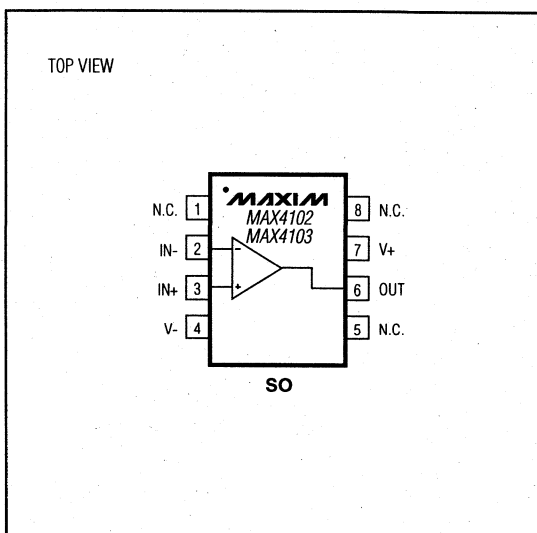
Features

- ♦ 300MHz Unity-Gain Bandwidth (MAX4102)
450MHz Gain Bandwidth ($A_{VCL} = 2V/V$, MAX4103)
- ♦ 300V/ μs Slew Rate (MAX4102)
375V/ μs Slew Rate (MAX4103)
- ♦ 0.008%/0.008° Differential Gain/Phase
- ♦ 115dB Open-Loop Gain
- ♦ High Output Drive: 70mA
- ♦ Low Power: 5mA Supply Current

Typical Application Circuit



Pin Configuration



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MAXIM

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Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

750MHz, Ultra-High-Speed, Low-Noise Op Amps

MAXIM

MAX4104/MAX4105

General Description

The MAX4104/MAX4105 op amps combine ultra-high-speed performance with moderate power operation. The MAX4104 is compensated for unity-gain stability, while the MAX4105 is compensated for stability in applications with a closed-loop gain (A_{VCL}) of 2V/V or greater.

The MAX4104/MAX4105 require only 15mA of supply current while delivering a 750MHz unity-gain bandwidth with a 250V/ μ s slew rate (MAX4104), or a 750MHz gain bandwidth with a 450V/ μ s slew rate (MAX4105). Voltage noise is a low 2nV/ $\sqrt{\text{Hz}}$, making these amplifiers ideal for low-noise video and telecommunications applications.

These high-speed op amps have a wide output voltage swing of $\pm 3.3\text{V}$ and a high current-drive capability of 70mA.

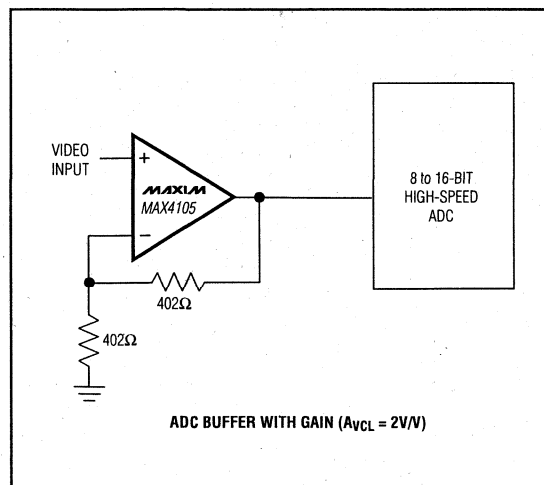
Applications

Video ADC Preamp
Pulse/RF Telecom Applications
Video Buffers and Cable Drivers
Ultrasound
Active Filters
ADC Buffers

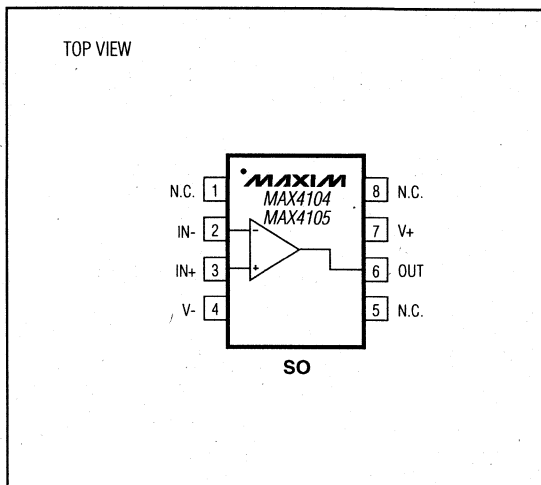
Features

- ♦ 750MHz Unity-Gain Bandwidth (MAX4104)
750MHz Gain Bandwidth ($A_{VCL} = 2\text{V/V}$, MAX4105)
- ♦ 250V/ μ s Slew Rate (MAX4104)
450V/ μ s Slew Rate (MAX4105)
- ♦ 2nV/ $\sqrt{\text{Hz}}$ Voltage Noise
- ♦ High Output Drive: 70mA

Typical Application Circuit



Pin Configuration



8

MAXIM

Maxim Integrated Products 8-13

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

550MHz, High-Speed, Ultra-Low-Noise Op Amps

MAX4106/MAX4107

General Description

The MAX4106/MAX4107 op amps combine high-speed performance with ultra-low-noise performance. The MAX4106 is compensated for closed-loop gains (A_{VCL}) of 5V/V, while the MAX4107 is stable in closed-loop gains of 10V/V or greater.

The MAX4106/MAX4107 require only 15mA of supply current while delivering bandwidths of 550MHz and 500MHz respectively. Voltage noise is an ultra-low 0.65nV/ $\sqrt{\text{Hz}}$, while a low-distortion architecture provides a spurious-free dynamic range (SFDR) of 85dB at 5MHz.

These high-speed op amps have a wide output voltage swing of $\pm 3.3\text{V}$ and a high current-drive capability of 70mA.

Applications

Ultra-Low-Noise ADC Preamp

Ultrasound

Low-Noise Preamplifier

High-Performance Receivers

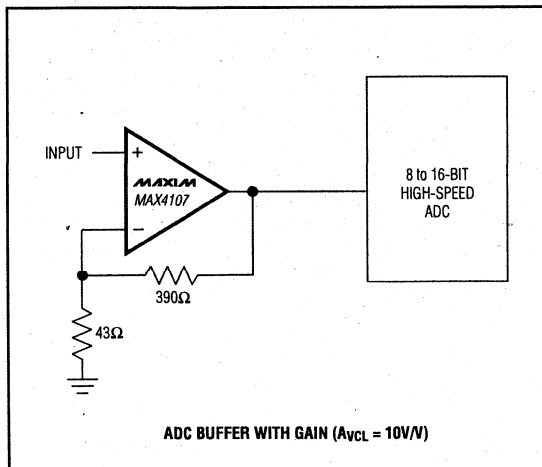
Active Filters

Pulse/RF Amplifier

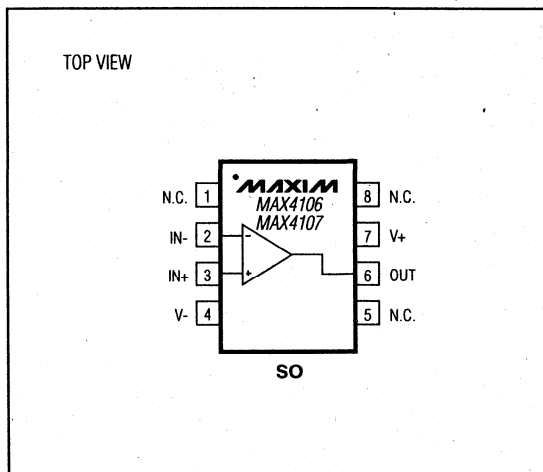
Features

- ◆ 550MHz Gain Bandwidth ($A_{VCL} = 5\text{V/V}$, MAX4106)
500MHz Gain Bandwidth ($A_{VCL} = 10\text{V/V}$, MAX4107)
- ◆ 325V/ μs Slew Rate (MAX4106)
700V/ μs Slew Rate (MAX4107)
- ◆ 0.65nV/ $\sqrt{\text{Hz}}$ Voltage Noise
- ◆ 85dB SFDR at $f_o = 5\text{MHz}$ ($R_L = 100\Omega$, $V_{OUT} = 2\text{Vp-p}$)
- ◆ High Output Drive: 70mA

Typical Application Circuit



Pin Configuration



8

MAXIM

Maxim Integrated Products 8-15

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

550MHz, High-Speed, Low-Distortion Op Amps

General Description

The MAX4108/MAX4109 op amps combine ultra-high-speed performance with low-distortion operation. The MAX4108 is compensated for unity-gain stability, while the MAX4109 is compensated for a closed-loop gain (A_{VCL}) of 2V/V or greater.

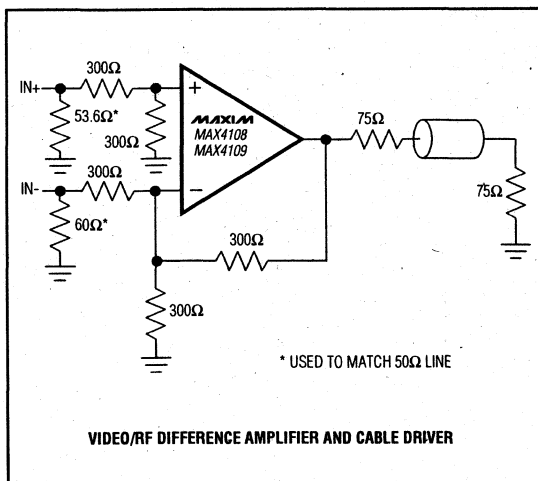
The MAX4108 delivers a 550MHz unity-gain bandwidth with a 1300V/ μ s slew rate, while the MAX4109 provides a 500MHz gain bandwidth with a 1500V/ μ s slew rate. The low-distortion design provides an unprecedented spurious-free dynamic range of 85dB and 80dB, respectively, at 20MHz ($V_O = 2V_{p-p}$, $R_L = 100\Omega$), making these amplifiers ideal for high-performance RF signal processing.

These high-speed op amps have a wide output voltage swing of $\pm 3.0V$ and a high current-drive capability of 70mA.

Applications

RGB and Composite Video
High-Performance Receivers
Pulse/RF Amplifier
ADC/DAC Preamp
Active Filters

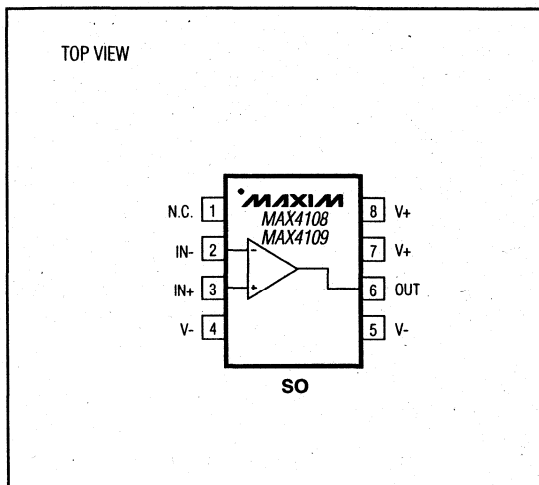
Typical Application Circuit



Features

- ◆ 550MHz Unity-Gain Bandwidth (MAX4108)
500MHz Gain Bandwidth ($A_{VCL} = 2V/V$, MAX4109)
- ◆ 1300V/ μ s Slew Rate (MAX4108)
1500V/ μ s Slew Rate (MAX4109)
- ◆ 85dB SFDR at $f_o = 20\text{MHz}$ (MAX4108)
80dB SFDR at $f_o = 20\text{MHz}$ (MAX4109)
- ◆ 200MHz Full-Power Bandwidth ($V_O = 2V_{p-p}$, MAX4108)
225MHz Full-Power Bandwidth ($V_O = 2V_{p-p}$, MAX4109)
- ◆ High Output Drive: 70mA

Pin Configuration



MAX4108/MAX4109

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MAXIM

Maxim Integrated Products 8-17

Call toll free 1-800-998-8800 for free samples or literature.

EVALUATION KIT
AVAILABLE**MAXIM**

330MHz Buffered Video Switches/ Crosspoint Building Blocks

General Description

The MAX4111/MAX4121/MAX4221 wideband video switches are optimized for high-definition, broadcast-quality, composite (HDTV, NTSC, PAL, SECAM, and RGB) video switching arrays. Their open-loop buffer amplifiers offer 0.1dB gain flatness to 150MHz. They operate from $\pm 5V$ supplies and feature differential phase and gain error of only 0.01°/0.01%, respectively. The ultra-low switching glitch (13mV) is positive to avoid confusion with any sync pulse.

Ideal as building blocks in large arrays, these devices feature a constant, high input impedance and a disable function that puts the outputs into a high-impedance state and reduces the operating current to only 250 μ A. The open-loop architecture allows the outputs to drive capacitive loads without oscillation. Other key features include -92dB crosstalk and -78dB isolation (MAX4121).

The MAX4111/MAX4121/MAX4221 are offered in narrow plastic DIP and SO packages. See the table below for key features:

PART	DESCRIPTION	PINS
MAX4111	SPST, single-input, single-output switch	8
MAX4121	SPDT, 2-input, single-output switch	8
MAX4221	Dual, SPDT, 2-input, single-output switch	16

Applications

Video-Router and Crosspoint Arrays
Broadcast/HDTV-Quality Color Signal Multiplexing
RF and IF Routing
Graphics Color-Signal Routing
Telecom Routing
Data Acquisition

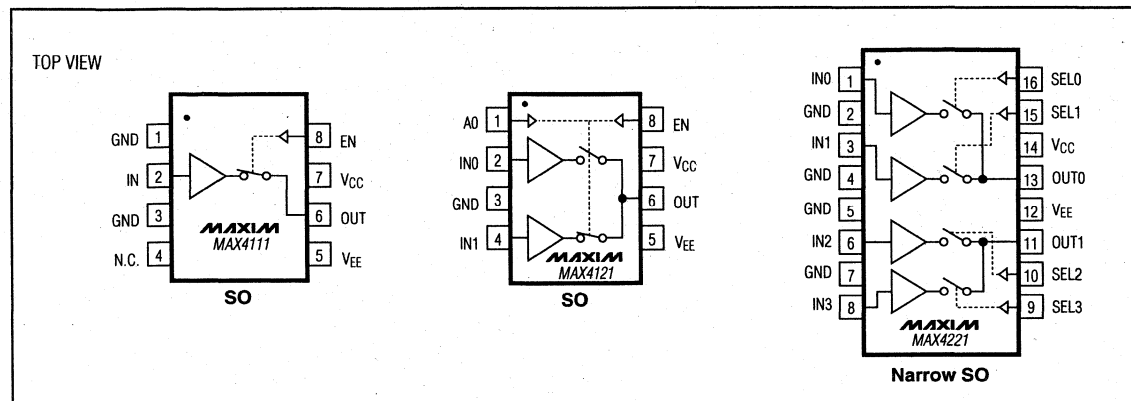
Features

- ◆ -3dB Bandwidth of 330MHz
- ◆ 0.1dB Gain Flatness of 150MHz
- ◆ 700V/ μ s Slew Rate
- ◆ 0.01°/0.01% Differential Phase/Gain
- ◆ Low Power: 5.5mA Max
- ◆ -92dB Crosstalk and -78dB Off Isolation at 30MHz
- ◆ High-Z Outputs when Disabled
- ◆ 3pF Input Capacitance
- ◆ Ultra-Low Switching Glitch
- ◆ On-Board Control Logic

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4111CSA	0°C to +70°C	8 SO
MAX4121CSA	0°C to +70°C	8 SO
MAX4221CSE	0°C to +70°C	16 Narrow SO

Pin Configurations/Functional Diagrams

**MAXIM**

Maxim Integrated Products 8-19

Call toll free 1-800-998-8800 for free samples or literature.

MAX4111/MAX4121/MAX4221

8

330MHz Buffered Video Switches/ Crosspoint Building Blocks

ABSOLUTE MAXIMUM RATINGS

Supply Voltages

VCC	+6V
VEE	-6V
VCC-VEE	+12V
Analog Input Voltage	(VEE - 0.3V) to (VCC + 0.3V)
Digital Input Voltage	-0.3V to (VCC + 0.3V)
Duration of Short Circuit to Ground	Continuous

Continuous Power Dissipation (T_A = +70°C)

8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)	696mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +160°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±5V, -2.5V ≤ V_{IN} ≤ +2.5V, R_L = 5kΩ, C_L ≤ 5pF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PARAMETERS							
Operating Supply Voltage	V _S			±4.5	±5.0	±5.5	V
Operating Supply Current	I _{CC} , I _{EE}	Per channel	T _A = +25°C	4.0		5.5	mA
			T _A = T _{MIN} to T _{MAX}	6.5			
Disabled Supply Current	I _{CC} , I _{EE}	MAX4111/MAX4121		150		200	μA
		MAX4221		250		350	
Input Voltage Range	V _{IN}			±2.5			V
Input Bias Current	I _B	V _{IN} = 0V	Channel selected	±2.5		±4.0	μA
			Channel disabled	±0.02			
Input Resistance	R _{IN}	Channel selected		0.4			MΩ
		Channel disabled		100			
Input Capacitance	C _{IN}	V _{IN} = 0V, channel enabled or disabled		3			pF
Output Offset Voltage	V _{OS}	T _A = +25°C		±5		±10	mV
		T _A = T _{MIN} to T _{MAX}				±15	
Power-Supply Rejection Ratio	PSRR	V _S = ±4.5V to ±5.5V		50			dB
Voltage Gain	A _V	V _{IN} = ±2.5V	T _A = +25°C	0.98		1.0	V/V
			T _A = T _{MIN} to T _{MAX}	0.97		1.0	
Output Resistance	R _{OUT}	f = DC to 50MHz		20			Ω
Disabled Output Current	I _{OUT} (OFF)	V _{OUT} = 0V		10			nA
Disabled Output Resistance	R _{OUT} (OFF)			30			MΩ
Disabled Output Capacitance	C _{OUT} (OFF)			5			pF
Logic Input High Voltage	V _{INH}	V _S = ±4.5V to ±5.5V		2.0			V
Logic Input Low Voltage	V _{INL}	V _S = ±4.5V to ±5.5V				0.8	V
Logic Input High Current	I _{INH}	V _S = ±4.5V to ±5.5V				10	μA
Logic Input Low Current	I _{INL}	V _S = ±4.5V to ±5.5V				10	μA

330MHz Buffered Video Switches/ Crosspoint Building Blocks

ELECTRICAL CHARACTERISTICS

($V_S = \pm 5V$, $-2.5V \leq V_{IN} \leq +2.5V$, $R_L = 5k\Omega$, $C_L \leq 5pF$, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC PARAMETERS							
Slew Rate	SR	V _{OUT} = 5Vp-p			700		V/μs
		V _{OUT} = 1.4Vp-p			500		
Full-Power Bandwidth (Note 1)	FPBW	V _{IN} = 1.4Vp-p			110		MHz
		V _{IN} = 5Vp-p			45		
-3dB Bandwidth	f _{3dB}	V _{IN} = 0.1Vp-p			330		MHz
Gain Flatness		DC to 30MHz			0.02		dB
		DC to 150MHz			0.1		
Gain Peaking					0.08		dB
Small-Signal Rise Time	t _r /t _f	V _{IN} = 0.1Vp-p			950		ps
Differential Gain (Note 2)	DG	f = 3.58MHz			0.01		%
Differential Phase (Note 2)	DP	f = 3.58MHz			0.01		degrees
All-Hostile Crosstalk		V _{IN} = 1Vp-p, f = 30MHz	MAX4121		-92		dB
			MAX4221		-70		
Off Isolation		V _{IN} = 1Vp-p, f = 30MHz, see test circuit	MAX4111		86		dB
			MAX4121		78		
			MAX4221		84		
Channel Switching Off Time	t _{OFF}				1.0		μs
Channel Switching On Time	t _{ON}				500		ns
Switching Transient					13		mVp-p
Group Delay					860		ps
Input-Output Delay Matching		Chip-to-chip, f = 3.58MHz			±0.2		degrees
Second Harmonic		f = 30MHz, V _{IN} = 1.4Vp-p			-65		dBc
Third Harmonic		f = 30MHz, V _{IN} = 1.4Vp-p			-70		dBc

Note 1: Full-Power Bandwidth is inferred from Slew Rate (SR) testing by the equation $SR = \omega E_p$, where E_p is the peak output voltage and $\omega = 2\pi f$.

Note 2: Differential Gain and Phase are tested using a modulated ramp, 100IRE (0.714V).

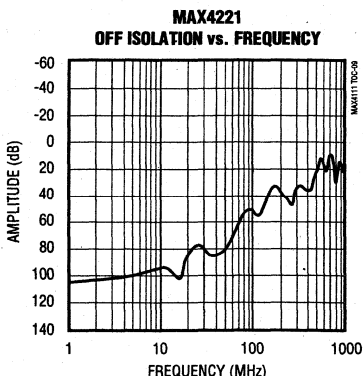
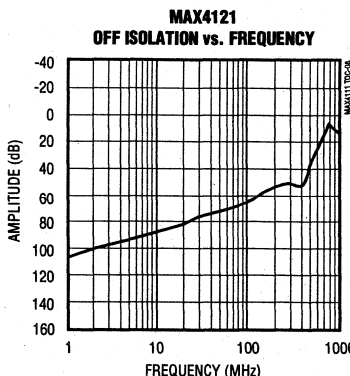
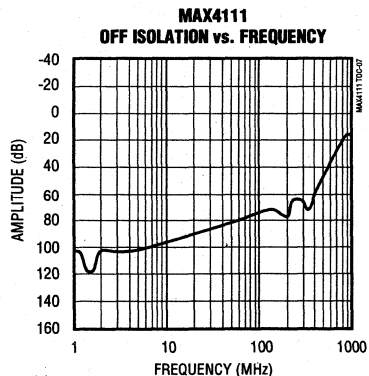
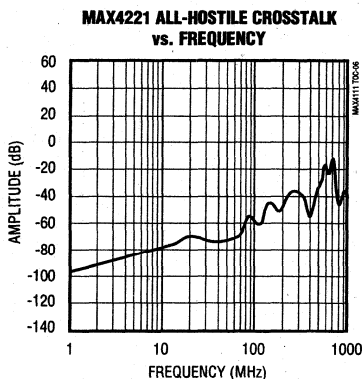
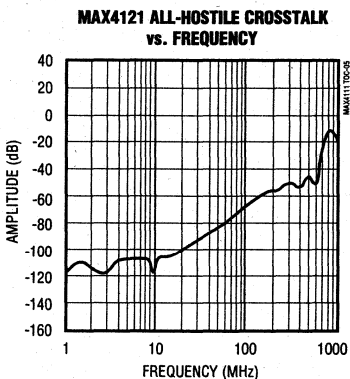
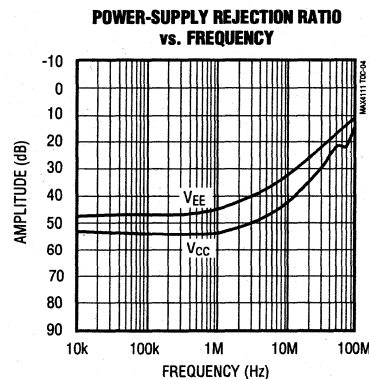
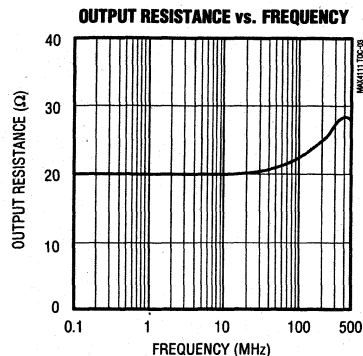
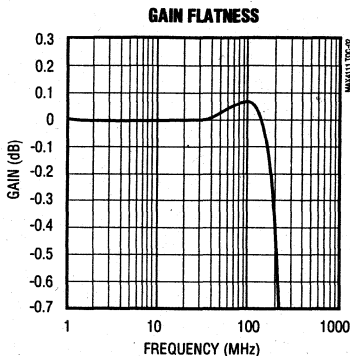
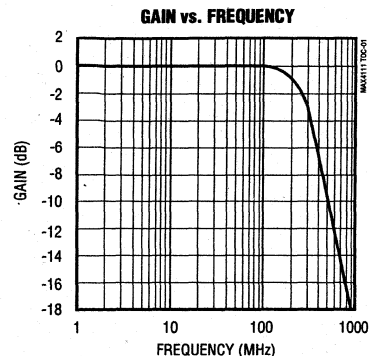
MAX4111/MAX4121/MAX4221

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330MHz Buffered Video Switches/ Crosspoint Building Blocks

Typical Operating Characteristics

($V_S = \pm 5V$, $R_L = 5k\Omega$, $C_L \leq 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)



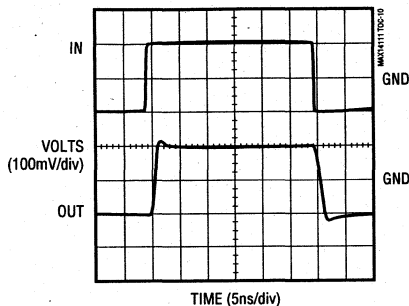
330MHz Buffered Video Switches/ Crosspoint Building Blocks

Typical Operating Characteristics (continued)

($V_S = \pm 5V$, $R_L = 5k\Omega$, $C_L \leq 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)

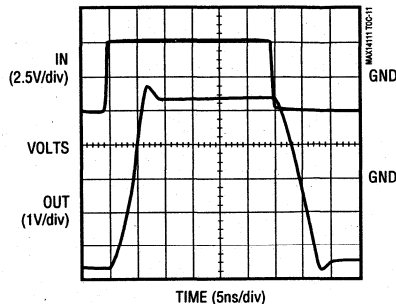
SMALL-SIGNAL PULSE RESPONSE

($R_L = 5k\Omega$)



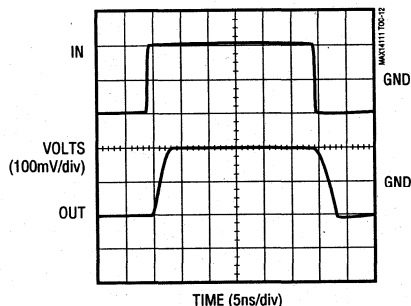
LARGE-SIGNAL PULSE RESPONSE

($R_L = 5k\Omega$)



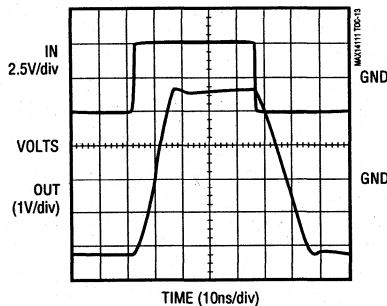
SMALL-SIGNAL PULSE RESPONSE

($C_L = 47pF$, $R_L = \text{open}$)



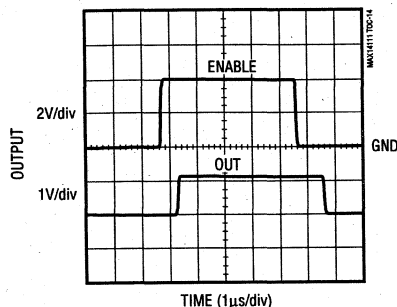
LARGE-SIGNAL PULSE RESPONSE

($C_L = 47pF$, $R_L = \text{open}$)

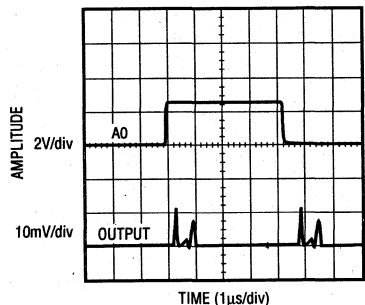


ENABLE/DISABLE DELAY TIME

(INPUT = 1.1V)



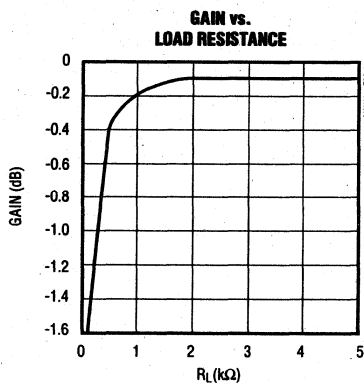
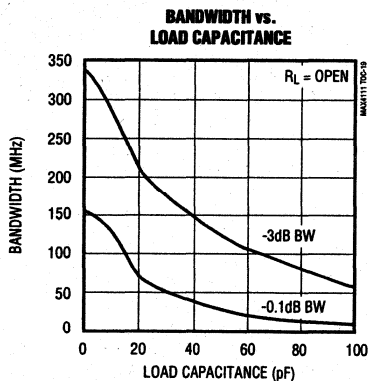
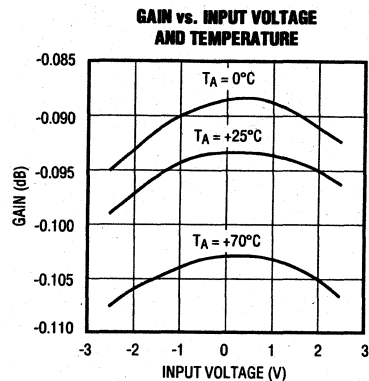
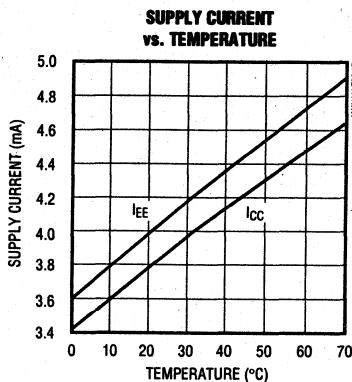
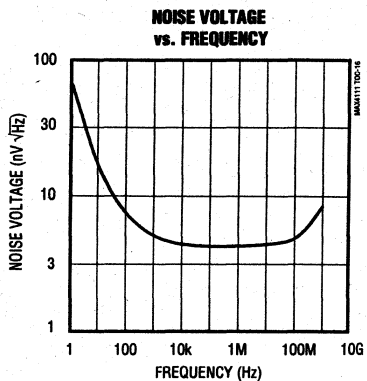
OUTPUT GLITCH AMPLITUDE



330MHz Buffered Video Switches/ Crosspoint Building Blocks

Typical Operating Characteristics (continued)

($V_S = \pm 5V$, $R_L = 5k\Omega$, $C_L \leq 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)



330MHz Buffered Video Switches/ Crosspoint Building Blocks

Pin Description

PIN			NAME	FUNCTION
MAX4111	MAX4121	MAX4221		
1, 3	3	2, 4, 5, 7	GND	Analog (signal) ground. Since inputs are isolated by these grounds, GND should be as noise-free as possible.
—	1	—	A0	Logic Input. Channel Selection Bit for the 2x1. See Table 2.
2	—	—	IN	Signal Input
—	2, 4	1, 3	IN0, IN1	Signal Input
4	—	—	N.C.	No Connect—not internally connected
5	5	12	VEE	Negative Power-Supply Voltage. Connect to -5V. Decouple to power ground.
6	6	—	OUT	Signal Output
—	—	6, 8	IN2, IN3	Signal Inputs for the dual 2x1 switch
7	7	14	VCC	Positive Power-Supply Voltage. Connect to +5V. Decouple to power ground.
8	8	—	EN	Logic Input. Output Enable for the 1x1, 2x1 switches. A logic high on this pin enables the output. A logic low causes the output to assume a high-impedance state, and reduces supply current.
—	—	9, 10	SEL3, SEL2	Logic Inputs. Channel Selection Bits for OUT1 of the dual 2x1 (MAX4221). See Table 3.
—	—	11, 13	OUT1, OUT0	Signal Outputs
—	—	15, 16	SEL1, SEL0	Logic Inputs. Channel Selection Bits for OUT0 of the dual 2x1 (MAX4221). See Table 3.

Detailed Description

The MAX4111/MAX4121/MAX4221 video switches are manufactured with Maxim's proprietary, ultra-high frequency, complementary bipolar process that yields high bandwidth and low capacitance. Make-before-break switching is used to reduce noise and glitches, even when switching from part to part in large arrays. The input buffers provide a constant high input impedance, and prevent the make-before-break action from feeding back to the input.

The design of the switching mechanism limits the inevitable glitch to less than 13mVp-p. In addition, the glitch pulse is positive to avoid confusion with negative sync pulses.

Unity-gain buffers isolate other inputs from the switching action of large multiplex arrays. These buffers can drive 5k Ω resistive loads. In addition, these devices drive capacitive loads without oscillation. Load capacitance is limited only by system bandwidth requirements.

The MAX4111/MAX4121/MAX4221 do not contain buffer latches. The digital inputs are transparent.

MAX4111/MAX4121/MAX4221

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330MHz Buffered Video Switches/ Crosspoint Building Blocks

Table 1. MAX4111 Truth Table

EN	OUT
0	High-Z
1	IN

Table 2. MAX4121 Truth Table

A0	EN	OUT
X	0	High-Z
0	1	IN0
1	1	IN1

Table 3. MAX4221 Truth Table

SEL0	SEL1	OUT0
0	0	High-Z
1	0	IN0
0	1	IN1
1	1	NA

SEL2	SEL3	OUT1
0	0	High-Z
1	0	IN2
0	1	IN3
1	1	NA

Note: SEL0 = SEL1 = 1 and/or SEL2 = SEL3 = 1 is not allowed. Enabling these states will not damage the device, but may cause excessive supply currents and distortion.

Applications Information

Grounding, Bypassing, and PC Board Layout

To obtain the full 330MHz bandwidth of these switches, Microstrip and Stripline techniques are recommended. To ensure your PC board does not degrade the switch's performance, it's wise to design the board for a frequency greater than 1GHz. Even with very short runs, it's good practice to use this technique at critical points such as inputs and outputs.

Use the following guidelines when designing the board:

- Do not use wire-wrap boards, because they are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.

- In general, surface-mount components have shorter leads and lower parasitic reactance, and give better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal side and the other a ground plane.
- Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

Bypass Components—Capacitors

Surface-mount ceramic capacitors are recommended to achieve good high-frequency bypassing. A 0.1µF capacitor in parallel with a 1000pF capacitor should be used for each supply. The capacitors should be located as close to the ICs supply pins as possible, with the smaller value capacitor being closer to the IC than the other.

Creating Larger Arrays

The MAX4111/MAX4121/MAX4221 were designed as building blocks for larger arrays. The single-pole switch allows the system designer much greater control over crosstalk than multiple switches in a single IC. For this reason, cable drivers have not been included in the switch design because of the high-power drive required (see Figure 6).

Even though the stability of these devices is not worsened by adding capacitance, you may want to limit the number of switches connected together. The MAX4111/MAX4121/MAX4221 have a finite input capacitance of about 3pF and a dynamic output resistance of about 20Ω. This causes a pole at a little more than 2.7GHz. However, in a large array with many switch inputs, the total capacitance is N x 3pF, where "N" is the number of switches connected in parallel. The pole will be located at:

$$\frac{1}{2\pi \times (N \times 3\text{pF} + C_{\text{STRAY}}) \times 20\Omega} \text{ MHz}$$

CSTRAY = Stray capacitance at the interconnect

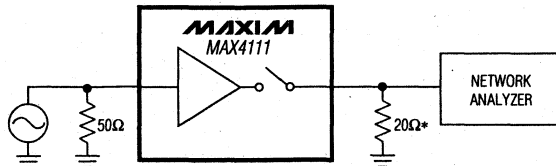
If the maximum number of switches that may be connected while still maintaining bandwidth is less than your system requirements, use a unity-gain buffer amplifier to isolate the switch from the remainder of the inputs.

330MHz Buffered Video Switches/ Crosspoint Building Blocks

Test Circuits

MAX4111/MAX4121/MAX4221

8



* 20Ω RESISTOR USED TO SIMULATE THE OUTPUT OF AN ON SWITCH.
IN THIS WAY, OPERATION IN AN ARRAY IS SIMULATED.

Figure 1. MAX4111 Off Isolation

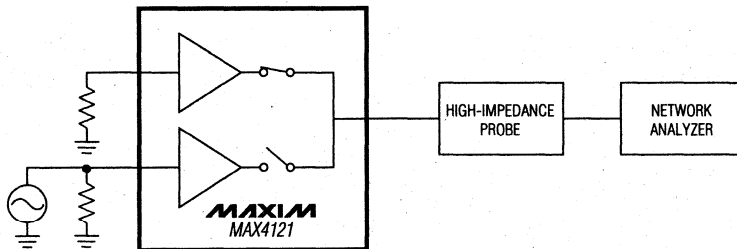
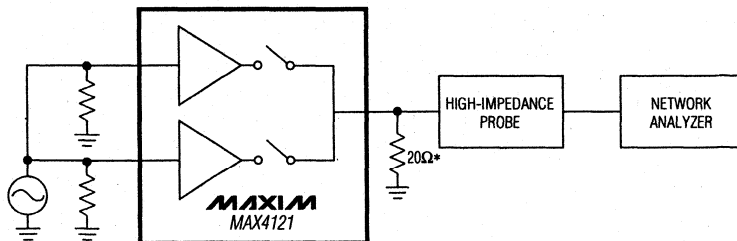


Figure 2. MAX4121 All-Hostile Crosstalk



* 20Ω RESISTOR USED TO SIMULATE THE OUTPUT OF AN ON SWITCH.
IN THIS WAY, OPERATION IN AN ARRAY IS SIMULATED.

Figure 3. MAX4121 Off Isolation

330MHz Buffered Video Switches/ Crosspoint Building Blocks

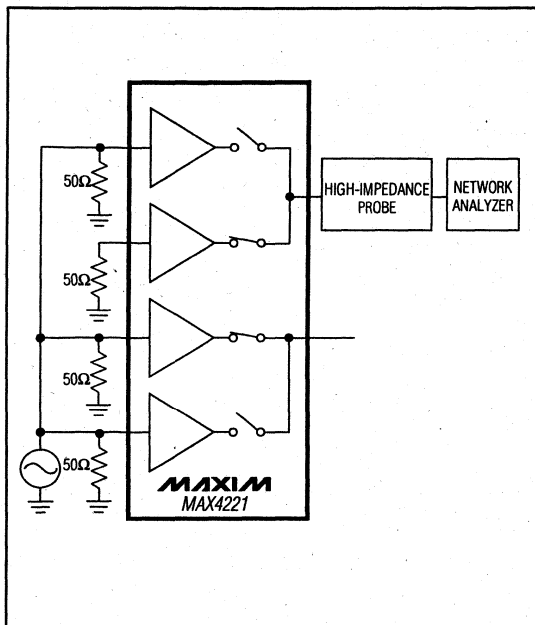


Figure 4. MAX4221 All-Hostile Crosstalk

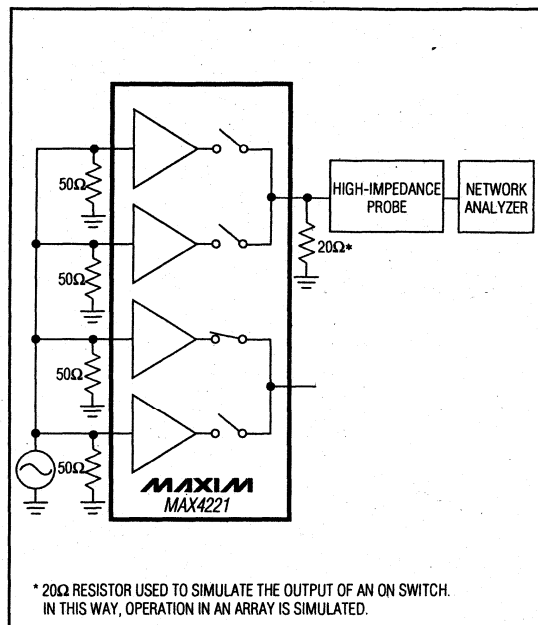


Figure 5. MAX4221 Off Isolation

330MHz Buffered Video Switches/ Crosspoint Building Blocks

MAX4111/MAX4121/MAX4221

8

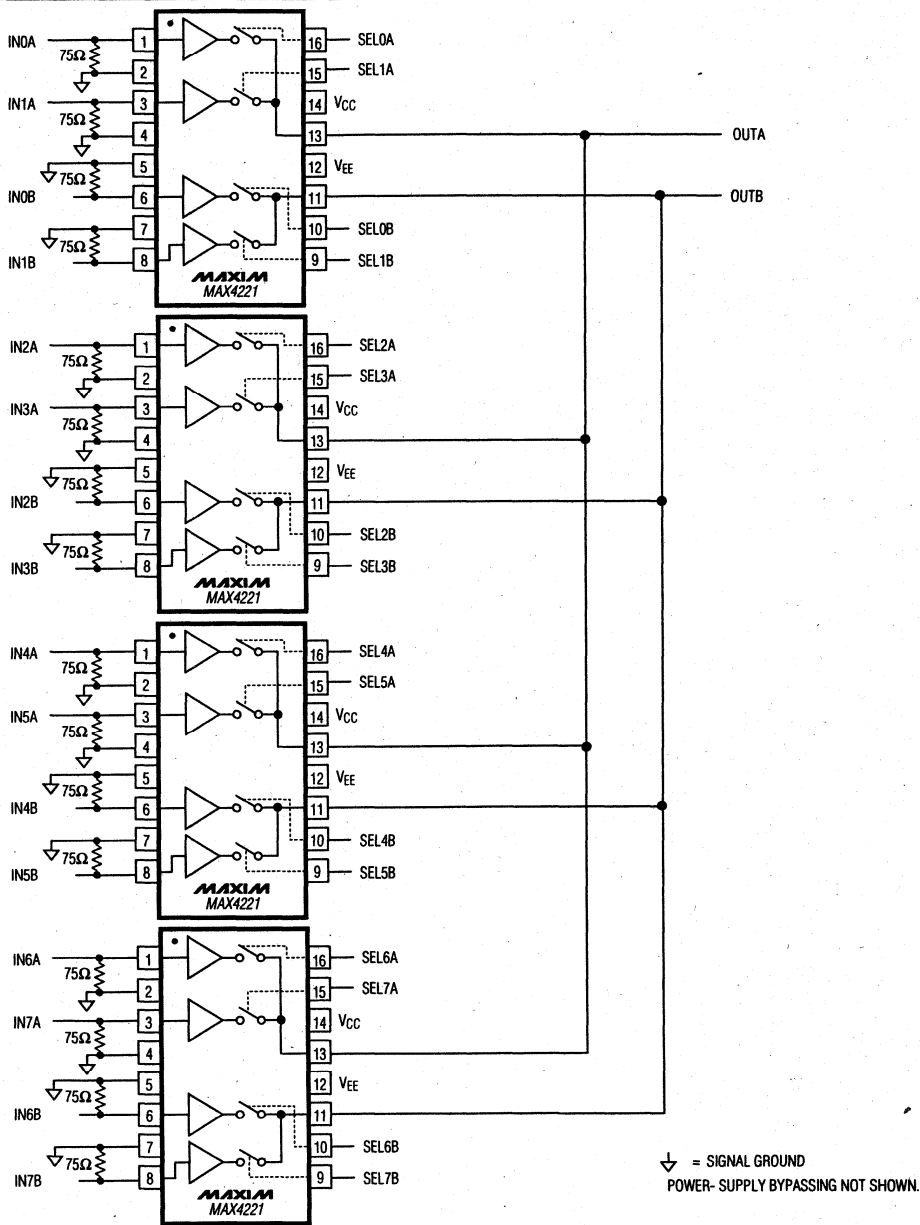


Figure 6. 8x2 Multiplexer Using MAX4221

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

500MHz, High-Speed, Current-Mode Feedback Op Amps

MAX4112/MAX4113

General Description

The MAX4112/MAX4113 current-mode feedback op amps combine high-speed performance with low-power operation. The MAX4112 is optimized for closed-loop gains (A_{VCL}) of 2V/V or greater, while the MAX4113 is optimized for gains of 10V/V or greater.

The MAX4112/MAX4113 require only 5mA of supply current to deliver bandwidths of 500MHz ($A_v \geq 2V/V$) and 375MHz ($A_v \geq 10V/V$) respectively, producing an effective gain-bandwidth product of 1GHz for the MAX4112 and 3.8GHz for the MAX4113. The high slew rates (1500V/ μ s and 1800V/ μ s) provide exceptional full-power bandwidths (225MHz and 275MHz), making these amplifiers ideal for high-performance pulse and RGB video applications.

These high-speed op amps have a wide output voltage swing of $\pm 3.5V$ and a high current-drive capability of 70mA.

Applications

Broadcast and High-Definition TV Systems

RGB Video

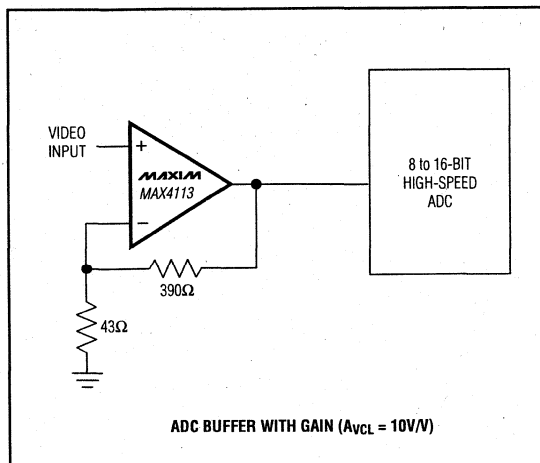
Pulse/RF Amplifier

Ultrasound

Active Filters

ADC Buffers

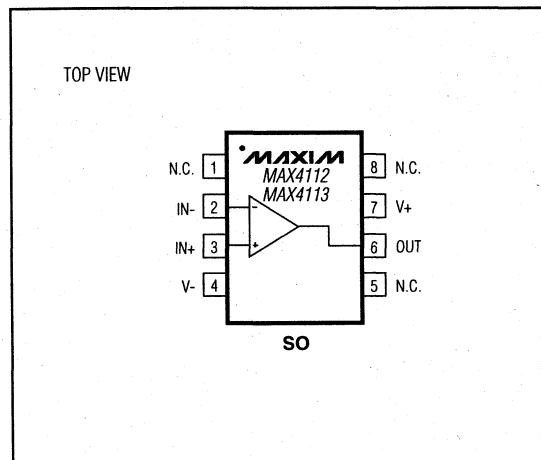
Typical Application Circuit



Features

- ♦ 500MHz Gain Bandwidth ($A_{VCL} = 2V/V$, MAX4112)
375MHz Gain Bandwidth ($A_{VCL} = 10V/V$, MAX4113)
- ♦ 1500V/ μ s Slew Rate (MAX4112)
1800V/ μ s Slew Rate (MAX4113)
- ♦ 225MHz Full-Power Bandwidth ($V_O = 2V_p$ -p, MAX4112)
275MHz Full-Power Bandwidth ($V_O = 2V_p$ -p, MAX4113)
- ♦ High Output Drive: 70mA
- ♦ Low Power: 5mA Supply Current

Pin Configuration



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MAXIM

Maxim Integrated Products 8-31

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EVALUATION KIT
AVAILABLE**MAXIM**

330MHz, 4x1 Precision Video Multiplexer

General Description

The MAX4141 is a wideband 330MHz, 700V/ μ s 4x1 multiplexer optimized for high-definition, broadcast-quality, composite (HDTV, NTSC, PAL, SECAM) video switching arrays. The device includes four open-loop buffer amplifiers with a 0.1dB gain flatness of 150MHz, and enable and switch-control logic. The MAX4141 operates from ± 5 V supplies and features differential phase and gain error of only 0.01°/0.01%. The ultra-low switching glitch (less than 13mV) is positive to avoid confusion with any sync pulses.

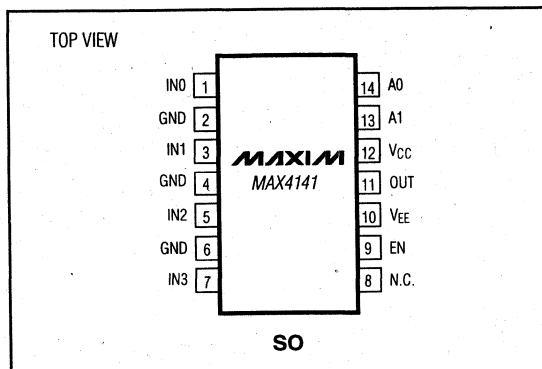
Ideal as a building block for large switch arrays, the MAX4141 features a constant, high input impedance and a disable function that puts the output into a high-impedance state and reduces the operating current to only 250 μ A. The open-loop architecture allows the output to drive capacitive loads without oscillation.

Other key features include -66dB crosstalk (30MHz), -74dB isolation (30MHz), less than 10mV offset voltage, and a 110MHz full-power bandwidth (1.4Vp-p). The MAX4141 is available in a 14-pin narrow SO package.

Applications

Broadcast/HDTV-Quality Color Signal Multiplexing
Video Routers and Crosspoint Arrays
RF and IF Routing
Graphics Color Signal Routing
Telecom Routing
Data Acquisition

Pin Configuration



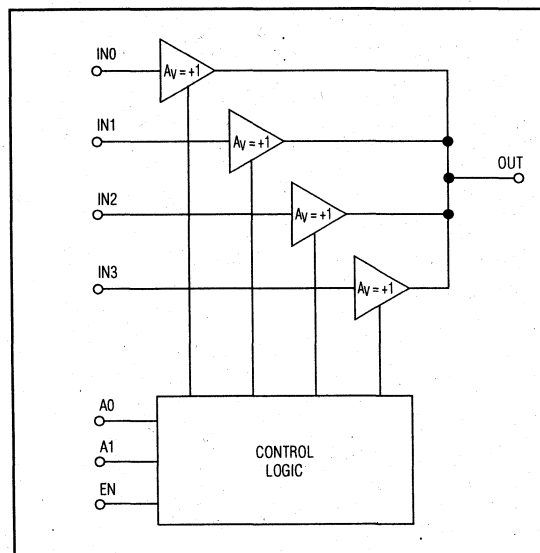
Features

- ◆ 330MHz -3dB Bandwidth
- ◆ 0.1dB Gain Flatness of 150MHz
- ◆ 700V/ μ s Slew Rate
- ◆ 0.01°/0.01% Differential Phase/Gain
- ◆ -66dB Crosstalk and -74dB Isolation at 30MHz
- ◆ High-Z Outputs when Disabled
- ◆ 3pF Input Capacitance
- ◆ Low Switching Glitch
- ◆ On-Board Control Logic

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4141CSD	0°C to +70°C	14 SO

Functional Diagram



MAX4141

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MAXIM

Maxim Integrated Products 8-33

Call toll free 1-800-998-8800 for free samples or literature.

330MHz, 4x1 Precision Video Multiplexer

ABSOLUTE MAXIMUM RATINGS

VCC.....	6V	Continuous Power Dissipation (T _A = +70°C)	
VEE.....	-6V	SO (derate 8.00mW/°C above +70°C)	640mW
VCC-VEE.....	12V	Operating Temperature Range.....	0°C to +70°C
Analog Input Voltage.....	(V _{EE} - 0.3V) to (V _{CC} + 0.3V)	Storage Temperature Range.....	-65°C to +160°C
Digital Input Voltage.....	-0.3V to (V _{CC} + 0.3V)	Junction Temperature.....	+150°C
Duration of Short Circuit to Ground.....	Continuous (Note 1)	Lead Temperature (soldering, 10sec).....	+300°C

Note 1: If maximum power-dissipation rating is met.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±5V, -2.5V ≤ V_{IN} ≤ +2.5V, R_L = 5kΩ, C_L = 5pF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PARAMETERS							
Operating Supply Voltage	V _S			±4.5	±5.0	±5.5	V
Operating Supply Current	I _{S(ON)}	Enabled	T _A = +25°C	5.0		5.5	mA
			T _A = T _{MIN} to T _{MAX}	6.5			
Disabled Supply Current	I _{S(OFF)}			250		350	μA
Input Voltage Range	V _{IN}			±2.5			V
Input Bias Current	I _B	V _{IN} = 0V	Channel selected	±2.5		±4.0	μA
			Channel disabled	±0.2			
Input Resistance	R _{IN}	Channel selected		0.4			MΩ
		Channel disabled		100			
Input Capacitance	C _{IN}	V _{IN} = 0V, channel enabled or disabled		3			pF
Output Offset Voltage	V _{OS}	T _A = +25°C		±3		±10	mV
		T _A = T _{MIN} to T _{MAX}				±15	
Power-Supply Rejection Ratio	PSRR	V _S = ±4.5V to ±5.5V		50			dB
Voltage Gain	A _v	V _{IN} = ±2.5V	T _A = +25°C	0.98		1.0	V/V
			T _A = T _{MIN} to T _{MAX}	0.97		1.0	
Output Resistance	R _{OUT}			20			Ω
Disabled Output Current	I _{OUT(OFF)}	V _{OUT} = 0V		10			nA
Disabled Output Resistance	R _{OUT}			30			MΩ
Disabled Output Capacitance	C _{OUT}			5			pF
Logic Input High Voltage	V _{INH}	V _S = ±4.5V to ±5.5V		2.0			V
Logic Input Low Voltage	V _{INL}	V _S = ±4.5V to ±5.5V				0.8	V
Logic Input High Current	I _{INH}	V _S = ±4.5V to ±5.5V				10	μA
Logic Input Low Current	I _{INL}	V _S = ±4.5V to ±5.5V				10	μA

330MHz, 4x1 Precision Video Multiplexer

MAX4141

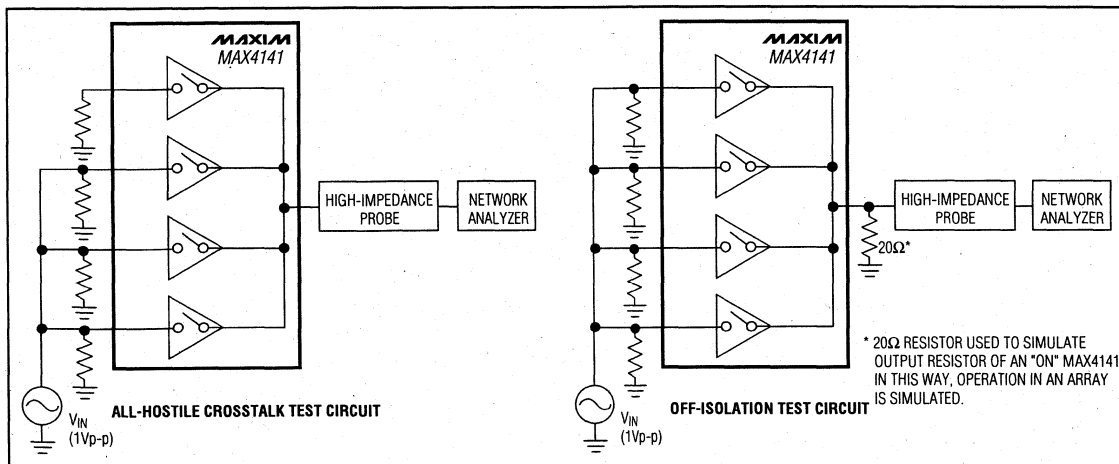
ELECTRICAL CHARACTERISTICS (continued)

($V_S = \pm 5V$, $-2.5V \leq V_{IN} \leq +2.5V$, $R_L = 5k\Omega$, $C_L = 5pF$, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PARAMETERS						
Slew Rate	SR	$V_{IN} = 5Vp-p$		700		V/ μs
		$V_{IN} = 1.4Vp-p$		500		
Full-Power Bandwidth (Note 2)	f_{PBW}	$V_{IN} = 1.4Vp-p$		110		MHz
		$V_{IN} = 5Vp-p$		45		
-3dB Bandwidth	f_{3dB}	$V_{IN} = 0.1Vp-p$		330		MHz
Gain Flatness		DC to 30MHz		0.02		dB
		DC to 150MHz		± 0.1		
Gain Peaking				0.08		dB
Small-Signal Rise Time	t_R	$V_{IN} = 0.2Vp-p$, 10% to 90%		950		ps
Differential Gain (Note 3)	DG	$f = 3.58MHz$		0.01		%
Differential Phase (Note 3)	DP	$f = 3.58MHz$		0.01		degrees
All-Hostile Crosstalk		$V_{IN} = 1Vp-p$, $f = 30MHz$, $R_{IN} = 50\Omega$		66		dB
Off Isolation		$V_{IN} = 1Vp-p$, $f = 30MHz$		74		dB
Channel Switching Off Time	t_{OFF}			1.0		μs
Channel Switching On Time	t_{ON}			500		ns
Switching Transient				13		mVp-p
Group Delay		$f = 3.58MHz$		860		ps
Input-Output Delay Matching		Chip-to-chip, $f = 3.58MHz$		± 0.2		degrees
Second Harmonic Distortion		$f = 30MHz$, $V_{IN} = 1.4Vp-p$, $R_L = 2k$		-65		dBc
Third Harmonic Distortion		$f = 30MHz$, $V_{IN} = 1.4Vp-p$, $R_L = 2k$		-70		dBc

Note 2: Full-Power Bandwidth is inferred from Slew Rate (SR) testing by the equation $SR = \omega E_p$, where E_p is the peak output voltage and $\omega = 2\pi f$.

Note 3: Differential Gain and Phase are tested using a modulated ramp, 100IRE (0.714V).

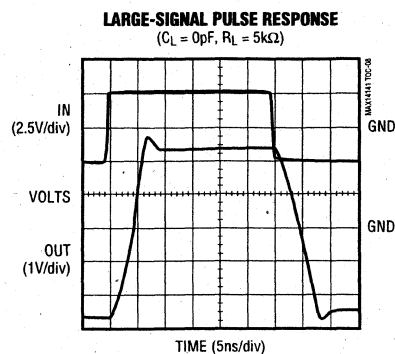
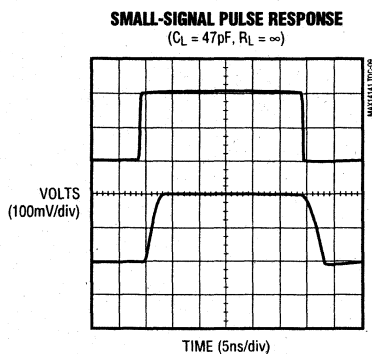
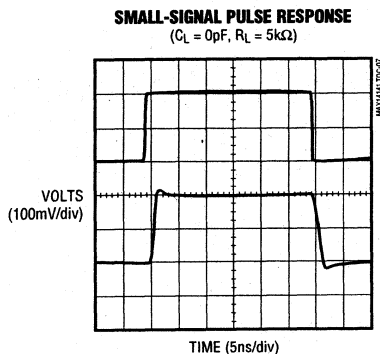
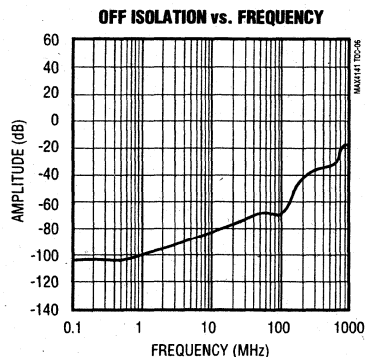
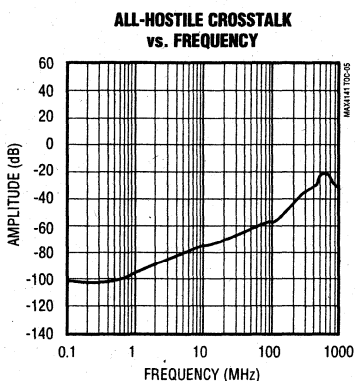
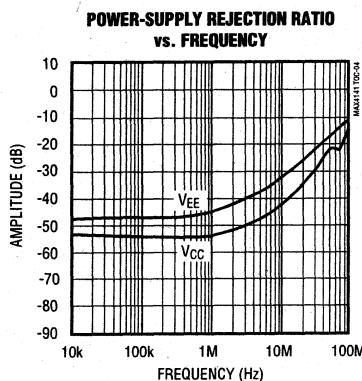
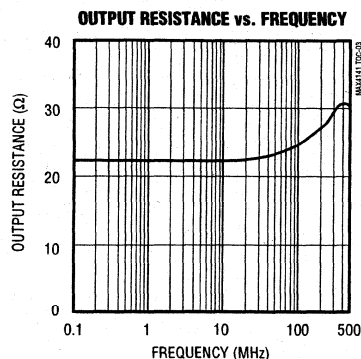
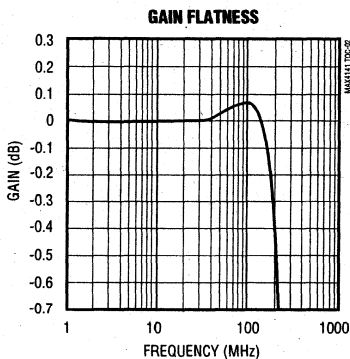
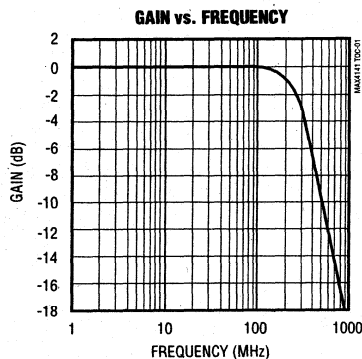


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330MHz, 4x1 Precision Video Multiplexer

Typical Operating Characteristics

($V_S = \pm 5V$, $R_L = 5k\Omega$, $C_L = 1pF$, $T_A = +25^\circ C$, unless otherwise noted.)



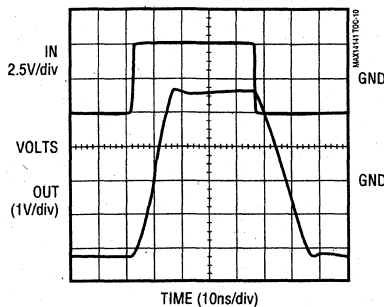
330MHz, 4x1 Precision Video Multiplexer

Typical Operating Characteristics (continued)

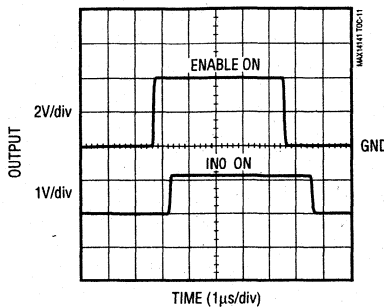
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

LARGE-SIGNAL PULSE RESPONSE

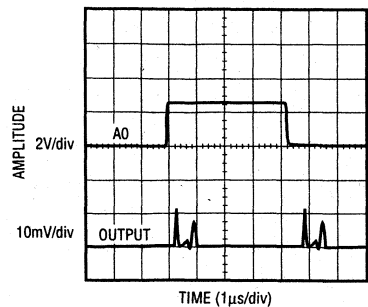
($C_L = 47\text{pF}$, $R_L = \infty$)



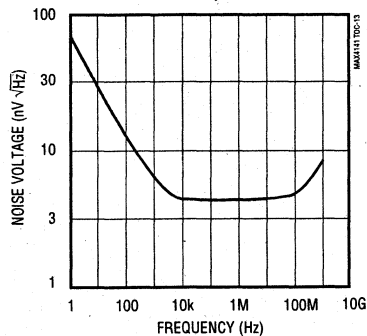
ENABLE/DISABLE DELAY TIME



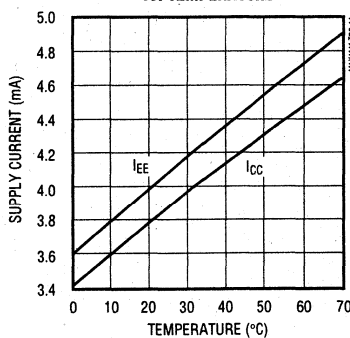
OUTPUT GLITCH AMPLITUDE



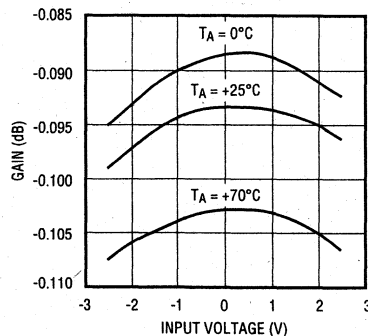
NOISE VOLTAGE vs. FREQUENCY



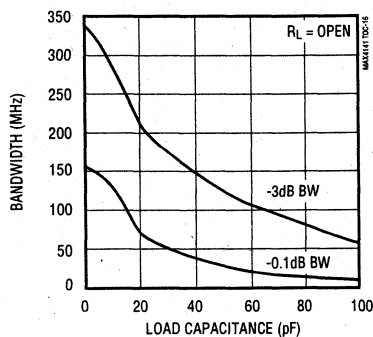
SUPPLY CURRENT vs. TEMPERATURE



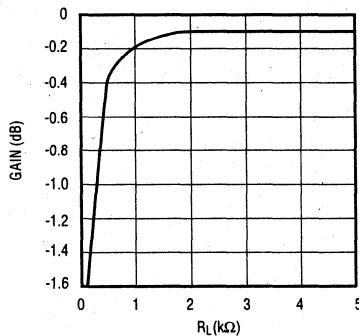
GAIN vs. INPUT VOLTAGE AND TEMPERATURE



BANDWIDTH vs. LOAD CAPACITANCE



GAIN vs. LOAD RESISTANCE



MAX4141

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330MHz, 4x1 Precision Video Multiplexer

Pin Description

PIN	FUNCTION	DESCRIPTION
1	IN0	Signal Input
2, 4, 6	GND	Analog (Signal) Ground. Since inputs are isolated by these grounds, they should be as noise-free as possible.
3	IN1	Signal Input
5	IN2	Signal Input
7	IN3	Signal Input
8	N.C.	No Connect—not internally connected.
9	EN	Output Enable and device shutdown. A logic high on this pin enables the output. A logic low causes the output to assume a high-impedance state and reduces operating current.
10	VEE	Negative Power-Supply Voltage. Decouple to power ground.
11	OUT	Signal Output
12	VCC	Positive Power-Supply Voltage. Decouple to power ground.
13	A1	Channel Selection Bit. See truth tables.
14	A0	Channel Selection Bit. See truth tables.

Detailed Description

The MAX4141 video switch is manufactured with Maxim's proprietary complementary bipolar process that yields high bandwidth and low capacitance. To maintain a wide bandwidth, the MAX4141 incorporates a straightforward structure of input and output buffers. Make-before-break switching is employed to reduce noise and glitches, even when switching from part to part in large arrays. The input buffers provide a constant, high input impedance. And, they prevent the make-before-break action from feeding back to the input and causing noise and/or glitches.

The design of the switching mechanism limits the inevitable glitch to within 13mVp-p. In addition, the glitch pulse is positive to avoid confusion with any negative sync pulses.

Unity-gain output buffers isolate other inputs from the switching action of large multiplex arrays. These buffers can drive 5k Ω resistive loads. Load capacitance is limited only by system bandwidth requirements.

The MAX4141 does not contain buffer latches. The digital inputs control the switch transparently.

Applications Information

Grounding, Bypassing, and PC Board Layout

In order to obtain the MAX4141's full 330MHz bandwidth, Microstrip and Stripline techniques are recommended in most cases. To ensure your PC board does not degrade the switch's performance, it's wise to design the board for a frequency greater than 1GHz. Even with very short runs, it's good practice to use this technique at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:

- Do not use wire-wrap boards, because they are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, and give better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

330MHz, 4x1 Precision Video Multiplexer

MAX4141

On Maxim's evaluation kit, the ground plane has been removed from areas where keeping the trace capacitance to a minimum is more important than maintaining ground continuity. For example, the ground plane has been removed from beneath the IC to minimize pin capacitance.

The signal input line is approximately 0.103 inches wide to minimize inductance and to provide a constant 50Ω impedance path. It is terminated by a 50Ω chip resistor.

Bypass Components—Capacitors

Electrolytic and tantalum capacitors are available from 0.1μF to over 300μF, but have resonant frequencies below 1MHz. Ceramic capacitors are highly recommended and are available to 1μF, with the smaller values having resonant frequencies to almost 1GHz. The less expensive capacitors are constructed using a multilayer approach; high values are available, but resonant frequencies beyond a few hundred megahertz are not, because of the inductive effect of the multiple layers. More expensive, solid dielectric microwave porcelain/ceramic capacitors are available up to 1000pF with resonant frequencies beyond 20GHz. In all types, resonant frequency depends on capacitor value, voltage rating, and physical size; the larger the capacitor, the lower the resonant frequency.

We recommend ceramic surface-mount/chip capacitors. Placement of bypass capacitors on the PC board is critical, and the smaller chip capacitors allow placement as close to the part as practical. The smaller, higher frequency capacitors should be placed as close to the chip as possible, with the higher-value capacitors placed farther away.

Creating Large Arrays

The MAX4141 was designed as a building block for large arrays. The high-power drive required for internal cable drivers has a negative effect on crosstalk and increases system power consumption. Figure 1 shows an 8x1 multiplexer circuit.

Even though the MAX4141 drives capacitive loads, you may want to limit the number of switches connected together to maximize bandwidth. The MAX4141 has a finite input capacitance of about 3pF and a dynamic output resistance of about 20Ω. This causes a pole at a little more than 2.6GHz. However, in a large array with many switch inputs, the total capacitance is (N x 3pF), where "N" is the number of switches connected in parallel. The pole will be located at:

$$\frac{1}{2\pi \times (N \times 3\text{pF} + C_{\text{STRAY}}) \times 20\Omega} \text{ MHz}$$

where CSTRAY is the stray capacitance from the interconnect.

If the maximum number of switches that may be connected while still maintaining bandwidth is less than your system requirements, use a unity-gain buffer amplifier to isolate the switch from the remainder of the inputs.

Table 1. Truth Table

A1	A0	EN	OUT
X	X	0	High-Z
0	0	1	IN0
0	1	1	IN1
1	0	1	IN2
1	1	1	IN3

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330MHz, 4x1 Precision Video Multiplexer

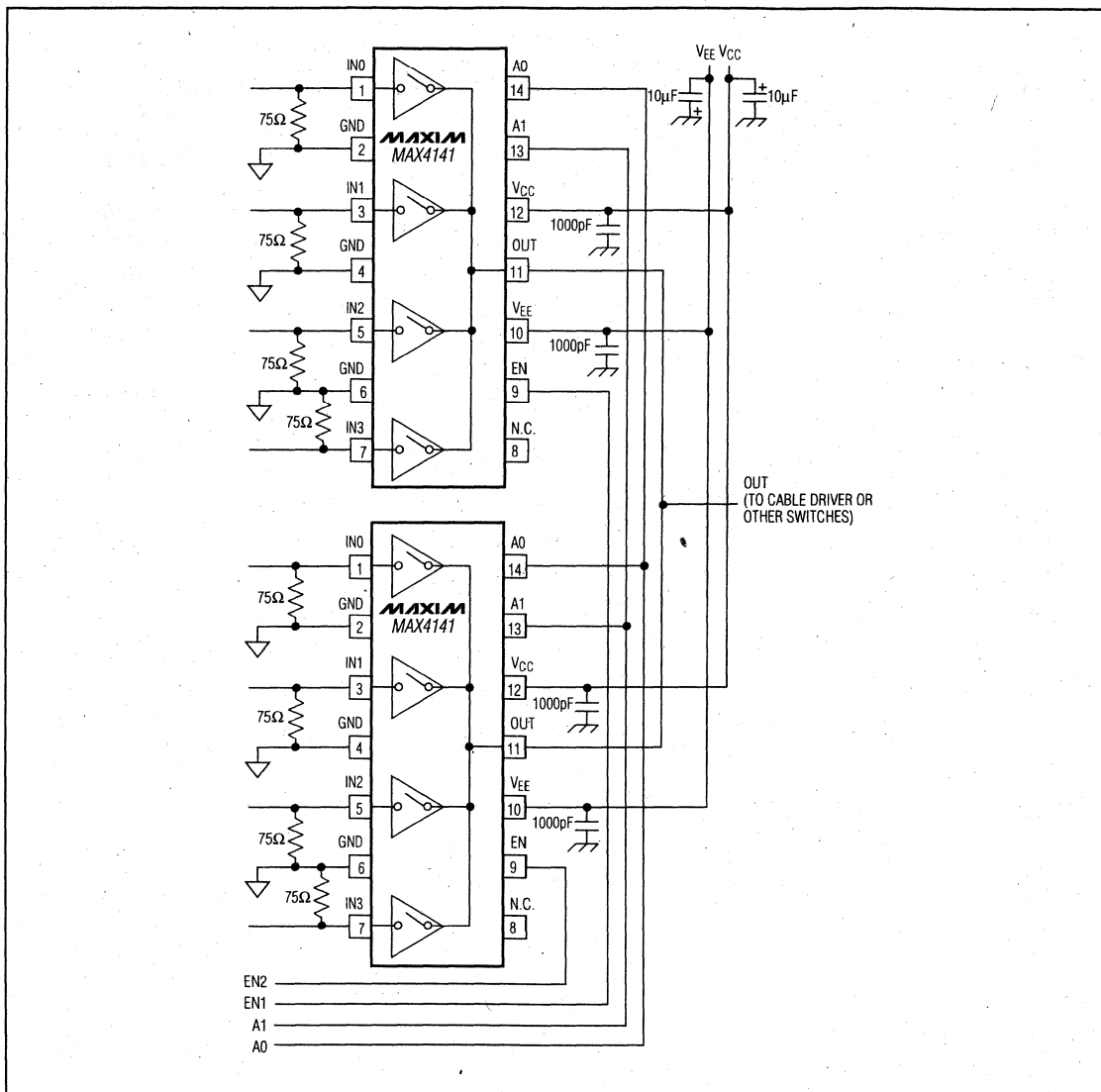


Figure 1. 8x1 Multiplexer Circuit

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

380MHz, Gain of +1/Gain of +2 High-Speed Buffers

General Description

The MAX4177/MAX4277 are wide-bandwidth, fast-settling buffer amplifiers featuring high slew rate, high precision, high output current, and low differential gain and phase errors. The MAX4177 is preset for unity voltage gain (0dB), and has a small-signal -3dB bandwidth of 380MHz. The MAX4277 is preset for a voltage gain of +2 (6dB), and has a small-signal -3dB bandwidth of 350MHz.

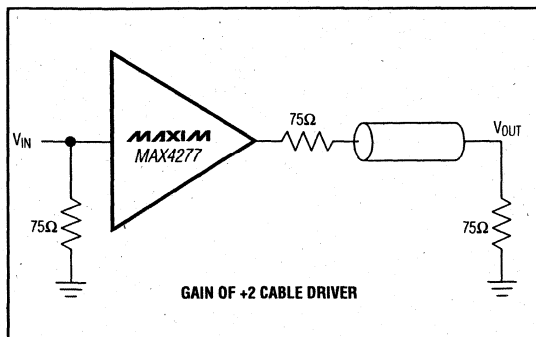
The MAX4177/MAX4277 feature the high slew rate and low power of current-mode feedback amplifiers. However, unlike conventional current-mode feedback amplifiers, these devices have a unique input stage that combines the benefits of current-feedback topology with those of the traditional voltage-feedback topology. This combination of architectures results in low input offset voltage and bias current, and high gain precision and power-supply rejection.

The MAX4177/MAX4277 are ideally suited for driving 50Ω or 75Ω loads. They are the perfect choice for high-speed cable-driving applications such as video routing. In addition, the devices incorporate a shutdown mode that can be used to disable the output in multiplexer applications and to conserve power. The MAX4177/MAX4277 are available in 8-pin DIP, SO and μMAX packages.

Applications

Broadcast and High-Definition TV Systems
Video Switching and Routing
High-Speed Cable Drivers
Communications
Medical Imaging
Precision High-Speed DAC/ADC Buffers

Typical Operating Circuit



Features

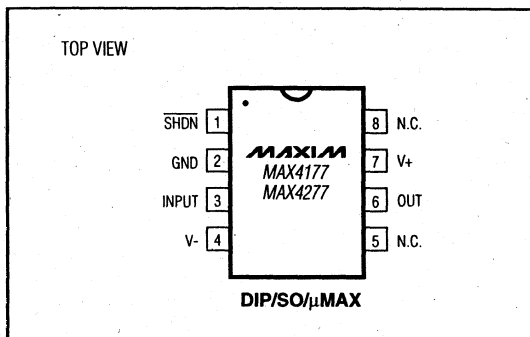
- ♦ High Speed:
 - 380MHz -3dB Bandwidth (MAX4177)
 - 350MHz -3dB Bandwidth (MAX4277)
 - 200MHz Full-Power Bandwidth (MAX4177, $V_{OUT} = 2V_{p-p}$)
 - 150MHz Full-Power Bandwidth (MAX4277, $V_{OUT} = 2V_{p-p}$)
 - 150MHz 0.1dB Flatness Bandwidth (MAX4177)
 - 120MHz 0.1dB Flatness Bandwidth (MAX4277)
- ♦ Low Differential Gain and Phase Error: 0.01%/0.01°
- ♦ High Slew Rate: 1800V/μs (MAX4177)
- ♦ Low Power: 8mA Quiescent Supply Current
400μA in Shutdown Mode
- ♦ High-Impedance Output in Shutdown Mode
- ♦ Low Input Bias Current: 2μA
- ♦ Low Input Offset Voltage: 0.5mV
- ♦ Low Input-Referred Voltage Noise: $5nV\sqrt{Hz}$
- ♦ High Gain Precision: 1.5% Max with 50Ω Load
- ♦ High PSRR: 75dB

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4177CPA	0°C to +70°C	8 Plastic DIP
MAX4177CSA	0°C to +70°C	8 SO
MAX4177CUA	0°C to +70°C	8 μMAX

Ordering Information continued on next page.

Pin Configuration



MAXIM

Maxim Integrated Products 8-41

Call toll free 1-800-998-8800 for free samples or literature.

MAX4177/MAX4277

380MHz, Gain of +1/Gain of +2 High-Speed Buffers

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4177EPA	-40°C to +85°C	8 Plastic DIP
MAX4177ESA	-40°C to +85°C	8 SO
MAX4177EUA	-40°C to +85°C	8 μ MAX
MAX4177MJA	-55°C to +125°C	8 CERDIP
MAX4277 CPA	0°C to +70°C	8 Plastic DIP
MAX4277CSA	0°C to +70°C	8 SO
MAX4277CUA	0°C to +70°C	8 μ MAX
MAX4277EPA	-40°C to +85°C	8 Plastic DIP
MAX4277ESA	-40°C to +85°C	8 SO
MAX4277EUA	-40°C to +85°C	8 μ MAX
MAX4277MJA	-55°C to +125°C	8 CERDIP

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

EVALUATION KIT WILL BE AVAILABLE

MAXIM

325MHz High-Speed Op Amp

MAX476

General Description

The MAX476 is a wide bandwidth, fast settling, unity-gain-stable op amp featuring low noise, low differential gain and phase errors, high slew rate, high precision, and high output current. The device architecture uses a standard voltage-feedback topology that can be configured into any desired gain setting, as with other general-purpose op amps.

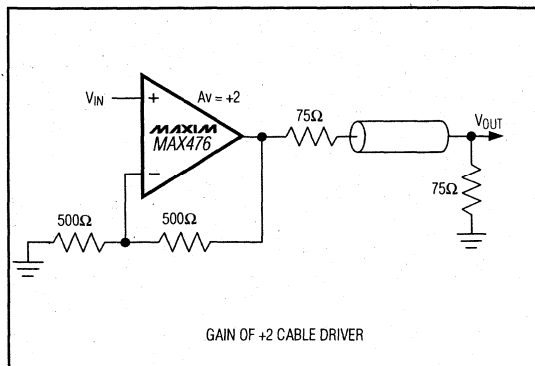
Unlike high-speed amplifiers using current-mode feedback architectures, the MAX476 has a unique input stage that combines the benefits of the voltage-feedback design (flexibility in choice of feedback resistor, two high-impedance inputs) with those of the current-feedback design. It also has the precision of voltage-feedback amplifiers, characterized by low input-offset voltage and bias current, low noise, and high common-mode and power-supply rejection.

The MAX476 is ideally suited for driving 50Ω or 75Ω loads. In addition, the device incorporates a high-speed shutdown mode to disable the output in multiplexed applications and to conserve power. Packages include 8-pin DIP, SO, and μ MAX.

Applications

Broadcast and High-Definition TV Systems
Video Switching and Routing
Communications
Medical Imaging
Precision DAC/ADC Buffer

Typical Operating Circuit



Features

- ♦ High Speed:
 - 325MHz Small-Signal Bandwidth ($A_v = 1$)
 - 150MHz Full-Power Bandwidth ($A_v = 1$, $V_o = 2V_{pp}$)
 - 1800V/ μ s Slew Rate
 - 100MHz 0.1dB Gain Flatness
- ♦ Low Differential Phase/Gain Error 0.01°/0.01%
- ♦ 8mA Quiescent Current (400 μ A in shutdown)
- ♦ High-Impedance Output in Shutdown Mode
- ♦ Low Input-Referred Voltage Noise: 5nV/ $\sqrt{Hz}$
- ♦ Low Input-Offset Voltage: 0.5mV
- ♦ 2 μ A Input Bias Current (either input)
- ♦ Voltage-Feedback Topology for Simple Design Configurations

Ordering Information

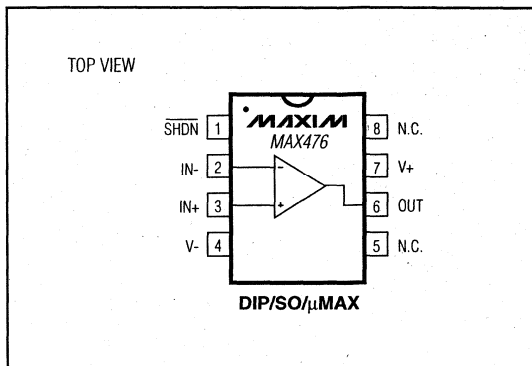
PART	TEMP. RANGE	PIN-PACKAGE
MAX476CPA	0°C to +70°C	8 Plastic DIP
MAX476CSA	0°C to +70°C	8 SO
MAX476CUA	0°C to +70°C	8 μ MAX
MAX476C/D	0°C to +70°C	Dice*
MAX476EPA	-40°C to +85°C	8 Plastic DIP
MAX476ESA	-40°C to +85°C	8 SO
MAX476EUA	-40°C to +85°C	8 μ MAX
MAX476MJA	-55°C to +125°C	8 CERDIP**

* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

** Contact factory for availability.

Pin Configuration

8



MAXIM

Maxim Integrated Products 8-43

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

EVALUATION KIT WILL BE AVAILABLE

MAXIM

430MHz Quad Video Buffers

MAX496/MAX497

General Description

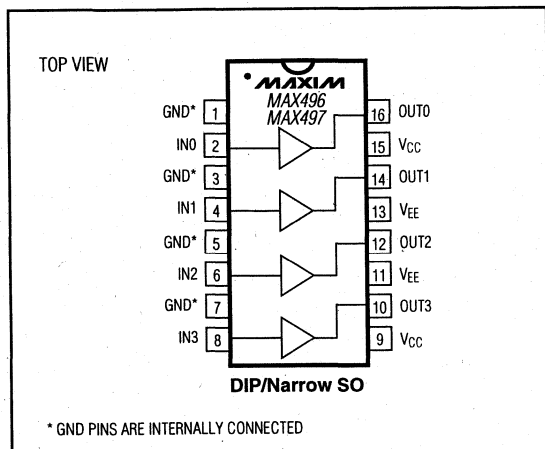
The MAX496 and MAX497 are quad, closed-loop $\pm 5V$ video buffer amplifiers that feature extremely high bandwidth and slew rate for both component video (RGB or YUV) and composite video (NTSC, PAL, SECAM). The MAX496 is a unity-gain buffer with a -3dB bandwidth of 430MHz and a 2400V/ μs slew rate. The MAX497 gain of +2 (6dB) buffer, optimized for driving back-terminated coaxial cable, features a -3dB bandwidth of 375MHz and a 2000V/ μs slew rate. The MAX496/MAX497 are not slew-rate limited, and provide a full-power bandwidth of 210MHz and 180MHz, respectively.

The MAX496/MAX497 incorporate a unique two-stage architecture that combines the low offset and noise benefits of voltage feedback with the high bandwidth and slew-rate benefits of current-feedback.

Applications

Computer Workstations
Surveillance Video
Broadcast and High-Definition TV Systems
Multimedia Products
Medical Imaging
High-Speed Signal Processing
Video Switching and Routing

Pin Configuration



Features

- ♦ High Speed:
Small-Signal -3dB Bandwidth = 430MHz (MAX496)
375MHz (MAX497)
Full-Power -3dB Bandwidth = 210MHz (MAX496)
180MHz (MAX497)
- ♦ Two Fixed Gain Options: $A_V = +1V/V$ (MAX496)
 $A_V = +2V/V$ (MAX497)
- ♦ 2400V/ μs Slew Rate (MAX496)
2000V/ μs Slew Rate (MAX497)
- ♦ Fast Settling Time: 12ns to 0.1%
- ♦ Low Differential Phase/Gain: 0.01°/0.01%
- ♦ 2pF Input Capacitance
- ♦ 5.0nV/ $\sqrt{Hz}$ Input Referred Voltage Noise
- ♦ Directly Drives 50 Ω or 75 Ω Back-Terminated Cables

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX496CPE	0°C to +70°C	16 Plastic DIP
MAX496CSE	0°C to +70°C	16 Narrow SO
MAX496C/D	0°C to +70°C	Dice*
MAX497CPE	0°C to +70°C	16 Plastic DIP
MAX497CSE	0°C to +70°C	16 Narrow SO
MAX497C/D	0°C to +70°C	Dice*

* Dice are specified at $T_A = +25^\circ C$, DC parameters only.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95



Two-Channel, Triple/Quad RGB Video Switches with Gain of +2 Buffers

General Description

The MAX498/MAX499 are high-speed, two-channel video switches with on-board high-speed, high-accuracy gain of +2 buffers. The MAX498 is a quad (RGB+SYNC) switch, and the MAX499 is a triple (RGB) switch. Fast switching time (3ns), fast settling times (9ns for a 4V step), and low differential gain and phase errors (0.01% and 0.02°) make these devices ideal for broadcast video applications. The buffer amplifiers feature +6dB of gain, 310MHz bandwidth, and 1500V/μs slew rate. The input voltage range is ±1.25V (V_{OUT} = ±2.5V) while driving a 50Ω or 75Ω back-terminated cable, and 1V (V_{OUT} = ±2V) while driving two 50Ω back-terminated cables.

These devices operate from ±5V and dissipate only 460mW. In addition, the buffer outputs can be placed in a high-impedance state that reduces power dissipation to 50mW and allows construction of larger switch arrays. Each video input is isolated by AC ground pins, reducing channel-to-channel crosstalk to -60dB at 30MHz and simplifying PC board layout. Input capacitance is a mere 2pF, which maximizes high-speed performance. Channel selection is controlled by a single TTL-compatible input.

The quad MAX498 is offered in 28-pin DIP and SO packages. The triple MAX499 is offered in 24-pin DIP and SO packages.

Applications

Video Signal Multiplexing	Video Security Systems
Broadcast-Quality Video	Multimedia Products
Workstations	Medical Imaging
RGB Color Video	High-Speed Signal Processing
Overlay Editors	

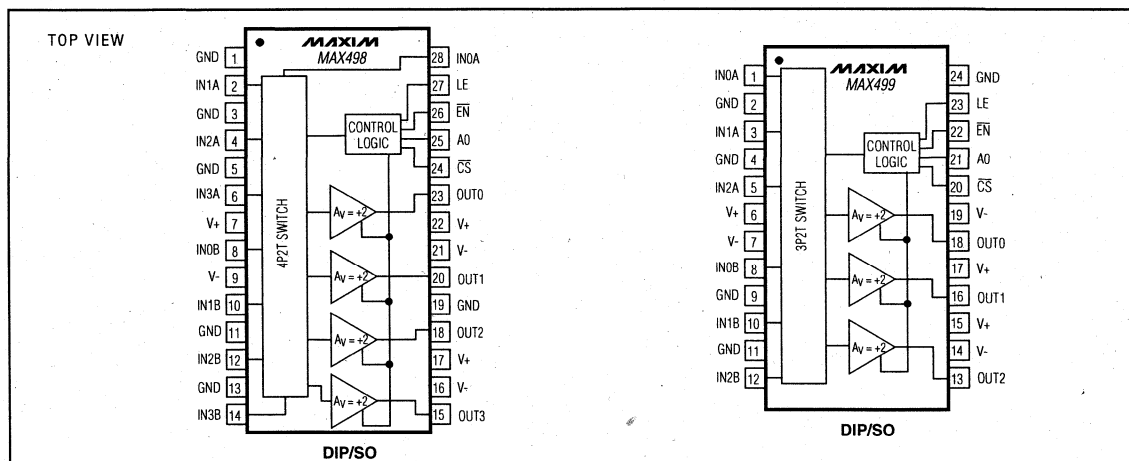
Features

- ♦ -3dB Small-Signal Bandwidth of 310MHz
- ♦ 0.1dB Gain Flatness of 150MHz
- ♦ 150MHz Full-Power Bandwidth
- ♦ 1500V/μs Slew Rate
- ♦ 0.01%/0.02° Differential Gain/Phase
- ♦ Drives 50Ω and 75Ω Back-Terminated Cable Directly
- ♦ Wide Output Swing:
±2V into 50Ω
±2.5V into 150Ω
- ♦ Fast Switching Time (3ns)
- ♦ Fast Settling Time (9ns to 0.1% for 4V step)
- ♦ 2pF On/Off Input Capacitance
- ♦ Outputs Can Be Paralleled for Larger Networks
- ♦ 7.8nV/√Hz Input Referred Noise

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX498CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX498CWI	0°C to +70°C	28 Wide SO
MAX499CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX499CWG	0°C to +70°C	24 Wide SO

Pin Configurations



8

MAXIM

Maxim Integrated Products 8-47

Call toll free 1-800-998-8800 for free samples or literature.

MAX498/MAX499

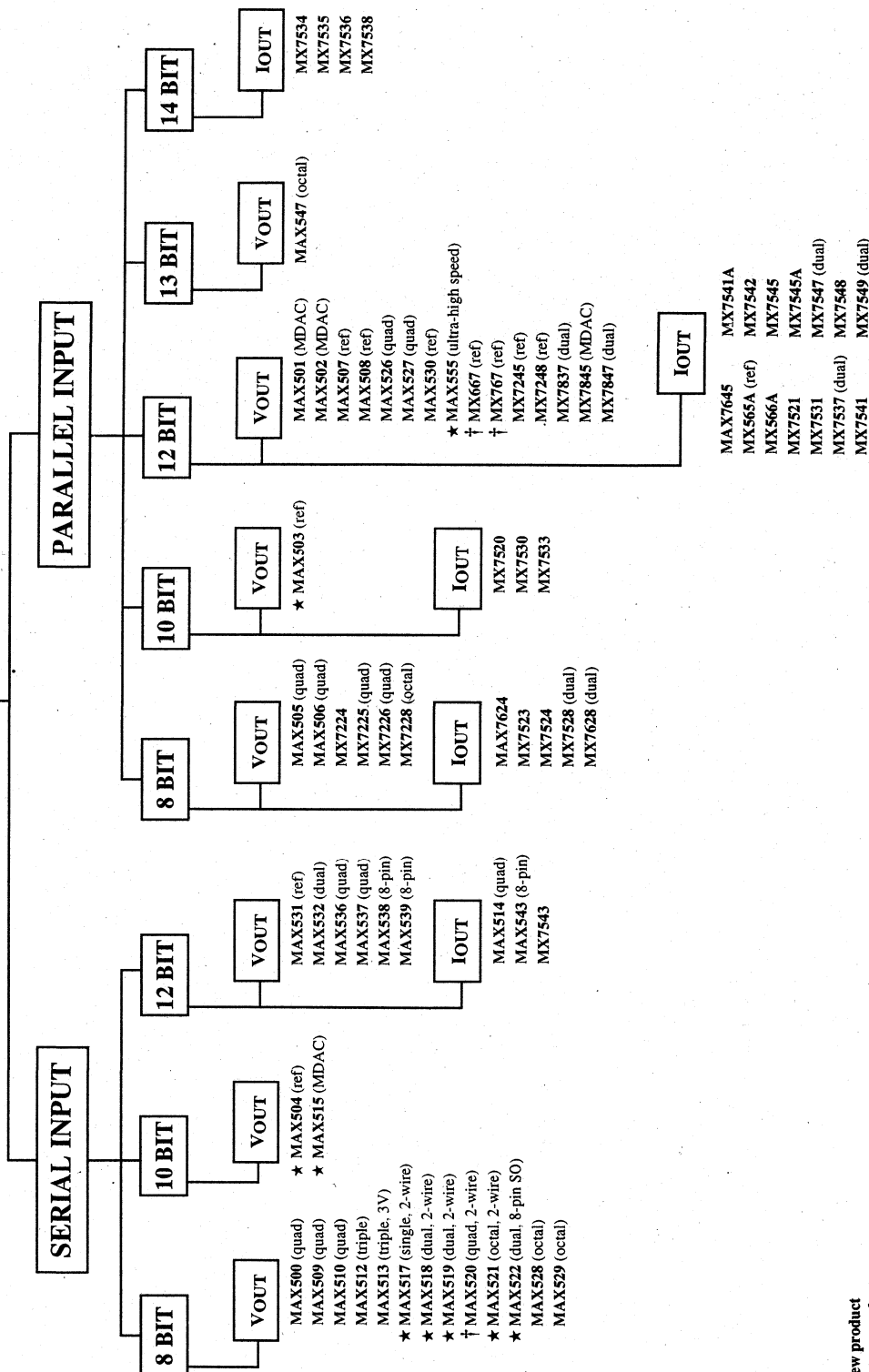


D/A Converters

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MAX503 5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC w/ Internal Reference.....	9-7
MAX504 5V, Low-Power, Voltage-Output, Serial 10-Bit DAC w/ Internal Reference	9-23
MAX515 5V, Low-Power, Voltage-Output, Serial 10-Bit DAC	9-23
MAX517 Single, 2-Wire, Serial 8-Bit DAC w/ Rail-to-Rail Outputs	9-37
MAX518 Dual, 2-Wire, Serial 8-Bit DAC w/ Rail-to-Rail Outputs in 8-Pin Package.....	9-37
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MAX520 Quad, 2-Wire, Serial 8-Bit DAC w/ Unbuffered Outputs*	9-53
MAX521 Octal, 2-Wire, Serial 8-Bit DAC w/ Rail-to-Rail Output.....	9-55
MAX522 Dual, Voltage-Output, Serial 8-Bit DAC in 8-Pin Package.....	9-69
MAX555 300Msps, 12-Bit DAC w/ Complementary Voltage Outputs.....	9-81

*Advance Information—first page of data sheet in preparation.

D/A CONVERTERS



★ New product
† Future product

Single D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (μs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up (\$)
MX7224	8	V	5.0	Ext	μP/8	+12 to +15 & -5	Single or dual supplies	3.16
MAX517	8	V	6.0	Ext	Serial, 2-wire	+5	2-wire interface	2.10
MX7523	8	I	0.15	MDAC	Logic	+15	Low-cost 8-bit DAC	2.60
MAX7624	8	I	0.25	MDAC	μP/8	+12 to +15	Improved MX7524	2.26
MX7524	8	I	0.4	MDAC	μP/8	+5 to +15	Low-cost 8-bit DAC	2.52
MAX503	10	V	25.0	Int/MDAC	μP/8	+5 or ±5	Ultra-low power, complete DAC	2.95
MAX504	10	V	25.0	Int/MDAC	Serial	+5 or ±5	Serial version of MAX503	2.80
MAX515	10	V	25.0	Ext	Serial	+5	Ultra-low power, 8-pin SO/DIP	2.50
MX7520	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7530	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7533	10	I	0.6	MDAC	Logic	+15	Low-cost 10-bit DAC	2.84
MAX555	12	V	0.5ns	Ext/MDAC	Parallel	-5.2	300MSPS update rate, 720B SFDR	‡
MX667	12	V	3.0	Int	μP/4 or 8	±12 to ±15	Compatible with 4- or 8-bit bus	‡
MX767	12	V	3.0	Int	μP/12	±12 to ±15	12-bit bus, fast logic interface	‡
MAX501	12	V	5.0	MDAC	μP/8	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX502	12	V	5.0	MDAC	μP/12	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX507	12	V	5.0	Int	μP/12	±12 to ±15	Complete 12-bit DAC with reference	7.65
MAX508	12	V	5.0	Int	μP/8	±12 to ±15	Complete 12-bit DAC with reference	7.65
MX7845	12	V	5.0	MDAC	μP/12	±15	4-range 4-quadrant multiplying DAC	6.26
MX7245	12	V	10.0	Int	μP/12	±15 or +12 to +15	Single or dual supplies with reference	8.33
MX7248	12	V	10.0	Int	μP/8	±15 or +12 to +15	8-bit interface MX7245	8.33
MAX530	12	V	25.0	Int/MDAC	μP/8	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX531	12	V	25.0	Int/MDAC	Serial	+5 or ±5	Serial version of MAX530	5.45
MAX538	12	V	25.0	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	25.0	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MX565A	12	I	0.25	Int	Logic	±15	Has +10V buried-zener reference	9.68
MX566A	12	I	0.35	Ext	Logic	-15	No built-in reference	9.04
MX7521	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.00
MX7531	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.08
MX7541A	12	I	0.6	MDAC	Logic	+15	12-bit data bus	5.72
MAX543	12	I	1.0	MDAC	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	4.80
MAX7645	12	I	1.0	MDAC	μP/12	+15	Improved MX7545	5.60
MX7541	12	I	1.0	MDAC	Logic	+15	12-bit data bus	5.07
MX7545A	12	I	1.0	MDAC	μP/12	+5 to +15	Improved MX7545	6.03
MX7548	12	I	1.0	MDAC	μP/8	+5 to +15	8-bit data bus with latches	6.06
MX7542	12	I	2.0	MDAC	μP/4	+5	4-bit data bus with latches	7.52
MX7543	12	I	2.0	MDAC	Serial	+5	12-bit multiplying DAC	7.52
MX7545	12	I	2.0	MDAC	μP/12	+5 to +15	12-bit data bus with latches	5.00
MX7534	14	I	1.5	MDAC	μP/8	+12 to +15	Double-buffered inputs	13.37
MX7535	14	I	1.5	MDAC	μP/8 or 14	+12 to +15	Double-buffered inputs	15.00
MX7536	14	I	1.5	MDAC	μP/8 or 14	+12 to +15	No external resistors needed	14.66
MX7538	14	I	1.5	MDAC	μP/14	+12 to +15	Low-cost 14-bit DAC	8.88

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

‡ Future product—contact factory for pricing and availability. Specifications are preliminary.

‡ Contact factory for pricing.

Multiple D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up (\$)
DUAL								
MAX518	8	V	6.0	Int (VDD)	Serial, 2-wire	+5	2-wire interface, 8-pin SO	2.25
MAX519	8	V	6.0	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	2.35
MAX522	8	V	70.0	MDAC	Serial	+2.7 to +5.5	Low-power dual in 8-pin SO	2.25
MAX528	8	I	0.48	MDAC	µP/8	+5 to +15	Data latches for both DACs	3.79
MAX7628	8	I	0.35	MDAC	µP/8	+12 to +15	Data latches for both DACs	3.80
MAX532	12	V	4.0	MDAC	Serial	±12 to ±15	16-pin DIP/SO	8.45
MAX7837	12	V	4.0	Ext	µP/8	±12 to ±15	Dual V _{OUT} DAC with 8-bit data bus	12.18
MAX7847	12	V	4.0	Ext	µP/12	±12 to ±15	Dual V _{OUT} DAC with 12-bit data bus	12.18
MAX7537	12	I	1.5	MDAC	µP/8	+12 to +15	Dual DAC with 8-bit data bus	11.23
MAX7547	12	I	1.5	MDAC	µP/12	+12 to +15	Dual DAC with 12-bit data bus	11.40
MAX7549	12	I	1.5	MDAC	µP/4	+15	Dual DAC with 4-bit data bus	12.97
TRIPLE								
MAX512	8	V	60.0	MDAC	Serial	+5 or ±5	Low-power with shutdown, 14-pin narrow SO	2.58
MAX513	8	V	70.0	MDAC	Serial	+2.7 to ±3.6	MAX512 for 3V systems	2.58
QUAD								
MAX500	8	V	4.0	Ext	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MAX7225	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Double buffered, separate reference inputs	14.14
MAX7226	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Single buffered, single reference input	11.80
MAX505	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs, separate reference inputs	5.95
MAX506	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs, single reference input	6.10
MAX509	8	V	6.0	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	6.0	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX520	8	V	6.0	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	††
MAX526	12	V	3.0	Ext	µP/8	+12 to +15 & -5	Quad voltage-output DACs, available in DIP/SO	19.44
MAX527	12	V	3.0	Ext	µP/8	±5	±5V version of MAX526	16.56
MAX536	12	V	3.0	Ext	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	3.0	Ext	Serial	±5	Serial version of MAX527	15.95
MAX514	12	I	1.0	MDAC	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25
OCTAL								
MAX528	8	V	5.0	Ext	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	5.0	Ext	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MAX7228	8	V	5.0	Ext	µP/8	+5 to +15 & -5 or +15	Single or dual supplies	24.57
MAX521	8	V	6.0	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	4.95
MAX547	13	V	5.0	Ext	µP/13	±5	Unipolar or bipolar, 4 reference inputs	29.60

* V = voltage, I = current

** MDAC= 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Serial D/A Converters

Part Number	Resolution (Bits)	Output Type*	DACs in Package	Reference**	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up (\$)
MAX517	8	V	1	Ext	6.0	Serial, 2-wire	+5	2-wire interface	2.10
MAX518	8	V	2	Int (V _{DD})	6.0	Serial, 2-wire	+5	2-wire interface, 8-pin SO	2.25
MAX519	8	V	2	Ext	6.0	Serial, 2-wire	+5	2-wire interface, two reference inputs	2.35
MAX522	8	V	2	MDAC	6.0	Serial	+2.7 to +5.5	Low-power dual in 8-pin SO	2.25
MAX512	8	V	3	MDAC	60.0	Serial	+5 or ±5	Low-power with shutdown, 14-pin narrow SO	2.58
MAX513	8	V	3	MDAC	70.0	Serial	+2.7 to ±3.6	MAX512 for 3V systems	2.58
MAX500	8	V	4	Ext	4.0	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MAX509	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX520	8	V	4	Ext	6.0	Serial, 2-wire	+5	2-wire interface, four reference inputs	††
MAX521	8	V	8	Ext	6.0	Serial, 2-wire	+5	2-wire interface, five reference inputs	4.95
MAX528	8	V	8	Ext	5.0	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	8	Ext	5.0	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MAX504	10	V	1	Int/MDAC	25.0	Serial	+5 or ±5	Ultra-low power, rail-to-rail	2.80
MAX515	10	V	1	Ext	25.0	Serial	+5	Ultra-low power, 8-pin SO/DIP	2.50
MAX531	12	V	1	Int/MDAC	25.0	Serial	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX538	12	V	1	Ext	25.0	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	1	Ext	25.0	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MAX532	12	V	2	MDAC	4.0	Serial	±12 to ±15	16-pin DIP/SO	8.45
MAX536	12	V	4	Ext	3.0	Serial	+12 to +15 & -5	Serial version of MAX5326	15.95
MAX537	12	V	4	Ext	3.0	Serial	±5	Serial version of MAX5327	15.95
MAX543	12	I	1	MDAC	1.0	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	4.80
MAX7543	12	I	1	MDAC	2.0	Serial	+5	12-bit multiplying DAC	7.52
MAX514	12	I	4	MDAC	1.0	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

MAXIM

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

General Description

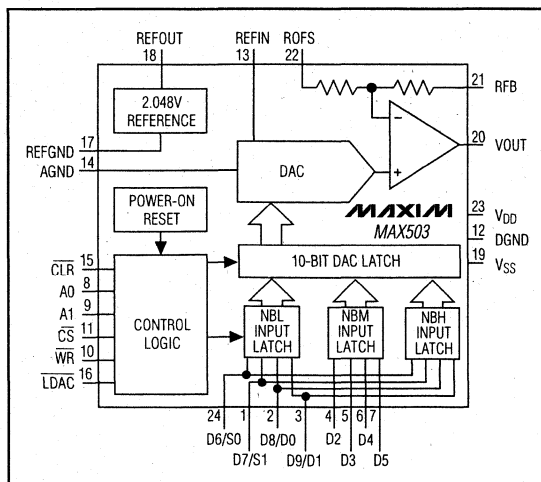
The MAX503 is a low-power, 10-bit, voltage-output digital-to-analog converter (DAC) that uses single 5V or dual $\pm 5V$ supplies. This device has an internal voltage reference plus an output buffer amplifier. Operating current is only 250 μA from a single 5V supply, making it ideal for portable and battery-powered applications. In addition, the shrink small-outline package (SSOP) measures only 0.1 square inches, using less board area than an 8-pin DIP. 10-bit resolution is achieved through laser trimming of the DAC, op amp, and reference. No further adjustments are necessary.

Internal gain-setting resistors can be used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V, or $\pm 2.048V$. Four-quadrant multiplication is possible without the use of external resistors or op amps. The parallel logic inputs are double buffered and are compatible with 4-bit, 8-bit, and 16-bit microprocessors. For a hardware and software compatible 12-bit upgrade, refer to the MAX530 data sheet. For DACs with similar features but with a serial data interface, refer to the MAX504/MAX515 data sheet.

Applications

Battery-Powered Data-Conversion Products
Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Microprocessor-Controlled Calibration

Functional Diagram



Features

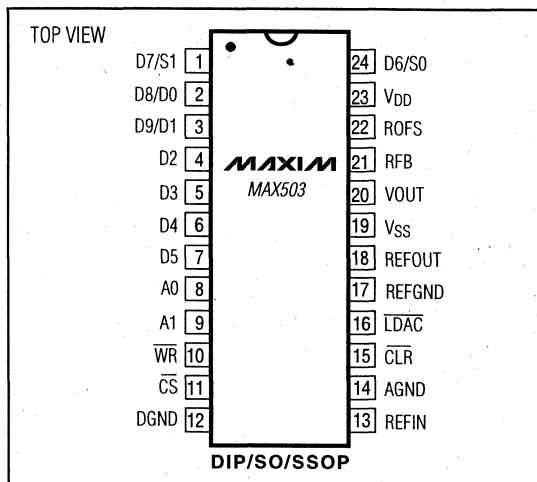
- ♦ Buffered Voltage Output
- ♦ Internal 2.048V Voltage Reference
- ♦ Operates from Single 5V or Dual $\pm 5V$ Supplies
- ♦ Low Power Consumption:
250 μA Operating Current
40 μA Shutdown-Mode Current
- ♦ SSOP Package Saves Space
- ♦ Relative Accuracy: $\pm 1/2$ LSB Max Over Temperature
- ♦ Guaranteed Monotonic Over Temperature
- ♦ 4-Quadrant Multiplication with No External Components
- ♦ Power-On Reset
- ♦ Double-Buffered Parallel Logic Inputs

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX503CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX503CWG	0°C to +70°C	24 Wide SO
MAX503CAG	0°C to +70°C	24 SSOP
MAX503ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX503EWG	-40°C to +85°C	24 Wide SO
MAX503EAG	-40°C to +85°C	24 SSOP

Refer to the MAX530 for military temperature or die equivalents.

Pin Configuration



5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND and V _{DD} to AGND	-0.3V, +6V
V _{SS} to DGND and V _{SS} to AGND	-6V, +0.3V
V _{DD} to V _{SS}	-0.3V, +12V
AGND to DGND	-0.3V, +0.3V
REFGND to AGND	-0.3V, (V _{DD} + 0.3V)
Digital Input Voltage to DGND	-0.3V, (V _{DD} + 0.3V)
REFIN	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
REFOUT	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
REFOUT to REFGND	-0.3V, (V _{DD} + 0.3V)
RFB	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
ROFS	(V _{SS} - 0.3V), (V _{DD} + 0.3V)

VOUT to AGND (Note 1)	V _{SS} , V _{DD}
Continuous Current, Any Input	±20mA
Continuous Power Dissipation (T _A = +70°C)	
Narrow Plastic DIP (derate 13.33mW/°C above +70°C)	1067mW
Wide SO (derate 11.76mW/°C above +70°C)	941mW
SSOP (derate 8.00mW/°C above +70°C)	640mW
Operating Temperature Ranges	
MAX503C_G	0°C to +70°C
MAX503E_G	-40°C to +85°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: The output may be shorted to V_{DD}, V_{SS}, DGND, or AGND if the continuous package power dissipation and current ratings are not exceeded. Typical short-circuit currents are 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = 5V, V_{SS} = 0V, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33μF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		10			Bits
Relative Accuracy	INL	(Note 2)			±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Offset Error	V _{OS}		0	0.25	3	LSB
Unipolar Offset Temperature Coefficient	TCV _{OS}			3		ppm/°C
Unipolar Offset-Error Supply Rejection	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
Gain Error (Note 2)	GE	DAC latch = all 1s, VOUT < V _{DD} - 0.4V (Note 2)			±1	LSB
Gain-Error Temperature Coefficient				1		ppm/°C
Gain-Error Power-Supply Rejection	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
DAC VOLTAGE OUTPUT (VOUT)						
Output Voltage Range			0		V _{DD} - 0.4	V
Resistive Load		VOUT = 2V, load regulation ≤ ±0.5LSB	2			kΩ
DC Output Impedance				0.2		Ω
Short-Circuit Current	I _{SC}			12		mA
REFERENCE INPUT (REFIN)						
Reference Input Range			0		V _{DD} - 2	V
Reference Input Resistance		Code dependent, minimum at code 0101...	40			kΩ
Reference Input Capacitance		Code dependent (Note 3)	10		50	pF
AC Feedthrough		(Note 4)		-80		dB

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

($V_{DD} = 5V$, $V_{SS} = 0V$, $AGND = DGND = REF_{GND} = 0V$, $REF_{IN} = 2.048V$ (external), $R_{FB} = ROFS = V_{OUT}$, $C_{REFOUT} = 33\mu F$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT)						
Reference Tolerance	VREFOUT	TA = +25°C	2.024	2.048	2.072	V
		MAX503C	2.015		2.081	
		MAX503E	2.011		2.085	
Reference Output Resistance	RREFOUT	(Note 5)			2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ VDD ≤ 5.5V		200		μV/V
Noise Voltage	en	0.1Hz to 10kHz		400		μVp-p
Temperature Coefficient				30		ppm/°C
Required External Capacitor	CREFOUT		3.3			μF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate		TA = +25°C	0.15	0.25		V/μs
Voltage Output Settling Time		To ±0.5LSB, VOUT = 2V		25		μs
Digital Feedthrough		WR = VDD, digital inputs all 1s to all 0s		5		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	Unity gain (Note 4)		68		dB
		Gain = 2 (Note 4)		68		
DIGITAL INPUTS (S0, S1, D0–D9, LDAC, CLR, CS, WR, A0, A1)						
Logic High Input	VIH		2.4			V
Logic Low Input	VIL				0.8	V
Digital Leakage Current		VIN = 0V or VDD			±1	μA
Digital Input Capacitance				8		pF
POWER SUPPLIES						
Positive Supply-Voltage Range	VDD		4.5		5.5	V
Positive Supply Current	IDD	Outputs unloaded, all digital inputs = 0V or VDD		250	400	μA
SWITCHING CHARACTERISTICS						
Address to WR Setup	tAWS		5			ns
Address to WR Hold	tAWH		5			ns
CS to WR Setup	tcWS		0			ns
CS to WR Hold	tcWH		0			ns
Data to WR Setup	tDS		45			ns
Data to WR Hold	tDH		0			ns
WR Pulse Width	tWR		45			ns
LDAC Pulse Width	tLDAC		45			ns
CLR Pulse Width	tCLR		45			ns
Internal Power-On Reset Pulse Width	tPOR	(Note 3)		1.3	10	μs

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

ELECTRICAL CHARACTERISTICS—Dual $\pm 5\text{V}$ Supplies

($V_{DD} = 5\text{V}$, $V_{SS} = -5\text{V}$, $AGND = DGND = REFGND = 0\text{V}$, $REFIN = 2.048\text{V}$ (external), $R_{FB} = R_{OFS} = V_{OUT}$, $C_{REFOUT} = 33\mu\text{F}$, $R_L = 10\text{k}\Omega$, $C_L = 100\text{pF}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		10			Bits
Relative Accuracy	INL				+0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			± 1	LSB
Bipolar Offset Error	V_{OS}				± 3	LSB
Bipolar Offset Temperature Coefficient	TCV_{OS}			3		ppm/ $^{\circ}\text{C}$
Bipolar Offset-Error Power-Supply Rejection	PSRR	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, $-5.5\text{V} \leq V_{SS} \leq -4.5\text{V}$		0.1		LSB/V
Gain Error					± 1	LSB
Gain-Error Temperature Coefficient	TC			1		ppm/ $^{\circ}\text{C}$
Gain-Error Power-Supply Rejection	PSRR	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, $-5.5\text{V} \leq V_{SS} \leq -4.5\text{V}$		0.1		LSB/V
DAC VOLTAGE OUTPUT (V_{OUT})						
Output Voltage Range			$V_{SS} + 0.4$	$V_{DD} - 0.4$		V
Resistive Load		$V_{OUT} = 2\text{V}$, load regulation $\leq \pm 0.5\text{LSB}$	2			$\text{k}\Omega$
DC Output Impedance				0.2		Ω
Short-Circuit Current	I_{SC}			20		mA
REFERENCE INPUT ($REFIN$)						
Reference Input Range			$V_{SS} + 2$	$V_{DD} - 2$		V
Reference Input Resistance		Code dependent, minimum at code 0101...	40			$\text{k}\Omega$
Reference Input Capacitance		Code dependent (Note 3)	10		50	pF
AC Feedthrough		(Note 4)		-80		dB
REFERENCE OUTPUT ($REFOUT$) —Specifications are identical to those under Single +5V Supply						
DYNAMIC PERFORMANCE —Specifications are identical to those under Single +5V Supply						
DIGITAL INPUTS ($S_0, S_1, D_0\text{--}D_9, LDAC, \overline{CLR}, CS, \overline{WR}, A_0, A_1$) —Specifications are identical to those under Single +5V Supply						
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Negative Supply Voltage	V_{SS}		-5.5		0	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}		250	400	μA
Negative Supply Current	I_{SS}	Outputs unloaded, all digital inputs = 0V or V_{DD}		150	200	μA
SWITCHING CHARACTERISTICS —Specifications are identical to those under Single +5V Supply						

Note 2: In single supply, INL and GE are calculated from code 3 to code 1023 (code excludes S_0 and S_1).

Note 3: Guaranteed by design.

Note 4: $REFIN = 1\text{kHz}$, 2.0Vp-p .

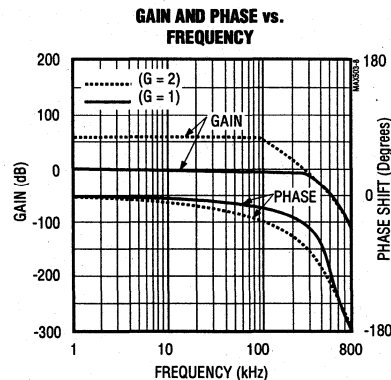
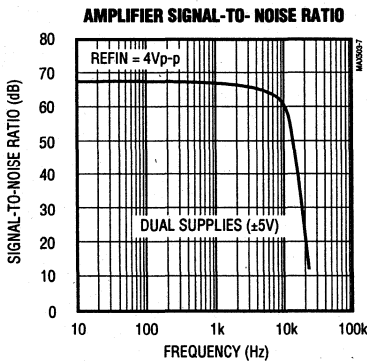
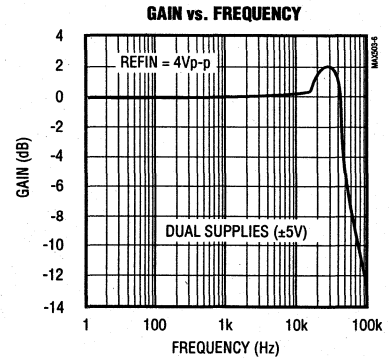
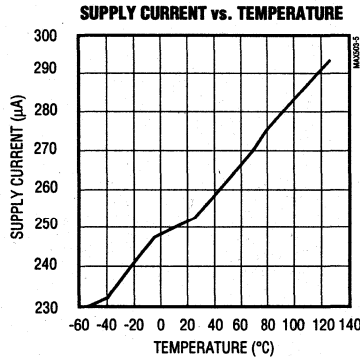
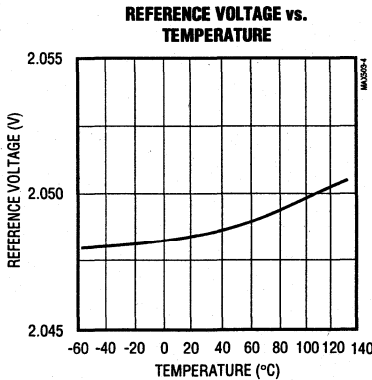
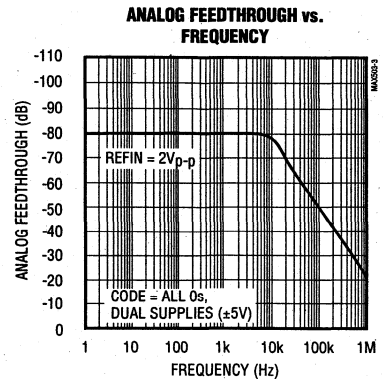
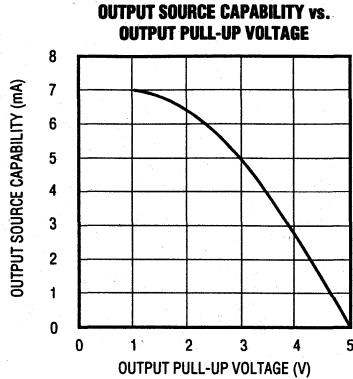
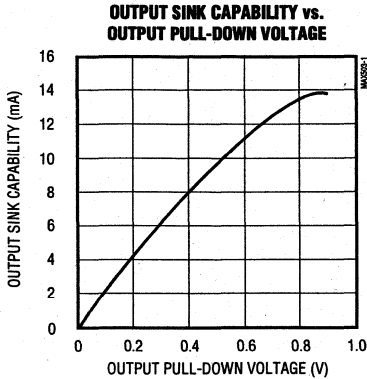
Note 5: Tested at $I_{OUT} = 100\mu\text{A}$. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Typical Operating Characteristics

(Single +5V supply, unity gain, code = all 1s, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX503

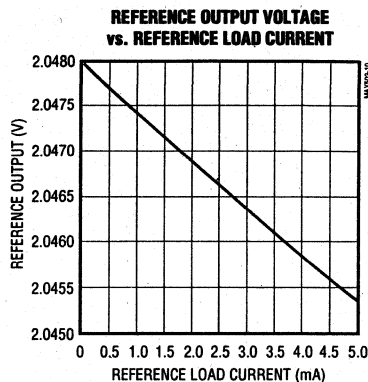
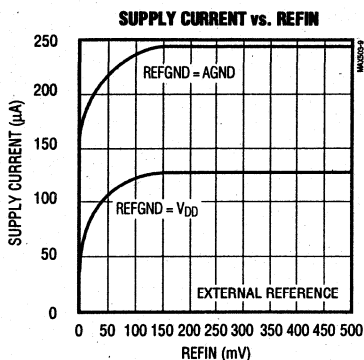


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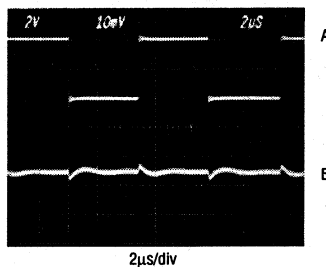
5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Typical Operating Characteristics (continued)

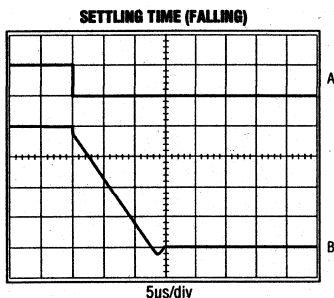
(Single +5V supply, unity gain, code = all 1s, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



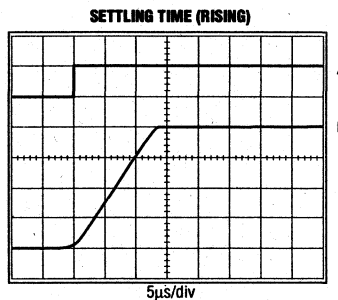
DIGITAL FEEDTHROUGH



A: S0, S1, D0-D9 = 100kHz, 4Vp-p
B: VOUT, 10mV/div
LDAC = CS = HIGH



A: DIGITAL INPUTS FALLING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY ($\pm 5\text{V}$)
LDAC = LOW
BIPOLEAR CONFIGURATION
 $V_{REFIN} = 2\text{V}$



A: DIGITAL INPUTS RISING EDGE,
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY ($\pm 5\text{V}$)
LDAC = LOW
BIPOLEAR CONFIGURATION
 $V_{REFIN} = 2\text{V}$

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Pin Description

MAX503

PIN	NAME	FUNCTION
1	D7/S1	D7 input when A0 = A1 = 1, or S1 input when A0 = 0 and A1 = 1. Always set S1 to 0.*
2	D8/D0	D8 input when A0 = A1 = 1, or D0 input when A0 = 0 and A1 = 1.*
3	D9/D1	D9 input when A0 = A1 = 1, or D1 input when A0 = 0 and A1 = 1.*
4	D2	D2 Input Data, or tie to S0 and multiplex when A0 = 1 and A1 = 0.*
5	D3	D3 Input Data, or tie to S1 and multiplex when A0 = 1 and A1 = 0.*
6	D4	D4 Input Data, or tie to D0 and multiplex when A0 = 1 and A1 = 0.*
7	D5	D5 Input Data, or tie to D1 and multiplex when A0 = 1 and A1 = 0.*
8	A0	Address Line A0. With A1, used to multiplex 4 of 12 data lines to load low (NBL), middle (NBM), and high (NBH) 4-bit nibbles. (12 bits can also be loaded as 8+4.)
9	A1	Address Line A1. Set A0 = A1 = 0 for NBL and NBM, A0 = 0 and A1 = 1 for NBL, A0 = 1 and A1 = 0 for NBM, or A0 = A1 = 1 for NBH. See Table 2 for complete input latch addressing.
10	$\overline{WR}$	Write Input (active low). Used with $\overline{CS}$ to load data into the input latch selected by A0 and A1.
11	$\overline{CS}$	Chip Select (active low). Enables addressing and writing to this chip from common bus lines.
12	DGND	Digital Ground
13	REFIN	Reference Input. Input for the R-2R DAC. Connect an external reference to this pin or a jumper to REFOUT (pin 18) to use the internal 2.048V reference.
14	AGND	Analog Ground
15	$\overline{CLR}$	Clear (active low). A low on $\overline{CLR}$ resets the DAC latches to all 0s.
16	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of the input latch to the DAC latch and updates VOUT.
17	REFGND	Reference Ground must be connected to AGND when using the internal reference. Connect to VDD to disable the internal reference and save power.
18	REFOUT	Reference Output. Output of the internal 2.048V reference. Tie to REFIN to drive the R-2R DAC.
19	VSS	Negative Power Supply. Usually ground for single-supply or -5V for dual-supply operation.
20	VOUT	Voltage Output. Op-amp buffered DAC output.
21	RFB	Feedback Pin. Op-amp feedback resistor. Always connect to VOUT.
22	ROFS	Offset Resistor Pin. Connect to VOUT for G = 1, to AGND for G = 2, or to REFIN for bipolar output.
23	VDD	Positive Power Supply (+5V)
24	D6/S0	D6 input when A0 = A1 = 1, or S0 input when A0 = 0 and A1 = 1. Always set S0 to 0.*

* This applies to 4 + 4 + 4 input loading mode. See Table 2 for 8 + 4 input loading mode.

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5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Detailed Description

The MAX503 consists of a parallel-input logic interface, a 10-bit R-2R ladder, a reference, and an op amp. The *Functional Diagram* shows the control lines and signal flow through the input data latch to the DAC latch, as well as the 2.048V reference and output op amp. Total supply current is typically 250 μ A with a single +5V supply. This circuit is ideal for battery-powered, microprocessor-controlled applications where high accuracy, no adjustments, and minimum component count are key requirements.

R-2R Ladder

The MAX503 uses an "inverted" R-2R ladder network with a BiCMOS op amp to convert 10-bit digital data to analog voltage levels. Figure 1 shows a simplified diagram of the R-2R DAC and op amp. Unlike a standard DAC, the MAX503 uses an "inverted" ladder network. Normally, the REFIN pin is the current output of a standard DAC and would be connected to the summing junction, or virtual ground, of an op amp. In this standard DAC configuration, however, the output voltage would be the inverse of

the reference voltage. The MAX503's topology makes the ladder output voltage the same polarity as the reference input, making the device suitable for single-supply operation. The BiCMOS op amp is then used to buffer, invert, or amplify the ladder signal.

Ladder resistors are nominally 80kΩ to conserve power and are laser trimmed for gain and linearity. The input impedance at REFIN is code dependent. When the DAC register is all 0s, all rungs of the ladder are grounded and REFIN is open or no load. Maximum loading (minimum REFIN impedance) occurs at code 010101.... Minimum reference input impedance at this code is guaranteed to be not less than 40kΩ.

The REFIN and REFOUT pins allow the user to choose between driving the R-2R ladder with the on-chip reference or an external reference. REFIN may be below analog ground when using dual supplies. See the *External Reference* and *Four-Quadrant Multiplication* sections for more information. •

Internal Reference

The on-chip reference is laser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typically, source current is 5mA and sink current is 100uA.

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50 μ A maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100 μ A to avoid gain errors.

A separate REFGND pin is provided to isolate reference currents from other analog and digital ground currents. To achieve specified noise performance, connect a 33 μ F capacitor from REFOUT to REFGND (see Figure 2). Using smaller capacitance values increases noise, and values less than 3.3 μ F may compromise the reference's stability. For applications requiring the lowest noise, insert a buffered RC filter between REFOUT and REFIN. When using the internal reference, REFGND must be connected to AGND. In applications not requiring the internal reference, connect REFGND to V_{DD}, which shuts down the reference. This saves typically 100 μ A of V_{DD} supply current and eliminates the need for CREFOUT.

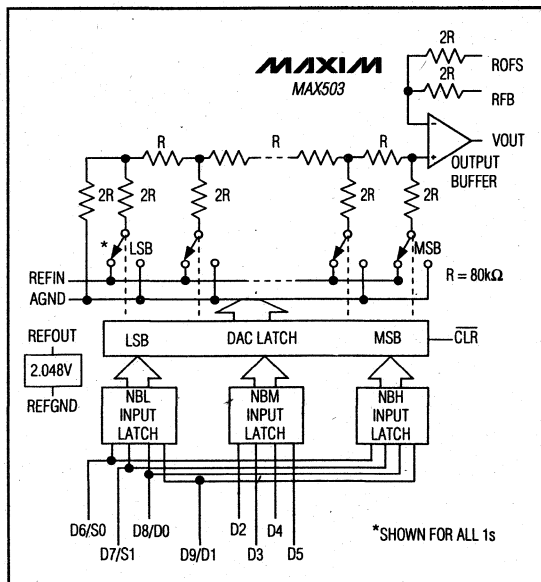


Figure 1. Simplified MAX503 DAC Circuit

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

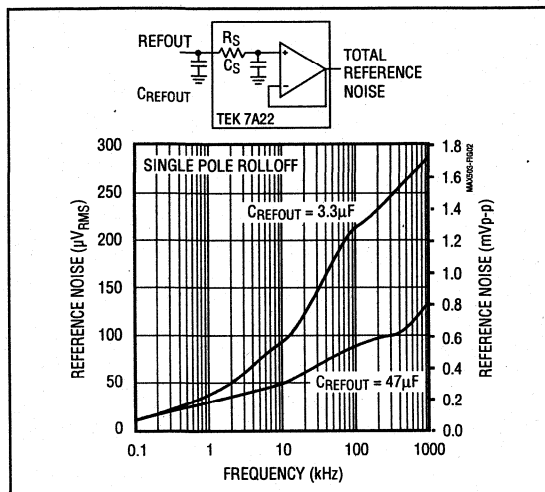


Figure 2. Reference Noise vs. Frequency

Output Buffer

The output amplifier uses a folded cascode input stage and a type AB output stage. Large output devices with low series resistance allow the output to swing to ground in single-supply operation. The output buffer is unity-gain stable. Input offset voltage and supply current are laser trimmed. Settling time is 25µs to 0.01% of final value. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF of load capacitance. The op amp may be placed in unity-gain ($G = 1$), in a gain of two ($G = 2$), or in a bipolar-output mode by using the ROFS and RFB pins. These pins are used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V or $\pm 2.048V$, by connecting ROFS to VOUT, GND, or REFIN. RFB is always connected to VOUT. Table 1 summarizes ROFS usage.

Table 1. ROFS Usage

ROFS CONNECTED TO:	DAC OUTPUT RANGE	OP-AMP GAIN
VOUT	0V to 2.048V	$G = 1$
AGND	0V to 4.096V	$G = 2$
REFIN	-2.048V to +2.048V	Bipolar

Note: Assumes RFB = VOUT and REFIN = REFOUT = 2.048V

External Reference

An external reference in the range ($V_{SS} + 2V$) to ($V_{DD} - 2V$) may be used with the MAX503 in dual-supply, unity-gain operation. In single-supply, unity-gain operation, the reference must be positive and may not exceed ($V_{DD} - 2V$). The reference voltage determines the DAC's full-scale output.

If an upgrade to the internal reference is required, the 2.5V MAX873A is ideal: $\pm 15mV$ initial accuracy, 7ppm/°C (max) temperature coefficient.

Power-On Reset

An internal power-on reset (POR) circuit forces the DAC register to reset to all 0s when V_{DD} is first applied. The POR pulse is typically 1.3µs; however, it may take 2ms for the internal reference to charge its large filter capacitor and settle to its trimmed value.

In addition to POR, a clear ($\overline{CLR}$) pin, when held low, sets the DAC register to all 0s. $\overline{CLR}$ operates asynchronously and independently from chip select ($\overline{CS}$). With the DAC input at all 0s, the op-amp output is at zero for unity-gain and $G = 2$ configurations, but it is at $-V_{REF}$ for the bipolar configuration.

Shutdown Mode

The MAX503 is designed for low power consumption. Understanding the circuit allows power consumption management for maximum efficiency. In single-supply mode ($V_{DD} = +5V$, $V_{SS} = GND$) the initial supply current is typically only 160µA, including the reference, op amp, and DAC. This low current occurs when the power-on reset circuit clears the DAC to all 0s and forces the op-amp output to zero (unipolar mode only). See the Supply Current vs. REFIN graph in the *Typical Operating Characteristics*. Under this condition, there is no internal load on the reference (DAC = all 0s, REFIN is open circuit) and the op amp operates at its minimum quiescent current. The $\overline{CLR}$ signal resets the MAX503 to these same conditions and can be used to control a power-saving mode when the DAC is not being used by the system.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

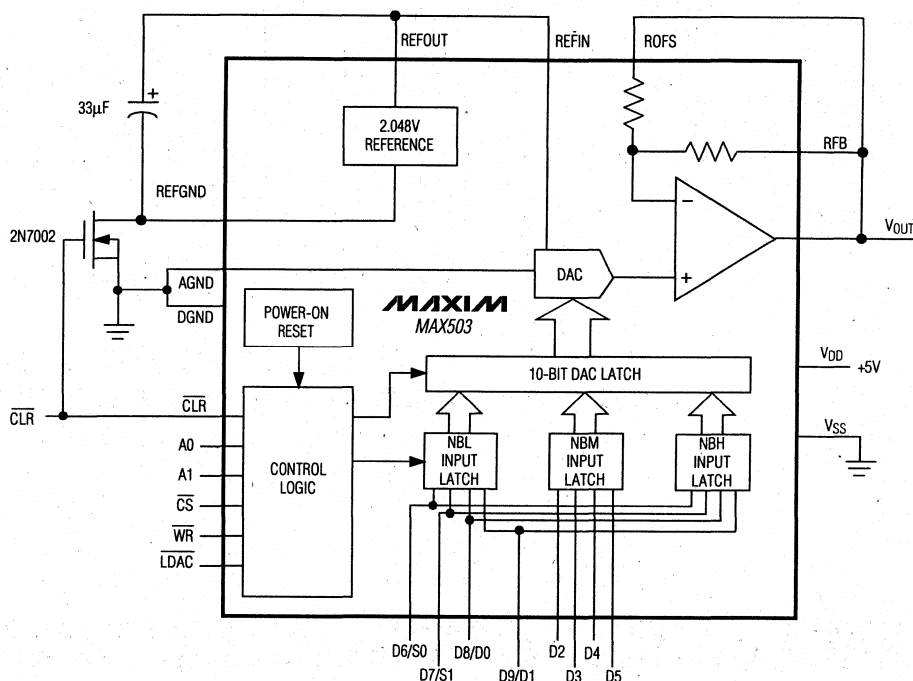


Figure 3. Low-Current Shutdown Mode

Table 2. Input Latch Addressing

CLR	CS	WR	LDAC	A0	A1	DATA UPDATED
L	X	X	X	X	X	Reset DAC latches
H	H	X	H	X	X	No operation
H	X	H	H	X	X	No operation
H	L	L	H	H	H	NBH (D6-D9)
H	L	L	H	H	L	NBM (D2-D5)
H	L	L	H	L	H	NBL (S0 = 0, S1 = 0, D0, D1)
H	H	H	L	X	X	Update DAC only
H	L	L	X	L	L	NBL and NBM (S0, S1, D0-D5), DAC not updated
H	L	L	L	H	H	NBH and update DAC

An additional 110µA of supply current can be saved when the internal reference is not used by connecting REFGND to V_{DD}. A low on-resistance N-channel FET, such as the 2N7002, can be used to turn off the internal reference to create a shutdown mode with minimum current drain (Figure 3). When $\overline{\text{CLR}}$ is high, the transistor pulls REFGND to AGND and the reference and DAC operate normally. When $\overline{\text{CLR}}$ goes low, REFGND is pulled up to V_{DD} and the reference is shut down. At the same time, $\overline{\text{CLR}}$ resets the DAC register to all 0s, and the op-amp output goes to 0V for unity-gain and G = 2 modes. This reduces the total single-supply operating current from 250µA (400µA max) to typically 40µA in shutdown mode.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

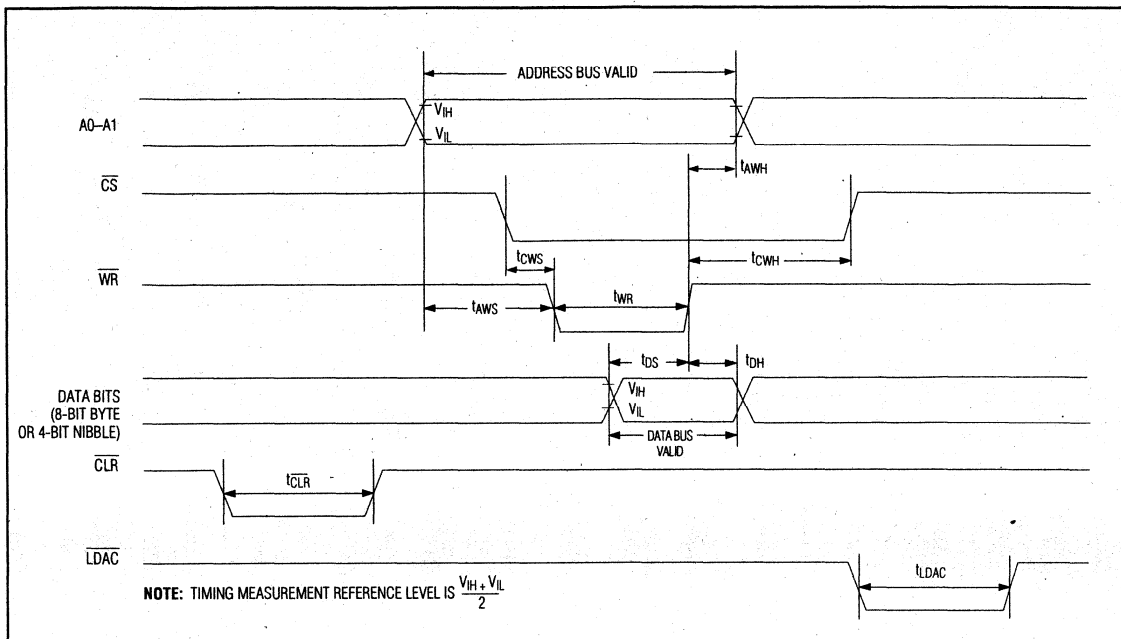


Figure 4. MAX503 Write-Cycle Timing Diagram

A small error voltage is added to the reference output by the reference current flowing through the N-channel pull-down transistor. The switch's on resistance should be less than 5Ω . A typical reference current of $100\mu A$ would add $0.5mV$ to REFOUT. Since the reference current and on resistance increase with temperature, the overall temperature coefficient will degrade slightly.

As data is loaded into the DAC and the output moves above GND, the op-amp quiescent current increases to its nominal value and the total operating current averages $250\mu A$. Using dual supplies ($\pm 5V$), the op amp is fully biased continuously, and the V_{DD} supply current is more constant at $250\mu A$. The V_{SS} current is typically $150\mu A$.

The MAX503 logic inputs are compatible with TTL and CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Parallel Logic Interface

In order to provide hardware and software compatibility with the 12-bit MAX530, the MAX503 employs a 12-bit digital interface. As shown in Figure 3, there is actually a 12-bit input latch, and therefore 12 bits of data should be written. The two least significant bits (S1 and S0) are sub-LSB, and must always be 0s. Designed to interface with 4-bit, 8-bit, and 16-bit microprocessors (μPs), the MAX503 uses 8 data pins and double-buffered logic inputs to load data as $4 + 4 + 4$ or $8 + 4$. The 12-bit DAC latch is updated simultaneously through the control signal LDAC. Signals A0, A1, WR, and CS select which input latches to update. The 12-bit data is broken down into nibbles (NB); NBL is the enable signal for the lowest 4 bits (S0, S1, D0, D1), NBM is the enable for the middle 4 bits, and NBH is the enable for the highest and most significant 4 bits. Table 2 lists the address decoding scheme.

Refer to Figure 4 for the MAX503 write-cycle timing diagram.

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5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

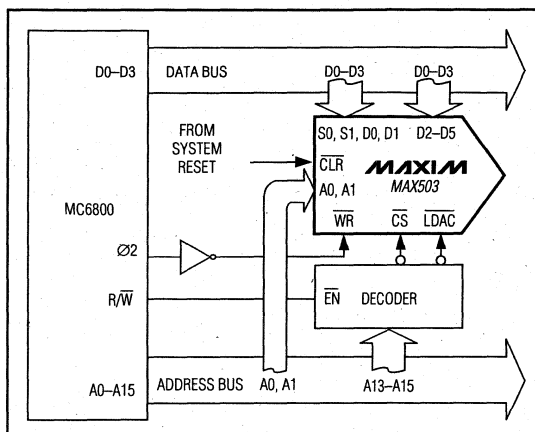


Figure 5. 4-Bit μ P Interface

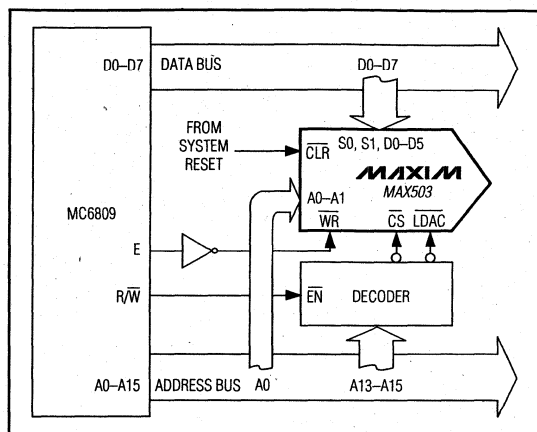


Figure 7. 8-Bit and 16-Bit μ P Interface

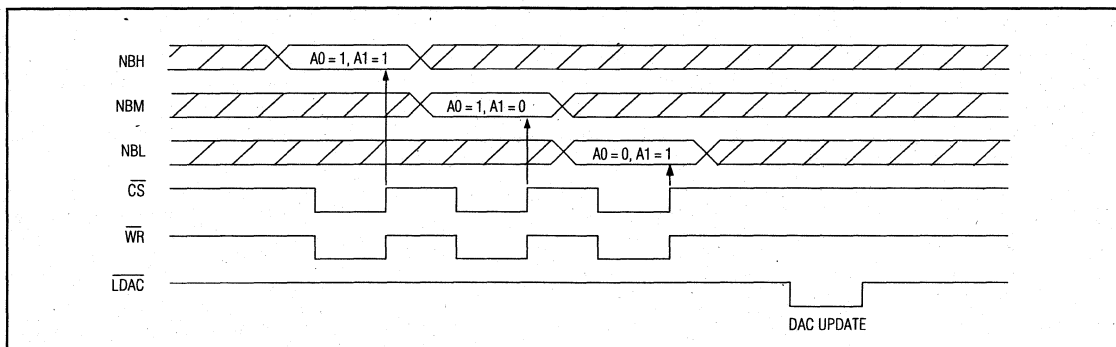


Figure 6. 4-Bit μ P Timing Sequence

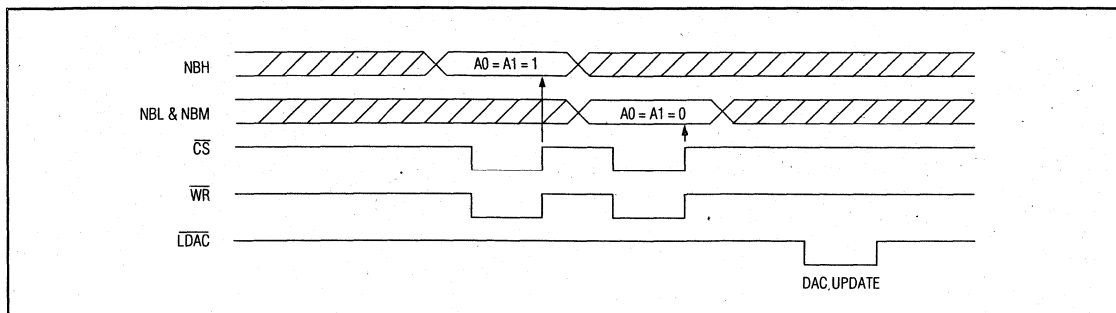


Figure 8a. 8-Bit and 16-Bit μ P Timing Sequence Using LDAC

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

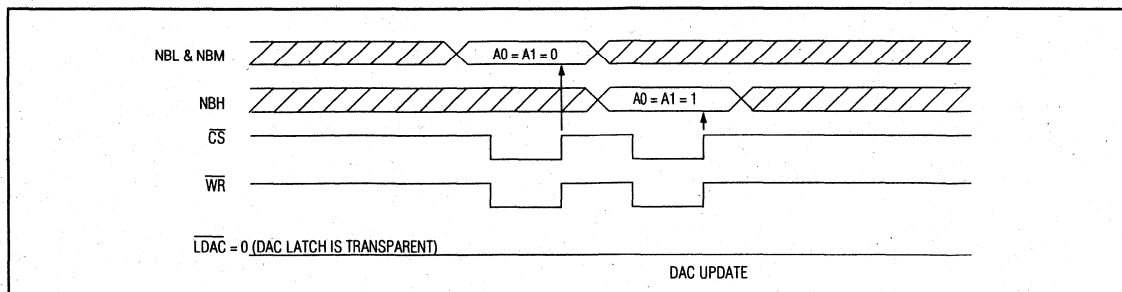


Figure 8b. 8-Bit and 16-Bit μ P Timing Sequence with $\overline{\text{LDAC}} = 0$

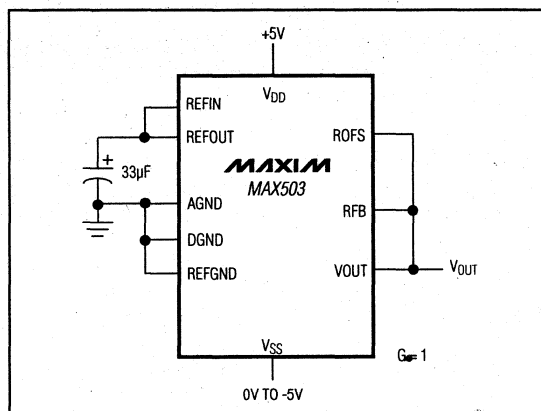


Figure 9. Unipolar Configuration (0V to +2.048V Output)

Figure 5 shows the circuit configuration for a 4-bit μ P application. Figure 6 shows the corresponding timing sequence. The 4 low bits (S0, S1, D0, D1) are connected in parallel to the other 4 bits (D2–D5) and then to the μ P bus. Address lines A0 and A1 enable the input data latches for the high, middle, or low data nibbles. The μ P sends chip select ($\overline{\text{CS}}$) and write ($\overline{\text{WR}}$) signals to latch in each of three nibbles in three cycles when the data is valid.

Figure 7 shows a typical interface to an 8-bit or a 16-bit μ P. Connect 8 data bits from the data bus to pins S0, S1, and D0–D5 on the MAX503. With $\overline{\text{LDAC}}$ held high, the user can load NBH or NBL + NBM in any order. Figure 8a shows the corresponding timing sequence. For fastest throughput, use Figure 8b's sequence. Address lines A0 and A1 are tied together and the DAC is loaded in 2 cycles as 8 + 4. In this scheme, with $\overline{\text{LDAC}}$ held low, the DAC latch is transparent. Always load NBL and NBM first, followed by NBH.

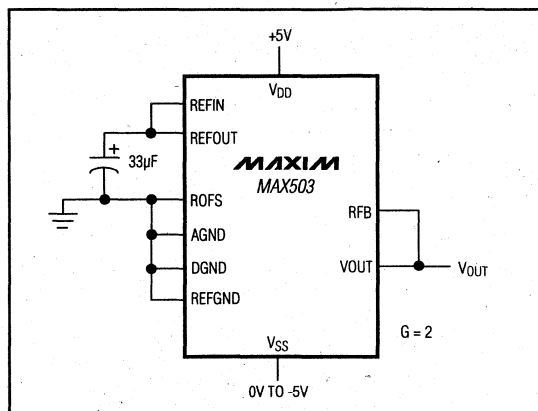


Figure 10. Unipolar Configuration (0V to +4.096V Output)

$\overline{\text{LDAC}}$ is asynchronous with respect to $\overline{\text{WR}}$. If $\overline{\text{LDAC}}$ is brought low before or at the same time $\overline{\text{WR}}$ goes high, $\overline{\text{LDAC}}$ must remain low for at least 50ns to ensure the correct data is latched. Data is latched into DAC registers on $\overline{\text{LDAC}}$'s rising edge.

Unipolar Configuration

The MAX503 is configured for a 0V to V_{REFIN} unipolar output range by connecting ROFS and RFB to VOUT (Figure 9). The converter operates from either single or dual supplies in this configuration. See Table 3 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, $1\text{LSB} = V_{\text{REFIN}}(2^{-10})$.

A 0V to $2V_{\text{REFIN}}$ unipolar output range is set up by connecting ROFS to AGND and RFB to VOUT (Figure 10). Table 4 shows the DAC-latch contents vs. VOUT. The MAX503 operates from either single or dual supplies in this mode. In this range, $1\text{LSB} = (2)(V_{\text{REFIN}})(2^{-10}) = (V_{\text{REFIN}})(2^{-9})$.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Table 3. Unipolar Binary Code Table
(0V to VREFIN Output), Gain = 1

INPUT*	OUTPUT
1111 1111 11(00)	$(V_{REFIN}) \frac{1023}{1024}$
1000 0000 01(00)	$(V_{REFIN}) \frac{513}{1024}$
1000 0000 00(00)	$(V_{REFIN}) \frac{512}{1024} = +V_{REFIN}/2$
0111 1111 11(00)	$(V_{REFIN}) \frac{511}{1024}$
0000 0000 01(00)	$(V_{REFIN}) \frac{1}{1024}$
0000 0000 00(00)	0V

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

Bipolar Configuration

A -VREFIN to +VREFIN bipolar range is set up by connecting ROFS to REFIN and RFB to VOUT, and operating from dual ($\pm 5V$) supplies (Figure 11). Table 5 shows the DAC-latch contents (input) vs. VOUT (output). In this range, 1LSB = VREFIN (2^{-9}).

Four-Quadrant Multiplication

The MAX503 can be used as a four-quadrant multiplier by connecting ROFS to REFIN and RFB to VOUT, and using (1) an offset binary digital code, (2) bipolar power supplies, and (3) a bipolar analog input at REFIN within the range $V_{SS} + 2V$ to $V_{DD} - 2V$, as shown in Figure 12.

In general, a 10-bit DAC's output is $D(V_{REFIN})(G)$, where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{10} or 1,024. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost because the number of steps is the same. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V ($G = 2$) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. The negative full scale is -VREFIN, while the positive full scale is +VREFIN - 1LSB.

Table 4. Unipolar Binary Code Table
(0V to 2VREFIN Output), Gain = 2

INPUT*	OUTPUT
1111 1111 11(00)	$+2 (V_{REFIN}) \frac{1023}{1024}$
1000 0000 01(00)	$+2 (V_{REFIN}) \frac{513}{1024}$
1000 0000 00(00)	$+2 (V_{REFIN}) \frac{512}{1024} = +V_{REFIN}$
0111 1111 11(00)	$+2 (V_{REFIN}) \frac{511}{1024}$
0000 0000 01(00)	$+2 (V_{REFIN}) \frac{1}{1024}$
0000 0000 00(00)	0V

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

Table 5. Bipolar (Offset Binary) Code Table
(-VREFIN to +VREFIN Output)

INPUT*	OUTPUT
1111 1111 11(00)	$(+V_{REFIN}) \frac{511}{512}$
1000 0000 01(00)	$(+V_{REFIN}) \frac{1}{512}$
1000 0000 00(00)	0V
0111 1111 11(00)	$(-V_{REFIN}) \frac{1}{512}$
0000 0000 01(00)	$(-V_{REFIN}) \frac{511}{512}$
0000 0000 00(00)	$(-V_{REFIN}) \frac{512}{512} = -V_{REFIN}$

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

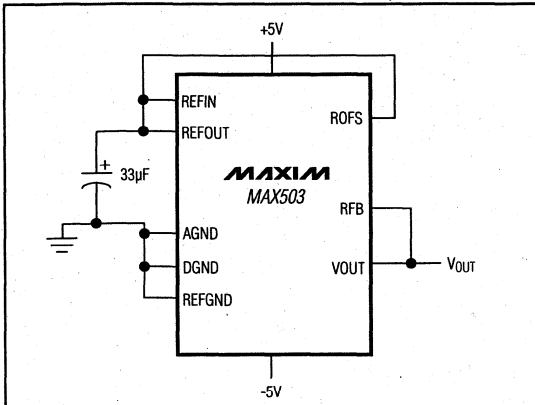


Figure 11. Bipolar Configuration (-2.048V to +2.048V Output)

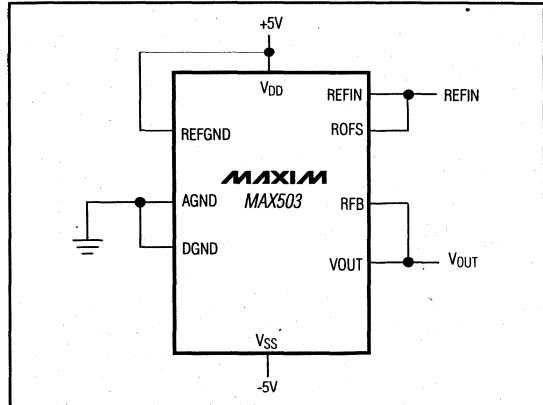


Figure 12. Four-Quadrant Multiplying Circuit

Applications Information

Single-Supply Linearity

As with any amplifier, the MAX503's output op amp offset can be positive or negative. When the offset is positive, it is easily accounted for. However, when the offset is negative, the output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive. The resulting transfer function is shown in Figure 13.

Normally, linearity is measured after allowing for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. In the MAX503, linearity and gain error are measured from code 3 to code 1023 (see Note 2 under *Electrical Characteristics*). The output amplifier offset does not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 1023.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

AGND and REFGND should be connected together, and then to DGND at the chip. For single-supply applications, connect VSS to AGND at the chip. The best

ground connection may be achieved by connecting the AGND, REFGND, and DGND pins together and connecting that point to the system analog ground plane. If DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass VDD (and VSS in dual-supply mode) with a 0.1µF ceramic capacitor connected between VDD and AGND (and between VSS and AGND). Mount the capacitors with short leads close to the device.

AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins may couple through the DAC package and cause internal stray capacitance to appear as noise at the DAC output, even though LDAC and CS are held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding LDAC and CS high and toggling the data inputs from all 1s to all 0s.

Analog Feedthrough

Because of internal stray capacitance, higher-frequency analog input signals at REFIN may couple to the output, even when the input digital code is all 0s, as shown in the *Typical Operating Characteristics* graph Analog Feedthrough vs. Frequency. It is tested by setting CLR to low (which sets the DAC latches to all 0s) and sweeping REFIN.

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5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

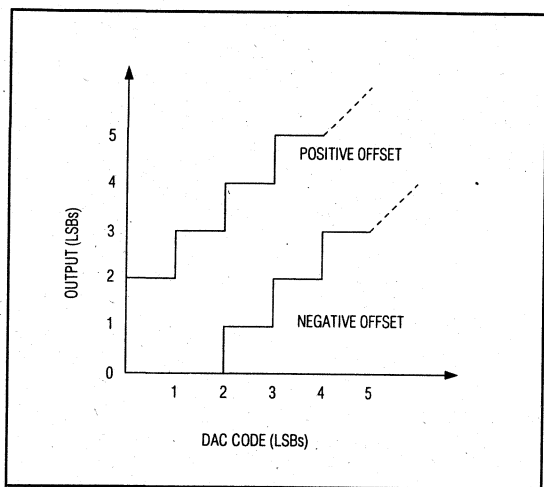


Figure 13. Single-Supply DAC Transfer Function

MAXIM

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

General Description

The MAX504/MAX515 are low-power, voltage-output, 10-bit digital-to-analog converters (DACs) specified for single +5V power-supply operation. The MAX504 can also be operated with $\pm 5\text{V}$ supplies. The MAX515 draws only $140\mu\text{A}$, and the MAX504 (with internal reference) draws only $260\mu\text{A}$. The MAX515 comes in 8-pin DIP and SO packages, while the MAX504 comes in 14-pin DIP and SO packages. Both parts have been trimmed for offset voltage, gain, and linearity, so no further adjustment is necessary.

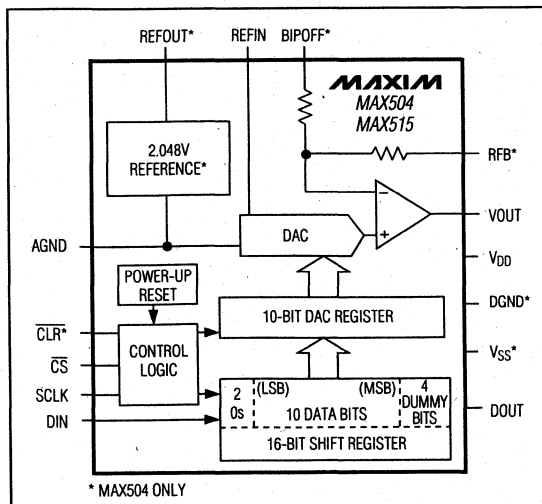
The MAX515's buffer is fixed at a gain of 2. The MAX504's internal op amp may be configured for a gain of 1 or 2, as well as for unipolar or bipolar output voltages. The MAX504 can also be used as a four-quadrant multiplier without external resistors or op amps.

For parallel data inputs, see the MAX503 data sheet.
For a hardware and software compatible 12-bit upgrade, refer to the MAX531/MAX538/MAX539 data sheet.

Applications

Battery-Powered Test Instruments
Digital Offset and Gain Adjustment
Battery-Operated/Remote Industrial Controls
Machine and Motion Control Devices
Cellular Telephones

Functional Diagram



Features

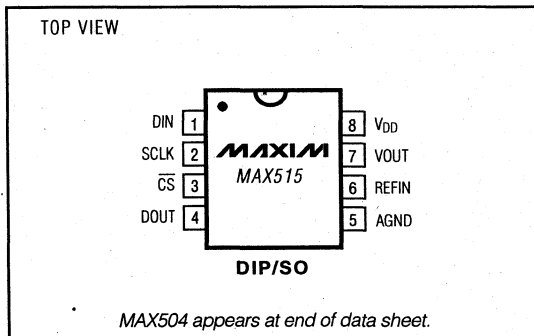
- ◆ Operate from Single +5V Supply
- ◆ Buffered Voltage Output
- ◆ Internal 2.048V Reference (MAX504)
- ◆ 140 μ A Supply Current (MAX515)
- ◆ INL = $\pm 1/2$ LSB (max)
- ◆ Guaranteed Monotonic Over Temperature
- ◆ Flexible Output Ranges:
 - 0V to V_{DD} (MAX504/MAX515)
 - V_{SS} to V_{DD} (MAX504)
- ◆ 8-Pin SO/DIP (MAX515)
- ◆ Power-On Reset
- ◆ Serial Data Output for Daisy-Chaining

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX504CPD	0°C to +70°C	14 Plastic DIP
MAX504CSD	0°C to +70°C	14 SO
MAX504EPD	-40°C to +85°C	14 Plastic DIP
MAX504ESD	-40°C to +85°C	14 SO
MAX515CPA	0°C to +70°C	8 Plastic DIP
MAX515CSA	0°C to +70°C	8 SO
MAX515EPA	-40°C to +85°C	8 Plastic DIP
MAX515ESA	-40°C to +85°C	8 SO

Refer to the MAX531/MAX538/MAX539 for military temperature or die equivalents.

Pin Configurations



5V, Low-Power, Voltage-Output Serial 10-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND and V _{DD} to AGND	-0.3V, +6V
V _{SS} to DGND and V _{SS} to AGND	-6V, +0.3V
V _{DD} to V _{SS}	-0.3V, +12V
AGND to DGND	-0.3V, +0.3V
Digital Input Voltage to DGND	-0.3V, (V _{DD} + 0.3V)
REFIN	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
REFOUT to AGND	-0.3V, (V _{DD} + 0.3V)
RFB	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
BIPOFF	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
V _{OUT} (Note 1)	V _{SS} , V _{DD}
Continuous Current, Any Pin	-20mA, +20mA

Continuous Power Dissipation (T _A = +70°C)	
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)	800mW
14-Pin SO (derate 8.33mW/°C above +70°C)	667mW
Operating Temperature Ranges	
MAX5_C_	0°C to +70°C
MAX5_E_	-40°C to +85°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: The output may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation limit is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = 5V, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = V_{OUT}
C_{REFOUT} = 33μF (MAX504), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		10			Bits
Relative Accuracy (Note 2)	INL				±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Offset Error	V _{OS}		0		3	LSB
Unipolar Offset Tempco	TCV _{OS}			3		ppm/°C
Unipolar Offset-Error Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
Gain Error (Note 2)	GE				±1	LSB
Gain-Error Tempco				1		ppm/°C
Gain-Error Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
VOLTAGE OUTPUT (V_{OUT})						
Output Voltage Range		MAX504 (G = 1)	0		V _{DD} - 2	V
		MAX504 (G = 2), MAX515	0		V _{DD} - 0.4	
Output Load Regulation		V _{OUT} = 2V, R _L = 2kΩ			0.5	LSB
Short-Circuit Current	I _{SC}			12		mA
REFERENCE INPUT (REFIN)						
Voltage Range			0		V _{DD} - 2	V
Input Resistance		Code dependent, minimum at code 0101...	40			kΩ
Input Capacitance		Code dependent (Note 3)	10		50	pF
AC Feedthrough		REFIN = 1kHz, 2Vp-p		-80		dB

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

MAX504/MAX515

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V_{DD} = 5V, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = V_{OUT} (MAX504), C_{REFOUT} = 33μF (MAX504), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT—MAX504 Only)						
Reference Output Voltage		T _A = +25°C	2.024	2.048	2.072	V
		MAX504C	2.015		2.081	
		MAX504E	2.011		2.085	
Temperature Coefficient	TCREFOUT			30		ppm/°C
Resistance	RREFOUT	(Note 4)		0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		200		μV/V
Noise Voltage	e _n	0.1Hz to 10kHz		400		μVp-p
Required External Capacitor	CREFOUT		3.3			μF
DIGITAL INPUTS (DIN, SCLK, CS, CLR)						
Input High	V _{IH}		2.4			V
Input Low	V _{IL}				0.8	V
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}			±1	μA
Input Capacitance	C _{IN}			8		pF
DIGITAL OUTPUT (DOUT)						
Output High	V _{OH}	I _{SOURCE} = 2mA	V _{DD} - 1			V
Output Low	V _{OL}	I _{SINK} = 2mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	T _A = +25°C	0.15	0.25		V/μs
Voltage-Output Settling Time		T _o ±1/2LSB, V _{OUT} = 2V		25		μs
Digital Feedthrough		CS = V _{DD} , DIN = 100kHz		5		nV-s
Signal-to-Noise Plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p (G = 1 or 2), code = 1111...		68		dB
POWER SUPPLY						
Positive Supply Voltage	V _{DD}		4.5		5.5	V
Power-Supply Current	I _{DD}	All inputs = 0V or V _{DD} , output = no load	MAX504	260	400	μA
			MAX515	140	300	
SWITCHING CHARACTERISTICS						
CS Setup Time	t _{CSS}		20			ns
SCLK Fall to CS Fall Hold Time	t _{CSH0}		15			ns
SCLK Fall to CS Rise Hold Time	t _{CSH1}		0			ns
SCLK High Width	t _{CH}		35			ns
SCLK Low Width	t _{CL}		35			ns
DIN Setup Time	t _{DS}		45			ns
DIN Hold Time	t _{DH}		0			ns
DOUT Valid Propagation Delay	t _{DO}	C _L = 50pF			80	ns
CS High Pulse Width	t _{CSW}		20			ns
CLR Pulse Width	t _{CLR}		25			ns
CS Rise to SCLK Rise Setup Time	t _{CS1}		50			ns

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

ELECTRICAL CHARACTERISTICS—Dual $\pm 5\text{V}$ Supplies (MAX504 Only)

($V_{DD} = 5\text{V}$, $V_{SS} = -5\text{V}$, $AGND = DGND = 0\text{V}$, $REFIN = 2.048\text{V}$ (external), $RFB = BIPOFF = V_{OUT}$, $C_{REFOUT} = 33\mu\text{F}$, $R_L = 10\text{k}\Omega$, $C_L = 100\text{pF}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N		10			Bits
Relative Accuracy	INL				± 0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			± 1	LSB
Bipolar Offset Error	V_{OS}	$BIPOFF = REFIN$			± 3	LSB
Bipolar Offset Tempco	TCV_{OS}	$BIPOFF = REFIN$		3		ppm/ $^{\circ}\text{C}$
Offset-Error Power-Supply Rejection Ratio	PSRR	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, $-5.5\text{V} \leq V_{SS} \leq -4.5\text{V}$		0.1		LSB/V
Gain Error (Unipolar or Bipolar)	GE				± 1	LSB
Gain-Error Tempco				1		ppm/ $^{\circ}\text{C}$
Gain-Error Power-Supply Rejection Ratio	PSRR	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, $-5.5\text{V} \leq V_{SS} \leq -4.5\text{V}$		0.1		LSB/V
REFERENCE INPUT (REFIN)						
Voltage Range			$V_{SS} + 2$		$V_{DD} - 2$	V
Input Resistance		Code dependent, minimum at code 0101...	40			k Ω
Input Capacitance		Code dependent (Note 3)	10		50	pF
AC Feedthrough		$REFIN = 1\text{kHz}$, 2.0V_{p-p}		-80		dB
REFERENCE OUTPUT (REFOUT—MAX504 Only)						
Reference Output Voltage		$T_A = +25^{\circ}\text{C}$	2.024	2.048	2.072	V
		MAX504C	2.015		2.081	
		MAX504E	2.011		2.085	
Temperature Coefficient	TC_{REFOUT}			30		ppm/ $^{\circ}\text{C}$
Resistance	R_{REFOUT}	(Note 4)		0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$		200		$\mu\text{V/V}$
Noise Voltage	e_n	0.1Hz to 10kHz		400		μV_{p-p}
Required External Capacitor	C_{REFOUT}		3.3			μF
DIGITAL INPUTS (DIN, SCLK, CS)						
Input High	V_{IH}		2.4			V
Input Low	V_{IL}				0.8	V
Input Current	I_{IN}	$V_{IN} = 0\text{V}$ or V_{DD}			± 1	μA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUT (DOUT)						
Output High	V_{OH}	$I_{SOURCE} = 2\text{mA}$	$V_{DD} - 1$			V
Output Low	V_{OL}	$I_{SINK} = 2\text{mA}$			0.4	V

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

MAX504/MAX515

ELECTRICAL CHARACTERISTICS—Dual $\pm 5\text{V}$ Supplies (MAX504 Only) (continued)

($V_{DD} = 5\text{V}$, $V_{SS} = -5\text{V}$, $AGND = DGND = 0\text{V}$, $REFIN = 2.048\text{V}$ (external), $RFB = BIPOFF = V_{OUT}$, $C_{REFOUT} = 33\mu\text{F}$, $R_L = 10\text{k}\Omega$, $C_L = 100\text{pF}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE OUTPUT (VOUT)						
Output Voltage Range		(G = 1)	VSS + 2		VDD - 2	V
		(G = 2)	VSS + 0.4		VDD - 0.4	
Output Load Regulation		VOUT = 2V, RL = 2kΩ			0.5	LSB
Short-Circuit Current	ISC			12		mA
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR		0.15	0.25		V/μs
Voltage-Output Settling Time		To ±1/2LSB, VOUT = 2V		16		μs
Digital Feedthrough		Step all 0s to all 1s		5		nV-s
Signal-to-Noise Plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p (G = 1)		68		dB
		REFIN = 1kHz, 2Vp-p (G = 2)		68		
POWER SUPPLY						
Positive Supply Voltage	VDD		4.5		5.5	V
Negative Supply Voltage	VSS		-5.5		0	V
Positive Supply Current	IDD	All inputs = 0V or VDD, no load		260	400	μA
Negative Supply Current	ISS	All inputs = 0V or VDD, no load		-120	-200	μA
SWITCHING CHARACTERISTICS						
CS Setup Time	tcSS		20			ns
SCLK Fall to CS Fall Hold Time	tCSH0		15			ns
SCLK Fall to CS Rise Hold Time	tCSH1		0			ns
SCLK High Width	tCH		35			ns
SCLK Low Width	tCL		35			ns
DIN Setup Time	tDS		45			ns
DIN Hold Time	tDH		0			ns
DOUT Valid Propagation Delay	tDO	CL = 50pF			80	ns
CS High Pulse Width	tCSW		20			ns
CLR Pulse Width	tCLR		25			ns
CS Rise to SCLK Rise Setup Time	tCS1		50			ns

Note 2: In single-supply operation, INL and GE calculated from Code 3 to Code 1023.

Note 3: Guaranteed by design.

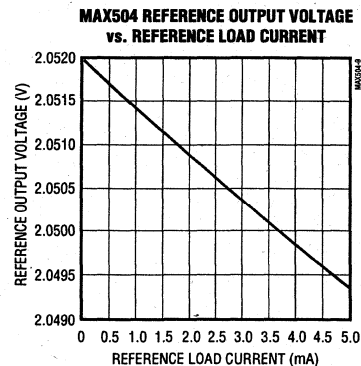
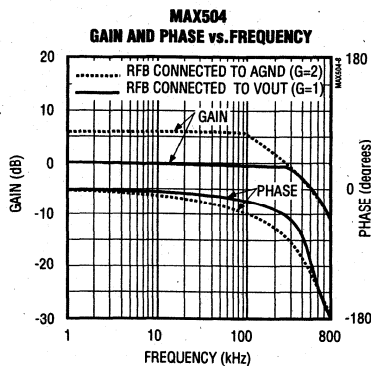
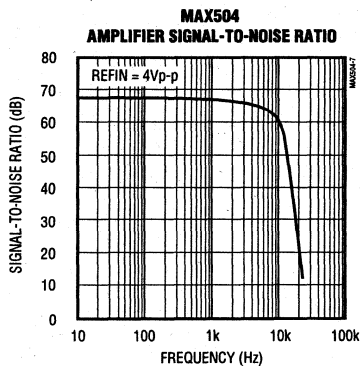
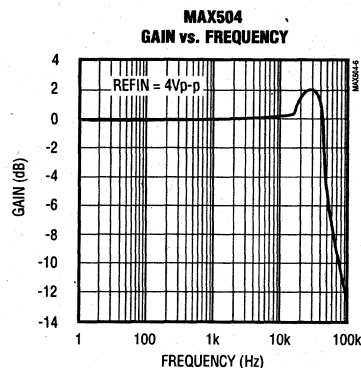
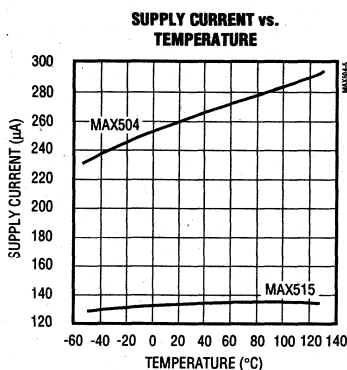
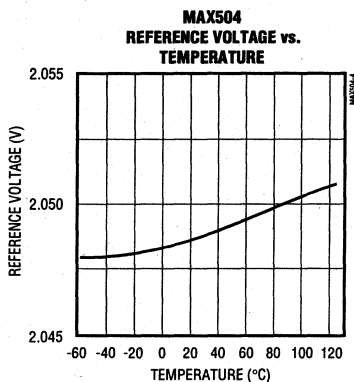
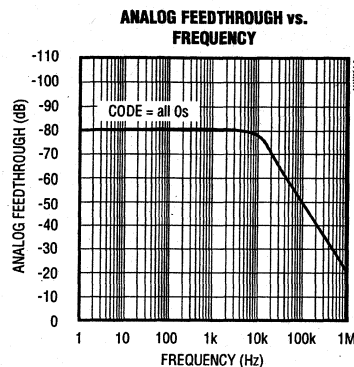
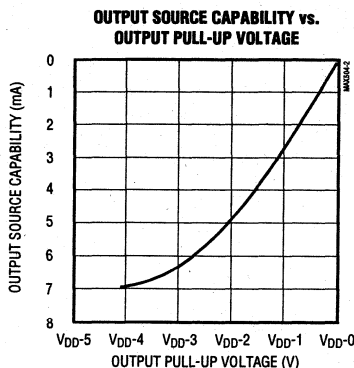
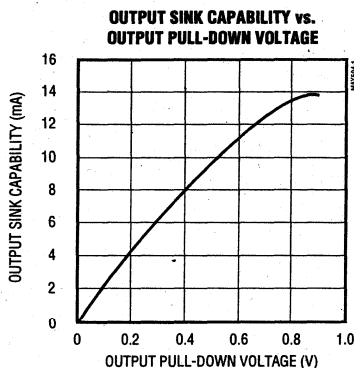
Note 4: Tested at $I_{OUT} = 100\mu\text{A}$. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

9

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

Typical Operating Characteristics

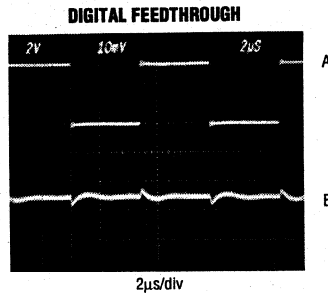
($V_{DD} = +5V$, $V_{REFIN} = 2.048V$, $T_A = +25^\circ C$, unless otherwise noted.)



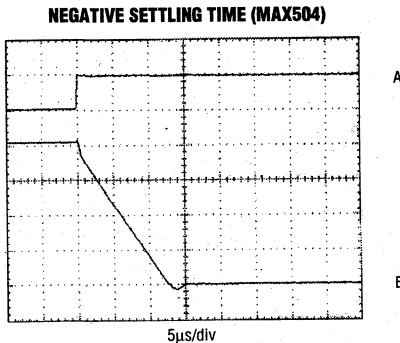
5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

Typical Operating Characteristics (continued)

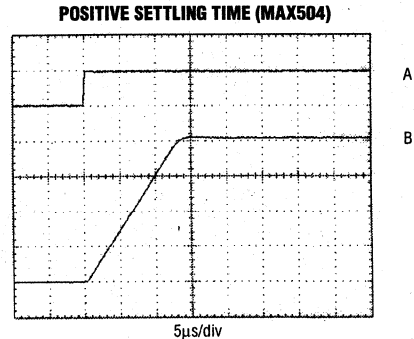
(VDD = +5V, VREFIN = 2.048V, TA = +25°C, unless otherwise noted.)



$\overline{CS}$ = HIGH
A: DIN = 4Vp-p, 100kHz
B: VOUT, 10mV/div



A: $\overline{CS}$ RISING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY $\pm 5V$
BIPOLAR CONFIGURATION
VREFIN = 2V



A: $\overline{CS}$ RISING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY $\pm 5V$
BIPOLAR CONFIGURATION
VREFIN = 2V

5V, Low-Power, Voltage-Output Serial 10-Bit DACs

Pin Description

PIN		NAME	FUNCTION
MAX504	MAX515		
1	—	BIPOFF	Bipolar offset/gain resistor
2	1	DIN	Serial data input
3	—	CLR	Clear. Asynchronously sets DAC register to all 0s.
4	2	SCLK	Serial clock input
5	3	CS	Chip select, active low
6	4	DOUT	Serial data output for daisy-chaining
7	—	DGND	Digital ground
8	5	AGND	Analog ground
9	6	REFIN	Reference input
10	—	REFOUT	Reference output, 2.048V. Connect to V _{DD} if not used.
11	—	VSS	Negative power supply
12	7	VOU	DAC output
13	8	VDD	Positive power supply
14	—	RFB	Feedback resistor

Detailed Description

General DAC Discussion

The MAX504/MAX515 use an "inverted" R-2R ladder network with a single-supply CMOS op amp to convert 10-bit digital data to analog voltage levels (see *Functional Diagram*). The term "inverted" describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX504/MAX515's topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to all 0s on power-up. Additionally, a clear (CLR) pin, when held low, sets the DAC register to all 0s. CLR operates asynchronously and independently from the chip select (CS) pin.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output, BiCMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 10-bit performance. Settling time is 25 μ s to 0.01% of final value. The output is short-circuit protected and can drive a 2k Ω load with more than 100pF load capacitance.

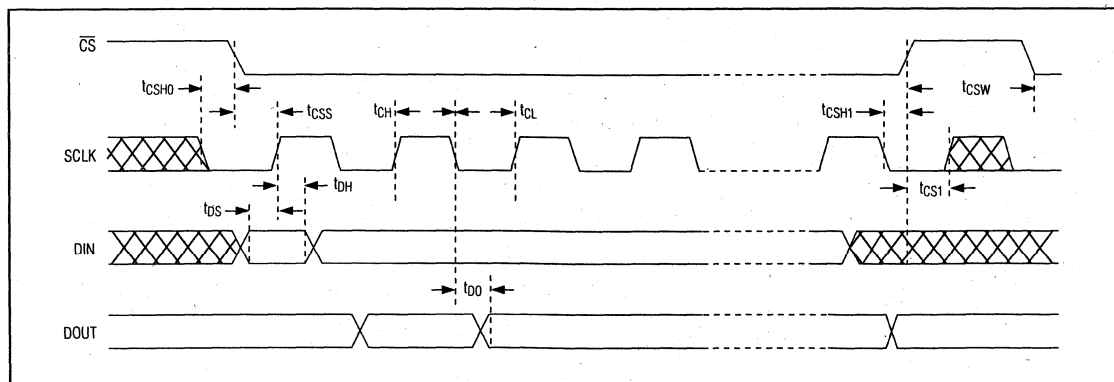


Figure 1. Timing Diagram

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

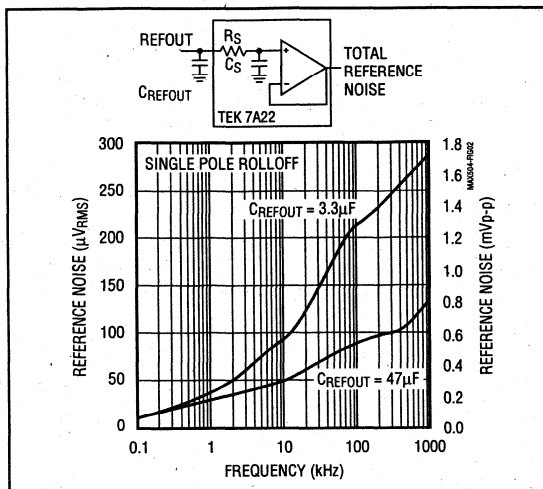


Figure 2. Reference Noise vs. Frequency

Internal Reference (MAX504 only)

The on-chip reference is laser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typically, source current is 5mA and sink current is 100µA.

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50µA maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100µA to avoid gain errors.

For applications requiring very low-noise performance, connect a 33µF capacitor from REFOUT to AGND. If noise is not a concern, a lower value (3.3µF min) capacitor may be used. To reduce noise further, insert a buffered RC filter between REFOUT and REFIN (Figure 2). The reference bypass capacitor CREFOUT is still required for reference stability. In applications not requiring the reference, connect REFOUT to VDD (to save power and to eliminate the need for CREFOUT) or use the MAX515 (no internal reference).

External Reference

An external reference in the range ($V_{SS} + 2V$) to ($V_{DD} - 2V$) may be used with the MAX504 in dual-supply operation. With the MAX515 or the MAX504 in single-supply use, the reference must be positive and may not exceed $V_{DD} - 2V$. The reference voltage determines the DAC's full-scale output. The DAC input resistance is code dependent and is

minimum (40kΩ) at code 0101... and virtually infinite at code 0000.... REFIN's input capacitance is also code dependent and has a 50pF maximum value at several codes.

If an upgrade to the internal reference is required, the 2.5V MAX873A is suitable: $\pm 15\text{mV}$ initial accuracy, $\text{TCV}_{\text{OUT}} = 7\text{ppm}/^\circ\text{C}$ (max).

Logic Interface

The MAX504/MAX515 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

Figure 1 shows the MAX504/MAX515 timing. The maximum serial clock rate is given by $1/(\text{t}_{\text{CH}} + \text{t}_{\text{CL}})$, approximately 14MHz. The digital update rate is limited by the chip-select period, which is $16 \times (\text{t}_{\text{CH}} + \text{t}_{\text{CL}}) + \text{t}_{\text{CSW}}$. This equals a 1.14µs, or 877kHz, update rate. However, the DAC settling time to 10 bits is 25µs, which may limit the update rate to 40kHz for full-scale step transitions.

Applications Information

Refer to Figures 3a and 3b for typical operating connections.

Serial Interface

The MAX504/MAX515 use a three-wire serial interface that is compatible with SPI™, QSPI™ (CPOL = CPHA = 0), and Microwire™ standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the *Functional Diagram*). 16 bits of serial data are clocked into the DAC in the following order: 4 fill (dummy) bits, 10 data bits, and 2 sub-LSB 0s. The 4 dummy bits are not normally needed, and are required **only** when DACs are daisy chained. The 2 sub-LSB 0s, however, are **always** needed, and allow hardware and software compatibility with the 12-bit MAX531/MAX538/MAX539. Transitions at $\overline{\text{CS}}$ should occur while SCLK is low. Data is clocked in on SCLK's rising edge while $\overline{\text{CS}}$ is low. The serial input data is held in a 16-bit serial shift register. On $\overline{\text{CS}}$'s rising edge, the 10 data-bits are transferred to the DAC register and update the DAC. With $\overline{\text{CS}}$ high, data cannot be clocked into the MAX504/MAX514.

The MAX504/MAX515 inputs data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The QSPI interface allows variable data input from 8 to 16 bits, and can be loaded into the DAC in one write cycle.

™ SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

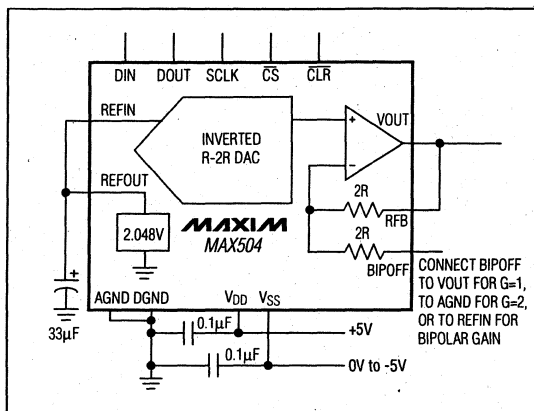


Figure 3a. MAX504 Typical Operating Circuit

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. DOUT does **not** go into a high-impedance state when $\overline{CS}$ is high. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

Any number of MAX504/MAX515 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that t_{CSS0} ($\overline{CS}$ low to SCLK high) is greater than $t_{DV} + t_{DS}$.

Unipolar Configuration

The MAX504 is configured for a gain of 1 (0V to V_{REFIN} unipolar output) by connecting BIPOFF and RFB to VOUT (Figure 6). The converter operates from either single or dual supplies in this configuration. See Table 1 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, $1\text{LSB} = V_{REFIN} (2^{-10})$, where V_{REF} is the voltage on REFIN.

A gain of 2 (0V to $2V_{REFIN}$ unipolar output) is set up by connecting BIPOFF to AGND and RFB to VOUT (Figure 7). Table 2 shows the DAC-latch contents vs. VOUT. The MAX504 operates from either single or dual supplies in this mode. In this range,

$$1\text{LSB} = (2)(V_{REFIN})(2^{-10}) = (V_{REFIN})(2^{-9}).$$

The MAX515 is internally configured for unipolar gain of 2 operation.

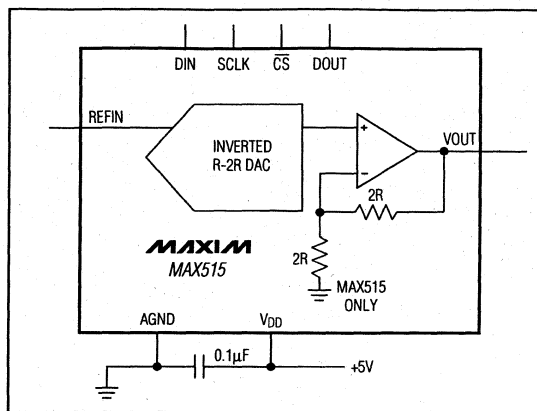


Figure 3b. MAX515 Typical Operating Circuit

Bipolar Configuration

A bipolar range is set up by connecting BIPOFF to REF and RFB to VOUT, and operating from dual ($\pm 5V$) supplies (Figure 8). Table 3 shows the DAC-latch contents (input) vs. VOUT (output). In this range, $1\text{LSB} = V_{REFIN} (2^{-9})$.

Four-Quadrant Multiplication

The MAX504 can be used as a four-quadrant multiplier by connecting BIPOFF to REF and RFB to VOUT, and using (1) an offset binary digital code, (2) bipolar power supplies, and (3) a bipolar analog input at REF within the range $V_{SS} + 2V$ to $V_{DD} - 2V$, as shown in Figure 9.

In general, a 10-bit DAC's output is $(D)(V_{REFIN})(G)$, where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{10} or 1,024. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost because the number of steps is the same. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V ($G = 2$) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. Negative full scale is $-V_{REFIN}$, while positive full scale is $+V_{REFIN} - 1\text{LSB}$.

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

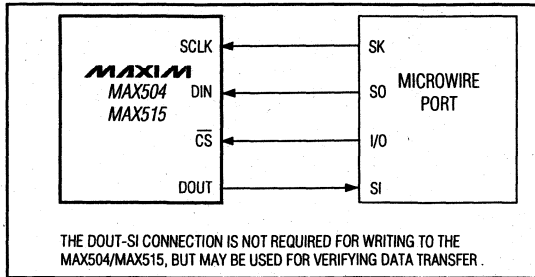


Figure 4. Microwire Connection

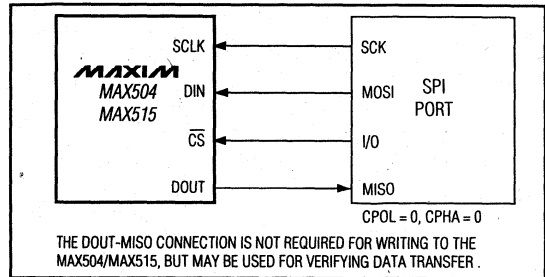


Figure 5. SPI/QSPI Connection

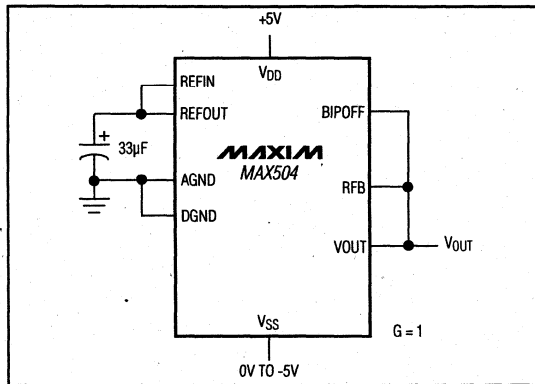


Figure 6. Unipolar Configuration (0V to +2.048V Output)

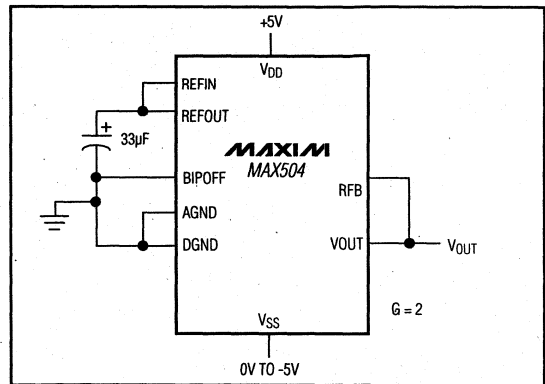


Figure 7. Unipolar Configuration (0V to +4.096V Output)

**Table 1. Unipolar Binary Code Table
(0V to VREFIN Output), Gain = 1**

INPUT*	OUTPUT
1111 1111 11(00)	(VREFIN) $\frac{1023}{1024}$
1000 0000 01(00)	(VREFIN) $\frac{513}{1024}$
1000 0000 00(00)	(VREFIN) $\frac{512}{1024} = +VREFIN/2$
0111 1111 11(00)	(VREFIN) $\frac{511}{1024}$
0000 0000 01(00)	(VREFIN) $\frac{1}{1024}$
0000 0000 00(00)	0V

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

**Table 2. Unipolar Binary Code Table
(0V to 2VREFIN Output), Gain = 2**

INPUT*	OUTPUT
1111 1111 11(00)	+2 (VREFIN) $\frac{1023}{1024}$
1000 0000 01(00)	+2 (VREFIN) $\frac{513}{1024}$
1000 0000 00(00)	+2 (VREFIN) $\frac{512}{1024} = +VREFIN$
0111 1111 11(00)	+2 (VREFIN) $\frac{511}{1024}$
0000 0000 01(00)	+2 (VREFIN) $\frac{1}{1024}$
0000 0000 00(00)	0V

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

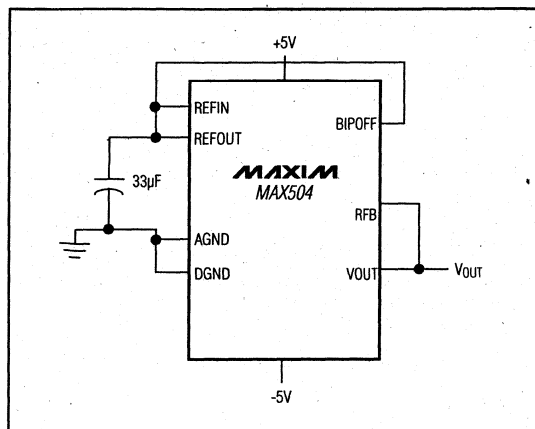


Figure 8. Bipolar Configuration (-2.048V to +2.048V Output)

Single-Supply Linearity

As with any amplifier, the MAX504/MAX515's output buffer offset can be positive or negative. When the offset is positive, it is easily accounted for (Figure 10). However, when the offset is negative, the buffer output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive.

Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinearity near-zero output when operating with a single supply. To account for this nonlinearity in the MAX504/MAX515, linearity and gain error are measured from code 3 to code 1023. The output buffer's offset and nonlinearity do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 1023.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

Table 3. Bipolar (Offset Binary) Code Table (-VREFIN to +VREFIN Output)

INPUT*			OUTPUT
1111	1111	11(00)	$(+V_{REFIN}) \frac{511}{512}$
1000	0000	01(00)	$(+V_{REFIN}) \frac{1}{512}$
1000	0000	00(00)	0V
0111	1111	11(00)	$(-V_{REFIN}) \frac{1}{512}$
0000	0000	01(00)	$(-V_{REFIN}) \frac{511}{512}$
0000	0000	00(00)	$(-V_{REFIN}) \frac{512}{512} = -V_{REFIN}$

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

DGND and AGND should be connected together at the chip. For the MAX504 in single-supply applications, connect VSS to AGND at the chip. The best ground connection may be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass VDD (and VSS in dual-supply mode) with a 0.1µF ceramic capacitor connected between VDD and AGND (and between VSS and AGND). Mount it with short leads close to the device. Ferrite beads may also be used to further isolate the analog and digital power supplies.

Figures 11a and 11b illustrate the grounding and bypassing scheme described.

Saving Power

When the DAC is not being used by the system, minimize power consumption by setting the appropriate code to minimize load current. For example, in bipolar mode, with a resistive load to ground, set the DAC code to mid-scale (see Table 3). If there is no output load, minimize internal loading on the reference by setting the DAC to all 0s (on the MAX504, use CLR). Under this condition, REFIN is high impedance and the op amp operates at its minimum quiescent current.

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

MAX504/MAX515

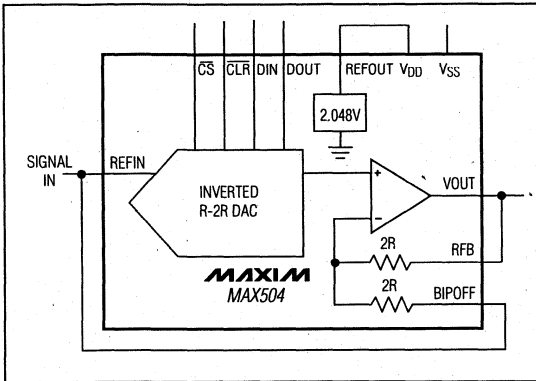


Figure 9. MAX504 Connected as Four-Quadrant Multiplier. The unused REFOUT is connected to V_{DD} .

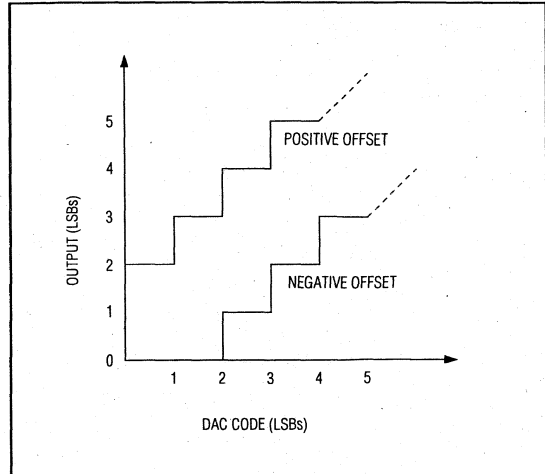


Figure 10. Single-Supply Offset

AC Considerations

Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package and cause internal stray capacitance to appear at the DAC output as noise, even though $\overline{CS}$ is held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding $\overline{CS}$ high transmitting 0101... from DIN to DOUT.

Analog Feedthrough

Because of internal stray capacitance, higher frequency analog input signals may couple to the output as shown in the Analog Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. It is tested by holding $\overline{CS}$ high, setting the DAC code to all 0s, and sweeping REFIN.

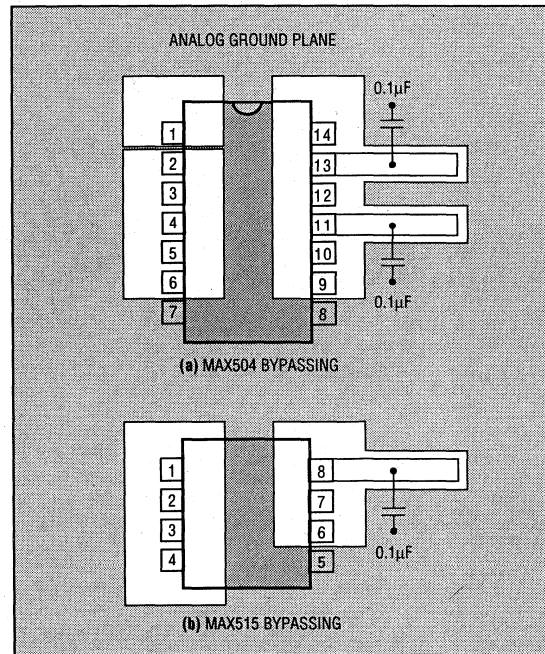
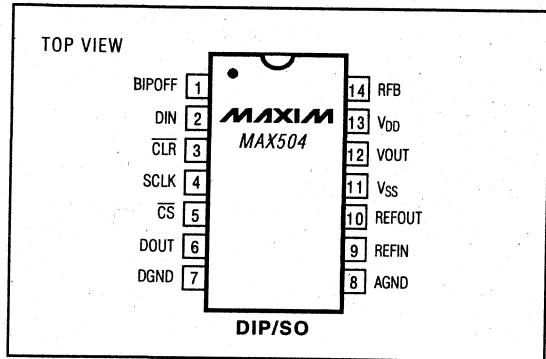


Figure 11. Power-Supply Bypassing

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

Pin Configurations (continued)



MAX517/MAX518/MAX519

Features

- ◆ Single +5V Supply
- ◆ Simple 2-Wire Serial Interface
- ◆ I²C Compatible
- ◆ Output Buffer Amplifiers Swing Rail-to-Rail
- ◆ Space-Saving 8-pin DIP/SO Packages (MAX517/MAX518)
- ◆ Reference Input Range Includes Both Supply Rails (MAX517/MAX519)
- ◆ Power-On Reset Clears All Latches
- ◆ 4μA Power-Down Mode

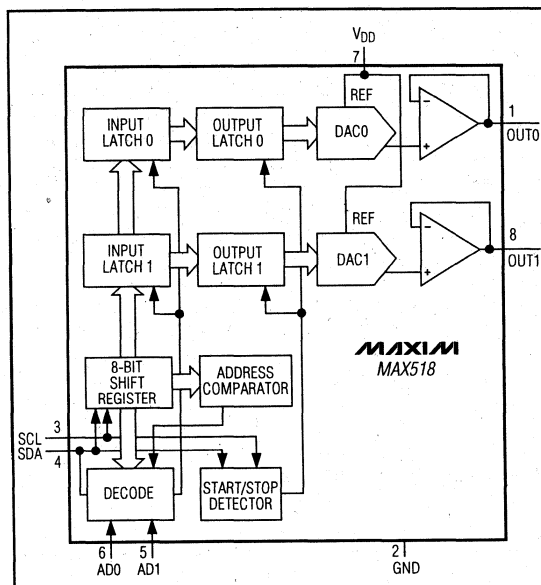
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX517ACPA	0°C to +70°C	8 Plastic DIP	1
MAX517BCPA	0°C to +70°C	8 Plastic DIP	1.5
MAX517ACSA	0°C to +70°C	8 SO	1
MAX517BCSA	0°C to +70°C	8 SO	1.5
MAX517BC/D	0°C to +70°C	Dice*	1.5

****Contact factory for availability and processing to MIL-STD-883.**

Functional Diagram

Pin Configurations



2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V to +6V
OUT ₋	-0.3V to (V _{DD} + 0.3V)
REF ₋ (MAX517, MAX519)	-0.3V to (V _{DD} + 0.3V)
AD ₋	-0.3V to (V _{DD} + 0.3V)
SCL, SDA to GND	-0.3V to +6V
Maximum Current into Any Pin	50mA
Continuous Power Dissipation (T _A = +70°C)	
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	...727mW
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C)	640mW

16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)	..842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)	...696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C)	800mW
Operating Temperature Ranges	
MAX51_C_	0°C to +70°C
MAX51_E_	-40°C to +85°C
MAX51_MJB	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, V_{REF-} = 4V (MAX517, MAX519), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error (Note 1)	TUE		MAX51_A	±1			LSB
			MAX51_B	±1.5			
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic			±1		LSB
Zero-Code Error	ZCE	Code = 00 hex	MAX51_C	18			mV
			MAX51_E	20			
			MAX51_BM	20			
Zero-Code-Error Supply Rejection		Code = 00 hex	MAX51_C	±1			mV
			MAX51_E	±1			
			MAX51_BM	±1			
Zero-Code-Error Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex, MAX518 unloaded	MAX51_C	±18			mV
			MAX51_E	±20			
			MAX51_BM	±20			
Full-Scale-Error Supply Rejection		MAX517, MAX519	MAX51_C	±1			mV
		Code = FF hex	MAX51_E	±1			
		VDD = +5V ±10%	MAX51_BM	±1			
Full-Scale-Error Temperature Coefficient		Code = FF hex			±10		µV/°C

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

MAX517/MAX518/MAX519

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±10%, V_{REF} = 4V (MAX517, MAX519), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUTS (MAX517, MAX519)						
Input Voltage Range			0		V _{DD}	V
Input Resistance	R _{IN}	Code = 55 hex (Note 2)	16	24		kΩ
Input Current		Power-down mode			±10	μA
Input Capacitance		Code = FF hex (Note 3)		30		pF
Channel-to-Channel Isolation (MAX519)		(Note 4)		-60		dB
AC Feedthrough		(Note 5)		-70		dB
DAC OUTPUTS						
Full-Scale Output Voltage			0		V _{DD}	V
Output Load Regulation		OUT ₋ = 4V, 0mA to 2.5mA		0.25		LSB
		MAX51 ₋ C/E, REF ₋ = V _{DD} (MAX517, MAX519), code = FF hex, 0μA to 500μA		1.5		
		MAX51 ₋ M, REF ₋ = V _{DD} (MAX517, MAX519), code = FF hex, 0μA to 500μA		2.0		
Output Leakage Current		OUT ₋ = 0V to V _{DD} , power-down mode			±10	μA
DIGITAL INPUTS SCL, SDA						
Input High Voltage	V _{IH}		0.7V _{DD}			V
Input Low Voltage	V _{IL}			0.3V _{DD}		V
Input Leakage Current	I _{IN}	0V ≤ V _{IN} ≤ V _{DD}			±10	μA
Input Hysteresis	V _{HYST}		0.05V _{DD}			V
Input Capacitance	C _{IN}	(Note 6)			10	pF
DIGITAL INPUTS AD0, AD1, AD2, AD3						
Input High Voltage	V _{IH}		2.4			V
Input Low Voltage	V _{IL}			0.8		V
Input Leakage Current	I _{IN}	V _{IN} = 0V to V _{DD}			±10	μA
DIGITAL OUTPUT SDA (Note 7)						
Output Low Voltage	V _{OL}	I _{SINK} = 3mA			0.4	V
		I _{SINK} = 6mA			0.6	
Three-State Leakage Current	I _L	V _{IN} = 0V to V _{DD}			±10	μA
Three-State Output Capacitance	C _{OUT}	(Note 6)			10	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate		Positive and negative	MAX51 ₋ C	2.0		V/μs
			MAX51 ₋ E	1.4		
			MAX51 ₋ M	1.0		
Output Settling Time		To 1/2 LSB, 10kΩ and 100pF load (Note 8)		6		μs
Digital Feedthrough		Code = 00 hex, all digital inputs from 0V to V _{DD}		5		nV-s

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 10\%$, $V_{REF-} = 4V$ (MAX517, MAX519), $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital-Analog Glitch Impulse		Code 128 to 127		12		nV-s
Signal to Noise + Distortion Ratio (MAX517, MAX519)	SINAD	$V_{REF-} = 4Vp-p$ at 1kHz, $V_{DD} = 5V$, Code = FF hex		87		dB
Multiplying Bandwidth (MAX517, MAX519)		$V_{REF-} = 4Vp-p$, 3dB bandwidth		1		MHz
Wideband Amplifier Noise				60		μV_{RMS}
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	Normal mode, output(s) unloaded, all digital inputs at 0V or V_{DD}	MAX517C	1.5	3.0	mA
			MAX517E/M	1.5	3.5	
			MAX518C, MAX519C	2.5	5	
			MAX518E/M, MAX519E/M	2.5	6	
		Power-down mode		4	20	μA

TIMING CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	fSCL		0		400	kHz
Bus Free Time Between a STOP and a START Condition	tBUF		1.3			μs
Hold Time, (Repeated) Start Condition	tHD, STA		0.6			μs
Low Period of the SCL Clock	tLOW		1.3			μs
High Period of the SCL Clock	tHIGH		0.6			μs
Setup Time for a Repeated START Condition	tSU, STA		0.6			μs
Data Hold Time	tHD, DAT	(Note 9)	0		0.9	μs
Data Setup Time	tSU, DAT		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	tR	(Note 10)	$20 + 0.1C_b$		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	tF	(Note 10)	$20 + 0.1C_b$		300	ns
Fall Time of SDA Transmitting (Note 7)	tF	$I_{SINK} \leq 6mA$ (Note 10)	$20 + 0.1C_b$		250	ns
Setup Time for STOP Condition	tSU, STO		0.6			μs
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spike Suppressed	tSP	(Notes 6, 11)	0		50	ns

Note 1: For the MAX518 (full-scale = V_{DD}) the last three codes are excluded from the TUE and DNL specifications, due to the limited output swing when loaded with $10k\Omega$ to GND.

Note 2: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.

Note 3: Input capacitance is code dependent. The highest input capacitance occurs at code FF hex.

Note 4: $V_{REF-} = 4Vp-p$, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.

Note 5: $V_{REF-} = 4Vp-p$, 10kHz, DAC code = 00 hex.

Note 6: Guaranteed by design.

Note 7: I^2C compatible mode.

Note 8: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

Note 9: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

Note 10: C_b = total capacitance of one bus line in pF. t_R and t_F measured between $0.3V_{DD}$ and $0.7V_{DD}$.

Note 11: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

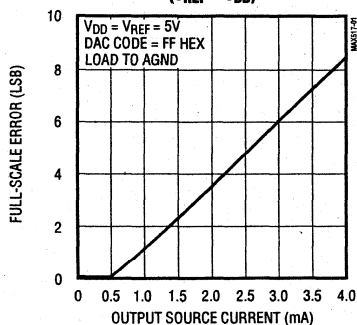
2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Typical Operating Characteristics

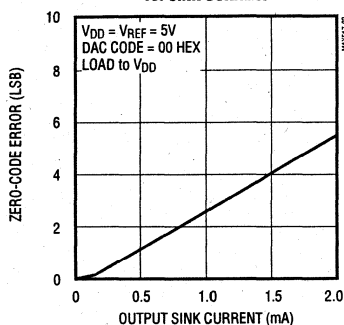
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX517/MAX518/MAX519

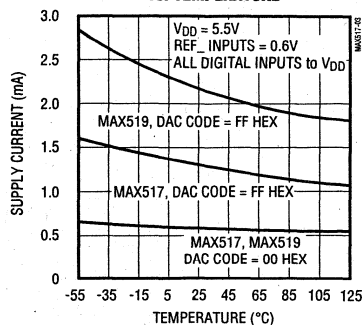
FULL-SCALE ERROR vs. SOURCE CURRENT
($V_{REF} = V_{DD}$)



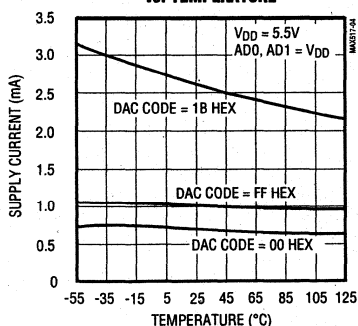
ZERO-CODE ERROR vs. SINK CURRENT



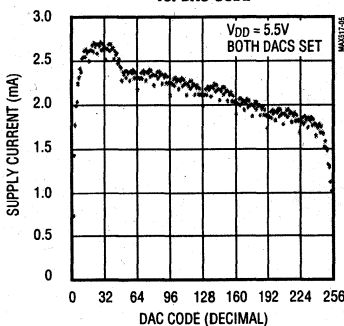
MAX517/MAX519 SUPPLY CURRENT vs. TEMPERATURE



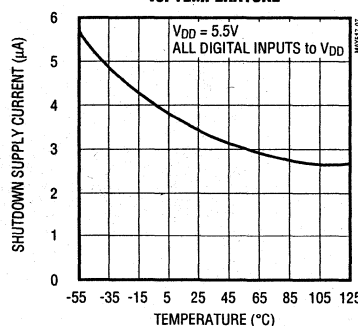
MAX518 SUPPLY CURRENT vs. TEMPERATURE



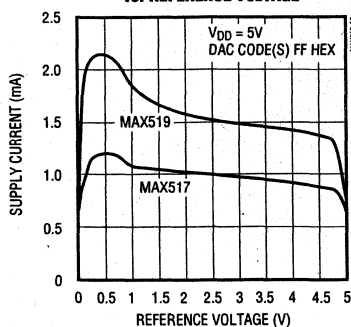
MAX518 SUPPLY CURRENT vs. DAC CODE



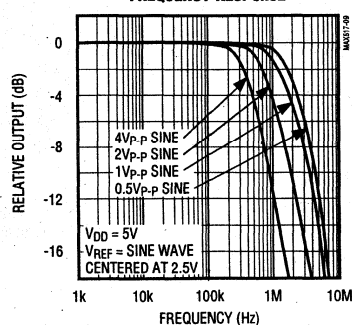
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



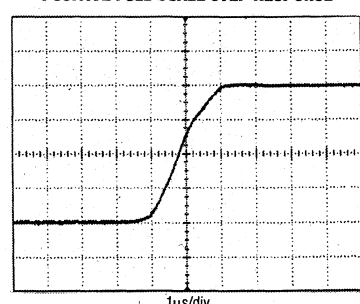
MAX517/MAX519 SUPPLY CURRENT vs. REFERENCE VOLTAGE



MAX517/MAX519 REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



POSITIVE FULL-SCALE STEP RESPONSE



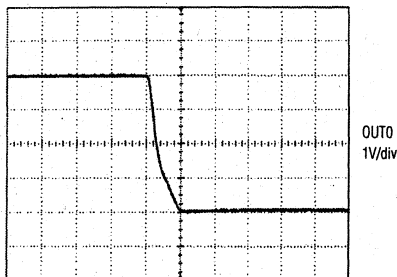
OUTPUT LOADED WITH $10\text{k}\Omega \parallel 100\text{pF}$
REF0 = 4V (MAX517/MAX519)
DAC CODE = 00 HEX TO FF HEX

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

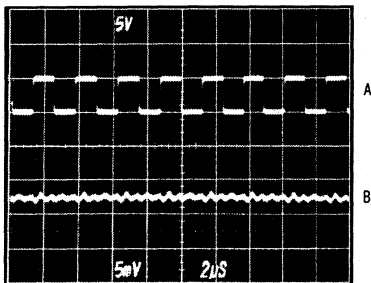
(TA = +25°C, unless otherwise noted.)

NEGATIVE FULL-SCALE STEP RESPONSE



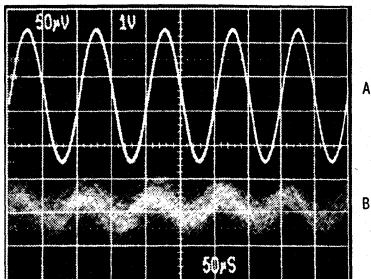
OUT0 LOADED WITH 10kΩ || 100pF
REF0 = 4V (MAX517/MAX519)
DAC CODE = FF HEX to 00 HEX

CLOCK FEEDTHROUGH



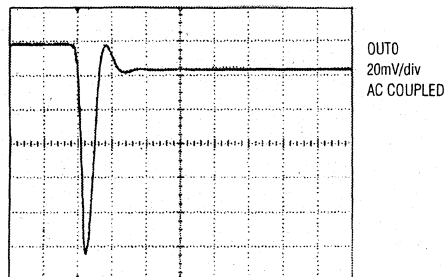
A = SCL, 400kHz, 5V/div
B = OUT0, 5mV/div
DAC CODE = 7F HEX
REF0 = 5V (MAX517/MAX519)

MAX517/MAX519 REFERENCE FEEDTHROUGH AT 10kHz



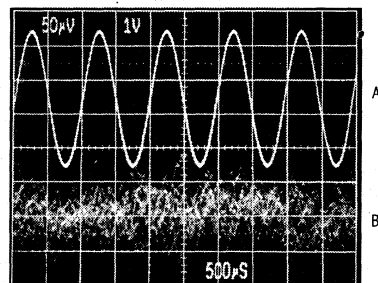
A = REF0, 1V/div (4Vp-p)
B = OUT0, 50μV/div, UNLOADED
FILTER PASSBAND = 1kHz to 100kHz
DAC CODE = 00 HEX

WORST-CASE 1LSB STEP CHANGE



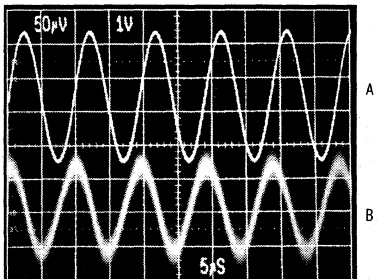
REF0 = 5V (MAX517/MAX519)
DAC CODE = 80 HEX to 7F HEX

MAX517/MAX519 REFERENCE FEEDTHROUGH AT 1kHz



A = REF0, 1V/div (4Vp-p)
B = OUT0, 50μV/div, UNLOADED
FILTER PASSBAND = 100Hz to 10kHz
DAC CODE = 00 HEX

MAX517/MAX519 REFERENCE FEEDTHROUGH AT 100kHz



A = REF0, 1V/div (4Vp-p)
B = OUT0, 50μV/div, UNLOADED
FILTER PASSBAND = 10kHz to 1MHz
DAC CODE = 00 HEX

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Pin Description

PIN			NAME	FUNCTION
MAX517	MAX518	MAX519		
1	1	1	OUT0	DAC0 Voltage Output
2	2	4	GND	Ground
—	—	5	AD3	Address Input 3; sets IC's slave address
3	3	6	SCL	Serial Clock Input
4	4	8	SDA	Serial Data Input
—	—	9	AD2	Address Input 2; sets IC's slave address
5	5	10	AD1	Address Input 1; sets IC's slave address
6	6	11	AD0	Address Input 0; sets IC's slave address
7	7	12	VDD	Power Supply, +5V; used as reference for MAX518
—	—	13	REF1	Reference Voltage Input for DAC1
8	—	15	REF0	Reference Voltage Input for DAC0
—	8	16	OUT1	DAC1 Voltage Output
—	—	2, 3, 7, 14	N.C.	No Connect—not internally connected.

MAX517/MAX518/MAX519

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Detailed Description

Serial Interface

The MAX517/MAX518/MAX519 use a simple 2-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor (μ P) port. Figure 2 shows the timing diagram for signals on the 2-wire bus. Figure 3 shows a typical application. The 2-wire bus can have several devices (in addition to the MAX517/MAX518/MAX519) attached. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. External pull-up resistors are not required on these lines. The MAX517/MAX518/MAX519 can be used in applications where pull-up resistors are required (such as in I²C systems) to maintain compatibility with existing circuitry.

The MAX517/MAX518/MAX519 are receive-only devices and must be controlled by a bus master device. They operate at SCL rates up to 400kHz. A master device sends information to the devices by transmitting their address over the bus and then transmitting the desired information. Each transmission consists of a START condition, the MAX517/MAX518/MAX519's programmable slave-address, one or more command-byte/output-byte pairs (or a command byte alone, if it is the last byte in the transmission), and finally, a STOP condition (Figure 4).

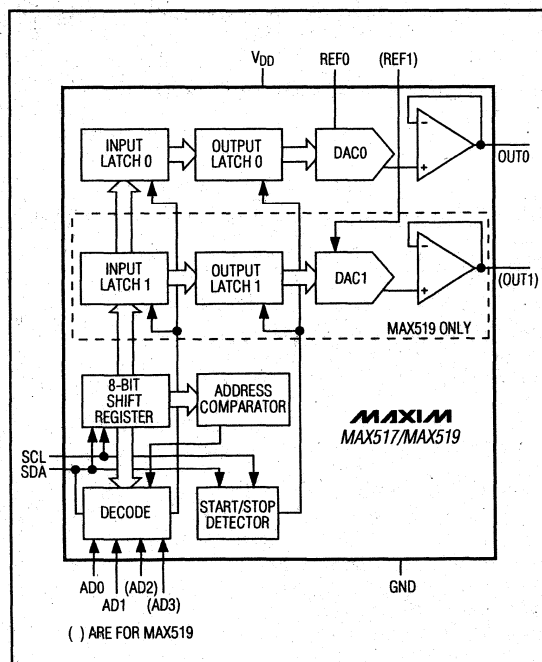


Figure 1. MAX517/MAX519 Functional Diagram

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

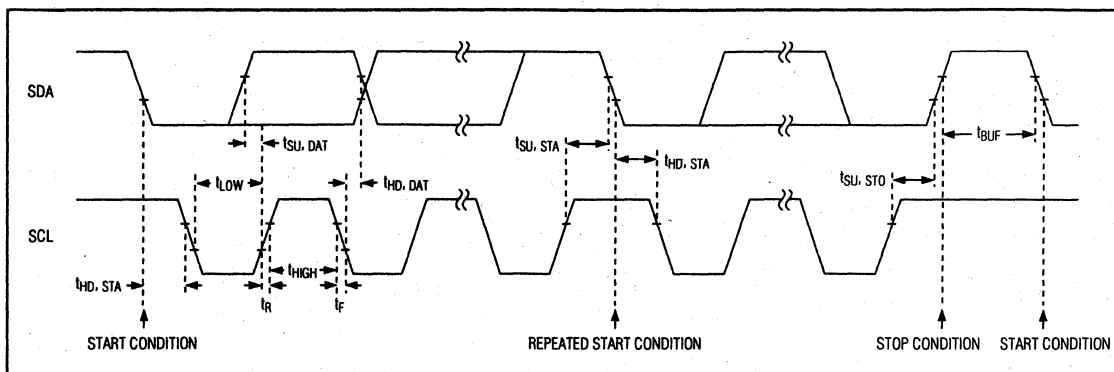


Figure 2. Two-Wire Serial Interface Timing Diagram

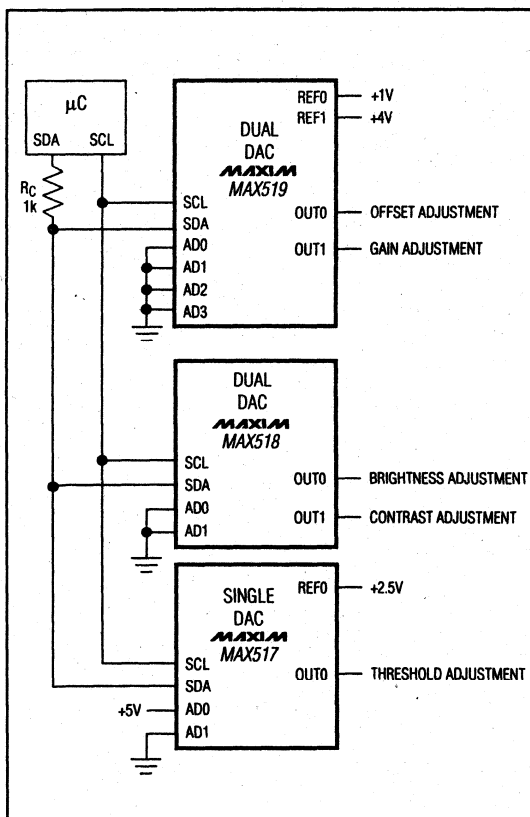


Figure 3. MAX517/MAX518/MAX519 Application Circuit

The address byte and pairs of command and output bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, with the exception of START and STOP conditions. SDA's state is sampled, and therefore must remain stable while SCL is high. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer the data bits to the MAX517/MAX518/MAX519. Set SDA low during the 9th clock cycle as the MAX517/MAX518/MAX519 pull SDA low during this time. R_C (see Figure 3) limits the current that flows during this time if SDA stays high for short periods of time.

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 5). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

The Slave Address

The MAX517/MAX518/MAX519 each have a 7-bit long slave address (Figure 6). The first three bits (MSBs) of the slave address have been factory programmed and are always 010. In addition, the MAX517 and MAX518 have the next two bits factory programmed to 1s. The logic state of the address inputs (AD0 and AD1 on the MAX517/MAX518; AD0, AD1, AD2, and AD3 on the MAX519) determine the LSB bits of the 7-bit slave address. These input pins may be connected to VDD or DGND, or they may be actively driven by TTL or CMOS logic levels. The MAX517/MAX518 have four possible slave addresses and therefore a maximum of four of

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

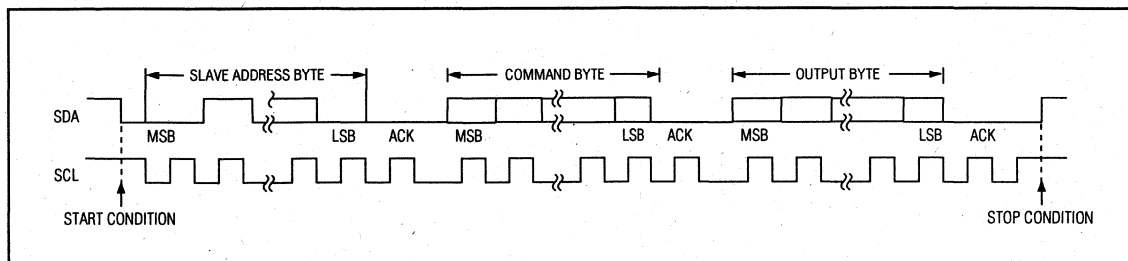


Figure 4. A Complete Serial Transmission

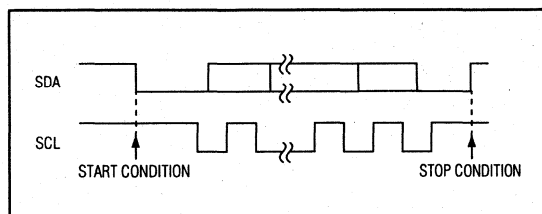


Figure 5. All communications begin with a START condition and end with a STOP condition, both generated by a bus master.

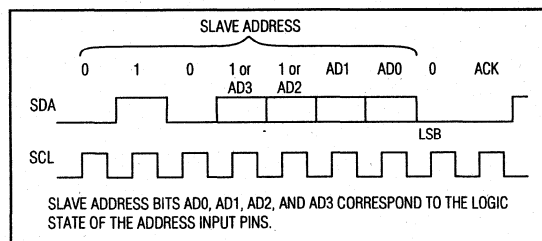


Figure 6. Address Byte

these devices may share the bus. The MAX519 has 16 possible slave addresses. The eighth bit (LSB) in the slave address byte should be low when writing to the MAX517/MAX518/MAX519.

The MAX517/MAX518/MAX519 monitor the bus continuously, waiting for a START condition followed by their slave address. When a device recognizes its slave address, it is ready to accept data.

The Command Byte and Output Byte

A command byte follows the slave address. Figure 7 shows the format for the command byte. A command byte is usually followed by an output byte unless it is the last byte in the transmission. If it is the last byte, all bits except PD (power-down) and RST (reset) are

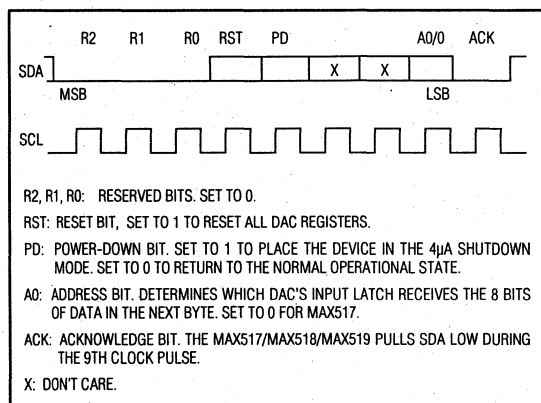


Figure 7. Command Byte

ignored. If an output byte follows the command byte, A0 of the command byte indicates the digital address of the DAC whose input data latch receives the digital output data. Set this bit to 0 when writing to the MAX517. The data is transferred to the DAC's output latch during the STOP condition following the transmission. This allows both DACs of the MAX518/MAX519 to be updated simultaneously (Figure 8).

Setting the PD bit high powers down the MAX517/MAX518/MAX519 following a STOP condition (Figure 9a). If a command byte with PD set high is followed by an output byte, the addressed DAC's input latch will be updated and the data will be transferred to the DAC's output latch following the STOP condition (Figure 9b).

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

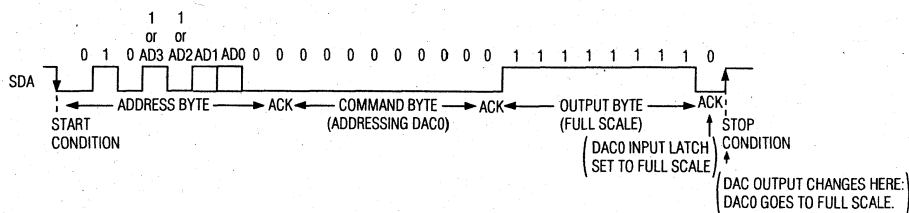


Figure 8a. Setting One DAC Output (MAX517/MAX518/MAX519)

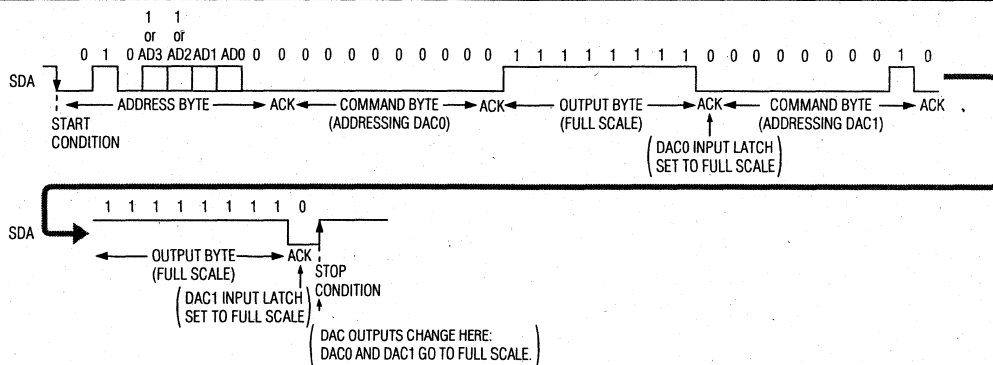


Figure 8b. Setting Both DAC Outputs (MAX518/MAX519)

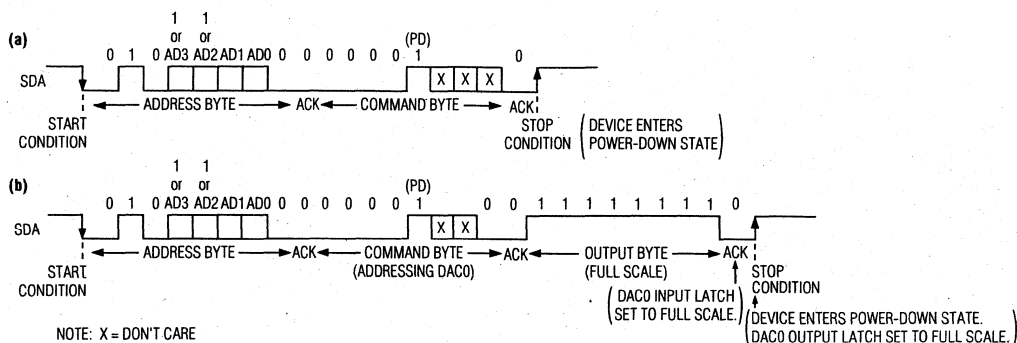


Figure 9. Entering the Power-Down State

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

Furthermore if the transmission's last command byte has PD high, the output latches are updated, but voltage outputs will not reflect the newly entered data because the DAC enters power-down mode when the STOP condition is detected. When in power-down, the DAC outputs float. In this mode, the supply current is a maximum of 20 μ A. A command byte with the PD bit low returns the MAX517/MAX518/MAX519 to normal operation following a STOP condition, with the voltage outputs reflecting the output-latch contents (Figures 10a and 10b). Because each subsequent command byte overwrites the previous PD bit, only the last command byte of a transmission affects the power-down state.

Setting the RST bit high clears the DAC input latches. The DAC outputs remain unchanged until a STOP condition is detected (Figure 11a). If a reset is issued, the

following output byte is ignored. Subsequent pairs of command/output bytes overwrite the input latches (Figure 11b).

All changes made during a transmission affect the MAX517/MAX518/MAX519's outputs only when the transmission ends and a STOP has been recognized.

The R0, R1, and R2 bits are reserved and must be set to zero.

I²C Compatibility

The MAX517/MAX518/MAX519 are fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the 9th clock pulse. Figure 12 shows a typical I²C application.

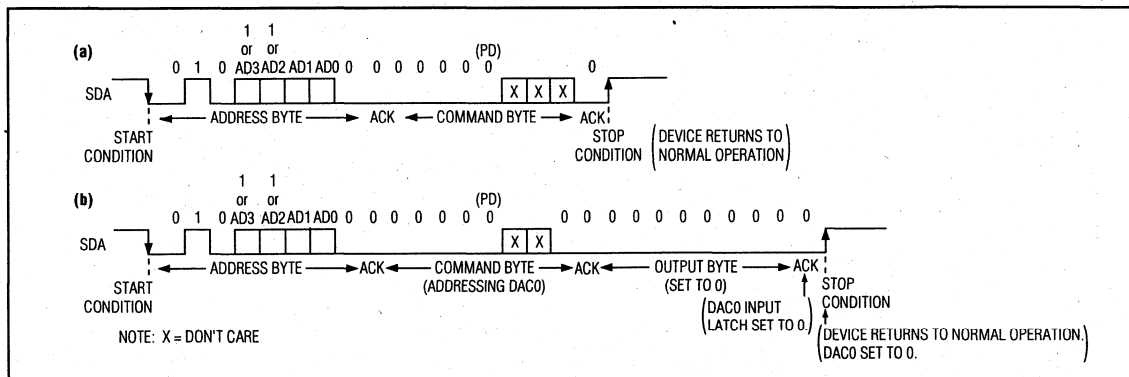


Figure 10. Returning to Normal Operation from Power-Down

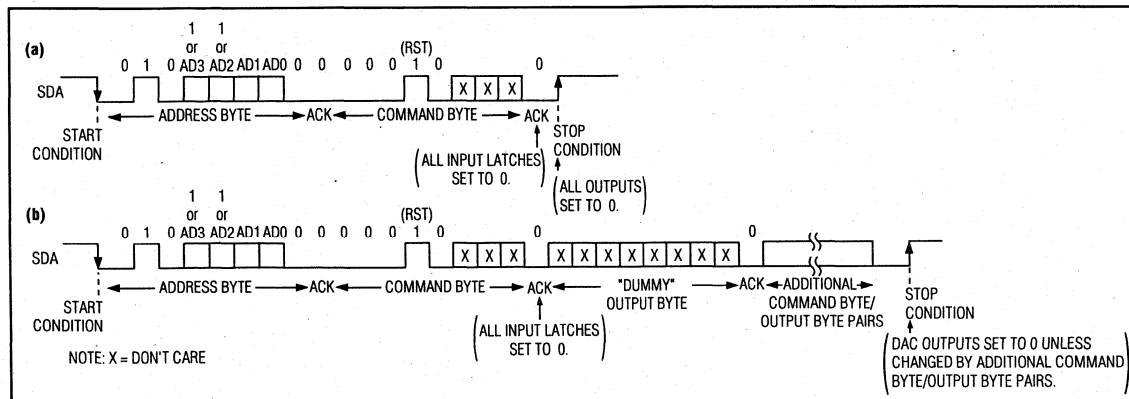


Figure 11. Resetting DAC Outputs

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

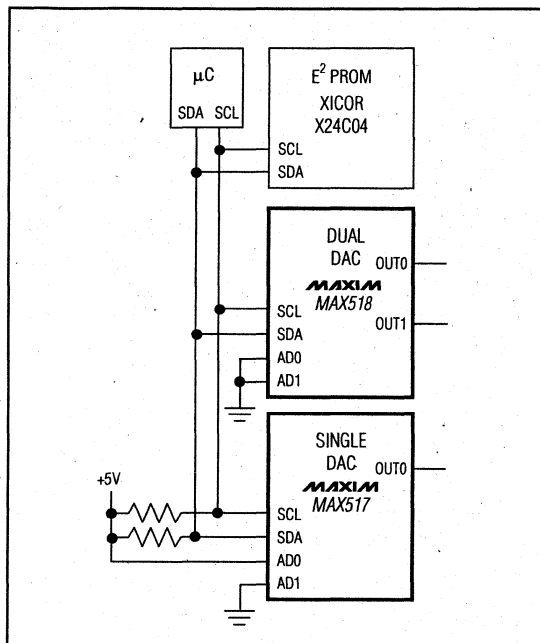


Figure 12. MAX517/MAX518/MAX519 Used in a Typical I²C Application Circuit

Additional START Conditions

It is possible to interrupt a transmission to a device with a new START (repeated start) condition (perhaps addressing another device), which leaves the input

latches with data that has not been transferred to the output latches (Figure 13). Only the currently addressed device will recognize a STOP condition and transfer data to its output latches. If the device is left with data in its input latches, the data can be transferred to the output latches the next time the device is addressed, as long as it receives at least one command byte and a STOP condition.

Early STOP Conditions

The addressed device recognizes a STOP condition at any point in a transmission. If the STOP occurs during a command byte, all previous uninterrupted command and output byte pairs are accepted, the interrupted command byte is ignored, and the transmission ends (Figure 14a). If the STOP occurs during an output byte, all previous uninterrupted command and output byte pairs are accepted, the final command byte's PD and RST bits are accepted, the interrupted output byte is ignored, and the transmission ends (Figure 14b).

Analog Section

DAC Operation

The MAX518 and MAX519 contain two matched voltage-output DACs. The MAX517 contains a single DAC. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. The MAX518 has both DAC's reference inputs connected to V_{DD}. Figure 15 shows a simplified diagram of one DAC.

MAX517/MAX519 Reference Inputs

The MAX517 and MAX519 can be used for multiplying applications. The reference accepts a 0V to V_{DD} volt-

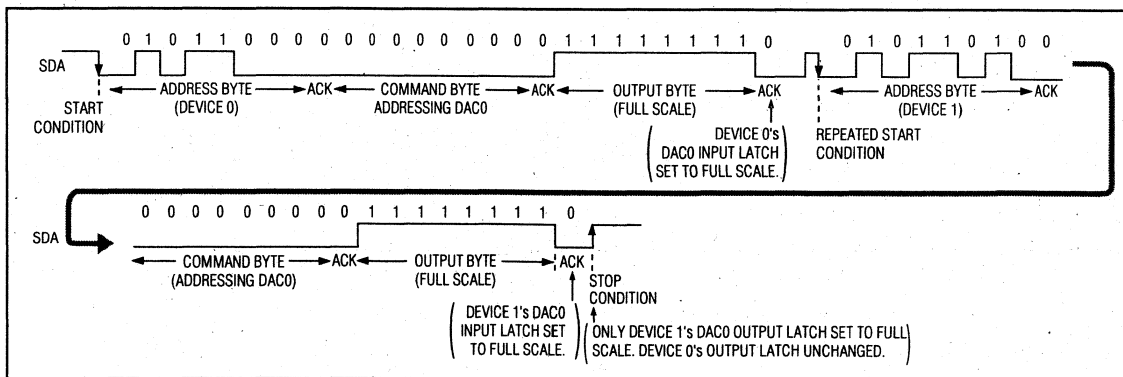


Figure 13. Repeated START Conditions

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

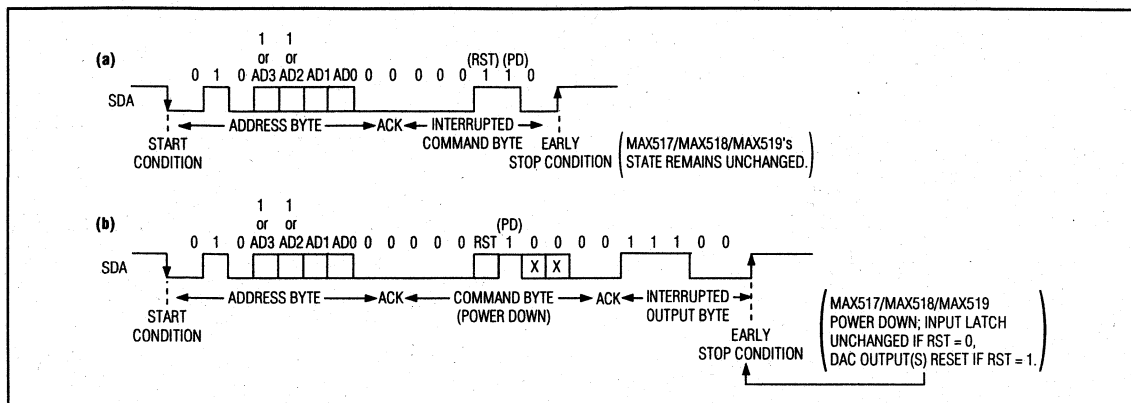


Figure 14. Early STOP Conditions

Table 1. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
11111111	$+V_{REF} \left(\frac{255}{256} \right)$
10000001	$+V_{REF} \left(\frac{129}{256} \right)$
10000000	$+V_{REF} \left(\frac{128}{256} \right) = \frac{V_{REF}}{2}$
01111111	$+V_{REF} \left(\frac{127}{256} \right)$
00000001	$+V_{REF} \left(\frac{1}{256} \right)$
00000000	0V

age, both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC. The reference voltage must be positive. The DAC's input impedance is code dependent, with the lowest value occurring when the input code is 55 hex or 0101 0101, and the maximum value occurring when the input code is 00 hex. Since the REF input resistance (R_{IN}) is code dependent, it must be driven by a circuit with low output impedance (no more than $R_{IN} \div 2000$) to maintain output linearity. The REF input capacitance is also code dependent, with the maximum value occurring at code FF hex (typically 30pF). The output voltage for any DAC can be represented by a digitally programmable voltage source as: $V_{OUT} = (N \times V_{REF}) / 256$, where N is the numerical value of the DAC's binary input code.

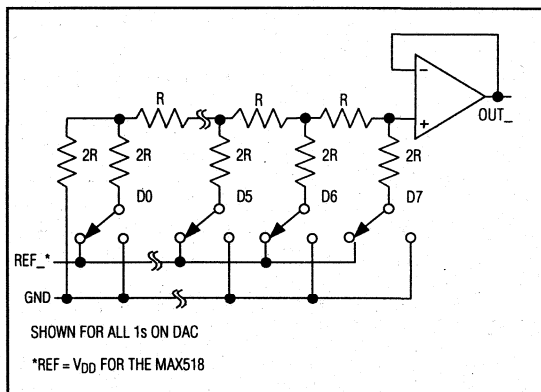


Figure 15. DAC Simplified Circuit Diagram

Output Buffer Amplifiers

The DAC voltage outputs are internally buffered precision unity-gain followers that slew up to $1V/\mu s$. The outputs can swing from 0V to V_{DD} . With a 0V to 4V (or 4V to 0V) output transition, the amplifier outputs typically settle to $1/2LSB$ in 6 μs when loaded with 10k Ω in parallel with 100pF. The buffer amplifiers are stable with any combination of resistive loads $\geq 2k\Omega$ and capacitive loads $\leq 300pF$.

The MAX517/MAX518/MAX519 are designed for unipolar-output, single-quadrant multiplication where the output voltages and the reference inputs are positive with respect to AGND. Table 1 shows the unipolar code.

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

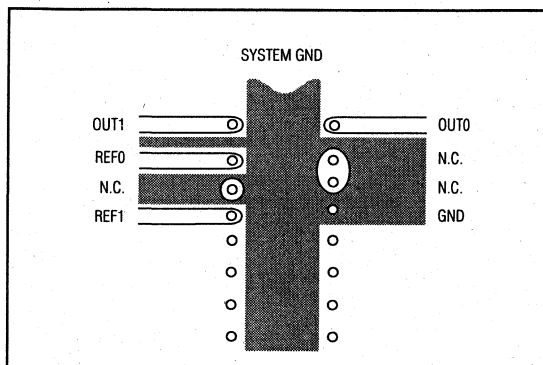


Figure 16. PC Board Layout for Minimizing MAX519 Crosstalk (bottom view)

Applications Information

Power-Supply Bypassing and Ground Management

Bypass V_{DD} with a 0.1 μ F capacitor, located as close to V_{DD} and GND as possible. Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figure 16 shows the suggested PC board layout to minimize crosstalk.

When using the MAX518 (or the MAX517/MAX519 with V_{DD} as the reference), you may want to add a noise filter to the V_{DD} supply (Figure 17) or to the reference input(s) (Figure 18), especially in noisy environments. The reference input's bandwidth exceeds 1MHz for AC signals, so disturbances on the reference input can easily affect the DAC output(s).

The maximum input current for a single reference input is $V_{REF}/16k\Omega = I_{REF}(\text{max})$. In Figure 17, choose R_F so that changes in the reference input current will have little effect on the reference voltage. For example, with $R_F = 6\Omega$, the maximum output error due to R_F is given by:

$$6\Omega \times I_{REF}(\text{max}) = 1.9\text{mV or } 0.1\text{LSB}$$

In Figure 18, there is a voltage drop across R_F that adds to the TUE. This voltage drop is due to the sum of the reference input current ($V_{REF}/16k\Omega$ maximum), supply current (6mA maximum), and the amplifier output current (V_{REF}/R_{LOAD}). Choose R_F to limit this voltage drop to an acceptable value. For example, with a 10k Ω load, you can limit the error due to R_F to 0.5LSB (9.8mV) by selecting R_F so that:

$$R_F = V_{REF} / I_{REF} \leq 9.8\text{mV} / (5\text{V} / 16k\Omega + 6\text{mA} + 5\text{V} / 10k\Omega)$$

$$R_F \leq 1.4\Omega$$

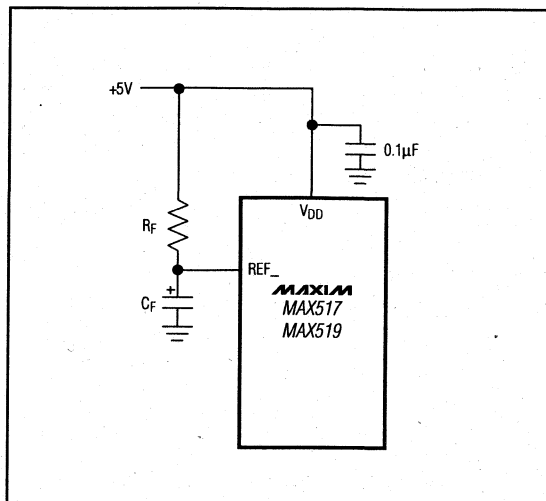


Figure 17. Reference Filter When Using V_{DD} as a Reference

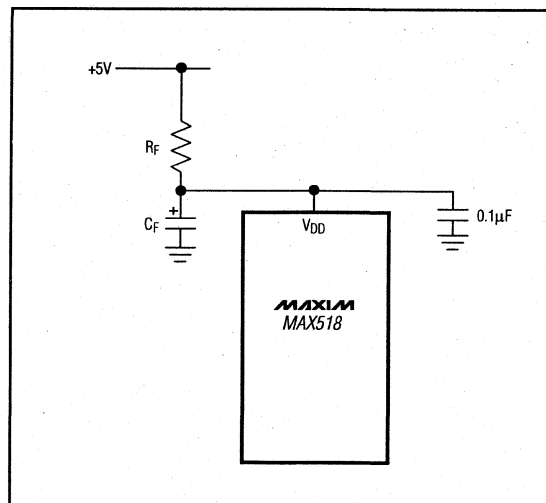


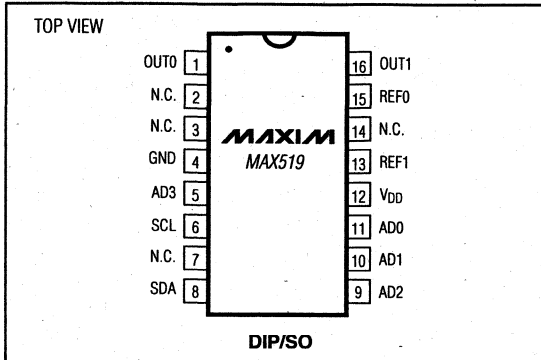
Figure 18. V_{DD} Filter When Using V_{DD} as a Reference

2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs

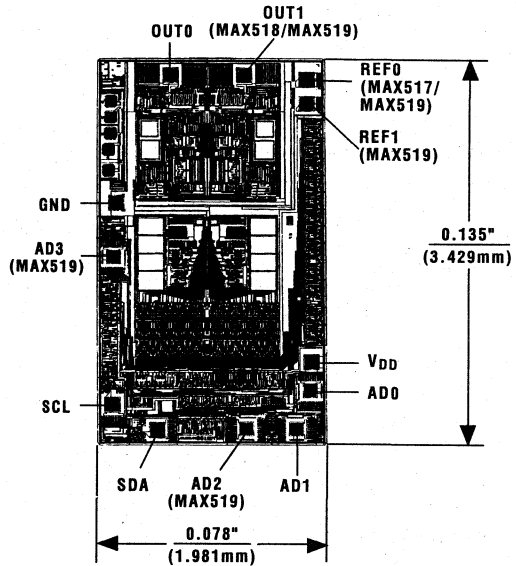
MAX517/MAX518/MAX519

9

Pin Configurations (continued)



Chip Topography



TRANSISTOR COUNT: 1797
SUBSTRATE CONNECTED TO V_{DD}

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX517AEPA	-40°C to +85°C	8 Plastic DIP	1
MAX517BEPA	-40°C to +85°C	8 Plastic DIP	1.5
MAX517AESA	-40°C to +85°C	8 SO	1
MAX517BESA	-40°C to +85°C	8 SO	1.5
MAX517BMJA	-55°C to +125°C	8 Cerdip**	1.5
MAX518ACPA	0°C to +70°C	8 Plastic DIP	1
MAX518BCPA	0°C to +70°C	8 Plastic DIP	1.5
MAX518ACSA	0°C to +70°C	8 SO	1
MAX518BCSA	0°C to +70°C	8 SO	1.5
MAX518BC/D	0°C to +70°C	Dice*	1.5
MAX518AEPA	-40°C to +85°C	8 Plastic DIP	1
MAX518BEPA	-40°C to +85°C	8 Plastic DIP	1.5
MAX518AESA	-40°C to +85°C	8 SO	1
MAX518BESA	-40°C to +85°C	8 SO	1.5
MAX518BMJA	-55°C to +125°C	8 Cerdip**	1.5
MAX519ACPE	0°C to +70°C	16 Plastic DIP	1
MAX519BCPE	0°C to +70°C	16 Plastic DIP	1.5
MAX519ACSE	0°C to +70°C	16 Narrow SO	1
MAX519BCSE	0°C to +70°C	16 Narrow SO	1.5
MAX519BC/D	0°C to +70°C	Dice*	1.5
MAX519AEPE	-40°C to +85°C	16 Plastic DIP	1
MAX519BEPE	-40°C to +85°C	16 Plastic DIP	1.5
MAX519AESE	-40°C to +85°C	16 Narrow SO	1
MAX519BESE	-40°C to +85°C	16 Narrow SO	1.5
MAX519BMJE	-55°C to +125°C	16 Cerdip**	1.5

*Dice are specified at T_A = +25°C, DC parameters only.

**Contact factory for availability and processing to MIL-STD-883.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Quad, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

General Description

The MAX520 is a quad, 8-bit voltage-output digital-to-analog converter (DAC) with a simple 2-wire serial interface that allows communication between multiple devices. It operates from a single +5V supply, and dissipates only 20 μ W of power from the supplies for all four DACs combined. The MAX520's unbuffered voltage outputs connect directly to the internal R-2R ladder network. With no output buffers, the supply current is reduced to 4 μ A and the buffer offset error is eliminated. The DAC output resistances are trimmed to 16k Ω $\pm$ 1% independent of the DAC code.

Each of the MAX520's four DACs has its own reference input and the reference input range includes both supply rails. The MAX520 features a serial interface and internal software protocol that is compatible with I²C™ and allows communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers to be updated simultaneously.

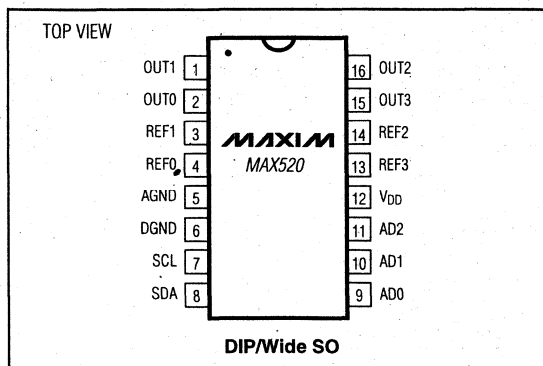
The MAX520 can be put into a low-power shutdown mode that reduces the reference currents. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

The MAX520 is available in 16-pin DIP and wide SO packages.

Applications

Minimum Component Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

Pin Configuration



I²C is a trademark of Philips Corp.

Features

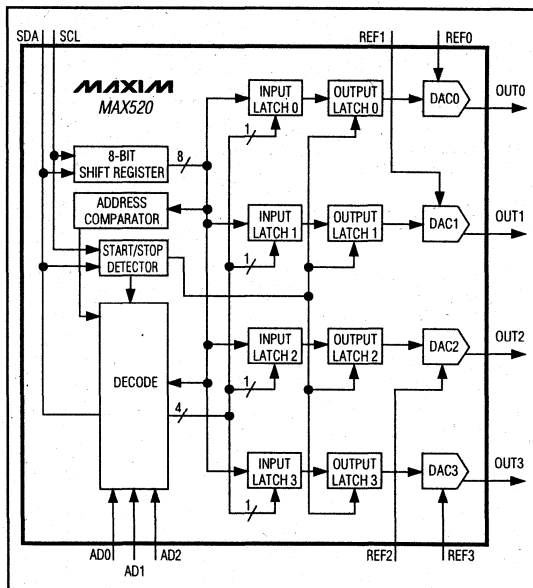
- ◆ Single +5V Supply
- ◆ Simple 2-Wire Serial Interface
- ◆ I²C Compatible
- ◆ Unbuffered Voltage Outputs Reduce Supply Current to 4 μ A
- ◆ Reference Input Range Includes Both Supply Rails
- ◆ Power-On Reset Clears All Latches
- ◆ DAC Output Resistances Trimmed to $\pm$ 1%

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX520CPE	0°C to +70°C	16 Plastic DIP
MAX520CWE	0°C to +70°C	16 Wide SO
MAX520C/D	0°C to +70°C	Dice*
MAX520EPE	-40°C to +85°C	16 Plastic DIP
MAX520EWE	-40°C to +85°C	16 Wide SO
MAX520MJE	-55°C to +125°C	16 CERDIP

*Dice are specified at T_A = +25°C, DC parameters only.

Functional Diagram



MAXIM

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

General Description

The MAX521 is an octal, 8-bit voltage-output digital-to-analog converter (DAC) with a simple 2-wire serial interface that allows communication between multiple devices. It operates from a single 5V supply and its internal precision buffers allow the DAC outputs to swing rail-to-rail. The reference input range includes both supply rails.

The MAX521 has five reference inputs. The first four DACs (DAC0–DAC3) each have a separate reference input (REF0–REF3), allowing each DAC's full-scale range to be set independently. The remaining four DACs (DAC4–DAC7) share the remaining reference input, REF4.

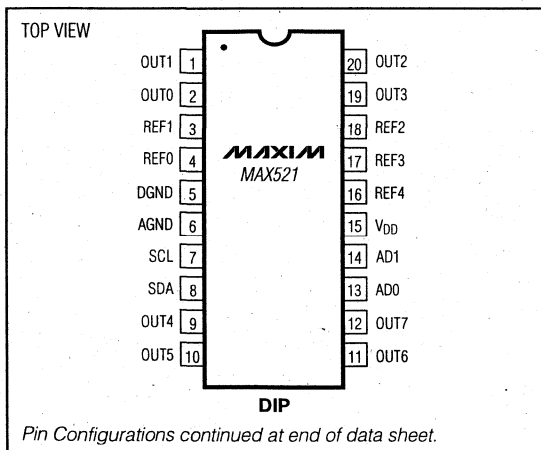
The MAX521 features a serial interface and internal software protocol, allowing communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers to be updated individually or simultaneously. In addition, the device can be put into a low-power shutdown mode that reduces supply current to 4 μ A. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

The MAX521 is available in 20-pin DIP and 24-pin SO package as well as a space-saving 24-pin SSOP package.

Applications

Minimum Component Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

Pin Configurations



Features

- ◆ Single +5V Supply
- ◆ Simple 2-Wire Serial Interface
- ◆ I²C Compatible
- ◆ Output Buffer Amplifiers Swing Rail-to-Rail
- ◆ Reference Input Range Includes Both Supply Rails
- ◆ Power-On Reset Clears All Latches
- ◆ 4 μ A Power-Down Mode

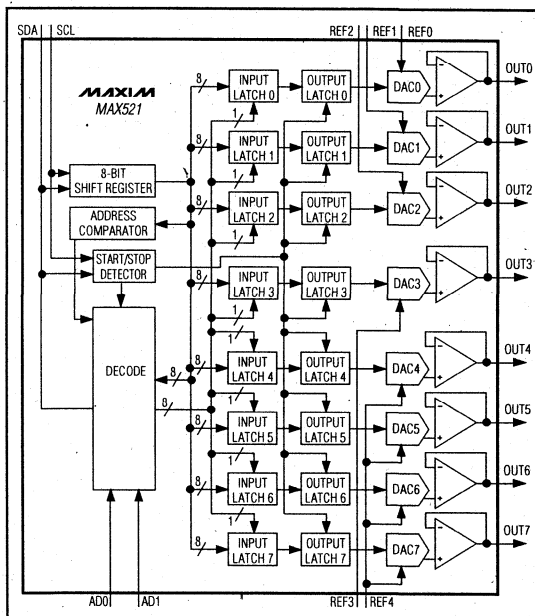
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX521ACPP	0°C to +70°C	20 Plastic DIP	1
MAX521BCPP	0°C to +70°C	20 Plastic DIP	2
MAX521ACWG	0°C to +70°C	24 Wide SO	1
MAX521BCWG	0°C to +70°C	24 Wide SO	2
MAX521ACAG	0°C to +70°C	24 SSOP	1
MAX521BCAG	0°C to +70°C	24 SSOP	2
MAX521BC/D	0°C to +70°C	Dice*	2

Ordering Information continued at end of data sheet.

*Dice are specified at T_A = +25°C, DC parameters only.

Functional Diagram



Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND	-0.3V to +6V
V _{DD} to AGND	-0.3V to +6V
OUT0–OUT7	-0.3V to (V _{DD} + 0.3V)
REF0–REF4	-0.3V to (V _{DD} + 0.3V)
AD0, AD1	-0.3V to (V _{DD} + 0.3V)
SCL, SDA to DGND	-0.3V to +6V
AGND to DGND	-0.3V to +0.3V
Maximum Current into Any Pin	50mA
Continuous Power Dissipation (T _A = +70°C)	
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)	889mW

24-Pin Wide SO (derate 11.76mW/°C above +70°C)	941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C)	640mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C)	889mW
Operating Temperature Ranges	
MAX521_C	0°C to +70°C
MAX521_E	-40°C to +85°C
MAX521BMJP	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, V_{REF} = 4V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE		MAX521A	±1.5			LSB
			MAX521B	±2.0			
Differential Nonlinearity	DNL	Guaranteed monotonic		±1.0			LSB
Zero-Code-Error	ZCE	Code = 00 hex	MAX521_C	18			mV
			MAX521_E	20			
			MAX521BM	20			
Zero-Code-Error Supply Rejection		Code = 00 hex	MAX521_C	±1			mV
			MAX521_E	±1			
			MAX521BM	±1			
Zero-Code-Error Temperature Coefficient		Code = 00 hex		±10			μV/°C
Full-Scale Error		Code = FF hex	MAX521_C	18			mV
			MAX521_E	20			
			MAX521BM	20			
Full-Scale-Error Supply Rejection		Code = FF hex V _{DD} = 5V ±10%	MAX521_C	±1			mV
			MAX521_E	±1			
			MAX521BM	±1			
Full-Scale-Error Temperature Coefficient				±10			μV/°C
REFERENCE INPUTS							
Input Voltage Range				0	V _{DD}		V
Input Resistance	R _{IN}	Code = 55 hex (Note 1)	REF4	4	6		kΩ
			REF0–REF3	16	24		
Input Current		PD = 1		±10			μA
Input Capacitance		Code = FF hex (Note 2)	REF4	120			pF
			REF0–REF3	30			
Channel-to-Channel Isolation		(Note 3)		-60			dB
AC Feedthrough		(Note 4)		-70			dB

Note 1: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.

Note 2: Input capacitance is code dependent. The highest input capacitance occurs at code = FF hex.

Note 3: V_{REF} = 4Vp-p, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.

Note 4: V_{REF} = 4Vp-p, 10kHz, DAC code = 00 hex.

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

MAX521

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 10\%$, $V_{REF-} = 4V$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC OUTPUTS						
Full-Scale Output Voltage			0		V_{DD}	V
Output Load Regulation		$OUT_- = 4V$, $0mA$ to $2.5mA$		0.25		LSB
		$V_{REF-} = V_{DD}$, code = FF hex, $0\mu A$ to $500\mu A$, MAX521_C/E		1.5		
		$V_{REF-} = V_{DD}$, code = FF hex, $0\mu A$ to $500\mu A$, MAX521BM		2.0		
Output Leakage Current		$OUT_- = 0V$ to V_{DD} , $PD = 1$			± 10	μA
DIGITAL INPUTS SCL, SDA						
Input High Voltage	V_{IH}		$0.7V_{DD}$			V
	V_{IL}			$0.3V_{DD}$		
Input Current	I_{IN}	$0V \leq V_{IN} \leq V_{DD}$			± 10	μA
Input Hysteresis	V_{HYST}	(Note 5)	$0.05V_{DD}$			V
Input Capacitance	C_{IN}	(Note 5)			10	pF
DIGITAL INPUTS AD0, AD1						
Input High Voltage	V_{IN}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage	I_{IN}	$V_{IN} = 0V$ to V_{DD}			± 10	μA
DIGITAL OUTPUT SDA (Note 6)						
Output Low Voltage	V_{OL}	$I_{SINK} = 3mA$			0.4	V
		$I_{SINK} = 6mA$			0.6	
Three-State Leakage Current	I_L	$V_{IN} = 0V$ to V_{DD}			± 10	μA
Three-State Output Capacitance	C_{OUT}	(Note 5)			10	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate		Positive and negative	MAX521_C	1.0		V/ μs
			MAX521_E	0.7		
			MAX521BM	0.5		
Output Settling Time		To 1/2 LSB, $10k\Omega$ and $100pF$ load (Note 7)		6		μs
Digital Feedthrough		Code = 00 hex, all digital inputs from $0V$ to V_{DD}		5		nV-s
Digital-Analog Glitch Impulse		Code 128 to 127		12		nV-s
Signal to Noise + Distortion Ratio	SINAD	$V_{REF-} = 4Vp-p$ at 1kHz, $V_{DD} = 5V$, Code = FF hex		87		dB
Multiplying Bandwidth		$V_{REF-} = 4Vp-p$, 3dB bandwidth		1		MHz
Wideband Amplifier Noise				60		μV_{RMS}
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	Normal mode, output unloaded, all digital inputs $0V$ or V_{DD}	MAX521_C	10	20	mA
			MAX521_E/BM	10	24	
		Power-down mode ($PD = 1$)		4	20	μA

Note 5: Guaranteed by design.

Note 6: I^2C compatible mode.

Note 7: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

9

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

TIMING CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			μs
Hold Time, (Repeated) Start Condition	$t_{HD, STA}$		0.6			μs
LOW Period of the SCL Clock	t_{LOW}		1.3			μs
High Period of the SCL Clock	t_{HIGH}		0.6			μs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			μs
Data Hold Time	$t_{HD, DAT}$	(Note 8)	0		0.9	μs
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 9)	$20 + 0.1C_b$		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Note 9)	$20 + 0.1C_b$		300	ns
Fall Time of SDA Transmitting (Note 6)	t_F	$I_{SINK} \leq 6mA$ (Note 9)	$20 + 0.1C_b$		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			μs
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spike Suppressed	t_{SP}	(Notes 10, 11)	0		50	ns

Note 8: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

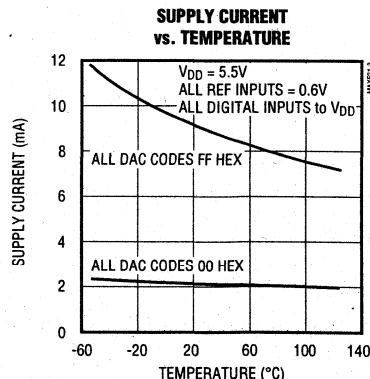
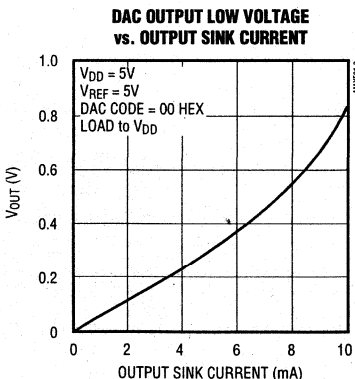
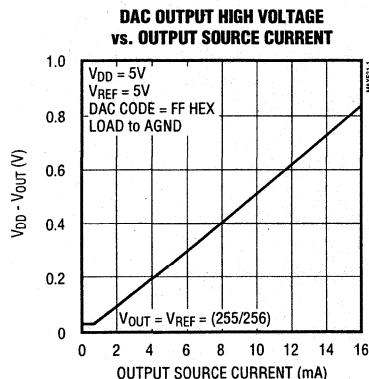
Note 9: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD} .

Note 10: An input filter on the SDA and SCL input suppresses noise spikes less than 50ns.

Note 11: Guaranteed by design.

Typical Operating Characteristics

($T_A = +25^\circ C$, unless otherwise noted.)



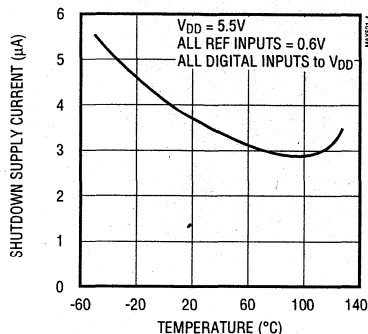
Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

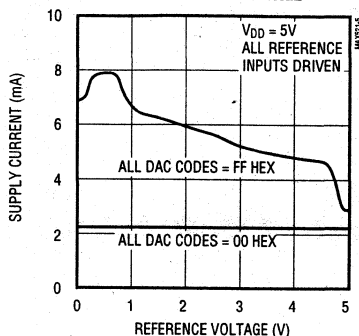
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX521

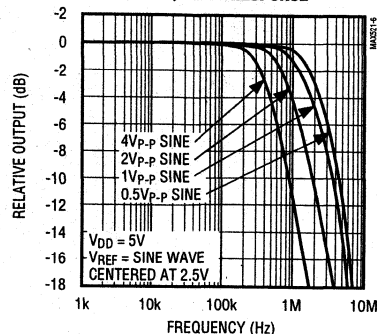
**SHUTDOWN SUPPLY CURRENT
vs. TEMPERATURE**



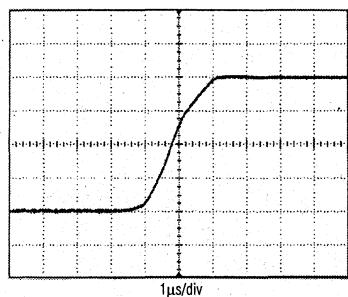
**SUPPLY CURRENT
vs. REFERENCE VOLTAGE**



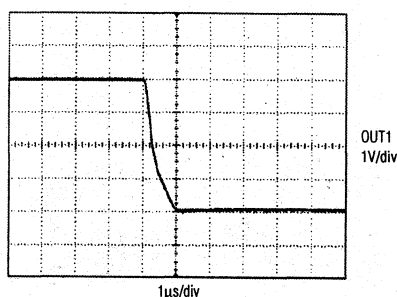
**REFERENCE VOLTAGE INPUT
FREQUENCY RESPONSE**



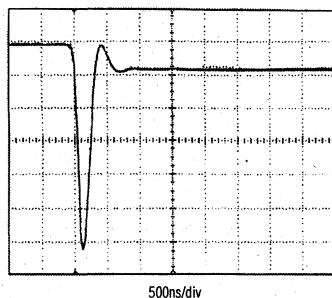
POSITIVE SETTLING TIME



NEGATIVE SETTLING TIME



WORST-CASE 1LSB DIGITAL STEP CHANGE



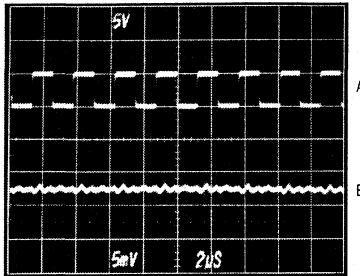
9

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

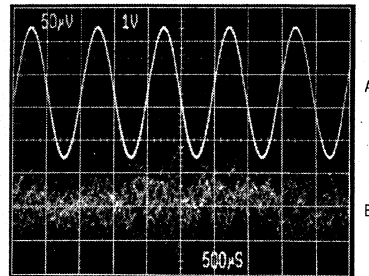
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

CLOCK FEEDTHROUGH



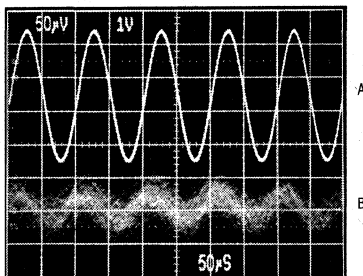
A = SCL, 400kHz, 5V/div
B = OUT1, 5mV/div
DAC CODE = 7F HEX
REF1 = 5V

REFERENCE FEEDTHROUGH AT 1kHz



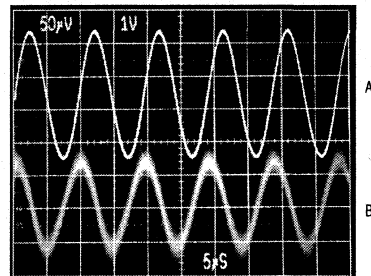
A = REF1, 1V/div (4Vp-p)
B = OUT1, 50μV/div, UNLOADED
FILTER PASSBAND = 100Hz to 10kHz
DAC CODE = 00 HEX

REFERENCE FEEDTHROUGH AT 10kHz



A = REF1, 1V/div (4Vp-p)
B = OUT1, 50μV/div, UNLOADED
FILTER PASSBAND = 1kHz to 100kHz
DAC CODE = 00 HEX

REFERENCE FEEDTHROUGH AT 100kHz



A = REF1, 1V/div (4Vp-p)
B = OUT1, 50μV/div, UNLOADED
FILTER PASSBAND = 10kHz to 1MHz
DAC CODE = 00 HEX

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

Pin Description

PIN		NAME	FUNCTION
DIP	SO/SSOP		
1	1	OUT1	DAC1 Voltage Output
2	2	OUT0	DAC0 Voltage Output
3	3	REF1	Reference Voltage Input for DAC1
4	4	REF0	Reference Voltage Input for DAC0
—	7, 9, 16, 20	N.C.	No Connect—not internally connected.
5	5	DGND	Digital Ground
6	6	AGND	Analog Ground
7	8	SCL	Serial Clock Input
8	10	SDA	Serial Data Input
9	11	OUT4	DAC4 Voltage Output
10	12	OUT5	DAC5 Voltage Output
11	13	OUT6	DAC6 Voltage Output
12	14	OUT7	DAC7 Voltage Output
13	15	AD0	Address Input 0; sets IC's slave address
14	17	AD1	Address Input 1; sets IC's slave address
15	18	VDD	Power Supply, +5V
16	19	REF4	Reference Voltage Input for DACs 4, 5, 6, and 7
17	21	REF3	Reference Voltage Input for DAC3
18	22	REF2	Reference Voltage Input for DAC2
19	23	OUT3	DAC3 Voltage Output
20	24	OUT2	DAC2 Voltage Output

Detailed Description

Serial Interface

The MAX521 uses a simple two-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor port. Figure 1 shows the timing diagram for signals on the wire bus. Figure 2 shows the typical application of the MAX521. The 2-wire bus can have several devices (in addition to the MAX521) attached. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. External pull-up resistors are not required on these lines. The MAX521 can be used in applications where pull-up resistors are required (such as in I²C systems) to maintain compatibility with the existing circuitry.

The MAX521 is a receive-only device and must be controlled by a bus master device. The MAX521 operates at SCL rates up to 400kHz. A master device sends information to the MAX521 by transmitting the MAX521's address over the bus and then transmitting the desired information. Each transmission consists of a START condition, the MAX521's programmable slave-address, one or more command-byte/output-byte pairs (or a command byte alone, if it is the last byte in the transmission), and finally, a STOP condition (Figure 3).

The address byte and pairs of command and output bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low. The only exceptions to this are the START and STOP conditions. SDA's state is sampled, and therefore must remain stable while SCL is high. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer the data bits to the MAX521. Set SDA low during the 9th clock cycle as the MAX521 pulls SDA low during this time. RC (see Figure 2) limits the current that flows during this time if SDA stays high for short periods of time.

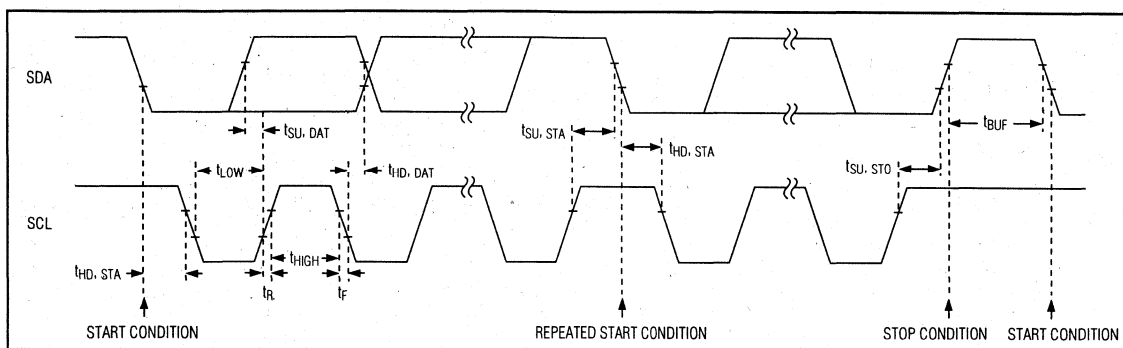


Figure 1. Two-Wire Serial Interface Timing Diagram

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

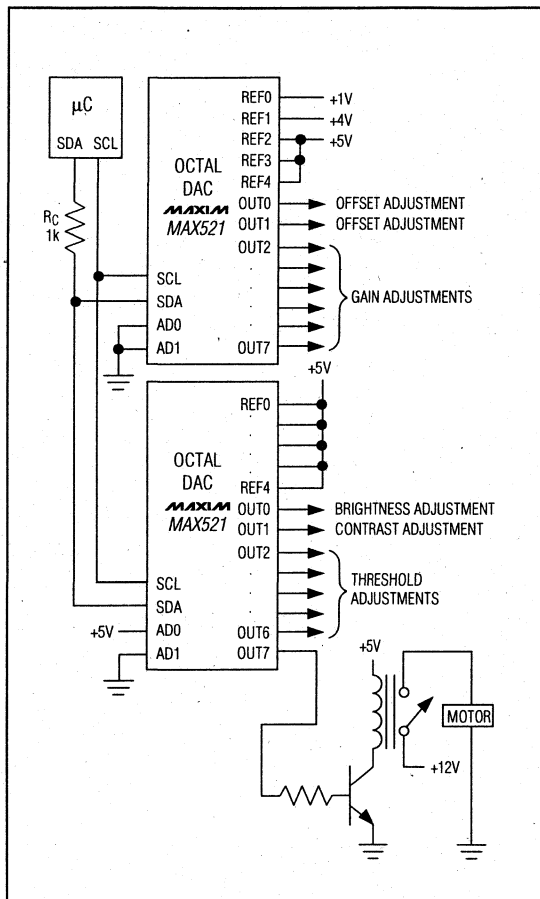


Figure 2. MAX521 Typical Application Circuit

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

The Slave Address

The MAX521's slave address is seven bits long (Figure 5). The first five bits (MSBs) of the slave address have been factory programmed and are always 01010. The state of the MAX521 inputs AD0 and AD1 determine the final two bits of the 7-bit slave address. These input pins may be connected to V_{DD} or DGND, or they may be actively driven by TTL or CMOS logic levels. There are four possible slave addresses for the MAX521, and therefore a maximum of four such devices may be on the bus at one time. The eighth bit (LSB) in the slave address byte should be low when writing to the MAX521.

The MAX521 watches the bus continuously, waiting for a START condition followed by its slave address. When it recognizes its slave address, it is ready to accept data.

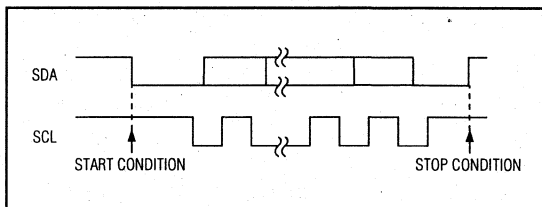


Figure 4. All communications begin with a START condition and end with a STOP condition, both generated by a bus master.

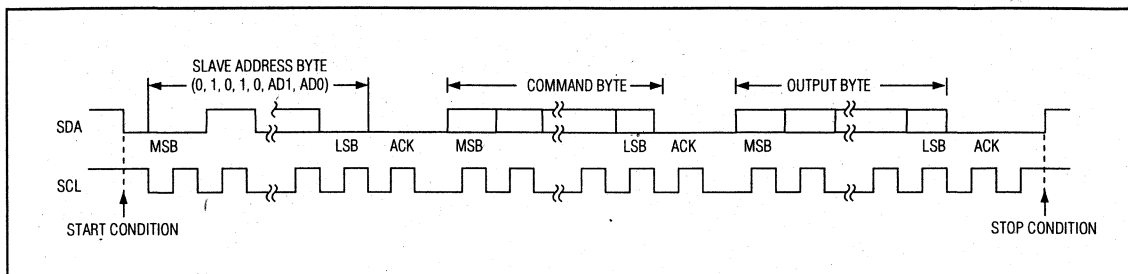


Figure 3. A Complete Serial Transmission

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

The Command Byte and Output Byte

A command byte follows the slave address. Figure 6 shows the format for the command byte. A command byte is usually followed by an output byte unless it is the last byte in the transmission. If it is the last byte, all bits except PD and RST are ignored. If an output byte

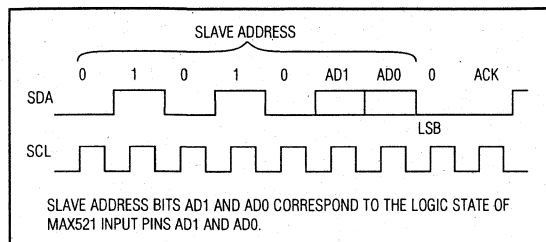


Figure 5. Address Byte

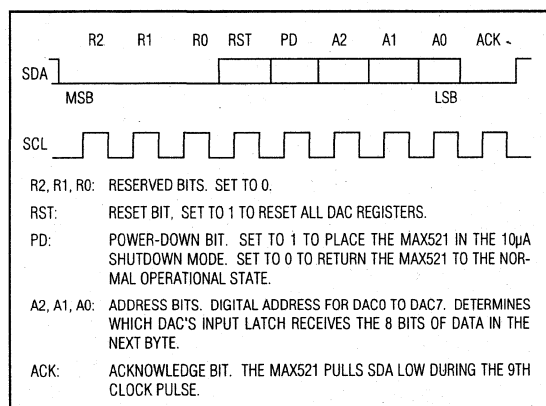


Figure 6. Command Byte

follows the command byte, A0–A2 of the command byte indicate the digital address of the DAC whose input data latch receives the digital output data. The data is transferred to the DAC's output latch during the STOP condition following the transmission. This allows all DACs to be updated and the new outputs to appear simultaneously (Figure 7).

Setting the PD bit high powers down the MAX521 following a STOP condition (Figure 8a). If a command byte with PD set high is followed by an output byte, the addressed DAC's input latch will be updated and the data will be transferred to the DAC's output latch following the STOP condition (Figure 8b). If the transmission's last command byte has PD high, the voltage outputs will not reflect the newly entered data because the DAC will enter power-down mode when the STOP condition is detected. When in power-down, the DAC outputs float. In this mode, the supply current is a maximum of 20µA. A command byte with the PD bit low returns the MAX521 to normal operation following a STOP condition, and the voltage outputs reflect the current output-latch contents (Figures 9a and 9b). Because each subsequent command byte overwrites the previous PD bit, only the last command byte of a transmission affects the MAX521's power-down state.

Setting the RST bit high clears all DAC input latches. The DAC outputs remain unchanged until a STOP condition is detected (Figure 10a). If a reset is issued, the following output byte is ignored. Subsequent pairs of command/output bytes overwrite the input latches (Figure 10b).

All changes made during a transmission affect the MAX521's outputs only when the transmission ends and a STOP has been recognized. The R0, R1, and R2 bits are reserved bits that must be set to zero.

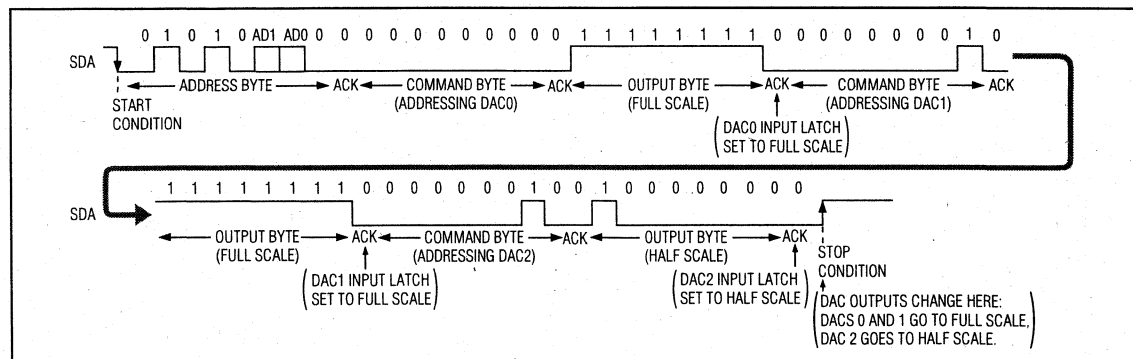


Figure 7. Setting DAC Outputs

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

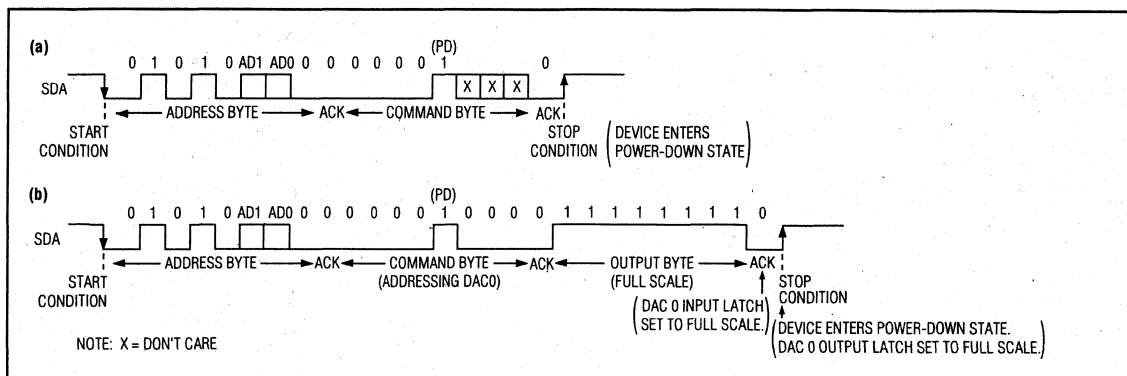


Figure 8. Entering the Power-Down State

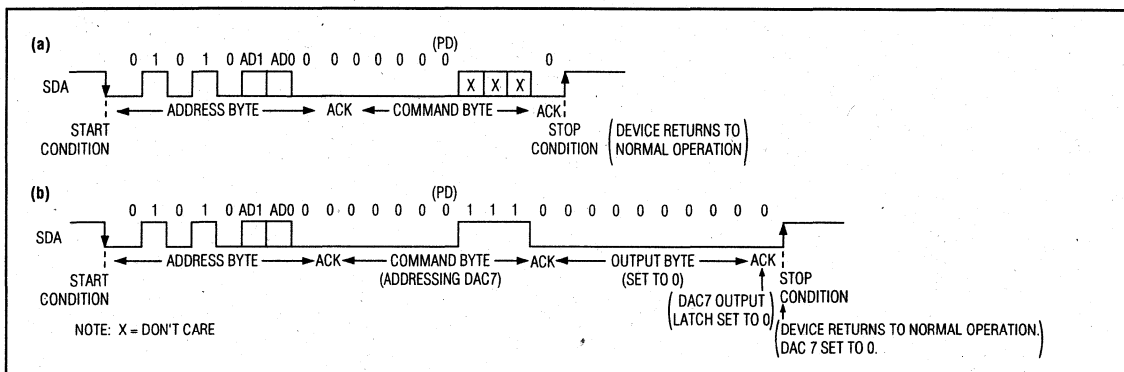


Figure 9. Returning to Normal Operation from Power-Down

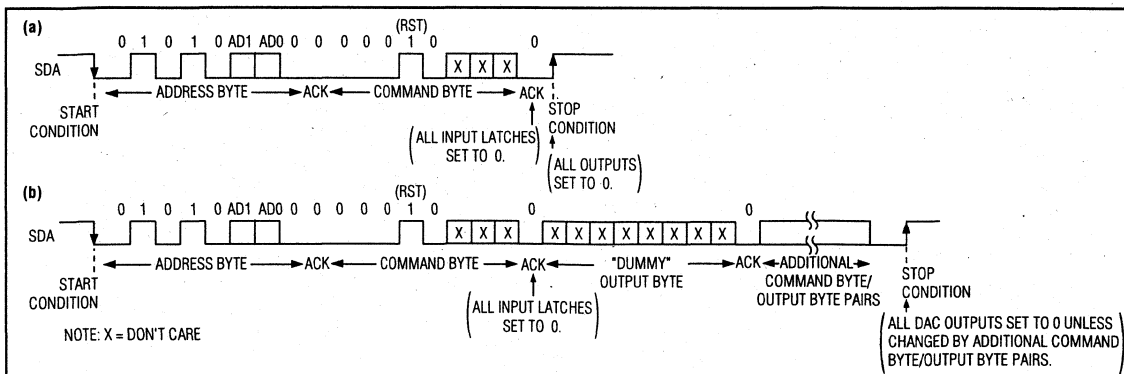


Figure 10. Resetting DAC Outputs

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

MAX521

I²C Compatibility

The MAX521 is fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain which pulls the data line low during the 9th clock pulse. Figure 11 shows the MAX521 being used in a typical I²C application.

Additional START Conditions

It is possible to interrupt a transmission to a MAX521 with a new START (repeated start) condition (perhaps addressing another device), which leaves the input latches with data that has not been transferred to the output latches (Figure 12). Only the currently addressed MAX521 will recognize a STOP condition and transfer data to its output latches. If the MAX521 is left with data in its input latches, the data can be transferred to the output latches the next time the device is addressed, as long as it receives at least one command byte and a STOP condition.

Early Stop Conditions

The addressed MAX521 recognizes a STOP condition at any point in a transmission. If the STOP occurs during a command byte, all previous uninterrupted command and output byte pairs are accepted, the transmission ends (Figure 13a). If the STOP occurs during an output byte, all previous uninterrupted command and output byte pairs are accepted, the final command byte's PD and RST bits are accepted, the interrupted output byte is ignored, and the transmission ends (Figure 13b).

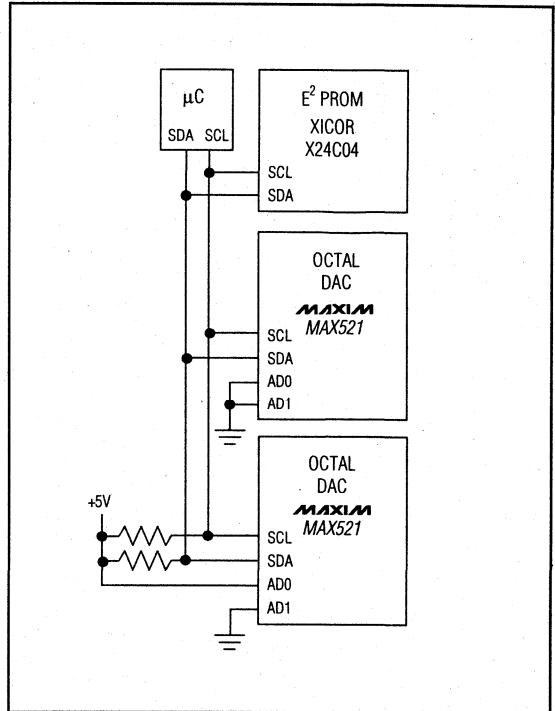


Figure 11. MAX521 Used in a Typical I²C Application Circuit

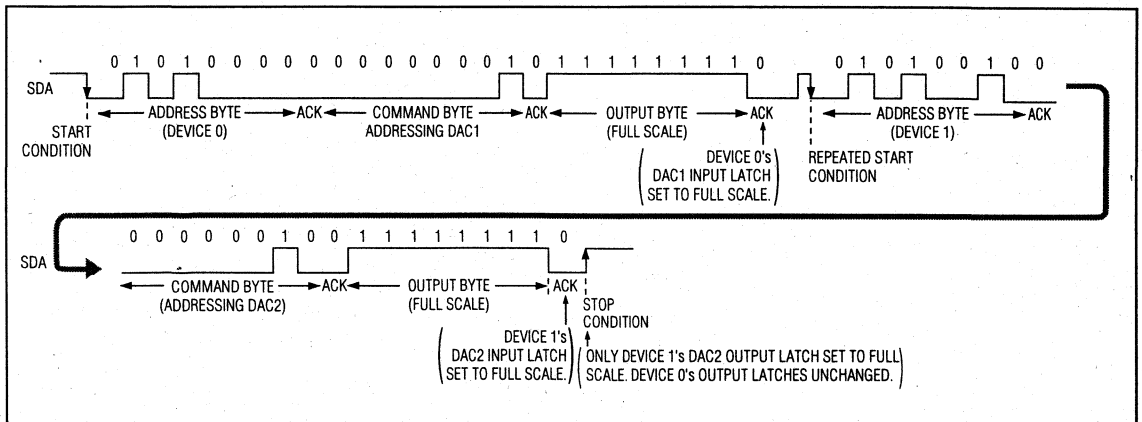


Figure 12. Repeated START Conditions

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

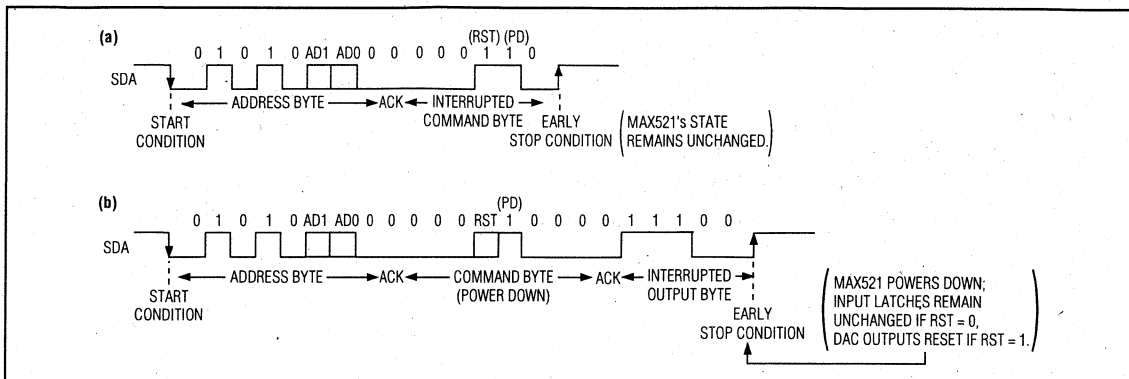


Figure 13. Early STOP Conditions

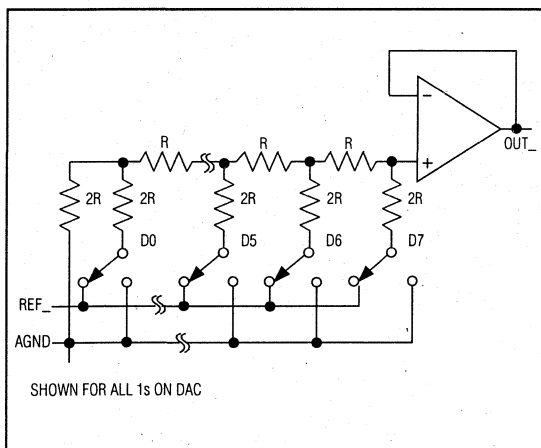


Figure 14. DAC Simplified Circuit Diagram

Analog Section

DAC Operation

The MAX521 contains eight matched voltage-output DACs. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. DAC0–DAC3 each have separate reference inputs while DAC4–DAC7 all share a common reference input. Figure 14 shows a simplified diagram of one of the eight DACs.

Reference Inputs

The MAX521 can be used for multiplying applications. The reference accepts a 0V to V_{DD} voltage, both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC(s). The reference voltage must be positive. The DAC's input impedance is code dependent, with the lowest value occurring when the input code is 55 hex or 0101 0101, and the maximum value occurring when the input code is 00 hex. Since the REF input resistance (R_{IN}) is code dependent, it must be driven by a circuit with low output impedance (no more than $R_{IN} \div 2000$) to maintain output linearity. The REF input capacitance is also code dependent, with the maximum value occurring at code FF hex (typically 120pF for REF4, and 30pF for REF0–REF3). The output voltage for any DAC can be represented by a digitally programmable voltage source as: $V_{OUT} = (N \times V_{REF}) / 256$, where N is the numerical value of the DAC's binary input code.

Output Buffer Amplifiers

The MAX521 voltage outputs (OUT0–OUT7) are internally buffered precision unity-gain followers that slew up to 1V/ μ s. The outputs can swing from 0V to V_{DD} . With a 0V to 4V (or 4V to 0V) output transition, the amplifier outputs typically settle to 1/2LSB in 6 μ s when loaded with 10k Ω in parallel with 100pF. The buffer amplifiers are stable with any combination of resistive loads $\geq 2k\Omega$ and capacitive loads $\leq 300pF$.

The MAX521 is designed for unipolar-output, single-quadrant multiplication where the output voltages and the reference inputs are positive with respect to AGND. Table 1 shows the unipolar code.

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

MAX521

Table 1. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
11111111	$+V_{REF} \left(\frac{255}{256} \right)$
10000001	$+V_{REF} \left(\frac{129}{256} \right)$
10000000	$+V_{REF} \left(\frac{128}{256} \right) = \frac{V_{REF}}{2}$
01111111	$+V_{REF} \left(\frac{127}{256} \right)$
00000001	$+V_{REF} \left(\frac{1}{256} \right)$
00000000	0V

Applications Information

Power-Supply Bypassing and Ground Management

Bypass V_{DD} with a 0.1 μ F capacitor, located as close to V_{DD} and DGND as possible. The analog ground (AGND) and digital ground (DGND) pins should be connected in a "star" configuration to the highest quality ground available, which should be located as close to the MAX521 as possible.

Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figure 15 shows the suggested PC board layout to minimize crosstalk.

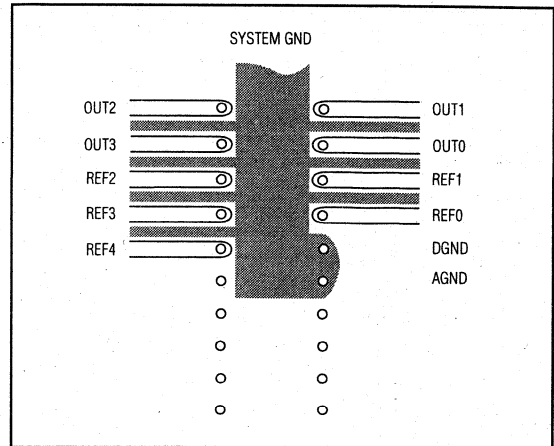


Figure 15. PC Board Layout for Minimizing Crosstalk (bottom view, DIP package)

Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

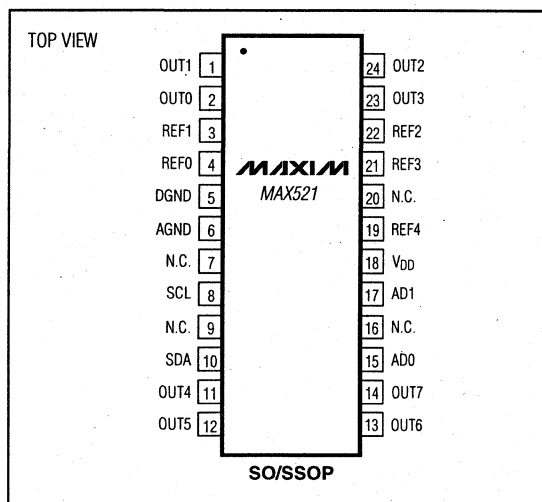
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX521AEPP	-40°C to +85°C	20 Plastic DIP	1
MAX521BEPP	-40°C to +85°C	20 Plastic DIP	2
MAX521AEWG	-40°C to +85°C	24 Wide SO	1
MAX521BEWG	-40°C to +85°C	24 Wide SO	2
MAX521AEAG	-40°C to +85°C	24 SSOP	1
MAX521BEAG	-40°C to +85°C	24 SSOP	2
MAX521BMJP	-55°C to +125°C	20 CERDIP**	2

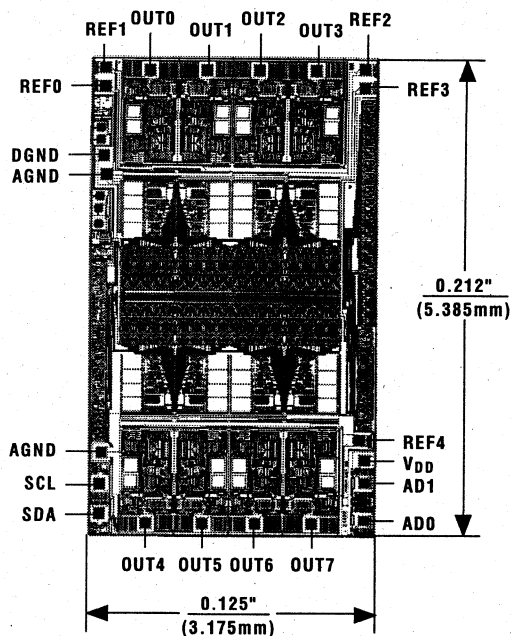
* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

**Contact factory for availability.

Pin Configurations (continued)



Chip Topography



TRANSISTOR COUNT: 4518
SUBSTRATE CONNECTED TO V_{DD}

MAXIM

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

General Description

The MAX522 contains two 8-bit, buffered, voltage-output digital-to-analog converters (DAC A and DAC B) in small 8-pin SO and DIP packages. DAC A's buffer can source and sink 5mA, and DAC B's output can source and sink 500 μ A, both to within 0.5V of ground and V_{DD} . The MAX522 operates with a single +2.7V to +5.5V supply.

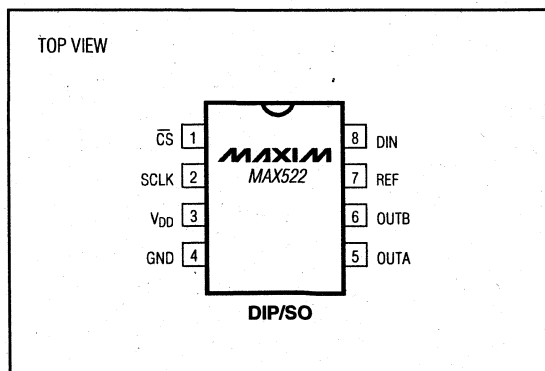
The device utilizes a 3-wire serial interface, which operates at clock rates up to 5MHz and is compatible with SPI™, QSPI™, and Microwire™ interface standards. The serial input shift register is 16 bits long and consists of eight bits of DAC input data and eight bits for DAC selection and shutdown control. DAC registers can be loaded independently or in parallel at the positive edge of $\overline{CS}$.

The MAX522's ultra-low power consumption and small 8-pin SO package make it ideal for portable and battery-powered applications. Supply current is less than 1mA and drops below 1 μ A in shutdown mode. In addition, the reference input is disconnected from the REF pin during shutdown, further reducing the system's total power consumption. The software format is compatible with the MAX512/MAX513 triple 8-bit DACs.

Applications

Digital Gain and Offset Adjustment
Programmable Current Source
Programmable Voltage Source
Power-Amp Bias Control
VCO Tuning

Pin Configuration



SPI and QSPI are trademarks of Motorola Inc.
Microwire is a trademark of National Semiconductor Corp.

MAXIM

Maxim Integrated Products 9-69

Call toll free 1-800-998-8800 for free samples or literature.

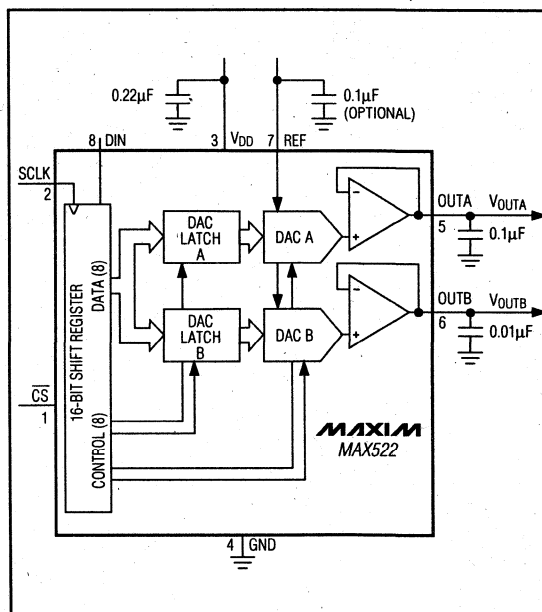
Features

- ◆ Operates from a Single +2.7V to +5.5V Supply
- ◆ Dual Buffered Voltage Output
- ◆ Low Power Consumption:
1mA Operating Current
<1 μ A Shutdown Current
- ◆ Independently Programmable Shutdown Mode
- ◆ 5MHz, 3-Wire Serial Interface
- ◆ SPI™, QSPI™, and Microwire™ Compatible
- ◆ Space-Saving 8-Pin SO Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX522CPA	0°C to +70°C	8 Plastic DIP
MAX522CSA	0°C to +70°C	8 SO
MAX522EPA	-40°C to +85°C	8 Plastic DIP
MAX522ESA	-40°C to +85°C	8 SO

Functional Diagram



MAX522

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Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V, +6V
Digital Inputs and Outputs to GND	-0.3V, (V _{DD} + 0.3V)
REF	-0.3V, (V _{DD} + 0.3V)
OUTA, OUTB (Note 1)	V _{DD}
Continuous Power Dissipation (T _A = +70°C)	
Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
SO (derate 5.88mW/°C above +70°C)	471mW

Operating Temperature Ranges

MAX522C_ A	0°C to +70°C
MAX522E_ A	-40°C to +85°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: The outputs may be shorted to V_{DD} or GND if the package power dissipation is not exceeded. Typical short-circuit current to GND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, REF = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Integral Nonlinearity	INL	(Note 2)			±1.5	LSB
Total Unadjusted Error	TUE	(Note 2)			±1	LSB
Zero-Code Temperature Coefficient				100		µV/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DD} ≤ 5.5V, REF = 4.096V		0.01		%/%
		2.7V ≤ V _{DD} ≤ 3.6V, REF = 2.4V		0.015		
REFERENCE INPUTS						
Reference Input Voltage Range			GND		V _{DD}	V
Reference Input Capacitance				25		pF
Reference Input Resistance	R _{REF}	(Note 3)	8			kΩ
Reference Input Resistance (shutdown mode)				2		MΩ
DAC OUTPUTS						
Output Voltage Range			0		REF	V
Capacitive Load at OUT ₋		DAC A	0.1			µF
		DAC B	0.01			
Output Resistance		DAC A		50		Ω
		DAC B		500		
DIGITAL INPUTS						
Input High Voltage	V _{IH}		(0.7)(V _{DD})			V
Input Low Voltage	V _{IL}			(0.3)(V _{DD})		V
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}		0.1	±10	µA
Input Capacitance	C _{IN}	(Notes 4, 5)			10	pF

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

MAX522

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7V$ to $+5.5V$, $REF = V_{DD}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	$C_L = 0.1\mu F$ (DAC A), $C_L = 0.01\mu F$ (DAC B)		0.1		V/ μs
Voltage-Output Settling Time		$To \pm 1/2 LSB$	$C_L = 0.1\mu F$ (DAC A)		70	μs
			$C_L = 0.01\mu F$ (DAC B)		70	
Digital Feedthrough and Crosstalk		All 0s to all 1s		10		nV-s
POWER SUPPLIES						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current	I_{DD}	All inputs = 0V	$V_{DD} = 5.5V$		1.3	mA
			$V_{DD} = 3.6V$		0.9	
Shutdown Supply Current		$V_{DD} = 5.5V$		0.1		μA

TIMING CHARACTERISTICS (Note 4)

($V_{DD} = +2.7V$ to $+5.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING						
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		150			ns
SCLK Rise to $\overline{CS}$ Rise Setup Time	t_{CSH}		150			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		50			ns
SCLK Pulse Width High	t_{CH}		100			ns
SCLK Pulse Width Low	t_{CL}		100			ns
$\overline{CS}$ Pulse Width High	t_{CSPWH}		200			ns

Note 2: Reduced digital code range (code 24 through code 232) is due to swing limitations of the output amplifiers. See *Typical Operating Characteristics*.

Note 3: Reference input resistance is code dependent. The lowest input resistance occurs at code 55hex. Refer to the *Reference Input* section in the *Detailed Description*.

Note 4: Guaranteed by design. Not production tested.

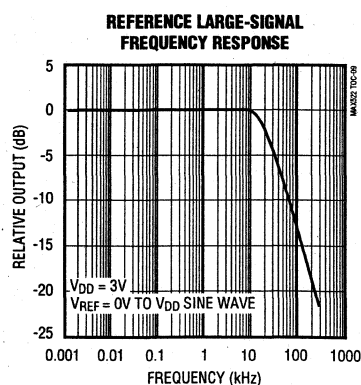
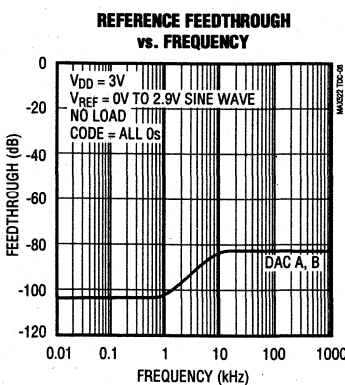
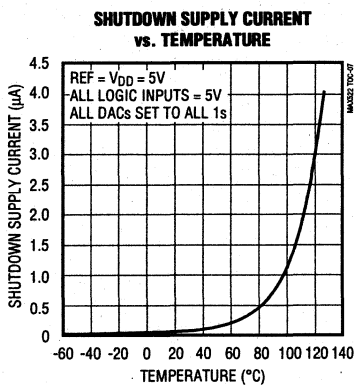
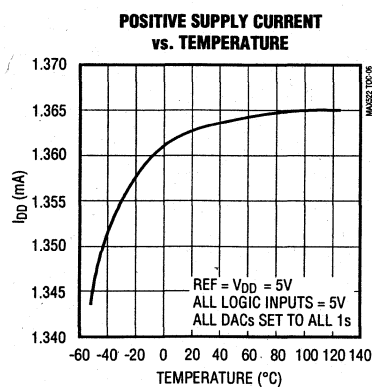
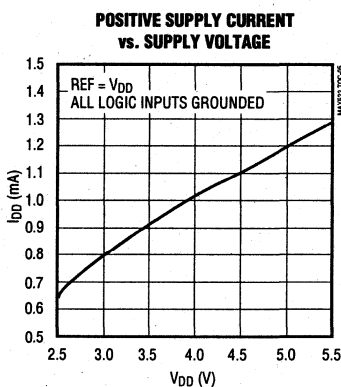
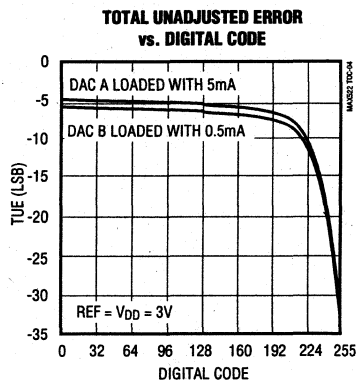
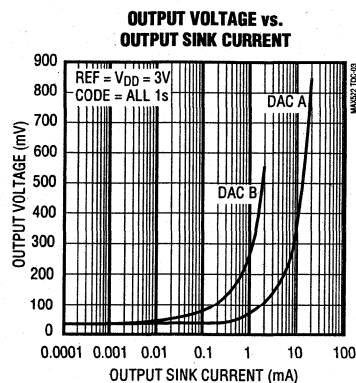
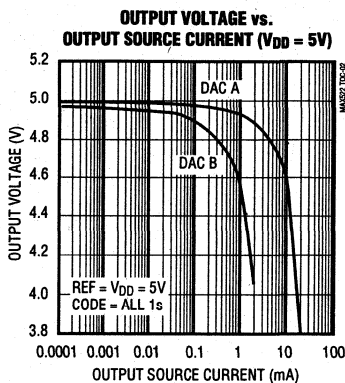
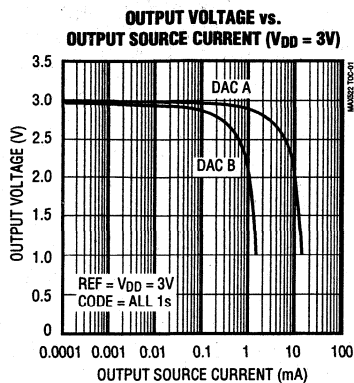
Note 5: Input capacitance is code dependent. The highest capacitance occurs at code 00hex.

9

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

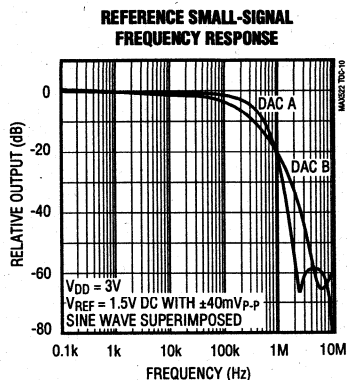


Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

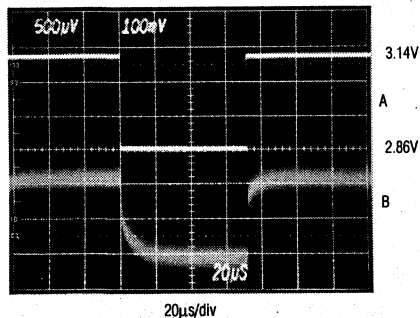
MAX522

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



LINE-TRANSIENT RESPONSE (OUTA)

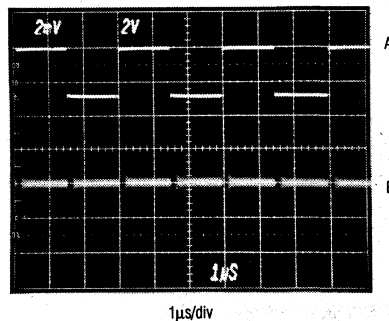


REF = 2.56V, NO LOAD, CODE = ALL 1s

A: V_{DD} , 100mV/div

B: OUTA, 500μV/div

CLOCK FEEDTHROUGH (OUTA)



$\overline{CS} = \text{HIGH}$

A: SCLK, 333kHz, 0V TO 2.9V, 2V/div

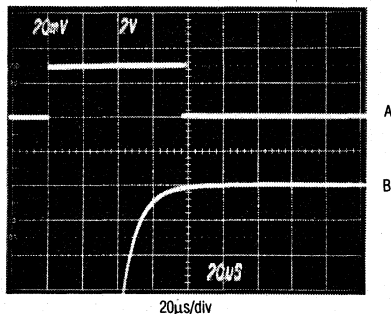
B: OUTA, 2mV/div

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted).

POSITIVE SETTLING TIME (DAC A)

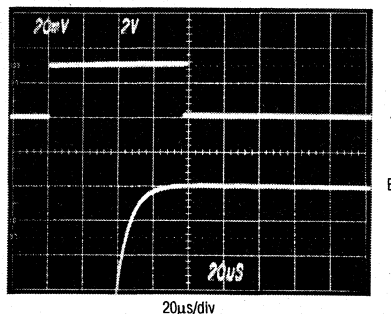


$V_{DD} = 3\text{V}$, $\text{REF} = V_{DD}$, $R_L = 1\text{k}\Omega$, $C_L = 0.1\mu\text{F}$,
ALL BITS OFF TO ALL BITS ON

A: $\overline{\text{CS}}$, 2V/div

B: OUTA, 20mV/div

POSITIVE SETTLING TIME (DAC B)

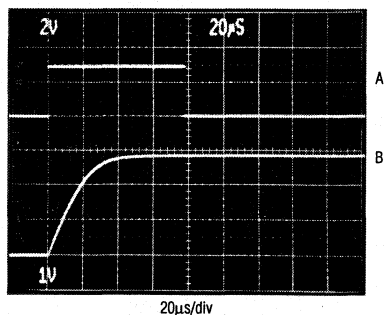


$V_{DD} = 3\text{V}$, $\text{REF} = V_{DD}$, $R_L = 10\text{k}\Omega$, $C_L = 0.01\mu\text{F}$,
ALL BITS OFF TO ALL BITS ON

A: $\overline{\text{CS}}$, 2V/div

B: OUTB, 20mV/div

TIME EXITING SHUTDOWN MODE

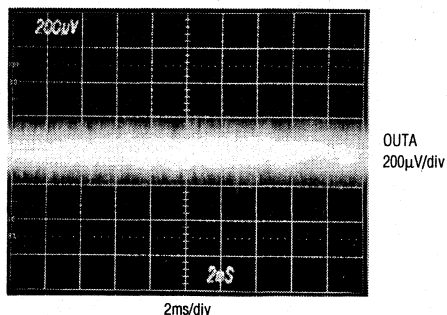


$V_{DD} = 3\text{V}$, $\text{REF} = V_{DD}$, $R_L = 1\text{k}\Omega$, $C_L = 0.1\mu\text{F}$,
DAC LOADED WITH ALL 1s

A: $\overline{\text{CS}}$, 2V/div

B: OUTA, 1V/div

OUTPUT VOLTAGE NOISE (DC TO 1MHz)



DIGITAL CODE = 80, $\text{REF} = V_{DD}$, NO LOAD

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

Pin Description

MAX522

PIN	NAME	FUNCTION
1	$\overline{CS}$	Chip Select (active low). Enables data to be shifted into the 16-bit shift register. Programming commands are executed at the rising edge of $\overline{CS}$.
2	SCLK	Serial Clock Input. Data is clocked in on the rising edge of SCLK.
3	V _{DD}	Positive Power Supply (2.7V to 5.5V). Bypass with 0.22 μ F to GND.
4	GND	Ground
5	OUTA	DAC A Output Voltage (Buffered). Connect 0.1μF capacitor or greater to GND.
6	OUTB	DAC B Output Voltage (Buffered). Connect 0.01μF capacitor or greater to GND.
7	REF	Reference Input for DAC A and DAC B
8	DIN	Serial Data Input of the 16-bit shift register. Data is clocked into the register on the rising edge of SCLK.

Detailed Description

Analog Section

The MAX522 contains two 8-bit, voltage-output digital-to-analog converters (DACs). The DACs are "inverted" R-2R ladder networks using complementary switches that convert 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage.

The MAX522 has one reference input which is shared by DAC A and DAC B. The device includes output buffer amplifiers for both DACs and input logic for simple microprocessor (μ P) and CMOS interfaces. The power-supply range is from +5.5V down to +2.7V.

Reference Input and DAC Output Range

The voltage at REF sets the full-scale output of the DACs. The input impedance of the REF input is code dependent. The lowest value, approximately 8k Ω , occurs when the input code is 01010101 (55hex). The maximum value of infinity occurs when the input code is zero.

In shutdown mode, the selected DAC output is set to zero while the value stored in the DAC register remains unchanged. This removes the load from the reference input to save power. Bringing the MAX522 out of shutdown mode restores the DAC output voltage. Because the input resistance at REF is code dependent, the DAC's reference sources should have an output impedance of no more than 5 Ω . The input capacitance at the REF pin is also code dependent and typically does not exceed 25pF.

The reference voltage on REF can range anywhere from GND to V_{DD}. See the *Output Buffer Amplifiers* section for more information.

Output Buffer Amplifiers

DAC A and DAC B voltage outputs are internally buffered. The buffer amplifiers have a rail-to-rail (GND to V_{DD}) output voltage range.

The DAC outputs are internally divided by two and the buffer is set to a gain of two, eliminating the need for a buffer input voltage range to the positive supply rail.

DAC A's output amplifier can source and sink up to 5mA of current (0.5mA for DAC B's buffer). See the *Total Unadjusted Error vs. Digital Code* graph in the *Typical Operating Characteristics*. The amplifier is unity-gain stable with a capacitive load of 0.1 μ F (0.01 μ F for DAC B's buffer) or greater. The slew rate is limited by the load capacitor and is typically 0.1V/ μ s with a 0.1 μ F load (0.01 μ F for DAC B's buffer).

Shutdown Mode

When programmed to shutdown mode, the outputs of DAC A and DAC B go into a high-impedance state. Virtually no current flows into or out of the buffer amplifiers in that state. In shutdown mode, the REF inputs are high impedance (2M Ω typical) to conserve current drain from the system reference; therefore, the system reference does not have to be powered down.

Coming out of shutdown, the DAC outputs return to the values kept in the registers. The recovery time is equivalent to the DAC settling time.

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Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

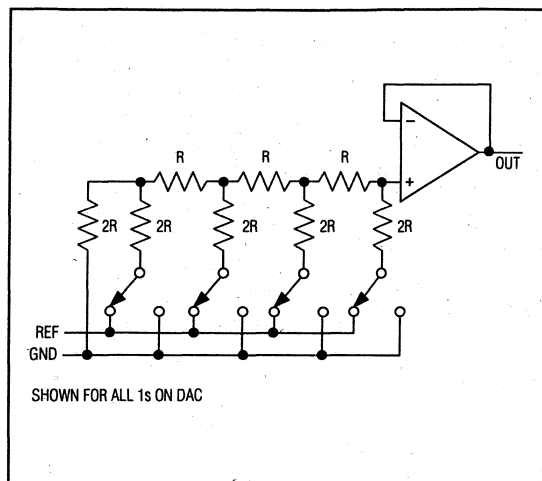


Figure 1. DAC Simplified Circuit Diagram

Serial Interface

An active-low chip select ($\overline{CS}$) enables the shift register to receive data from the serial data input. Data is clocked into the shift register on every rising edge of the serial clock signal (SCLK). The clock frequency can be as high as 5MHz.

Data is sent MSB first and can be transmitted in one 16-bit word. The write cycle can be segmented when $\overline{CS}$ is kept active (low) to allow, for example, two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, the rising edge of $\overline{CS}$ updates the DAC outputs and the shutdown status. Because of their single buffered structure, DACs cannot be simultaneously updated to different digital values.

Table 1. Input Shift Register

DATA BITS	B0*	DAC Data Bit 0 (LSB)
	B1	DAC Data Bit 1
	B2	DAC Data Bit 2
	B3	DAC Data Bit 3
	B4	DAC Data Bit 4
	B5	DAC Data Bit 5
	B6	DAC Data Bit 6
	B7	DAC Data Bit 7 (MSB)
CONTROL BITS	LA	Load Reg DAC A, Active High
	LB	Load Reg DAC B, Active High
	UB4	Uncommitted Bit 4
	SA	Shut Down DAC A, Active High
	SB	Shut Down DAC B, Active High
	UB3	Uncommitted Bit 3
	UB2	Uncommitted Bit 2
	UB1**	Uncommitted Bit 1

* Clocked in last.

**Clocked in first.

Serial-Input Data Format and Control Codes

Table 2 lists the serial-input data format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally. Every control bit performs one function. Data is clocked in starting with UB1 (Uncommitted Bit), followed by the remaining control bits and the data byte. The LSB of the data byte (B0) is the last bit clocked into the shift register (Figure 2).

Table 3 is an example of a 16-bit input word. It performs the following functions:

- 80hex (128 decimal) loaded into DAC registers A and B.
- DAC A and DAC B are active.

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

MAX522

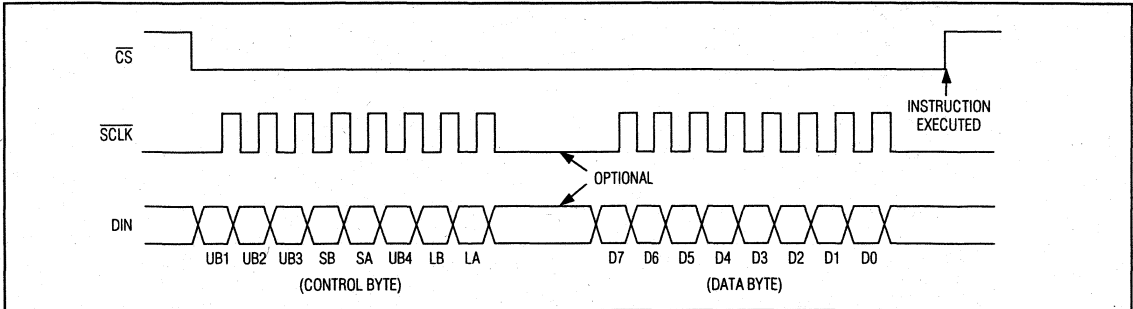


Figure 2. MAX522 3-Wire Serial-Interface Timing Diagram

Table 2. Serial-Interface Programming Commands

CONTROL								DATA								FUNCTION
UB1	UB2	UB3	SB	SA	UB4	LB	LA	B7 MSB	B6	B5	B4	B3	B2	B1	B0 LSB	
X	X	1	*	*	0	0	0	X	X	X	X	X	X	X	X	No Operation to DAC Registers
X	X	1	*	*	0	0	0									Unassigned Command
X	X	1	*	*	0	1	0	8-Bit DAC Data								Load Register to DAC B
X	X	1	*	*	0	0	1	8-Bit DAC Data								Load Register to DAC A
X	X	1	*	*	0	1	1	8-Bit DAC Data								Load Both DAC Registers
X	X	1	0	0	0	*	*	X	X	X	X	X	X	X	X	All DACs Active
X	X	1	0	0	0	*	*	X	X	X	X	X	X	X	X	Unassigned Command
X	X	1	1	0	0	*	*	X	X	X	X	X	X	X	X	Shut Down DAC B
X	X	1	0	1	0	*	*	X	X	X	X	X	X	X	X	Shut Down DAC A
X	X	1	1	1	0	*	*	X	X	X	X	X	X	X	X	Shut Down All DACs

X = Don't care.

* = Not shown, for the sake of clarity. The functions of loading and shutting down the DACs and programming the logic can be combined in a single command.

Table 3. Example of a 16-Bit Input Word

Loaded in First								Loaded in Last							
UB1	UB2	UB3	SB	SA	UB4	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0
X	X	1	0	0	0	1	1	1	0	0	0	0	0	0	0

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

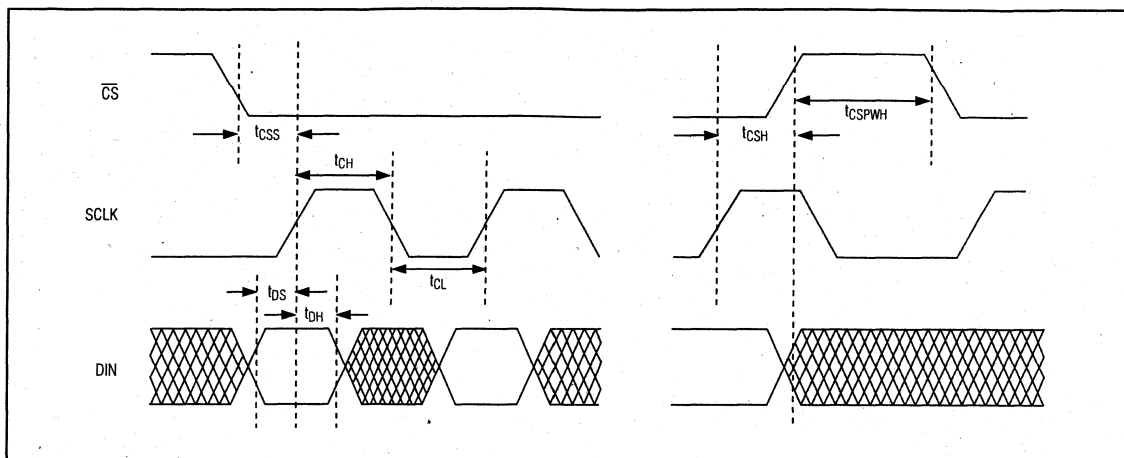


Figure 3. MAX522 Detailed Serial-Interface Timing Diagram

Digital Inputs

The digital inputs are compatible with CMOS logic. Supply current increases slightly when toggling the logic inputs through the transition zone between $(0.3)(V_{DD})$ and $(0.7)(V_{DD})$.

Microprocessor Interfacing

The MAX522 serial interface is compatible with Microwire, SPI, and QSPI. For SPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the inactive clock state to zero and CPHA = 0 changes data at the falling edge of SCLK. This setting allows SPI to run at full clock speeds (0.5MHz). If a serial port is not available on your μP , three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the voltage outputs by operating the serial clock only when necessary.

Table 4. Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF \times \left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+REF \times \left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+REF \times \left(\frac{128}{256}\right) = +\frac{REF}{2}$
0	1	1	1	1	1	1	1	$+REF \times \left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+REF \times \left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

Note:

$$1\text{LSB} = REF \times 2^{-8} = REF \times \left(\frac{1}{256}\right)$$

$$\text{ANALOG OUTPUT} = REF \times \left(\frac{D}{256}\right) \quad \text{where D = Decimal Value of Digital Input}$$

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SO Package

Applications Information

The MAX522 is specified for single-supply operation with V_{DD} ranging from 2.7V to 5.5V, covering all commonly used supply voltages in 3V and 5V systems.

Initialization

There is no internal power-on reset. Therefore, at power-up, perform an initial write operation to set the outputs to the desired voltage.

Power-Supply and Ground Management

GND should be connected to the highest quality ground available. Bypass V_{DD} with a 0.1 μ F to 0.22 μ F capacitor to GND. The reference input can be used without bypassing. For optimum line/load-transient response and noise performance, bypass the reference input with 0.1 μ F to 4.7 μ F to GND. Careful PC board layout minimizes crosstalk among DAC outputs, the reference, and digital inputs. Separate analog lines with ground traces between them. Make sure that high-frequency digital lines are not routed in parallel to analog lines.

MAX522

EVALUATION KIT
AVAILABLE

MAXIM

300Msps, 12-Bit DAC with Complementary Voltage Outputs

MAX555

General Description

The MAX555 is an advanced, monolithic, 12-bit digital-to-analog converter (DAC) with complementary 50Ω outputs. Fabricated using an oxide-isolated bipolar process, the MAX555 is designed for signal-reconstruction applications at an output update rate of 300Msps. It incorporates an analog multiplying function with 10MHz useable input bandwidth. The voltage-output DAC uses precision laser trimming to achieve 12-bit accuracy with $\pm 1/2$ LSB integral and differential linearity ($\pm 0.012\%$ FS). Absolute gain error is a low 1% of full scale. Full-scale transitions occur in less than 0.5ns. Internal registers and a unique decoder reduce glitching and allow the MAX555 to achieve precise RF performance with over 72dBc of spurious-free dynamic range at 50Msps with $f_{OUT} = 3.1$ MHz, or 58dBc at 300Msps with $f_{OUT} = 18.6$ MHz.

The MAX555 operates from a single -5.2V supply and dissipates 980mW (nominal). It comes in a 68-pin thermally enhanced PLCC package capable of accepting a heatsink.

Applications

Direct Digital Synthesis
Arbitrary Waveform Generation
HDTV/High-Resolution Graphics
Instrumentation
Communications Local Oscillators
Automated Tester Applications

Features

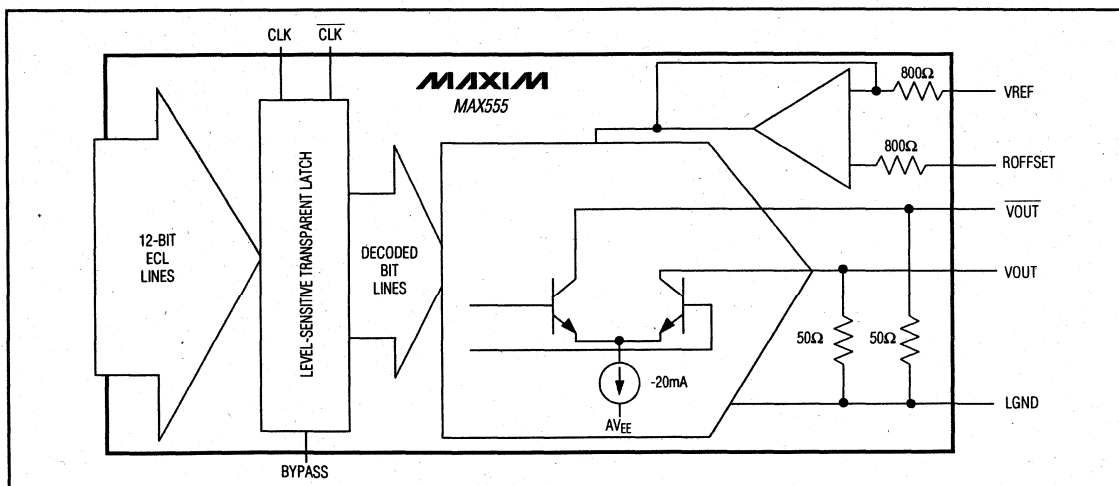
- ◆ 12-Bit Resolution
- ◆ $\pm 1/2$ LSB Integral and Differential Nonlinearity
- ◆ Capable of 300Msps Min Update Rate
- ◆ Complementary 50Ω Outputs
- ◆ Multiplying Reference Input
- ◆ Low Glitch Energy (5.6pVs)
- ◆ Single -5.2V Power Supply
- ◆ On-Chip Data Registers
- ◆ ECL-Compatible Inputs with Differential Clock

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX555CQK	0°C to +70°C	68 Thermally Enhanced PLCC

Pin Configuration appears at end of data sheet.

Simplified Block Diagram



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MAXIM

Maxim Integrated Products 9-81

Call toll free 1-800-998-8800 for literature.

300Msps, 12-Bit DAC with Complementary Voltage Outputs

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (A _{VEE})	-7V to +0.3V	Continuous Power Dissipation (T _A = +70°C)	
Digital Supply Voltage (D _{VEE})	-7V to +0.3V	(without additional heatsink)	1.3W
Digital Input Voltage (D ₀ -D ₁₁)	-5.5V to 0V	Operating Temperature Range	0°C to +70°C
Reference Input Voltage (V _{IN})	0V to +1.25V	Junction Temperature Range (Note 1)	0°C to +150°C
Reference Input Current	0mA to +1.56mA	Storage Temperature Range	-65°C to +150°C
Output Compliance Voltage (V _{OC})	-1.25V to +1.0V	Lead Temperature (soldering, 10sec)	+300°C
Output Common-Mode Voltage (V _{CM})	-0.25V to +1.0V		

Note 1: Typical thermal resistance, junction-to-case R_{θJC} = 28°C/W. See *Package Information*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(A_{VEE} = D_{VEE} = -5.2V, V_{REF} = 1.000V, T_{MIN} to T_{MAX} = 0°C to +70°C, unless otherwise noted.) (Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DC ACCURACY							
Differential Linearity Error	DLE1	VREF = 1.000V, current out, into virtual ground, end-point linearity	$\overline{V_{OUT}}$	-0.012	±0.003	0.012	% Full Scale
	DLE2		VOUT	-0.05	±0.01	0.05	% Full Scale
Integral Linearity Error	ILE1	VREF = 1.000V, current out, into virtual ground, end-point linearity	$\overline{V_{OUT}}$	-0.012	±0.006	0.012	% Full Scale
	ILE2		VOUT	-0.05	±0.01	0.05	% Full Scale
Absolute Gain Error	EG	VREF = 1.000V, voltage out, $\overline{V_{OUT}}/V_{IN}$ (Note 3)	-1.0	±0.2	1.0	% Full Scale	
12-Bit Monotonicity			Guaranteed				
Output Offset Current	Ios	D0–D11 = logic 1, VREF = 1.000V, measured at VOUT		40	100	μA	
Output Leakage Current	I _{LEAK}	D0–D11 = logic 0, VREF = 0V, measured at VOUT		3	50	μA	
TIME-DOMAIN PERFORMANCE (Note 4)							
Fall Time	tFALL	90% to 10%, TA = +25°C		510		ps	
Rise Time	tRISE	10% to 90%, TA = +25°C		450		ps	
Glitch Energy		Major carry, TA = +25°C		5.6		pVs	
Settling Time		±0.1% FSR		4		ns	
		±0.024% FSR, 1LSB change		15			
DYNAMIC PERFORMANCE (Notes 4, 5)							
Spurious-Free Dynamic Range		fOUT = 5MHz, fCLK = 50MHz		70		dBc	
		fOUT = 10MHz, fCLK = 50MHz		69			
		fOUT = 20MHz, fCLK = 100MHz		62			
		fOUT = 30MHz, fCLK = 100MHz		56			
		fOUT = 30MHz, fCLK = 200MHz		54			
		fOUT = 40MHz, fCLK = 200MHz		53			
		fOUT = 40MHz, fCLK = 250MHz		50			
		fOUT = 50MHz, fCLK = 250MHz		48			
		fOUT = 40MHz, fCLK = 300MHz		48			
		fOUT = 50MHz, fCLK = 300MHz		47			
Output Noise		Bits 0–11 high, TA = +25°C		10.6		$\frac{nV}{\sqrt{Hz}}$	

300Msps, 12-Bit DAC with Complementary Voltage Outputs

MAX555

ELECTRICAL CHARACTERISTICS (continued)

($A_{VEE} = D_{VEE} = -5.2V$, $V_{REF} = 1.000V$, T_{MIN} to $T_{MAX} = 0^{\circ}C$ to $+70^{\circ}C$, unless otherwise noted.) (Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input Current, Logic High	I_{IH}	$V_{IH} = -0.75V$		10	200	μA
Input Current, Logic Low	I_{IL}	$V_{IL} = -1.95V$		1	2	μA
Logic "1" Voltage	V_{IH}		-1.1	-0.75	0	V
Logic "0" Voltage	V_{IL}		-2.0	-1.95	-1.48	V
DIGITAL TIMING						
Data Update Rate	f_D	Minimum data rate = DC (Note 6)	300			MHz
Data-to-Clock Setup Time	t_{SU}	Bypass = 0, clocked mode (Notes 4, 7)		1		ps
Data-to-Clock Hold Time	t_{HOLD}	Bypass = 0, clocked mode (Notes 4, 7)		1.8		ns
Clock-to-VOUT Propagation Delay	t_{PD3}	Bypass = 0, clocked mode (Notes 4, 7)		2.0		ns
LSBs Data-to-VOUT Propagation Delay	t_{PD2}	Bypass = 1, transparent mode (Notes 4, 7)		1.5		ns
MSBs Data-to-VOUT Propagation Delay	t_{PD1}	Bypass = 1, transparent mode (Notes 4, 7)		2.1		ns
MSBs Decode Delay	t_{DD}	Bypass = 1, transparent mode (Notes 4, 7)		600		ps
CONTROL AMPLIFIER						
Amplifier Input Resistance	R_{IN}	$V_{REF} = 1.000V$	775	800	825	Ω
Multiplying Input Bandwidth	BW	-3dB		10		MHz
Open-Loop Gain	A_{VOL}	$T_A = +25^{\circ}C$	3	20		kV/V
Input Offset Voltage	V_{OS}	$T_A = +25^{\circ}C$	-250	0	250	μV
OUTPUT PERFORMANCE						
Full-Scale Output Current	I_{OUT}	$V_{REF} = 1.000V$, $R_L = 0\Omega$	19.0	20.0	21.0	mA
Output Resistance	R_{OUT}	V_{OUT} , $\overline{V_{OUT}}$	49.5	50.0	50.5	Ω
Output Capacitance	C_{OUT}	V_{OUT} , $\overline{V_{OUT}}$		15		pF
POWER SUPPLIES						
Analog Power-Supply Current	A_{IEE}	$A_{VEE} = D_{VEE} = -5.2V$	30	46	60	mA
Digital Power-Supply Current	D_{IEE}	$A_{VEE} = D_{VEE} = -5.2V$	110	150	190	mA
Power Dissipation	PD			0.98	1.3	W
Package Thermal Resistance, Junction to Ambient	T_{JA}			28		$^{\circ}C/W$

Note 2: All devices are 100% production tested at $+25^{\circ}C$ and are guaranteed by design for $T_A = T_{MIN}$ to T_{MAX} as specified.

Note 3: The gain-error method of calculation is shown below:

$$\begin{aligned}
 \text{Definition:} & \quad \frac{[V_{MEASURE}(FS) - V_{IDEAL}(FS)] \times 100}{V_{IDEAL}(FS)} \\
 \text{EG}(\%) = & \quad \frac{[V_{MEASURE}(FS) - V_{IDEAL}(FS)] \times 100}{V_{IDEAL}(FS)} \\
 \text{where FS indicates full-scale measurements.} & \quad \text{EG Method:} \\
 & \quad EG = \frac{[(4096 / 4095) V_{MEASURE} - 16(V_{REF} / R_{IN}) (R_{OUT})] \times 100}{16(V_{REF} / R_{IN}) (R_{OUT})} \% \\
 & \quad = \frac{[(4096 / 4095) V_{MEASURE} - 1] \times 100}{1} \% \\
 & \quad \text{where: } V_{REF} = 1.000V, R_{IN} = 800\Omega, R_{OUT} = 50\Omega, V_{MEASURE} = \overline{V_{OUT}} (FS).
 \end{aligned}$$

Note 4: Dynamic and timing specifications are obtained from device characterization and simulation testing and are not production tested.

Note 5: Spurious-free dynamic range is measured from the fundamental frequency to any harmonic or non-harmonic spurs within the bandwidth $f_{CLK}/2$, unless otherwise specified.

Note 6: Guaranteed by design.

Note 7: Timing definitions are detailed in Figure 2.

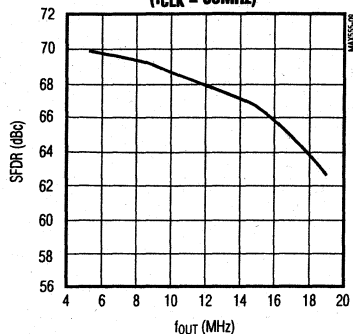
9

300Mps, 12-Bit DAC with Complementary Voltage Outputs

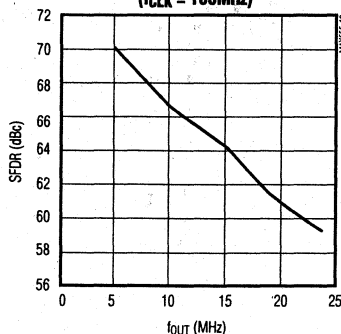
Typical Operating Characteristics

(VREF = 0.75V, T_A = +25°C, unless otherwise noted.)

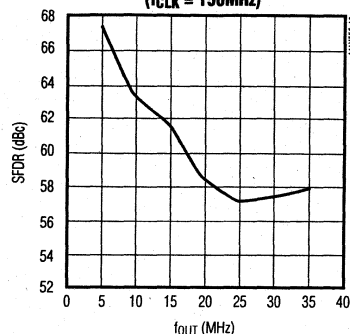
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vs. OUTPUT FREQUENCY
(f_{CLK} = 50MHz)**



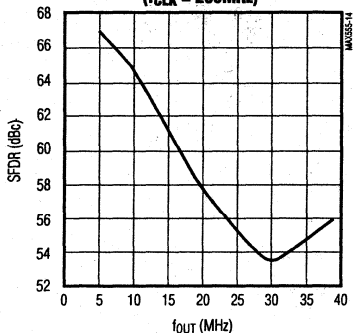
**SPURIOUS-FREE DYNAMIC RANGE
vs. OUTPUT FREQUENCY
(f_{CLK} = 100MHz)**



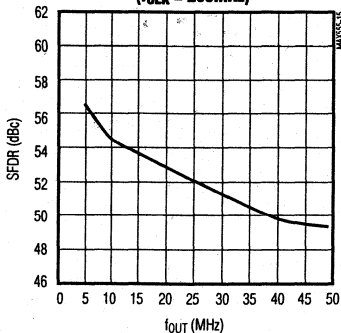
**SPURIOUS-FREE DYNAMIC RANGE
vs. OUTPUT FREQUENCY
(f_{CLK} = 150MHz)**



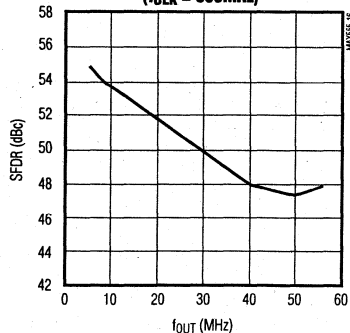
**SPURIOUS-FREE DYNAMIC RANGE
vs. OUTPUT FREQUENCY
(f_{CLK} = 200MHz)**



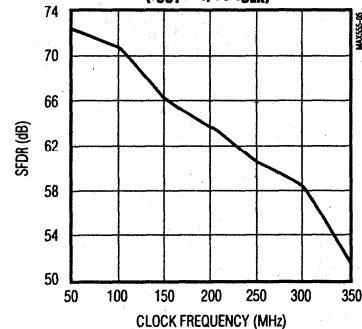
**SPURIOUS-FREE DYNAMIC RANGE
vs. OUTPUT FREQUENCY
(f_{CLK} = 250MHz)**



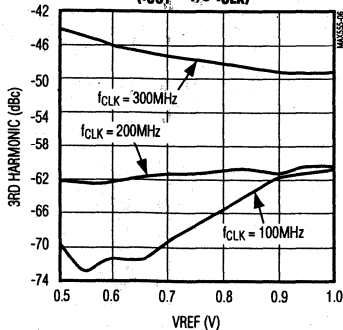
**SPURIOUS-FREE DYNAMIC RANGE
vs. OUTPUT FREQUENCY
(f_{CLK} = 300MHz)**



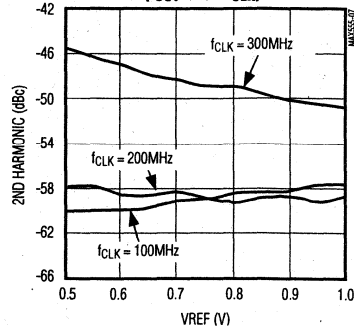
**SPURIOUS-FREE DYNAMIC RANGE
vs. CLOCK FREQUENCY
(f_{OUT} ~ 1/16 f_{CLK})**



**3RD HARMONIC DISTORTION
vs. VREF VOLTAGE
(f_{OUT} ~ 1/5 f_{CLK})**



**2ND HARMONIC DISTORTION
vs. VREF VOLTAGE
(f_{OUT} ~ 1/5 f_{CLK})**



300Msps, 12-Bit DAC with Complementary Voltage Outputs

MAX555

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Pin Description

PIN	NAME	FUNCTION
1	BYPASS	Disables latching of data when high (ECL input)
2	CLK	Data Clock (ECL input)
3	$\overline{\text{CLK}}$	Data Clock Not (ECL input)
4, 56, 57, 63, 66	DGND	Digital Signal Grounds
5, 55	DVEE	-5.2V Digital Power Supplies
10, 11, 12, 21–25, 27, 31, 36, 37, 40, 41, 43, 45, 46, 61	N.C.	No Connection
13, 14	VOUT	DAC Outputs
15, 16	LGND	Ladder Grounds
17, 18	$\overline{\text{VOUT}}$	DAC Output Complements
19, 49, 51, 52, 53, 68	TN	Test Node—internal test point, do not connect
20, 29, 30, 48	AGND	Analog Signal Grounds
26, 44	HS	Heatspreader Connections—bypass with 0.1 μ F to AVEE
28	ALTCOMPIB	PTAT-IB Reference Compensation Output (connect bypass capacitor to AVEE)
32	LOOPCRNT	Test node—must connect to AGND
33, 34	AVEE	-5.2V Analog Power Supplies
35	VREF/2	Analog Reference Voltage Center-Tap Input
38, 39	VREF	Analog Reference Voltage Inputs (Kelvin connection)
42	ROFFSET	Offset Compensation Input
47	ALTCOMPC	Control-Amplifier PTAT Reference Compensation Input (connect bypass capacitor to AVEE)
50	LBIAS	Ladder-Bias Alternate Compensation Output (connect bypass capacitor to AVEE)
54, 58, 59, 60, 62, 64, 65, 67, 6, 7, 8, 9	D11(MSB)–D0(LSB)	Data Words (ECL inputs)

Detailed Description

Figure 1's functional diagram shows the MAX555's three-major divisions: a digital section, a control-amplifier section, and a resistor-divider network. The digital section consists of a master/slave register, decoding logic, and current switches. The control-amplifier section includes a control amplifier and an array of 23 current sources divided into three groups. The resistor divider scales the currents from these groups to achieve the correct binary weighting at the output. The output of the resistor-divider network is laser trimmed to 50 Ω , a key feature for driving into controlled impedance transmission lines.

The first group of current sources comprises the six MSBs, D11–D6 (resulting in 15 identical, plus two binary weighted currents), which are applied directly to the output of the resistor-divider network. The second group, bits D5–D3 (three binary weighted currents), is applied to the middle of the divider network. The middle of the network divides the current seen at the output by 8. The third group, bits D2–D0 (three additional binary weighted current sources), is applied to the input of the resistive network, dividing the current seen at the output by 64.

Glitching is reduced by decoding the four MSBs into 15 identical current sources and synchronizing data with a master/slave register at every current switch. Data bits are transferred to the output on the positive-going edge of the clock, with the BYPASS input asserted low. In the asynchronous mode with the BYPASS input asserted high, the latches are transparent and data is transferred to the output regardless of the clock state. All digital inputs are ECL compatible. The clock input is differential.

The control amplifier forces a reference current, which is replicated in the current sources. This reference current is nominally 1.25mA. It can be supplied by an external current source, or by an external voltage source of 1.000V applied to the VREF input.

A reference input of VREF = 1.000V will produce a full-scale output voltage of VFS = -1.000V; where:

$$V_{FS} = 4096 / 4095 \times \overline{\text{VOUT}} \text{ (code 0)}$$

for the $\overline{\text{VOUT}}$ output. The output coding is summarized in Table 1.

The DAC's control amplifier has a typical open-loop voltage gain of 85dB, and its gain-magnitude bandwidth is flat up to 10MHz. When the control amplifier is not being used for high-speed multiplying applications, it is recommended that a 0.4 μ F capacitor be connected from LBIAS to AVEE to increase control-amplifier stability and reduce current-source noise.

300Mbps, 12-Bit DAC with Complementary Voltage Outputs

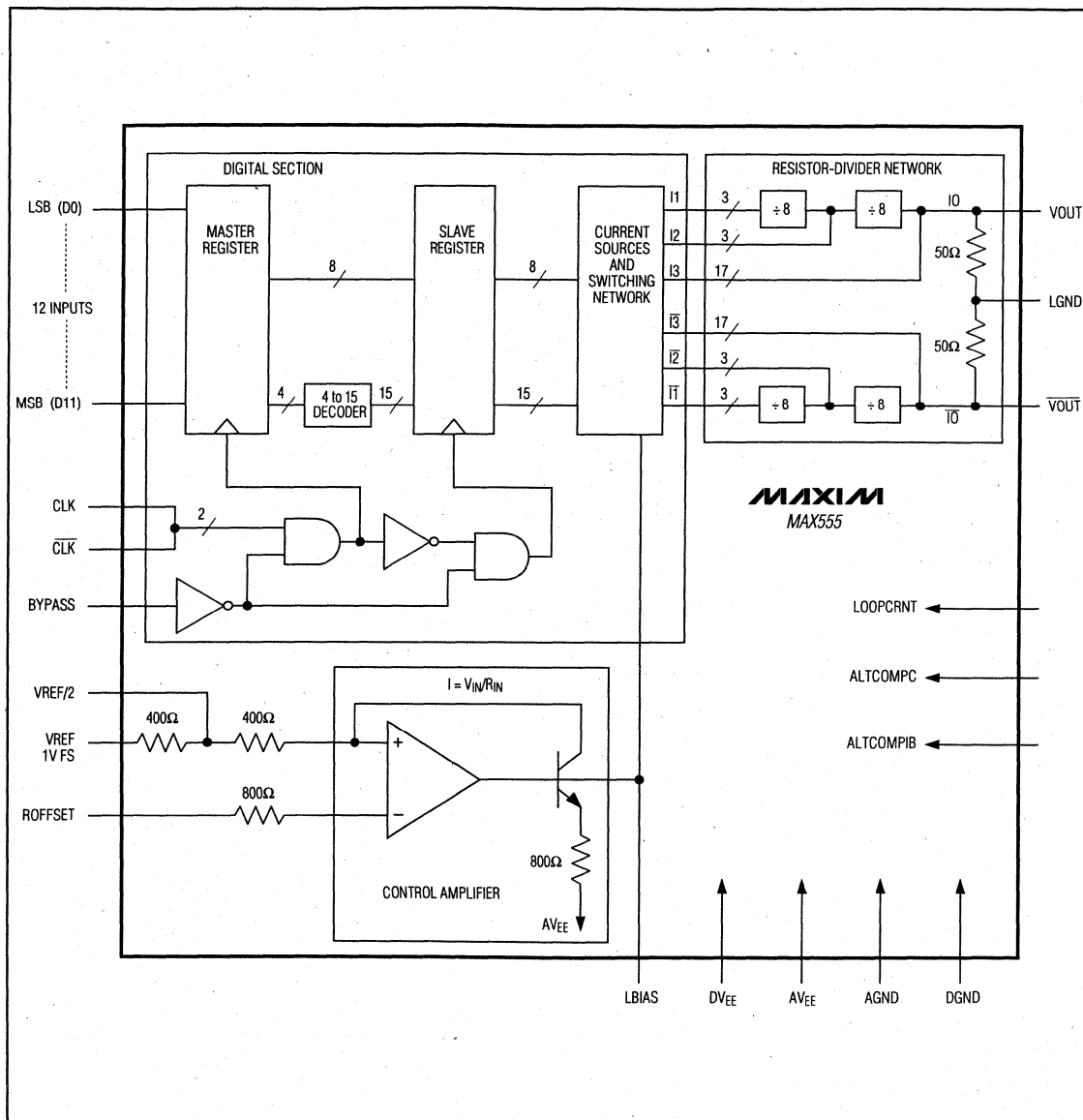


Figure 1. Functional Diagram

300Msps, 12-Bit DAC with Complementary Voltage Outputs

MAX555

Table 1. Output Coding

DIGITAL CODE (D11-D0)	V _{OUT} (V)	V _{OUT} (V)
000000000000	-0.999756	0
000000000001	-0.999512	-0.000244
011111111111	-0.500000	-0.499756
100000000000	-0.499756	-0.500000
111111111111	0	-0.999756

Timing Information

The MAX555 features a differential ECL clock input with selective transparent operation (BYPASS = 1). It is possible to drive the MAX555 clock single-ended if desired by tying the $\overline{\text{CLK}}$ input to an external voltage of -1.3V (ECL V_{BB}). However, using a differential clock provides greater noise immunity and improved dynamic performance.

In the clocked mode (BYPASS = 0), when the clock line is low, the slave register is locked out and information on the digital inputs is permitted to enter the master register. The clock transition from low to high locks the master register in its present state and ignores further changes on the digital inputs. This transition simultaneously transfers the contents of the master register to the slave register, causing the DAC output to change.

Figure 2's timing diagram illustrates the importance of operating the MAX555 in the clocked mode. In the transparent mode (BYPASS = 1), both the master and slave registers are transparent, and changes in input data rip-

ple directly to the output. Because the four MSBs are decoded into 15 identical currents, there is a decode delay for these bits that is longer than for the eight LSBs. For the full-scale transition case shown, an intermediate output of 1/16 full-scale occurs until the four MSBs are properly decoded. This decode delay seriously degrades the device's spurious performance. In addition, skew in the timing of the input data also directly appears at the DAC output, further degrading high-speed performance.

MAX555 operation in the clocked mode (BYPASS = 0) with a differential clock precludes both of these potential problems and is required for high-speed operation. Since input data can only enter the master register when the clock is low (while the slave register is locked out), data-bus timing skew and the internal MBS decode delay will not appear at the DAC output. The DAC currents are switched only when the clock transitions from low to high, after the internal data stabilizes.

Layout and Power Supplies

The MAX555 has separate pins for analog and digital supplies. A_{VEE} and D_{VEE} are connected to each other through the substrate of the IC. These potentials should be derived from the same supply to minimize voltage mismatch, which would cause substrate current flow and possible latchup. Appropriate decoupling is needed to prevent digital-section current spikes from affecting the analog section (Figure 4).

It is recommended that a multilayer PC board be used, containing a solid ground and power planes. All analog

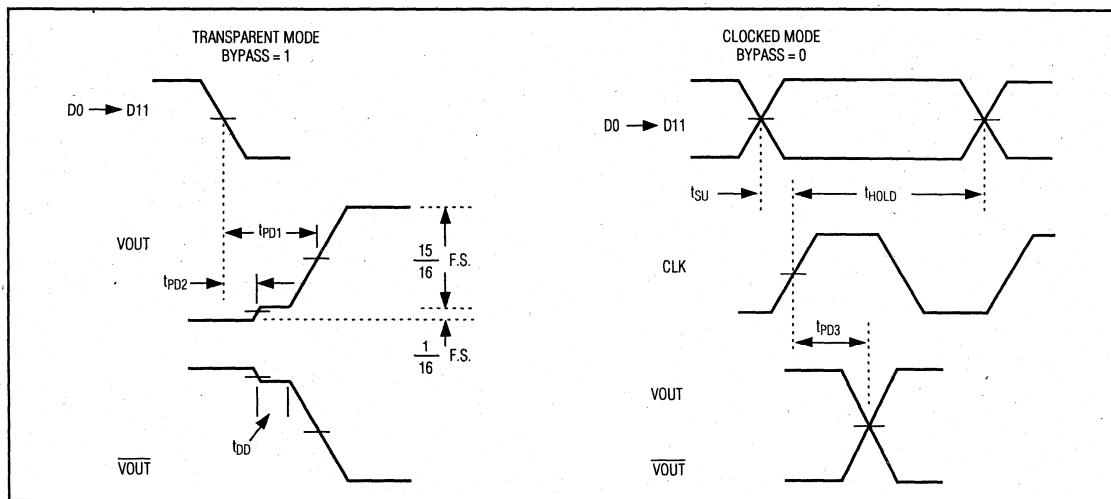


Figure 2. Timing Diagram

300Mps, 12-Bit DAC with Complementary Voltage Outputs

and digital ground pins must be connected directly to the analog ground plane at the MAX555, preferably with a "star connection" at the LGND pins (15 and 16).

High-speed ECL inputs, as well as the output from the MAX555, should employ good transmission-line techniques, with terminations close to the device pins. Separate power-supply buses for analog and digital power supplies are recommended as good general practice. Best results will be achieved by bypassing the device pins with high-quality ceramic chip capacitors connected physically close to the pins.

Applications Information

Reference Input

The MAX555 uses an internal op-amp circuit to buffer the reference current. The input to the op amp may be driven with a 1.25mA external current source or a 1V external voltage reference. The reference input is the VREF pin. The input impedance to the op amp is 800 Ω . As shown in Figure 1, VREF/2 is brought out externally with 400 Ω of impedance to the op amp. These reference inputs can be used to vary the full-scale output for high-speed multiplying applications. ROFFSET must be connected to analog ground. In addition, a 0.1 μ F capacitor should be connected from VREF/2 to analog ground to reduce reference current noise.

Outputs

The analog outputs are laser trimmed to 50 Ω . They can be used either as a voltage drive with 50 Ω impedance, or to drive into a virtual null using a transimpedance amplifier. Greater speed is achieved driving into 50 Ω loads. The differential outputs of the MAX555 may be used to drive a balun for conversion to a single-ended output, while at the same time greatly reducing the second-harmonic content of the output.

Dynamic Performance

The *Typical Operating Characteristics* graphs show the MAX555's performance when used in direct digital synthesis (DDS) applications for generating RF sine waves. The first six graphs show the MAX555's spurious-free dynamic range (SFDR) for clock frequencies of 50MHz to 300MHz at various output frequencies. The seventh graph shows the SFDR for clock frequencies from 50MHz to 350MHz while producing an output frequency of about 1/16 the clock frequency.

The last two graphs show the MAX555's third and second harmonic distortion while producing an output frequency of about 1/5 fCLK for clock frequencies from 100MHz to 300MHz as a function of the reference voltage. The third harmonic content of the output can be reduced at clock frequencies below about 200MHz by

reducing the reference voltage from its 1.000V nominal value. At clock frequencies above about 200MHz, the output's third harmonic content is dominated by coupling from the high-speed digital inputs to the output. Reducing the reference voltage at these high clock rates actually increases the third harmonic distortion in the output, since the carrier amplitude drops but the third harmonic level remains relatively constant.

The second harmonic distortion of the outputs is shown as a function of clock frequency and reference voltage. It is relatively constant for clock frequencies below about 200MHz at different VREF values. As with the third harmonic distortion however, the second harmonic distortion also increases at clock frequencies over 200MHz for lower VREF values. Minimize these effects by bypassing the MAX555 heatspreader (pins 26 and 44) to VEE with a good quality RF chip capacitor. Reducing the swing of the input logic levels and/or decreasing the rise time of the digital signals can also improve the output's harmonic content. Combining these techniques achieves the best results. Some experimentation may be required to optimize the MAX555's performance for a particular application.

Figure 3 shows the spectrum analyzer plots of the MAX555 when used in DDS applications. These plots show the MAX555's output spectrum at clock frequencies from 50MHz to 300MHz while producing various output frequencies. Observing the output spectrum while adjusting the reference voltage or varying the logic levels is a sensitive method of optimizing MAX555 performance. The plots shown were obtained with a +0.75V reference voltage with 500mV ECL logic swings.

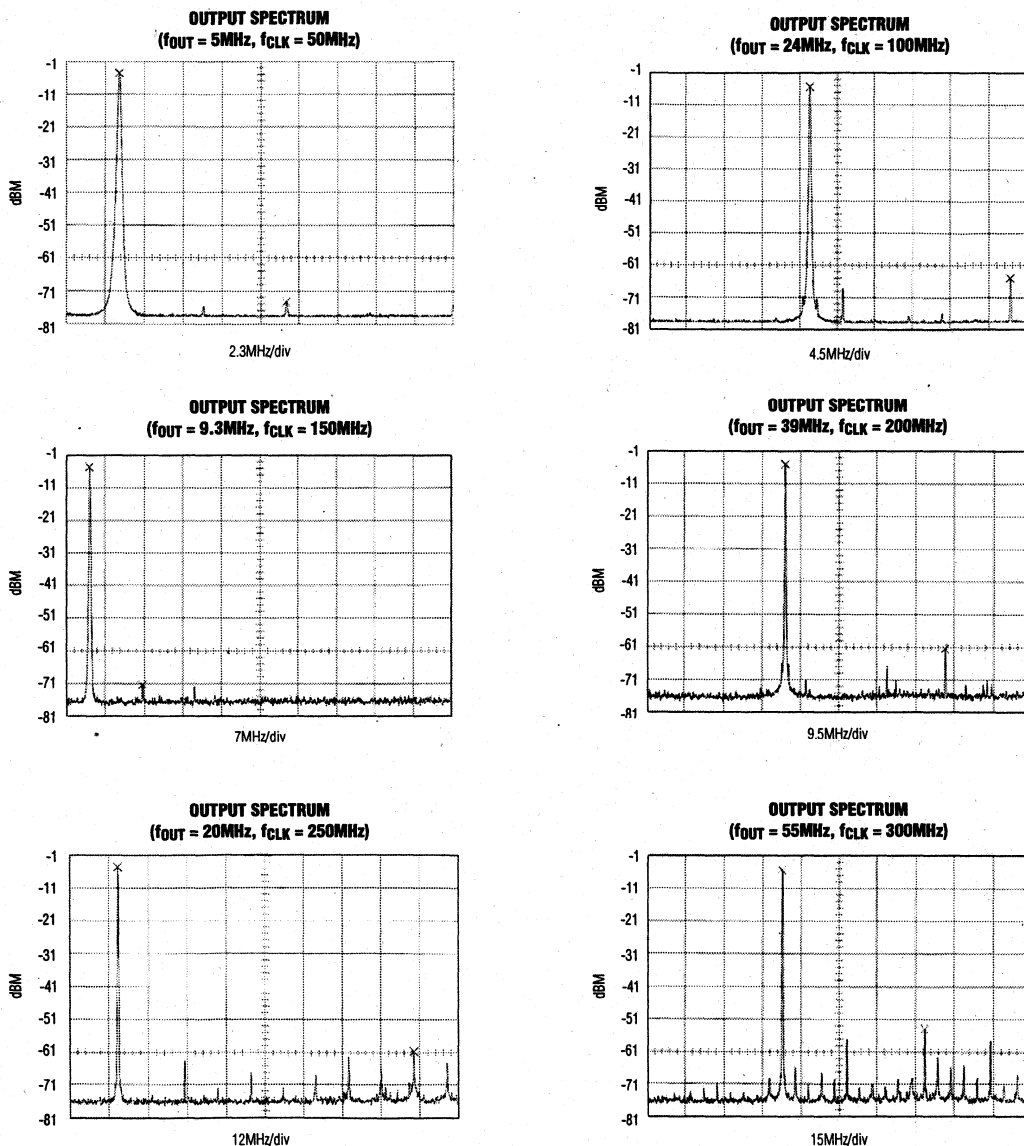
Typical Application

Figure 4 shows a typical connection. With VOUT used to drive a 50 Ω line, the unused complementary output, VOUT, should also be terminated to 50 Ω . A 1V reference voltage at VREF gives a -0.5V full-scale voltage at VOUT (when doubly terminated with 50 Ω on the output). Because some loads may represent a complex impedance, be sure to match the output impedance with the load. Mismatching the impedances can cause reflections that will affect AC-performance parameters.

In all applications, the LOOPCRNT pin is always connected to AGND, and compensation capacitors are connected to pins ALTCOMPC, ALTCOMPIB, and LBIAS. The LBIAS compensation is recommended for non-multiplying applications. AC grounding the heat spreader on the package (with pins 26 and 44) reduces digital noise feedthrough and improves the MAX555's spurious performance at high data rates.

300Mps, 12-Bit DAC with Complementary Voltage Outputs

MAX555



Measurement Conditions: 10dB/div vertical display, 300Hz video filter, TEK2755AP spectrum analyzer $V_{REF} = 0.75\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

Figure 3. Spectrum Analyzer Plots

300Mbps, 12-Bit DAC with Complementary Voltage Outputs

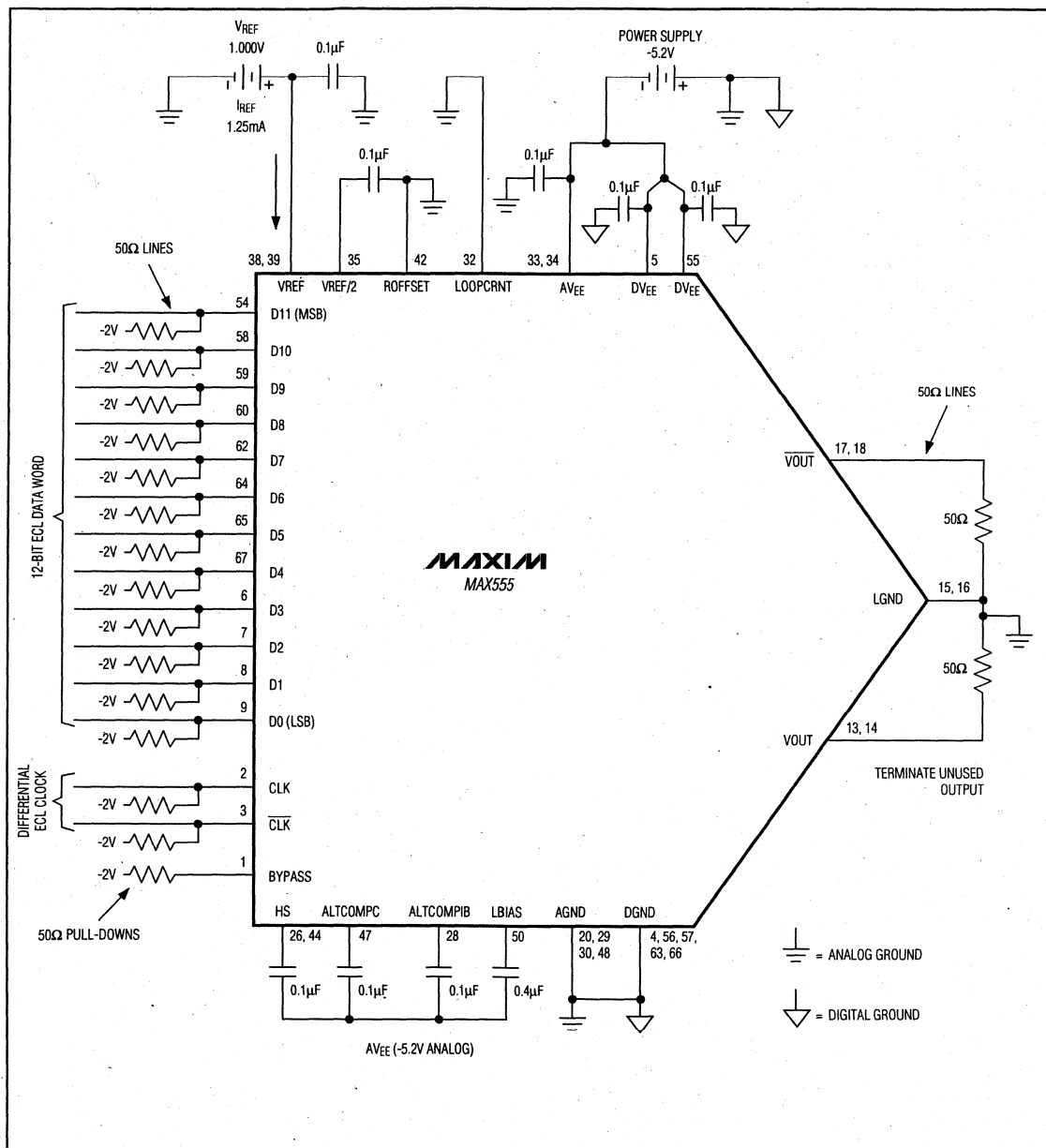


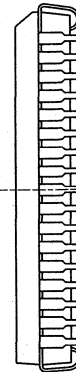
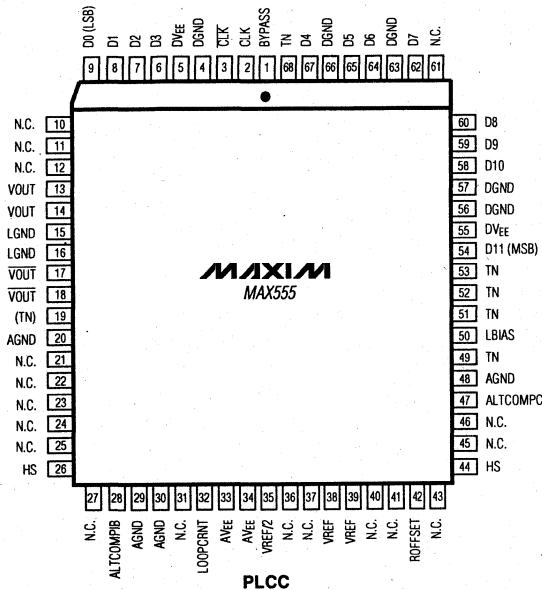
Figure 4. Typical Application

300Msps, 12-Bit DAC with Complementary Voltage Outputs

Pin Configuration

MAX555

TOP VIEW





Wireless/RF Products

Wireless/RF Products, Product Table	10-2
MAX2100 Quadrature Digitizer Circuits	10-3
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MAX2402 800MHz to 1000MHz Spread-Spectrum Transmitter	10-33
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MAX2452 70MHz Modulator*	10-45

*Advance Information—first page of data sheet in preparation.

Wireless RF Products

Part Number	Supply Voltage (V)	IF Frequency (MHz)	IF Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	AGC Range (dB)	Pins- Package Options*	Features	Applications	Price† 25,000-up (\$)
SATELLITE RECEIVER PRODUCTS										
MAX2101	4.75 to 5.25	400 to 700	60	0.5	1.5	40	100-MQFP	I/Q demodulator with dual 5th-order Butterworth filters, 10MHz to 30MHz bandwidth, and dual 6-bit ADCs	DBS, VSAT	11.49

Part Number	Supply Voltage (V)	Supply Current (mA)	IF Frequency (MHz)	IF Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	Pins- Package Options*	Features	Applications	Price† 1000-up (\$)
MODULATORS AND DEMODULATORS										
MAX2450	2.7 to 3.3	9	70	10	0.3	3	20-SO	70MHz I/Q modulator/demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	††
MAX2451	2.7 to 3.3	8.5	70	10	0.3	3	16-SO	70MHz I/Q demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	††
MAX2452	2.7 to 3.3	7.5	70	10	0.3	3	16-SO	70MHz I/Q modulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	††

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Output Power (mW)	Power Control (dB)	Class	Pins- Package Options*	Features	Applications	Price† 1000-up (\$)
TRANSMITTERS AND POWER AMPLIFIERS									
MAX2402	4.75 to 5.5	800 to 1000	100	40	AB to B, adj.	20-SSOP	Power amplifier with balanced modulator, linear modulation to 2V, shutdown mode	ISM spread spectrum, DS, FH, BPSK, ASK, FSK	3.78
MAX2430	3 to 5	800 to 1000	100 @ 3V	32	AB	16-SO	Power amplifier with 100mW at 3V, power on/off ramp control, 30dB gain, shutdown mode	900MHz cordless phones, cellular PA predrivers	††

* Package Options: MQDP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

NOTES: IF = Intermediate Frequency
I/Q = In-Phase/Quadrature-Phase
AGC = Automatic Gain Control

MAXIM

Quadrature Digitizer Circuits

General Description

The MAX2100 family of quadrature digitizers offers complete solutions to digital demodulation problems. The flagship of the MAX2100 family is the MAX2101 6-bit Quadrature Digitizer. The subcircuits derived from the MAX2101 provide excellent starting points for the RF IC designer to develop components that bridge the gap between existing RF downconverters and CMOS digital signal processors.

Each MAX2100 subcircuit comes with a detailed schematic, TEKSPICE or PSPICE netlist, models, and GDSII layout for incorporation in your own custom ASIC design. These subcircuits can be used separately or in combination to produce complete demodulation and digitization components for intermediate frequencies (IF) ranging from 70MHz to 700MHz, and for base bandwidths to 80MHz*. All are powered by a +5V supply, and are implemented in Maxim's proprietary GST-1 wafer fabrication process with NPN $f_T = 13\text{GHz}$.

Maxim does not guarantee specifications or fitness for use of these subcircuits in your custom ASIC. The subcircuits are intended to demonstrate Maxim's process and design capability, and to provide circuit designers with a "head start" in developing their own ASIC. Operation of these subcircuits in a customer-designed ASIC is the responsibility of the customer.

Applications

Recovery of PSK and QAM Modulated RF Carriers
Direct-Broadcast Satellite (DBS) Systems
Television Receive-Only (TVRO) Systems
Cable Television (CATV) Systems

Features

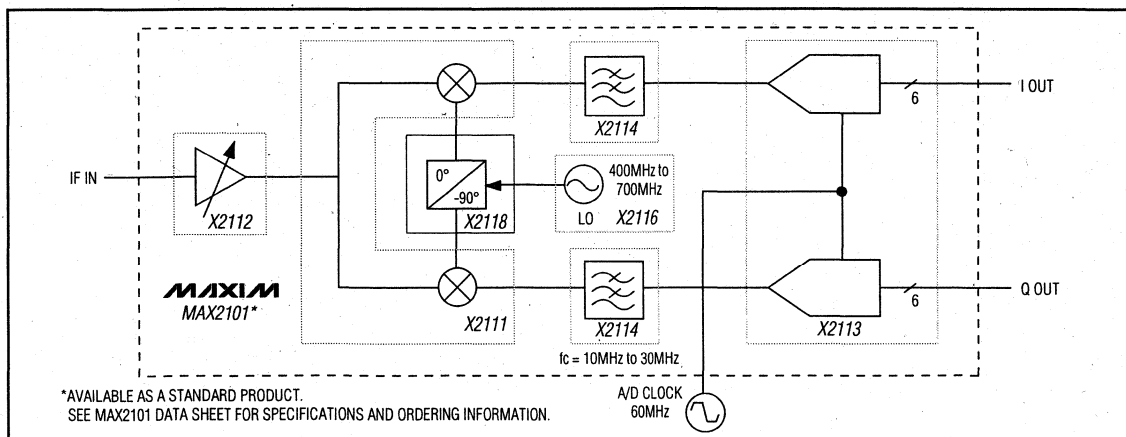
- ♦ Operation at IFs from 70MHz to 700MHz*
- ♦ Precision Quadrature Demodulation (1° , 0.2dB typ Mismatch, $f = 650\text{MHz}$)
- ♦ Matched Active Filters with Electronically Variable Cutoff from 10MHz to 30MHz
- ♦ 40dB of AGC Range
- ♦ High-Speed 6-Bit ADCs with 5.8 (typ) Effective Bits ($f_{IN} = 30\text{MHz}$, $f_c = 120\text{Msps}$) and 200MHz Input Bandwidth

Ordering Information

PART	SIMULATOR	MEDIUM	FORMAT
X21nnPFD	PSPICE	3.5" Floppy	DOS
X21nnPFT	PSPICE	3.5" Floppy	TAR
X21nnPTT	PSPICE	Tape	TAR
X21nnPHT	PSPICE	9-track 6250 bpi	TAR
X21nnPLT	PSPICE	9-track 1600 bpi	TAR
X21nnPET	PSPICE	Electronic mail	TAR
X21nnTFT	TEKSPICE	3.5" Floppy	TAR
X21nnTTT	TEKSPICE	Tape	TAR
X21nnTHT	TEKSPICE	9-track 6250 bpi	TAR
X21nnTLT	TEKSPICE	9-track 1600 bpi	TAR
X21nnTET	TEKSPICE	Electronic mail	TAR

The MAX2100 cells are available in the above formats to customers who have purchased a GST-1 ASIC Start-Up Package and signed Maxim's Non-Disclosure Agreement.

Block Diagram



*VCO and Quadrature Generator limited to 400MHz to 700MHz

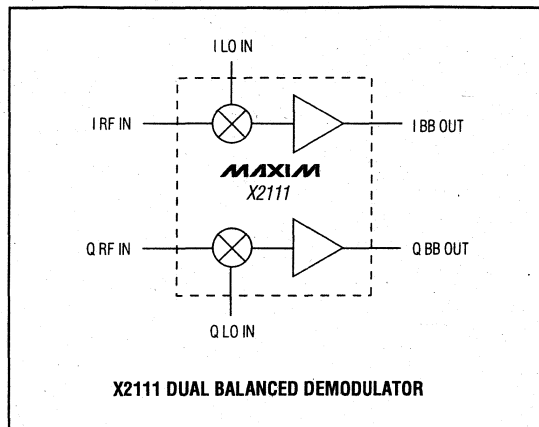
MAXIM

Maxim Integrated Products 10-3

Call toll free 1-800-998-8800 for free samples or literature.

Dual Balanced Demodulator

Block Diagram



Features

- ◆ Wide Output Bandwidth (>80MHz)
- ◆ Matched Demodulation to 700MHz
- ◆ 10dB Conversion Gain

Description

The X2111 Dual Balanced Demodulator cell comprises two Gilbert-cell, double-balanced mixers. In combination with the X2118 precision quadrature generator, the X2111 provides precise quadrature demodulation of QPSK and QAM modulated carriers to 700MHz.

Cell Dimensions: 2 x [300µm x 230µm]

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

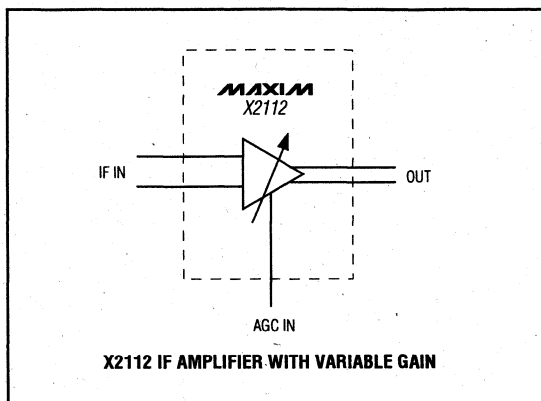
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5V						
LO Input Frequency	f _{LO}		400		700	MHz
Output Baseband Gain Flatness		5Hz to 20MHz			0.4	dB
I/Q Amplitude Imbalance	ΔM(I/Q)	f _{LO} = 650MHz			0.4	dB
I/Q Phase Imbalance	Δφ(I/Q)	f _{LO} = 650MHz			1.5	°
Noise Figure	NF	f _{LO} = 650MHz			15	dB
Conversion Gain	A	f _{LO} = 650MHz	10			dB
Input Third-Order Intercept	IIP3	f _{LO} = 650MHz	+10			dBm
Supply Current	I _{CC}			18		mA
Output Bandwidth	f _{-3dB}		80			MHz

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V _{CC} (I/Q)	+5V supply to I/Q mixer	SUB	Substrate connection (GND)
BIAS (I/Q)	500µA PTAT reference current input (from X2112 or equivalent)	OSC (I/Q)	+ LO input
V _{EE} (I/Q)	GND for I/Q mixer	OSCB (I/Q)	- LO input
IP (I/Q)	+ RF input	OPA (I/Q)	+ Baseband output
IPB (I/Q)	- RF input	OPAB (I/Q)	- Baseband output

IF Amplifier with Variable Gain

Block Diagram



Features

- ♦ 24dB Gain
- ♦ 800MHz Bandwidth
- ♦ Over 40dB of Gain Range

Description

The X2112 IF Amplifier with Variable Gain cell comprises a differential input amplifier with 10dB insertion gain, an AGC amp with 40dB of control range, and a second IF amp with 12dB gain. The differential input can be driven single-ended by proper AC grounding or by terminating the inverting input. There is sufficient linearity to provide IIP3 of +10dBm at minimum AGC setting.

Cell Dimensions: 780μm x 725μm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

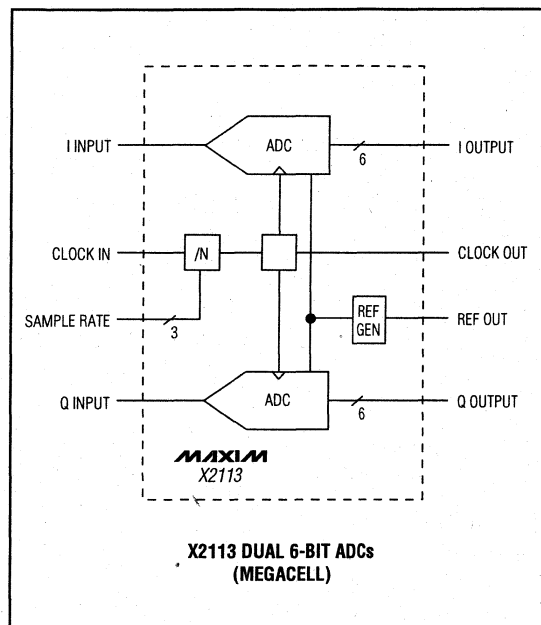
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%, R_L = 1kΩ, C_L = 2pF						
Bandwidth (-3dB)	BW-3dB	Max gain, Pin = -48dBm		800		MHz
Maximum Gain	AVmax	f = 650MHz, V _{AGC} = max	22			dB
Minimum Gain	AVmin	f = 650MHz, V _{AGC} = min			-18	dB
Gain-Control Range	ΔAV	f = 650MHz	40			dB
Noise Figure	NF	f = 650MHz, V _{AGC} = max		15	18	dB
Noise-Figure Variation	ΔNF	Max gain to min gain			1	dB/dB
Input Third-Order Intercept	IIP3	f = 650MHz, max gain	-35			dBm
		f = 650MHz, min gain	+10			
Input VSWR		Z ₀ = 50Ω/side			2:1	
Output VSWR		Z ₀ = 50Ω/side			2:1	
Supply Current	I _{CC}			20		mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V _{CC}	+5V supply	AGCIP	AGC control voltage input
V _{EE}	Ground	2R5	Bandgap-derived 2.5V output
SUB	Substrate connection (ground)	OP	+ IF output
IP	+ IF input	OPB	- IF output
IPB	- IF input	BGR	Bandgap reference (1.2V) output
K250	250μA constant reference current for X2118	VPTAT	Voltage proportional to absolute T output
P250	250μA PTAT reference current for X2118	(I/Q)BIAS	250μA PTAT reference current for X2114
MIX(I/Q)	500μA PTAT reference current for X2111		

Dual 6-Bit ADCs (Megacell)

Block Diagram



Features

- ◆ Dual, 6-Bit, 120Msps Flash Architecture
- ◆ Programmable Sample Rate
- ◆ Excellent Dynamic Performance
(5.8 effective bits at $f_{IN} = 30\text{MHz}$)
- ◆ Low Incidence of Metastable States
- ◆ All Reference Generation Circuitry Included

Description

The X2113 "Megacell" contains two 6-bit flash ADCs and associated reference and clock generation circuitry. The comparator array in each ADC contains 63 identical differential comparator and latch cells. The proprietary differential architecture minimizes integral linearity error and the occurrence of metastable states. The thermometer code output of the comparator array is translated into gray code using a fully differential wired-AND/wired-OR scheme. This maximizes noise immunity. The gray code is then converted to binary using a modified XOR array.

The reference generator applies a precision bandgap signal to the differential ladder in the comparator array. Additional circuitry is provided to adjust the half-scale ladder voltage to the common-mode voltage of the differential input signal.

A programmable divider allows the user to change sample rate from a fixed external-clock oscillator.

Cell Dimensions: 2800 μm x 1500 μm

KEY ELECTRICAL CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC} = 5.0\text{V} \pm 5\%$						
Maximum Sample Rate, Each Channel	SRmax		120			Msps
0.1dB Bandwidth	BW0.1dB		20			MHz
Effective Number of Bits	ENOB	$f_{IN} = 30\text{MHz}$, $f_s = 60\text{Msps}$, 95% FS		5.8		Bits
Input Third-Order Intermod	IM3	$f_1 = 10\text{MHz}$, FS-7dB; $f_2 = 12\text{MHz}$, FS-7dB		-38		dBc
Settling Time	tTRAN	Full-scale to <1%			10	ns
Full-Scale Input Range	ΔV_{INFS}			± 0.75		V
Common-Mode Input Range	V_{INcm}		2.25		2.75	V
Input Resistance	RIN		5			k Ω
Input Capacitance	CIN				2	pF
Amplitude Response Mismatch	ΔA	Channel-to-channel			0.3	dB
Aperture Uncertainty		$f_s = 60\text{Msps}$			80	ps
Aperture Delay Match, Channel-to-Channel					20	ps

Dual 6-Bit ADCs (Megacell)

KEY ELECTRICAL CHARACTERISTICS (continued)

(T_A = 0°C to +70°C, unless otherwise noted.)

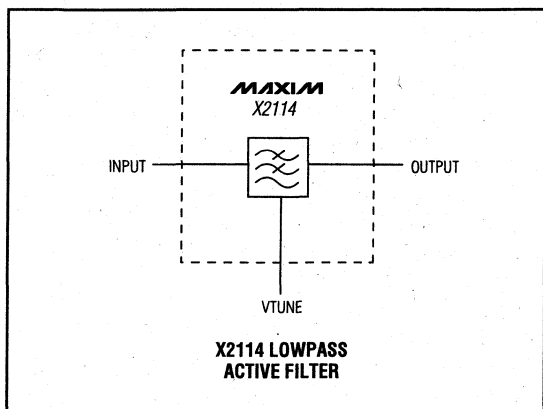
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset	V _{OS}	LSB = 24mV, either channel			0.5	LSB
Differential Nonlinearity	DNL				0.5	LSB
Integral Nonlinearity	INL				0.5	LSB
Data Output High	V _{OH}	R _L = 1MΩ, C _L = 15pF	2.4			V
Data Output Low	V _{OL}	R _L = 1MΩ, C _L = 15pF			0.5	V
Supply Current	I _{CC}			80	100	mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V _{CC} AD	+5V supply, quantizer	AIN (I/Q)	+ Analog input
V _{CC} D	+5V supply, digital	AINB (I/Q)	- Analog input
V _{CC} O	+5V supply, outputs	BGR	Bandgap reference output
V _{CC} C	+5V supply, clock	D0 (I/Q)	Digital output, LSB
SUBA	Substrate (ground), analog	D1 (I/Q)	Digital output
SUBD	Substrate (ground), digital	D2 (I/Q)	Digital output
VGNDAD	Ground connection, quantizer	D3 (I/Q)	Digital output
VGND DD	Ground connection, encoder	D4 (I/Q)	Digital output
VGND DO	Ground connection, output	D5 (I/Q)	Digital output, MSB
VGND C	Ground connection, clock	BINEN	Binary enable/Two's complement
MCLK	Master clock input	S2	Programmable sample-rate control, MSB
RCLK	Reference clock (div 6) output	S1	Programmable sample-rate control
DCLK	Data clock output	S0	Programmable sample-rate control, LSB
DCLKB	Data clock complement output	P250 (I/Q)	250μA PTAT reference current input (from cell X2114 or equivalent)

Active Lowpass Filter

Block Diagram



Features

- ◆ 5-Pole Butterworth Response
- ◆ Adjustable Cutoff Frequency
- ◆ No External Components Required

Description

The X2114 cell is an Active Lowpass Filter for anti-aliasing. The 5th-order Butterworth response is realized using a Gyrator topology. Cutoff frequency can be adjusted from 10MHz to 30MHz. Other pole-only filter characteristics, as well as different cutoff frequency ranges, can be designed by changing capacitor values.

Filter cutoff-frequency control requires a linear PTAT voltage between 1V and 4V (at +27°C). An on-chip reference generator provides the necessary voltage variation with temperature.

Cell Dimensions: 620 x 780 + 260 x 520μm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

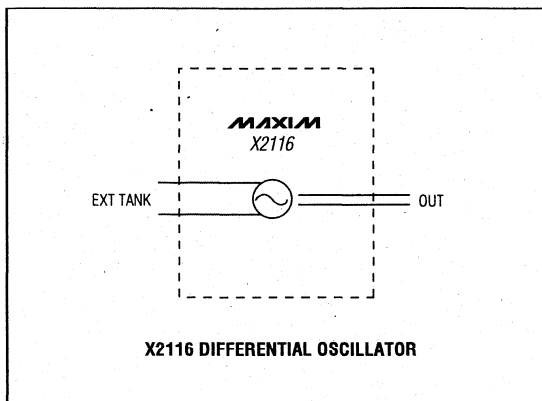
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%						
Cutoff Frequency	f _c	VTUNE = 2.1V, 3dB, T _A = +25°C	16		24	MHz
Minimum Cutoff	f _{CMIN}	VTUNE = 1V, 3dB, T _A = +25°C			10	MHz
Maximum Cutoff	f _{CMAX}	VTUNE = 4V, 3dB, T _A = +25°C	30			MHz
Passband Attenuation	APB	f = 5MHz		0	2	dB
Stop-Band Attenuation	ASB	f = 2 x f _c (with respect to signal level at f = 0.5 x f _c)	27			dB
Maximum Input Signal, p-p	V _{IN} (max)		30			mV
Supply Current	I _{CC}			2.5		mA
Equivalent Input Noise	e _n	f = 5MHz, R _S = 50Ω		58		nV/√Hz

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
VCC	+5V supply	OP	Output
VEE	Ground	REF1	Output reference
BIAS	250μA PTAT reference current input (from X2112 or equivalent)	REF	Bandgap voltage in (from X2112 or equivalent)
IP	+ Input	ADC	250μA PTAT reference current output for X2113
IPB	- Input	VTUNE	Tuning voltage input (PTAT)
SUB	Substrate connection (GND)		

Differential Oscillator

Block Diagram



Features

- ◆ Oscillates from <400MHz to >700MHz
- ◆ Low Phase Noise
(-88dBc/Hz @ 10kHz Offset, Qr >20)
- ◆ Differential Resonator Port for Immunity to Interference and Crosstalk

Description

The X2116 cell is a Differential Oscillator suitable for use as the LO in a receiver system. The differential inputs present a negative resistance for use with an external resonator. A differential topology is used to provide maximum interference rejection.

Cell Dimensions: 520μm x 260μm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

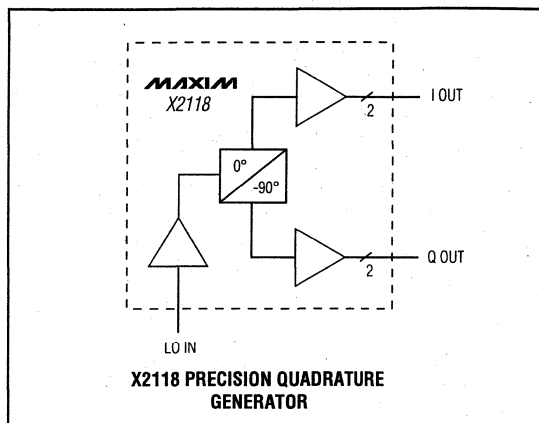
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%						
Oscillation Frequency	f _C	External resonator	400		700	MHz
Phase Noise Floor	Φ _N	20MHz off f _C , 1Hz BW, Qr = 20		-140		dBc
Phase Noise	Φ _N	10MHz off f _C , 1Hz BW, Qr = 20		-88		dBc
Output Level, Differential, p-p	V _O	C _L = 1pF/side, R _L = 10k/side		600		mV
Supply Current	I _{CC}				10	mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V _{CC}	+5V supply	OP	+ Output
TNKA	Differential tank connection A	OPB	- Output
TNKB	Differential tank connection B	SUB	Substrate connection (GND)
K125	125μA constant reference current input (from X2118 or equivalent)	P250	250μA PTAT reference current input (from X2118 or equivalent)
V _{EE}	Ground		

Precision Quadrature Generator

Block Diagram



Features

- ◆ Precision Quadrature Generation (<1.5° at 650MHz)
- ◆ Wide Input Frequency Range (400MHz to 700MHz)

Description

The X2118 Precision Quadrature Generator cell uses a delay-locked loop to provide tight amplitude and phase matching. The input from an external VCO drives a buffer and a delay line consisting of three electronically variable delay cells. The output of the delay line drives a second buffer identical to the first. The buffer outputs are compared by a phase detector whose error signal drives the variable delay cells to adjust the phase difference to 90°. This method provides precise quadrature generation over the wide input frequency range of 400MHz to 700MHz.

Cell Dimensions: 570μm x 1800μm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%						
LO Frequency	f _{LO}		400		700	MHz
Output Phase Mismatch	ΔΦ	f _{LO} = 650MHz			1.5	°
Output Level	V _O (pk-pk)			400		mV
Output Amplitude Mismatch	ΔV _O	f _{LO} = 650MHz			12	mV
LO Input Level	V _{LO}		-10		0	dBm
LO Input VSWR		Z _C = 50Ω			2:1	
Supply Current	I _{CC}			20		mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V _{CC}	+5V supply	Q	+ Quadrature output
IP	+ Input	QB	- Quadrature output
IPB	- Input	I	+ Inphase output
VEE	GND	IB	- Inphase output
K250	250μA constant reference current input (from X2112 or equivalent)	P250	250μA PTAT reference current input (from X2112 or equivalent)
SUB	Substrate connection (GND)		

6-Bit Quadrature Digitizer

General Description

The MAX2101 6-bit quadrature digitizer combines quadrature demodulation with analog-to-digital conversion on a single bipolar silicon die. This unique RF-to-Bits™ function bridges the gap between existing RF downconverters and CMOS digital signal processors (DSP).

The MAX2101's simple receiver subsystem is designed for digital communications systems such as those used in DBS, TVRO, WLAN, and other applications.

The MAX2101 accepts input signals from 400MHz to 700MHz and applies adjustable gain, providing at least 40dB of dynamic range.

Each baseband is filtered by an on-chip, 5th-order Butterworth lowpass filter, or the user can select an external filter path. Baseband sample rate is 60Msps. The MAX2101 is available in a commercial temperature range, 100-pin MQFP package.

Applications

Recovery of PSK and QAM Modulated RF Carriers
Direct-Broadcast Satellite (DBS) Systems
Television Receive-Only (TVRO) Systems
Cable Television (CATV) Systems
Wireless Local Area Networks (WLANs)

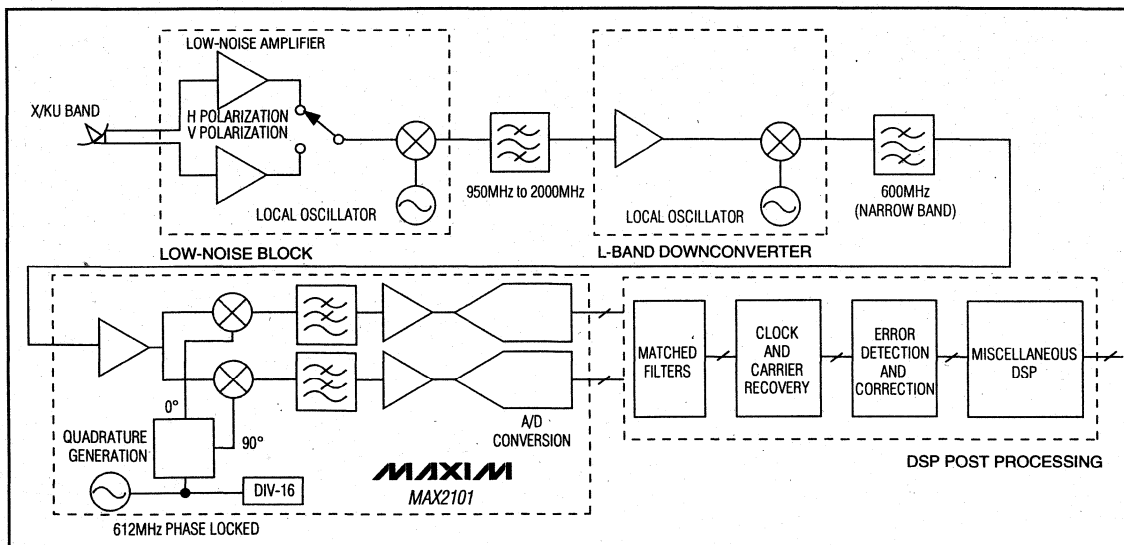
Features

- ◆ ADCs Provide Greater than 5.5 Effective Bits at $f_s = 60\text{Msps}$, $f_{IN} = 15\text{MHz}$
- ◆ Fully Integrated Lowpass Filters with Externally Variable Bandwidth (10MHz to 30MHz)
- ◆ 40dB Dynamic Range
- ◆ Integrated VCO and Quadrature Generation Network for I/Q Demodulation
- ◆ Divide-by-16 Prescaler for Oscillator PLL
- ◆ Programmable Counter for Variable Sample Rates
- ◆ Signal-Detection Function
- ◆ Selectable Offset Binary or Twos-Complement Output Data Format
- ◆ Automatic Baseband Offset Cancellation

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2101CMQ	0°C to +70°C	100 MQFP

Typical Application Circuit



™RF-to-Bits is a registered trademark of Tektronix, Inc.

6-Bit Quadrature Digitizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Ranges (Note 1)

V _{CC}	(-0.3V to +6.5V)
V _{INA}	(V _{CCA} + 0.3V)
V _{IND}	(V _{CCD} + 0.3V)

Continuous Power Dissipation (T _A = +70°C)	1.6W
Operating Temperature Range.....	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, <10sec).....	+300°C

Note 1: The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high-energy electrostatic fields. Keep unused units in conductive foam or shunt the terminals together. Discharge the conductive foam to the destination socket before insertion.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS (V_{GND} = System Ground, V_{CCA} = V_{CCD} = 5.0V ±5%)						
Digital Supply Current	I _{CCD}	V _{CCA} , V _{CCO} , V _{CCD} , V _{CCQ}			95	mA
ADC Supply Current	I _{CCAD}	V _{CCAD}			80	mA
RF Blocks Supply Current	I _{CCRF}	V _{CCIF} , V _{CC2} , V _{CC1} , V _{CCQ}			170	mA
IF Port DC Dynamic Range	V _{IF}		0.5		100	mV
IF Port Input Resistance	R _{IF}		40		75	Ω
AGC Input Voltage	V _{AGMIN}	V _{IF} = 100mV	1.0		1.5	V
	V _{AGMAX}	V _{IF} = 0.5mV	2.3		2.9	
AGC Input Resistance	R _{AGC}		50		100	kΩ
AGC Input Capacitance	C _{AGC}	(Note 2)			2	pF
AGC Range	AGCR		40			dB
AGC Control Slope Variation	SV _{AGC}	Variation dB/V			4:1	
AGC Control Input Bias Current	I _{AGC}	Voltage range = 1V to 4V		±20		μA
Mixer Buffer Output Drive	I _{MO}	V _{MO} = 2.4V	-750		750	μA
Mixer Buffer DC Gain	AV _{MIX}		5		7.5	dB
Lowpass Filter Tune Input Resistance	R _{ILPF}		10			kΩ
Lowpass Filter Tune Input Capacitance	C _{ILPF}	(Note 2)			2	pF
TNKA, TNKB Resonant Port Bias Voltage	V _{LO}	4.1V on complementary input	1		3	V
LO Resonant Port Input Resistance	R _{ILO}	(Note 2)	10			kΩ
LO Resonant Port Input Capacitance	C _{ILO}	(Note 2)			2	pF
LO Prescaler Output High (Note 3)	V _{OH}	R _L = 1MΩ, C _L = 15pF	2.4			V
LO Prescaler Output Low	V _{OL}	R _L = 1MΩ, C _L = 15pF			0.5	V
LO Prescaler Output Source Current	I _{OH}	R _L = 1MΩ, C _L = 15pF, V _O = 2.4V	400			μA
LO Prescaler Output Sink Current	I _{OL}	R _L = 1MΩ, C _L = 15pF, V _O = 0.5V	50			μA
Baseband Amplifier DC Gain	AV _{BB}		27	29	31	dB
Baseband Input Bias Current	I _{IBB}	V _{BBIN} = 2.5V	0.5		3	μA
Baseband Input—Input Resistance	R _{IBB}		5			kΩ
Baseband Input—Input Capacitance	C _{IBB}	(Note 2)			2	pF
Baseband Amplifier I/Q Offset Match (Note 4)	V _{OFFBB}	LSB = 24mV, ENOPB = 0V, V _{TUNE} = V _{TMIN} to V _{TMAX}			0.75	LSB
Baseband Amplifier Offset Adjust Input Resistance	R _{OFFBB}	Voltage Range = 1V to 4V	10			kΩ

6-Bit Quadrature Digitizer

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Detect Output Minimum	V _{PWR}	V _{OBB} = 0V _{p-p}			1.5	V
Power Detect Output Maximum	V _{PWR}	V _{OBB} > 2V DC	3.75			V
ADC LSB Size	LSB		21		25	mV
ADC Amplitude Response Match	A _{VM}	Channel to channel			0.4	dB
ADC Input Offset	V _{OFFAD}	LSB = 24mV, either channel			0.5	LSB
ADC Differential Nonlinearity	DNL				0.5	LSB
ADC Integral Nonlinearity	INL				0.5	LSB
RF Signal Path DC Gain	A _{VRF}	AGC set to maximum gain	63			dB
Composite I/Q Gain Mismatch	ΔM _(IQ)	Entire signal path, DC V _{TUNE1} = V _{TUNEQ} = V _{2R5}			0.5	dB
Buffered Reference Voltage (Zero Temperature Coefficient)	V _{REF}	R _L = 1kΩ, C _L = 0.1μF	1.18		1.25	V
Buffered Reference Voltage (Proportional to Absolute Temperature)	V _{PTAT}	R _L = 40kΩ, C _L = 0.01μF	T _A = +25°C		1.0	V
			T _A = 0°C to +70°C Guaranteed		0.9	
Buffered Reference Voltage (2 x V _{REF})	V _{2R5}	Ratio of V _{2R5} to V _{REF}	1.9		2.1	V
Data Output High (Note 3)	V _{OH}	R _L = 1MΩ, C _L = 15pF	2.4			V
Data Output Low	V _{OL}	R _L = 1MΩ, C _L = 15pF			0.5	V
Data Output Source Current (Note 3)	I _{OH}	R _L = 1MΩ, C _L = 15pF, V _O = 2.4V	400			μA
Data Output Sink Current	I _{OL}	R _L = 1MΩ, C _L = 15pF, V _O = 0.5V	50			μA
Data Clock Output High (Note 3)	V _{OH}	R _L = 1MΩ, C _L = 15pF	2.4			V
Data Clock Output Low	V _{OL}	R _L = 1MΩ, C _L = 15pF			0.5	V
Data Clock Output Source Current (Note 3)	I _{OH}	R _L = 1MΩ, C _L = 15pF, V _O = 2.4V	400			μA
Data Clock Output Sink Current	I _{OL}	R _L = 1MΩ, C _L = 15pF, V _O = 0.5V	50			μA
Master Clock Input Dynamic Range	PMCLK	R _L = 50Ω external, f = 5MHz	0		10	dBm
Master Clock Input Resistance	R _{IMCLK}		2			kΩ
Master Clock Input Capacitance	C _{IMCLK}				5	pF
Reference Clock Output High (Note 3)	V _{OH}	R _L = 10MΩ, C _L = 15pF	2.4			V
Reference Clock Output Low	V _{OL}	R _L = 10MΩ, C _L = 15pF			0.5	V
Reference Clock Output Source Current (Note 3)	I _{OH}	R _L = 1MΩ, C _L = 15pF, V _O = 2.4V	400			μA
Reference Clock Output Sink Current	I _{OL}	R _L = 1MΩ, C _L = 15pF, V _O = 0.5V	50			μA
Digital Input High Threshold (Note 5)	V _{IH}				2.0	V
Digital Input Low Threshold (Note 5)	V _{IL}		0.8			V
Digital Input Current High (Note 5)	I _{IH}	V _{IH} = 2.0V	-200		-400	μA
Digital Input Current Low (Note 5)	I _{IL}	V _{IL} = 0.8V	-400		-600	μA
FLTRSEL Input Current High	I _{IH}	V _{IH} = 2.0V				μA
FLTRSEL Input Current Low	I _{IL}	V _{IL} = 0.8V				μA

MAX2101

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6-Bit Quadrature Digitizer

ELECTRICAL CHARACTERISTICS (continued)

(VCC = 4.75V to 5.25V, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC SPECIFICATIONS (GND = System Ground, VCC = VCCD = 5.0V ±5%)						
IF Port Dynamic Range (Note 2, 6)	PIF	RS = 50Ω, fIF = 400MHz to 700MHz	-50		-10	dBm
IF Port VSWR (Note 6)	VSWR	RS = 50Ω, RTERM = 25Ω, no matching network, fIF = 400MHz to 700MHz		1.7		
IF Input Frequency Range	fIF	(Note 2)	400		700	MHz
Noise Figure (Note 6)	NF	RTERM = 50Ω, gain configured for PIF = -50dBm		20		dB
Noise Figure Variation	ΔNF	Maximum gain to minimum gain		1		dB/dB
Input 3rd-Order Intercept Point	IIP3	Gain configured for PIF = -10dBm, fBB1 = 5MHz, fBB2 = 6MHz		6		dBm
		Gain configured for PIF = -50dBm, fBB1 = 5MHz, fBB2 = 6MHz		-34		
LO Frequency Coverage	fLO	External resonator, guaranteed	400		700	MHz
LO Device Phase Noise Floor	ΦN	10MHz off fC, 1Hz bandwidth		-140		dBc/Hz
LO Device Phase Noise	ΦN	10kHz off fC, 1Hz bandwidth (limited by external tank Q)		-88		dBc/Hz
MIXER Output Baseband Gain Flatness	ΔAV	5Hz to 20MHz		0.4		dB
Lowpass Filter Stop-Band Attenuation	ASB	f = 2 x fC (with respect to signal level at f = 0.5 x fC)		28		dB
Lowpass Filter Tune Voltage	VFTMIN	fC = 10MHz	1.5		2	V
	VFTMAX	fC = 30MHz	2.3		2.9	
Composite I/Q Amplitude Balance	ΔM(IQ)	fLO = 650MHz		0.3		dB
Composite I/Q Phase Balance	ΔΦ(IQ)	fLO = 650MHz		1.5		degree
Composite Group Delay Variation	ΔT	100Hz to 15MHz, each channel excluding filter		0.5		ns
ADC 0.1dB Bandwidth	BW0.1dB			20		MHz
ADC Maximum Sample Rate, Each Section	SRMAX	(Note 2)	60			Msp/s
ADC Aperture Uncertainty	τAU	fS = 60Msp/s		80		ps
ADC Transient Response	tTRAN	Full-scale transition, settle to within 1%		10		ns
Baseband Overdrive Recovery	Recover	VBASEBAND = 3Vp-p		10		ns
ADC Effective Number of Bits	ENB	fIN = 15MHz, fS = 60Msp/s, VIN = 95% FS		5.5		Bits
ADC Input IP3 Rejection	IIP3AD	f1 = 10MHz, FS - 7dB; f2 = 12MHz, FS - 7dB		-38		dBc

Note 2: Guaranteed by design.

Note 3: A warm-up of 10 seconds is required at TA = 0°C.

Note 4: Sample characterization at TA = 0°C to +70°C.

Note 5: Digital inputs include Programmable Sample Rate Control (S0-S2), Binary Enable (BINEN).

Note 6: RS = Source Resistance of signal source driving IF input (IFIN, pin 90).

RTERM = Termination Resistance for inverting IF input (IFINB, pin 91).

6-Bit Quadrature Digitizer

TIMING CHARACTERISTICS

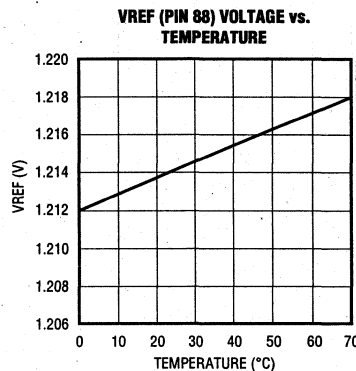
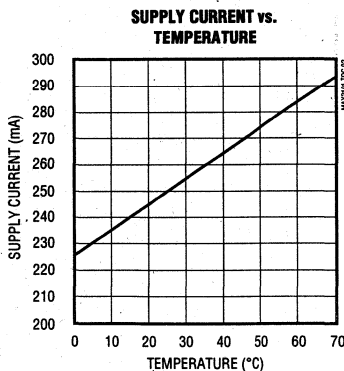
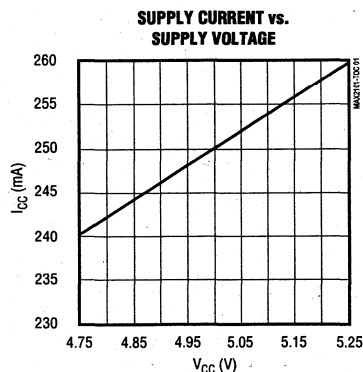
(V_{GND} = system ground, V_{CCA} = V_{CCD} = 5.0V ±5%, T_A = +25°C, unless otherwise noted. Note 4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Clock Period (Figure 2)	t _{PC}		16		ns
Propagation Delay, Clock to Data (Figure 2)	t _{PCQ}		4		ns
Data Output Skew (all 12 outputs) Settled within 20% (Figure 2)	t _{SKEW}		1		ns
Aperture Delay Relative to Data Clock (Figure 2)	t _{APERATURE}		1		ns
Aperture Delay Match, Channel to Channel	t _{AP-MATCH}		20		ps
Data Output Rise, Fall Time (20% to 80%) (Note 7)	t _r , t _f		4		ns
Data Clock Output Rise, Fall Time (20% to 80%) (Note 7)	t _r , t _f		3		ns
Reference (Div 6) Clock Output Rise, Fall Time (20% to 80%) (Note 7)	t _r , t _f		5		ns
Reference Clock Output Jitter, RMS	t _j		30		ps
VCO Prescaler Output Rise, Fall Time (20% to 80%) (Note 7)	t _r , t _f		3		ns

Note 7: R_L = 1MΩ, C_L = 15pF

Typical Operating Characteristics

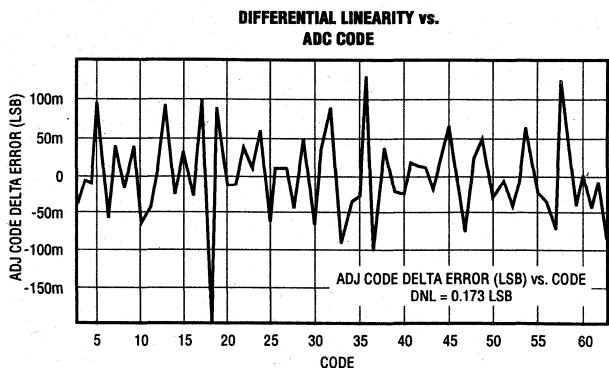
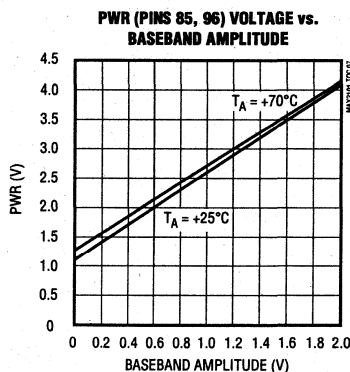
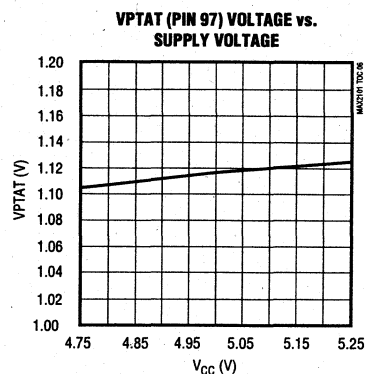
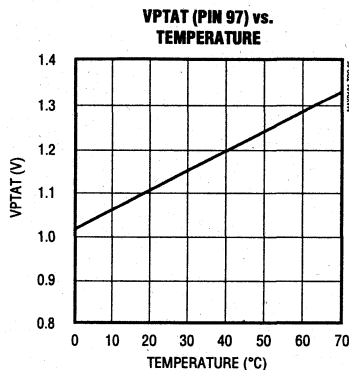
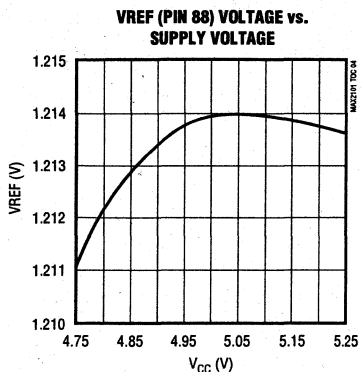
(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)



6-Bit Quadrature Digitizer

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $T_A = +25^\circ C$, unless otherwise noted.)

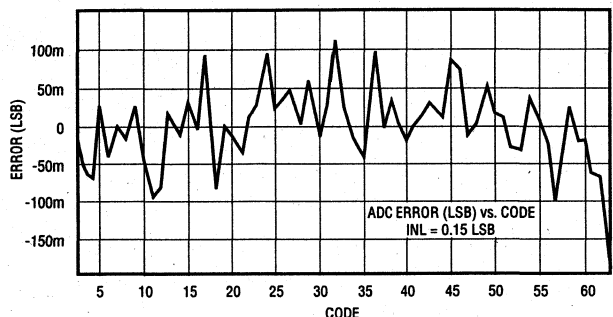


6-Bit Quadrature Digitizer

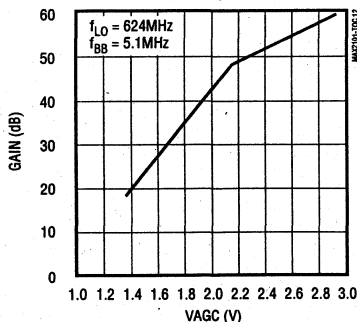
Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $T_A = +25^\circ C$, unless otherwise noted.)

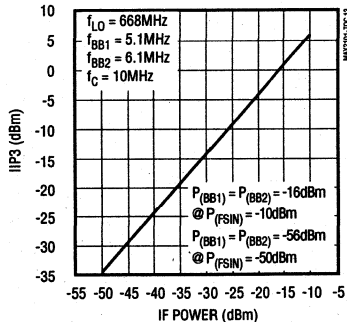
INTEGRAL NONLINEARITY vs.
ADC CODE



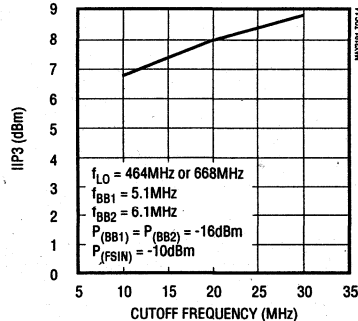
RF SIGNAL PATH GAIN vs.
AGC (PIN 93) VOLTAGE



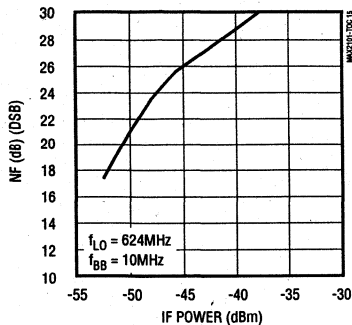
INPUT IP3 vs.
IF POWER



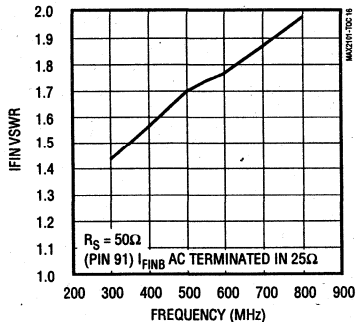
INPUT IP3 vs.
FILTER CUTOFF FREQUENCY



NOISE FIGURE vs.
IF INPUT POWER



IFIN (PIN 90) VSWR vs.
FREQUENCY



6-Bit Quadrature Digitizer

Pin Description

PIN	NAME	FUNCTION
1, 9, 12, 13, 18, 19, 63, 67, 82, 83, 89, 92, 98, 99	GND	Ground
2	VGNDQ	Q Channel Baseband Ground
3	BBINQ	Q Channel Baseband Amplifier, External Input
4	FTUNEQ	Q Channel Filter Cutoff Frequency Control
5	OFFQ	Q Channel Baseband Amplifier Offset Adjust
6	BBOUTQ	Q Channel Baseband Amplifier Output
7	BBOUTQB	Q Channel Baseband Amplifier Inverted Output
8	VCCQ	Q Channel Baseband +5V Supply
10	VGNDP	Prescaler Ground
11	VCCP	Prescaler +5V Supply
14	TNKB	Oscillator Resonator Port
15	VCC2	Oscillator +5V Supply
16	VGND2	Oscillator Ground
17	TNKA	Oscillator Resonator Port
20, 21	VGNDAD	A/D Converter Ground
22, 59	VSUBAD	A/D Converter Substrate
23	VCOPRE	Divide-by-16 Prescaler Output
24	VCOPREB	Divide-by-16 Prescaler Complementary Output
25, 29, 38, 40, 44, 52	VCCO	Digital Output +5V Supply
26	VGND0	Digital Output Ground
27	D5Q	Q Channel Data Output, bit 5 (MSB)
28	D4Q	Q Channel Data Output, bit 4
30, 37, 43, 51, 55	VGND0	Digital Output Ground
31	D3Q	Q Channel Data Output, bit 3
32	D2Q	Q Channel Data Output, bit 2
33, 48	VCCD	Digital Logic +5V Supply
34, 47	VGND0	Digital Logic Ground

PIN	NAME	FUNCTION
35	D1Q	Q Channel Data Output, bit 1
36	D0Q	Q Channel Data Output, bit 0 (LSB)
39	RCLK	Reference Clock, divide by six from master clock (MCLK)
41	DCLKB	Data Clock Complementary Output
42	DCLK	Data Clock Output
45	D0I	I Channel Data Output, bit 0 (LSB)
46	D1I	I Channel Data Output, bit 1
49	D2I	I Channel Data Output, bit 2
50	D3I	I Channel Data Output, bit 3
53	D4I	I Channel Data Output, bit 4
54	D5I	I Channel Data Output, bit 5 (MSB)
56	BINEN	Binary Enable
57	S2	Programmable Sample Rate Control Input, bit 2 (MSB)
58	S1	Programmable Sample Rate Control Input, bit 1
60, 61	VCCAD	A/D Converter +5V Supply
62	S0	Programmable Sample Rate Control Input, bit 0 (LSB)
64	VCCC	Clock Buffer +5V Supply
65	MCLK	Master Clock
66	VGND0	Clock Buffer Ground
68	ENOPB	Offset Correction/Enable Correction
69	CQB	Inverting Input Q Channel Offset Correction
70	CQ	Noninverting Input Q Channel Offset Correction
71	CI	Noninverting Input I Channel Offset Correction
72	CIB	Noninverting Input I Channel Offset Correction
73	VCCI	I Channel Baseband +5V Supply
74	BBOUTIB	I Channel Baseband Amplifier Inverted Output
75	BBOUTI	I Channel Baseband Amplifier Output
76	OFFI	I Channel Baseband Amplifier Offset Adjust
77	FTUNEI	I Channel Filter Cutoff Frequency Control

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Pin Description (continued)

PIN	NAME	FUNCTION
78	BBINI	I Channel Baseband Amplifier, External Input
79	VGNDI	I Channel Baseband Ground
80	VREFIN	High Impedance, connect to VREF (pin 88)
81	MIXOUTI	I Channel Mixer Output
84	VSUBRF	RF Demodulator Substrate
85	PWRI	I Channel Power Indicator
86	2R5	2x VREF Output
87	VCCIF	IF Signal Processing +5V Supply
88	VREF	Bandgap Reference Voltage Output
90	IFIN	IF Amplifier Noninverting Input
91	IFINB	IF Amplifier Inverting Input
93	AGC	Automatic Gain Control Input
94	VGNDIF	IF Signal-Processing Ground
95	FLTRSEL	Baseband Signal Path Select
96	PWRQ	Q Channel Power Indicator
97	VPTAT	PTAT Reference Voltage Output
100	MIXOUTQ	Q Channel Mixer Output

Detailed Description

The MAX2101 6-bit quadrature digitizer solves one of the most challenging problems of high dynamic range digital-receiver design by combining quadrature demodulation and analog-to-digital (A/D) conversion in a single device. The MAX2101's unique RF-to-Bits function bridges the gap between RF downconverters and CMOS digital signal processors (DSP). Figure 1 is a simplified connection diagram.

The MAX2101 accepts input signals from 400MHz to 700MHz and applies gain depending on the input amplitude. The signal is then split and downconverted to baseband by two mixers, which are driven by two local oscillator (LO) signals in quadrature. An internal voltage-controlled oscillator (VCO) feeds the two LOs.

Each baseband is filtered by an internal 5th-order Butterworth lowpass filter. The on-board lowpass filters have an externally variable bandwidth of 10MHz to 30MHz. Each baseband is then converted by a 6-bit analog-to-digital converter (ADC). The conversion result is stored in a register and is output using the data clock. See Figure 2 for the relation between baseband signal, sample and data clock, and digitized data. The external master clock is internally divided by six and is available at RCLK for external system functions, frequency synthesizers, etc. See Figures 3 and 4 for functional diagrams.

IF Input Port (IFIN, IFINB)

The MAX2101 provides a balanced IF input. The inputs are self-biasing, so the input signals should be AC terminated, depending on system requirements. To minimize noise, the unused input should be AC terminated with 25 Ω . To minimize distortion, AC terminate the unused input with a 50 Ω resistor.

VCO Resonator Tank Ports (TNKA, TNKB) and Prescaler

The MAX2101 integrates a negative impedance oscillator with balanced inputs. Use a parallel tank network, as shown in Figure 5. The phase-noise performance of the oscillator near the carrier is dominated by the resonant network. The resonant inductor must have a sufficiently high Q and a self-resonant frequency (SRF) that is more than twice the intended LO frequency. Be sure to minimize parasitic elements surrounding the tank network by using proper layout techniques. See the *Applications Information* section.

The VCO prescaler output provides phase-lock loop capability for controlling the VCO frequency. The prescaler generates the VCO frequency divided by 16. As a result, the prescaler delivers a 25MHz to 43.75MHz signal over the VCO operating frequency range of 400MHz to 700MHz. The differential outputs should have equivalent termination.

6-Bit Quadrature Digitizer

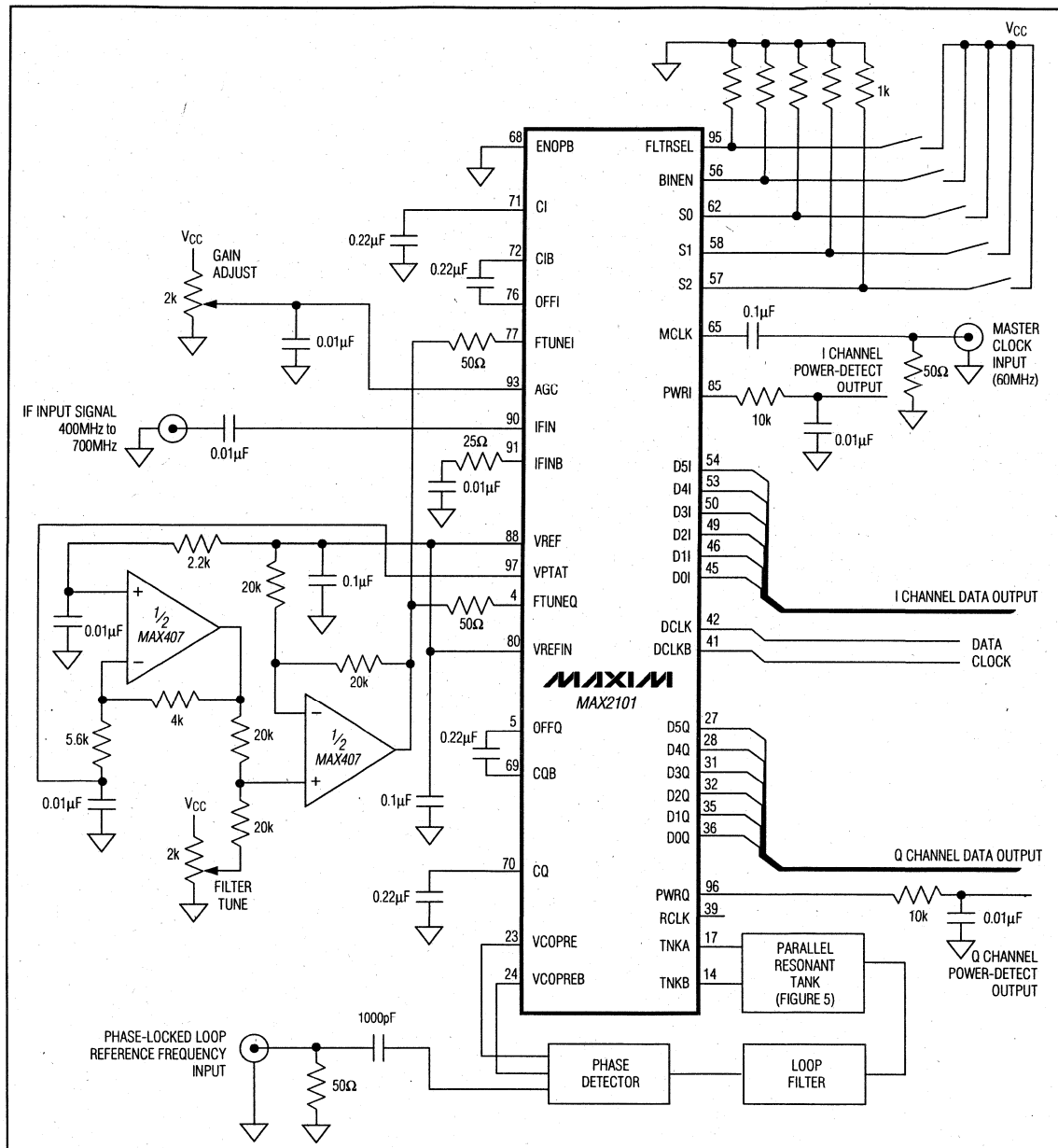


Figure 1. Typical Connection Diagram

6-Bit Quadrature Digitizer

MAX2101

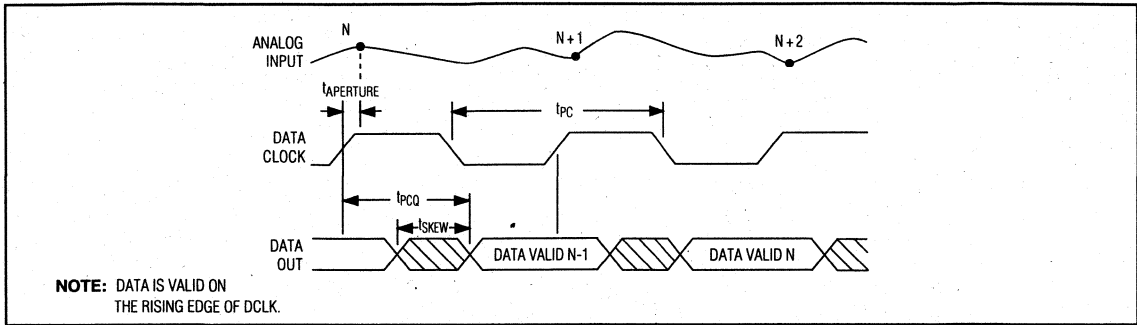


Figure 2. Baseband Signal, Sample/Data Clock, and Digitized Data Timing

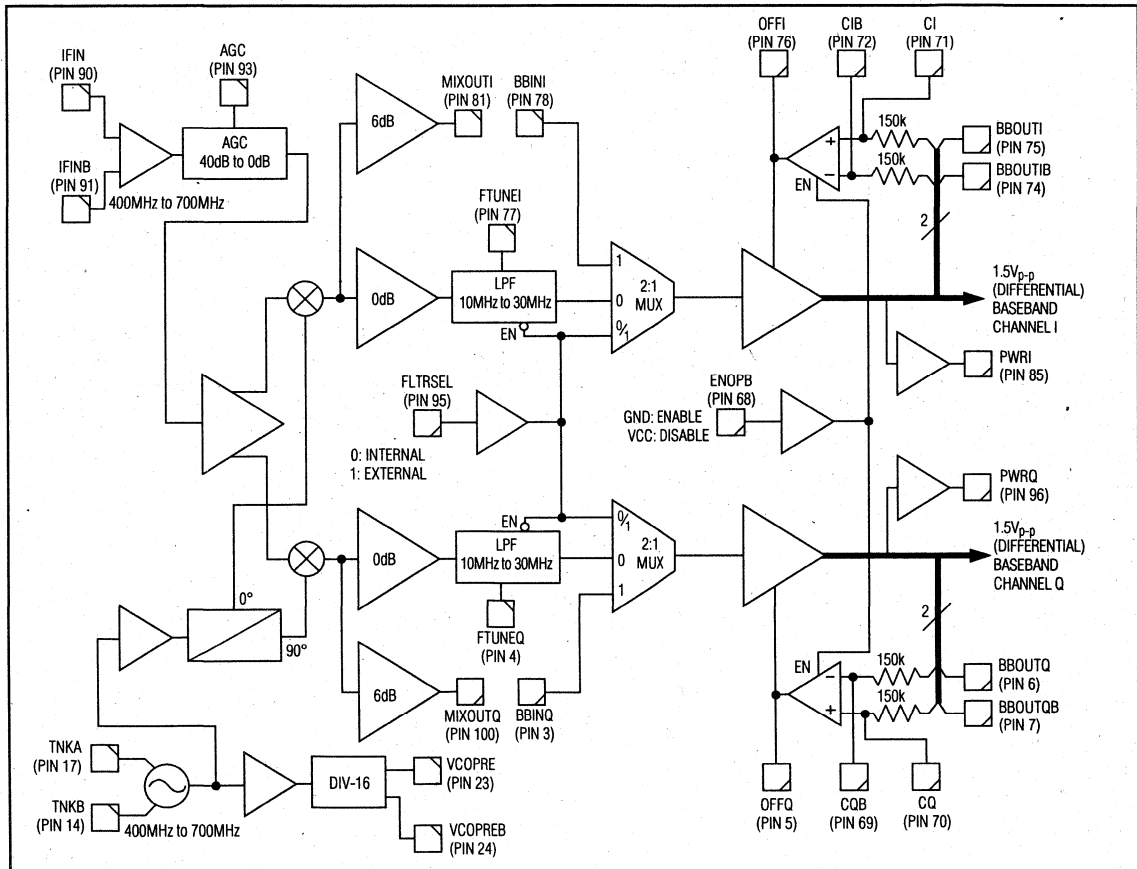


Figure 3. Functional Diagram—MAX2101 RF Front End Section

6-Bit Quadrature Digitizer

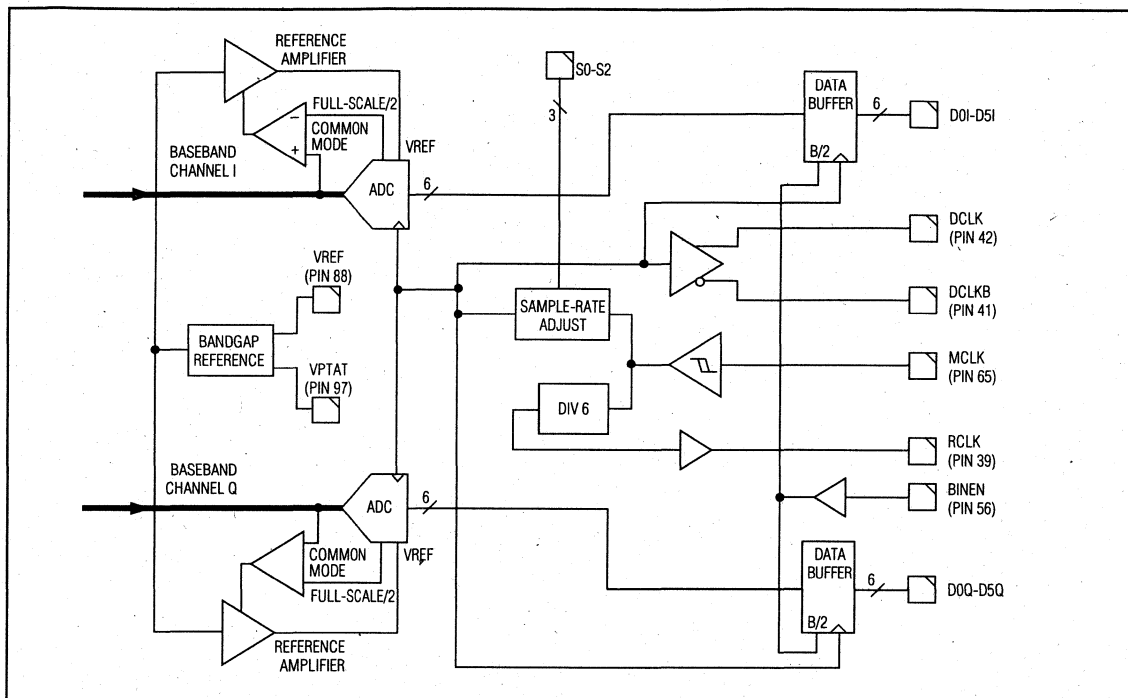


Figure 4. Functional Diagram—MAX2101 ADCs and Supporting Sections

Filter Tuning

The MAX2101 integrates two 5th-order Butterworth low-pass filters for anti-alias filtering of the baseband signal. One filter exists for each of the I and Q channels. The filters' cutoff frequency is set by driving the FTUNE pins, pin 77 (I channel) and pin 4 (Q channel). The user sets the I/Q channel filters independently. Figure 6 shows a typical transfer curve of a filter's cutoff frequency versus FTUNE voltage.

The MAX2101's anti-aliasing filtering function provides superior channel-to-channel matching compared to a discrete implementation. The filters are realized using a gyrator topology, which inherently has a strong temperature dependency. The temperature dependency of the filters must be compensated to achieve a consistent filter response over ambient temperature. This compensation is easily summed with the user-supplied filter tune signal, with the techniques discussed for both current-drive and voltage-drive implementations later in this section. Figure 7 shows a typical characteristic of the FTUNE signal required to provide a constant filter cutoff frequency over temperature.

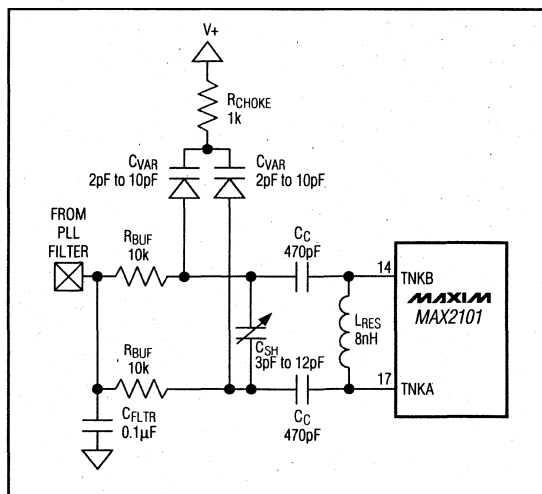


Figure 5. Typical Parallel Resonant Network

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MAX2101

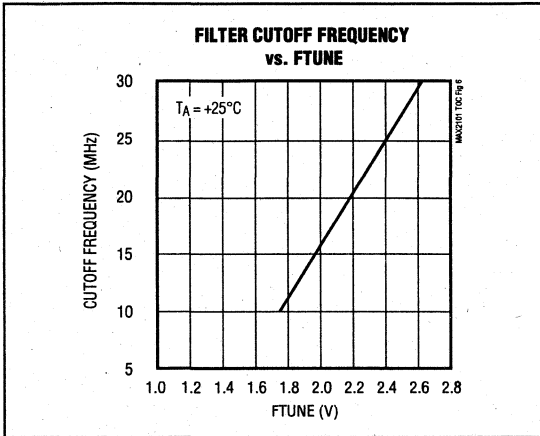


Figure 6. Typical Filter Cutoff Frequency vs. FTUNE Input Voltage

The MAX2101 provides temperature-compensated bias voltages that, when scaled and summed with the user-supplied filter-control signal, provide the necessary compensation for the filters. The filter-control signal can originate in one of two forms: an analog current, or an analog voltage. The temperature compensation signal will be added to the control signal as discussed below.

Voltage Drive

A suggested technique of filter drive uses a voltage source, such as a voltage output DAC. The temperature compensation signals, VPTAT and VREF, are shifted and scaled, then summed with the control voltage, and the sum is applied to the FTUNE inputs. See Figure 8 for a possible implementation.

The transfer function for Figure 8's voltage drive configuration can be evaluated as follows:

$$V_{TC} = V_{REF} + \frac{R_F}{R_{TC}}(V_{REF} - V_{PTAT})$$

$$V_{FTUNE} = V_{SET} + \frac{R_F}{R_{TC}}(V_{REF} - V_{PTAT})$$

Thus, the user-supplied signal V_{SET} , which is characterized by a very small (ideally 0) temperature coefficient, will be summed with a small signal ($|V_{REF} - V_{PTAT}| \leq 200\text{mV}$) whose temperature dependence compensates for the filter's TC.

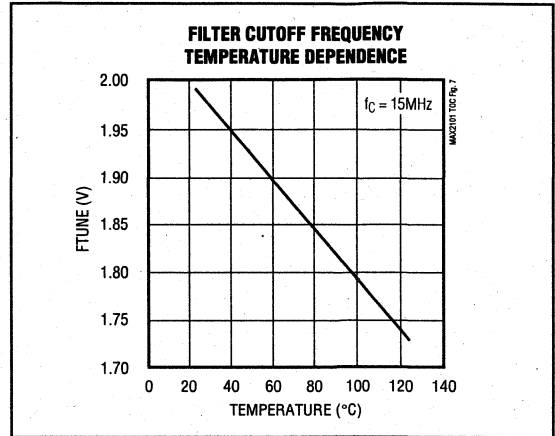


Figure 7. Typical Filter Cutoff Frequency Temperature Dependence

Current Drive

An alternate form of filter drive uses a current source, such as a current-output DAC. The current is transformed to the appropriate voltage via a transresistance network, which will drive the FTUNE input(s). The temperature compensation signals, VPTAT and VREF, are shifted and scaled, transformed to current, added to the user-supplied current, and the sum is transformed back into the temperature compensated control voltage (Figure 9).

Amplifier U1A generates a shifted reference signal, VTC. VTC is transformed into a current through the resistor R_{TC} . R_{TC} also scales this signal such that, when compared to the feedback resistor R_F , the proper temperature dependence is added to the user-supplied filter control current I_{SET} to compensate for the TC of the filter.

The expression for the final filter tune signal is expressed as:

$$V_{FTUNE} = I_{SET}(R_F) + \frac{R_F}{R_{TC}}(V_{REF} - V_{PTAT})$$

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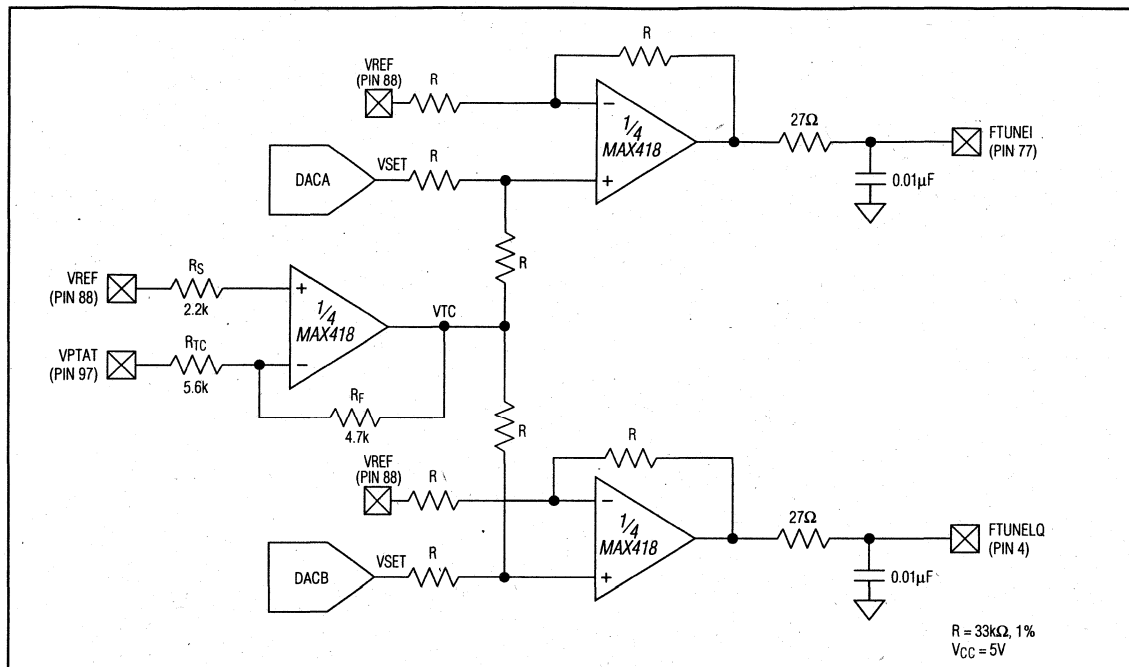


Figure 8. Independent Filter Tune Control Using Two Voltage-Output DACs

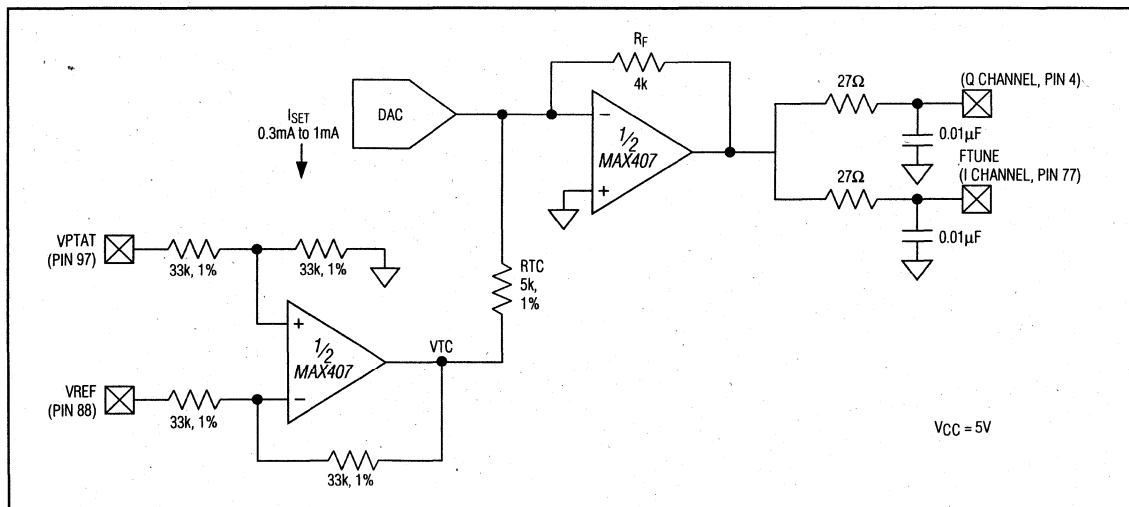


Figure 9. Filter Tune Control Using a Single Current-Output DAC

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Filter Temperature Compensation

In both techniques discussed above, the ratio R_F/R_{TC} determines the compensation required to produce a filter response with OTC. As noted in the VPTAT vs. Temperature graph in the *Typical Operating Characteristics*, this ratio should be set at 0.8.

Baseband Offset Correction

The MAX2101 integrates a high level of RF signal processing, and applies substantial gain from the IF inputs to the baseband signals applied to the ADC. Offset in the signal path can seriously decrease the component's dynamic range, and variation in offset between I and Q channels can seriously degrade overall receiver performance. Several circuit design techniques are used to minimize offset within the chip. However, two characteristics of the component contribute to offset in the signal path.

The off-chip tank network for the VCO resonates the LO frequency with a relatively large amplitude. If the LO couples into the IF input, the coupled LO will mix down to a DC value, which depends on the AGC setting. This DC signal manifests itself as an offset in the baseband signal. The second source of offset is the active low-pass anti-aliasing filters. This offset depends on the cutoff frequency. These two elements represent the major contributors to DC offset in the signal path.

Offset Adjust Pins OFFI, OFFQ

The MAX2101 offers an offset adjust pin for each of the I and Q channels, labeled OFFI and OFFQ, respectively. The offset adjust input exhibits an adjustment range that is sufficient to correct for the errors mentioned above. The polarity of the OFF_ input is such that a positive change of the OFF_ voltage results in a negative transition in the baseband signal, BBOUT_. The offset adjust range compensates for up to 5LSBs of offset.

A feedback-controlled, offset-correction network can be realized that will null any offset detected in the baseband signal applied to the ADCs. The differential baseband signal is sampled at the input to the ADC and integrated over a sufficiently large period of time (determined by the minimum frequency of the baseband signal), extracting the offset signal. This error signal is internally applied to the OFF_ input, completing the feedback loop. The MAX2101 integrates the op amps and 150k Ω pickoff resistors of the offset correction network. Figure 10 shows a simplified schematic diagram of the network. Simply connect the appropriate capacitors as shown in Figure 11.

The network in Figure 11 is a lowpass filter with a 5Hz cutoff frequency. The user can tailor the cutoff frequency

by choosing the appropriate value of capacitance, according to the following relation:

$$C = \frac{1}{2\pi f_O(150k\Omega)}$$

where:

C = integrator capacitance
for cutoff frequency

Frequency components of the baseband signal near or below the cutoff frequency will interfere with the operation of this network. Fortunately, the compressed and encoded nature of baseband signals at this stage of the signal chain in typical applications will insure minimal low-frequency components. Hence, this technique will eliminate all offsets, independent of AGC setting, filter cutoff frequency, or changes in ambient temperature.

Pin 68, ENOPB, is normally connected to ground. Pulling ENOPB to V_{CC} disables the op amps, thus opening the servo loop, and disabling offset correction. The baseband pins (6, 7, 74, 75) should be left unconnected, or buffered with a high-impedance load (resistive load greater than 10k Ω and capacitive load less than 3pF).

Sample Clock Generation

The master sample clock (MCLK) input for the MAX2101 is typically driven by a low-noise, low-drift crystal oscillator. The signal should be between 0dBm and +10dBm, and must be AC coupled to the MCLK input. This signal is buffered and divided according to the programmable sample-rate prescaler (PSRP). The actual sample rates are binary weighted divisors of the MCLK frequency. Program the sample rates with pins S0, S1, and S2, as shown in Table 1.

Table 1. Sample-Rate Control

S2 S1 S0	Sample Rate	Description
0 0 0	$f_c/1$	Full Sample Rate
0 0 1	$f_c/2$	Div-2 Sample Rate
0 1 0	$f_c/4$	Div-4 Sample Rate
0 1 1	$f_c/8$	Div-8 Sample Rate
1 0 0	$f_c/8$	Div-8 Sample Rate
1 0 1	$f_c/16$	Div-16 Sample Rate
1 1 0	$f_c/32$	Div-32 Sample Rate
1 1 1	$f_c/64$	Div-64 Sample Rate

Note: The inputs S0, S1, and S2 are **not** latched.

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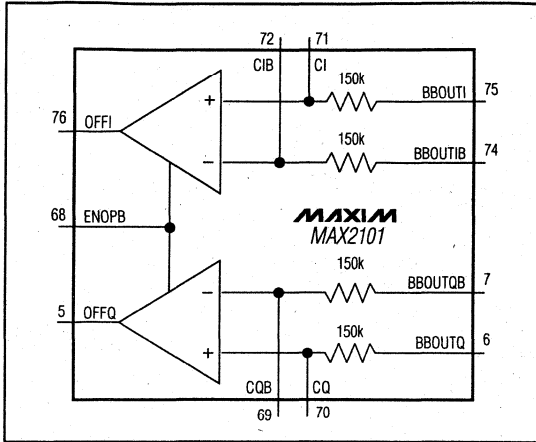


Figure 10. Offset Correction Network

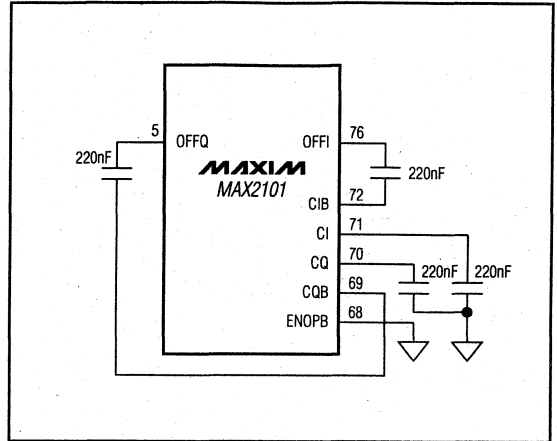


Figure 11. Offset Correction

Digital Signal Interfacing

The single-ended, LS-TTL compatible data outputs from the ADCs are clocked out with respect to the rising edge of the data clock (DCLK). The output drivers provide sufficient logic levels at speeds up to 60Mbps into a fanout of 1 with a total load capacitance of 15pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold timing.

The data clock outputs are also LS-TTL compatible and provide a signal to latch the data at rates up to 60Mbps. The outputs are differential to minimize the harmonic energy that might feed back into the LO or IF inputs. The balanced outputs should have equivalent termination to minimize unwanted EMI.

Select either binary or twos-complement output with the binary enable (BINEN) pin. A logic high will select offset binary, and a logic low will select a twos-complement format.

Input Termination Network

The MAX2101 accepts as an input a narrow band IF whose center frequency is located somewhere in the UHF range, between 400MHz and 700MHz. The MAX2101 comprises a significant part of a receiver chain characterized by extremely high dynamic range coupled with demanding intermodulation requirements. As such, it is imperative to provide proper input termination to the MAX2101, to minimize effective VSWR and noise figure at this stage of the system RF signal processing chain.

The input of the MAX2101 is designed to deliver a VSWR less than 2:1 over the 400MHz to 700MHz range.

The equivalent input network of the input pins IFIN and IFINB is discussed and illustrated below. However, standard narrow-band impedance matching techniques can be used to improve on this VSWR for the intended IF of the system.

Equivalent Input Circuitry

The MAX2101's input amplifier is designed to provide a controlled input impedance, provide gain for the signal path, and provide for the component's minimum noise figure. The amplifier uses a feedback topology to provide gain that is insensitive to input frequency, in addition to delivering constant input impedance. Figure 12 illustrates the amplifier's input portion.

Ideally, the input amplifier will be designed to match to an anticipated source impedance of 50Ω. The resistive portion of the input impedance at pin IFIN can be approximated as follows:

$$R_{IN} = \frac{R_F + r_E}{(1 + A_V)}$$

where r_E is the dynamic resistance at Q3's emitter, and A_V is the open-loop gain of the differential-pair amplifier stage.

The amplifier can be designed so the frequency response does not appreciably affect the input impedance. Details of the amplifier are left out for simplicity.

Figure 12 shows how several parasitic elements contribute to the input impedance over the frequencies of interest. CPAD represents the parasitic capacitance associated with the bond pad and input metallization.

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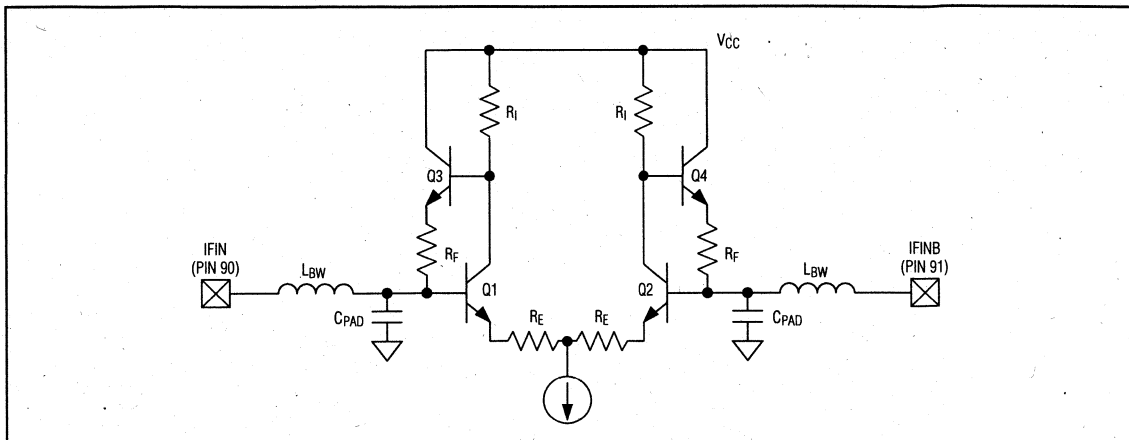


Figure 12. Equivalent Input Network

At frequencies of interest, C_{PAD} will add a small phase error to the impedance term. The inductance L_{BW} models the bond wire and lead frame in series with the input amplifier. This inductor represents a significant portion of the input impedance, and will contribute the majority of the variation in input impedance as the input frequency is swept from 400MHz to 700MHz. These variables combine to produce an actual input impedance versus frequency (Figure 13).

As a result, it is challenging to achieve an extremely low VSWR for the input of a monolithic amplifier, especially over a wide range of frequencies. The MAX2101 provides a VSWR less than 2:1, and delivers this performance over the wide range of anticipated IFs currently considered. Fortunately, for DBS, TVRO, and related applications, the UHF IF is relatively narrow band, allowing the use of standard techniques for narrow-band impedance matching.

Narrow-Band Match

Many references cover narrow-band matching techniques. The match network synthesis is simplified by assuming the impedance of the source driving the MAX2101's IFIN port is positive, real, and equal to 50Ω . For a given IF, you can simply use a Smith chart to "map" an impedance to the intended source resistance. Using a two-element matching network, you can choose the element next to the input (C_{SH} in Figure 14) to translate the real portion of the impedance to match the source resistance. The second element (L_{SER} in Figure 14) cancels the reactive component of the network (including the effect of C_{SH}), resulting in a real, matched input impedance that provides maximum

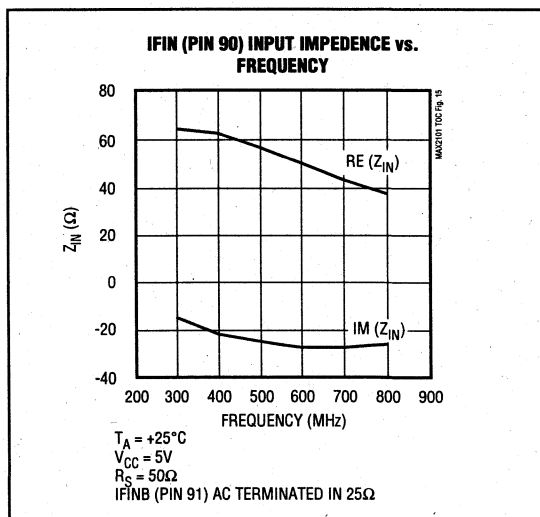


Figure 13. Typical MAX2101 IFIN Z_{IN} vs. Frequency ($Z_s = 50$)

power transfer. The transformation uses only reactive elements so that no additional resistive thermal noise is added, which would degrade the noise figure.

Figure 14 shows the resulting impedance matching network. The incident signal is AC coupled by C_C . L_{SER} and C_{SH} are the matching elements. C_{SH} includes board layout capacitance. The values of these ele-

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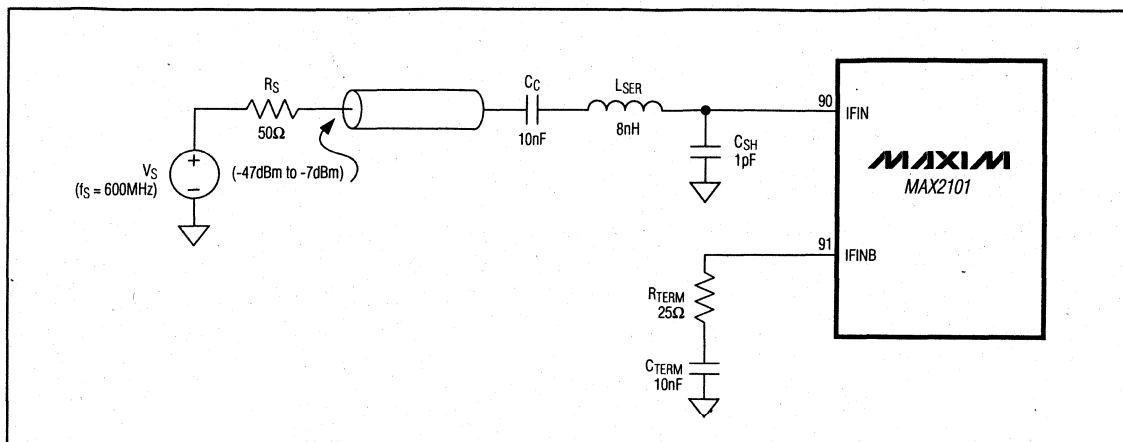


Figure 14. Example of Input Network to Minimize VSWR and Noise Figure

ments were calculated assuming a 600MHz source frequency. Capacitor C_{TERM} provides an AC termination for the complementary input IFINB. Resistor R_{TERM} provides superior noise figure performance by optimizing the tradeoff between thermal induced noise and the gain of the input amplifier. This network also provides ancillary rejection of out-of-band energy, improving the receiver noise figure and resulting SNR. The topology shown above produces a VSWR less than 1.7:1 over the intended UHF band. Do not DC couple the inputs to ground, as this would result in saturation of the input stage.

More elaborate matching networks can be designed depending on the need of the receiver system.

Applications Information

Voltage-Controlled Oscillator Equivalent Input Network and Resonator Issues

The MAX2101 performs the quadrature demodulation and digitizing functions within a digital receiver system. A vital component of the quadrature detection function is the generation of a local oscillator (LO) frequency. This signal is typically generated by a VCO controlled by a phase-locked loop. The VCO topology normally used for high dynamic range receivers is the negative resistance amplifier and resonator, due to superior phase-noise performance. The MAX2101 provides the negative resistance amplifier on-chip, and can be easily interfaced with an off-chip resonant network.

The MAX2101's VCO amplifier uses a differential topology for several reasons. The differential interface with

the resonator network provides superior rejection of spurious signals that might otherwise add to or distort the resulting LO. The differential interface minimizes the effect of parasitic package-related elements that affect the resonant frequency and the loaded Q of the network. The differential-drive network minimizes second-harmonic distortion that might create undesirable mixing products within the signal chain.

Figure 15 shows the simplified input network of the negative impedance amplifier, configured as a Wilson oscillator. The amplifier is a simple differential emitter coupled pair with emitter degeneration for controlled open-loop gain. The positive feedback necessary to create the negative input impedance is performed with the feedback capacitors, C_F , and the coupling capacitors, C_C . The capacitors ensure operation over the intended 400MHz to 700MHz spectrum, and add minimal noise to the system. R_{B1} provides a proper bias voltage for the capacitors (partially constructed with voltage-dependent pn junctions) and provides for DC interface with a shunting resonant inductor. Note that biasing networks are simplified for brevity.

The MAX2101's negative impedance amplifier expects a parallel resonant network. Figure 5 shows an example of a tunable resonant network. The resonator is driven from the phase-locked loop filter output, as noted. The loaded Q of the resonant network, and to a lesser extent the absolute values of the resonant elements, determine the VCO's phase-noise performance. As a result, take care during the design of the resonator to maximize the loaded Q. To achieve the phase-noise

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MAX2101

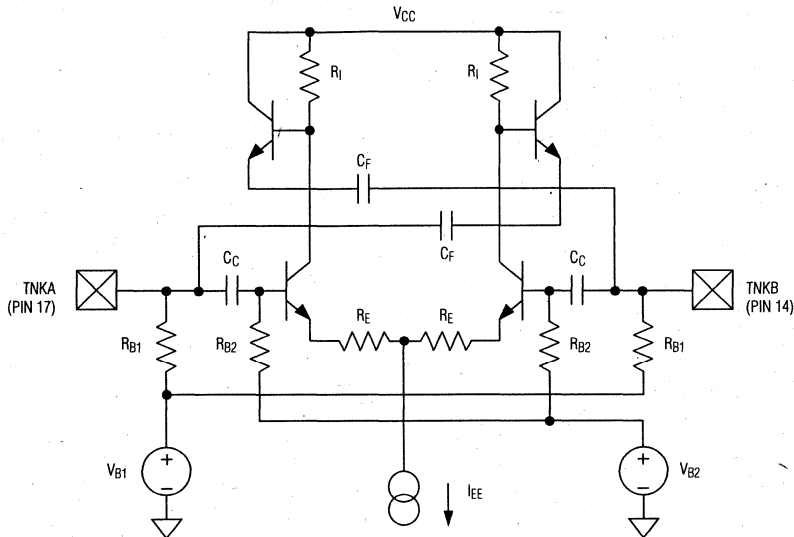


Figure 15. Simplified Input Network for VCO Resonator Ports

performance in the specification, the resonant network should exhibit a loaded Q greater than 20.

The resonating inductor L_{RES} should exhibit as high a Q factor as is reasonably possible. The inductor's self-resonant frequency (SRF) should be well in excess of the intended frequencies of operation. An air-wound design is a simple example of an inductor that would fit these criteria.

A dual varactor topology is recommended for CVAR to compensate for the large-signal amplitude incident across the resonator ports. The dual varactor in the arrangement shown in Figure 5 (to first order) allows cancellation of capacitance modulation due to the large signals, as the two diodes are driven in a complementary fashion by the LO signal. The dual varactor design also allows use of devices with larger C_0 values, simplifying device selection. The varactor should be driven with a large reverse bias to increase the MAX2101's effective Q.

The resonant frequency is primarily determined by C_{SH} , which shunts the varactor diodes. C_{SH} is trimmed (selected) to determine the approximate tuning range of the phase-locked loop. For applications relevant to the MAX2101, this frequency range can cover the UHF

spectrum from 400MHz to 700MHz. The varactor within the loop will then determine the actual LO frequency within a much narrower tuning range. Depending on the expected tuning range variation, C_{SH} could be made of a combination of fixed capacitance and trimmed capacitance. This shunt capacitance will increase the loaded Q of the resonator and lower the V to F gain constant, improving the oscillator's phase-noise performance.

The coupling capacitors C_C couple the variable capacitor network to the tank ports and resonating inductor. These elements should be selected to present low impedance (less than 1Ω) at the lowest expected operating frequency. These capacitors should also exhibit low effective series resistance (ESR) to maintain a high resonator-loaded Q. RCHOKE provides a DC bias for the varactors, while ensuring a high impedance at the intended operating frequency. The magnitude of the choke network's series impedance should be approximately 10 times the resonant inductor's impedance at the operating frequency. Resistors R_{BUF} provide drive for the varactor while ensuring adequate isolation between the two differential resonator ports. C_{FLTR} , in combination with R_{BUF} , provides additional filtering of the drive signal from the loop.

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DBS System Application

A direct-broadcast satellite (DBS) receiver consists of an antenna to receive the X/Ku band carrier from the satellite, a low-noise block (LNB), an L-band downconverter, and a quadrature demodulator. The system stages include a dual ADC, a matched filter, clock and carrier recovery, error detection and correction, and additional system-dependent DSP. See the *Typical Application Circuit* on the first page of the data sheet.

The LNB provides polar demodulation (vertical and horizontal) and downconversion of the X/Ku band signals to a first intermediate frequency (IF₁) in the 950MHz to 2000MHz range. The L-band downconverter converts IF₁ to a second IF (IF₂) in the 400MHz to 700MHz range. The MAX2101 performs the next stages as follows: 1) the quadrature demodulator converts IF₂ to two baseband signals, I and Q; and 2) the dual ADCs digitize the baseband signals, which are then processed by the various digital blocks to compensate for transmission distortion and to extract the digital baseband data.

One interface that causes system designers trouble is the quadrature demodulator to ADC interface. Power is needed to drive the low-impedance interconnect between these two functions. Additionally, this portion of the signal path can introduce phase and amplitude errors that complicate back-end error correction. The integrated MAX2101 solves all of these design problems associated with DBS systems.

The MAX2101 combines bipolar technology with excellent RF and data-converter design to integrate the quadrature demodulation and ADC functions. The MAX2101 also includes an IF gain block, a VCO and prescaler necessary to generate an accurate LO frequency, and fully integrated baseband anti-aliasing filters for both I and Q channels. By integrating several functions supporting the quadrature demodulation and A/D block, the MAX2101 replaces several components and eliminates many board-level design and manufacturing problems.

Layout, Grounding, Bypassing

The MAX2101's supply pins are separated to isolate high-current digital noise spikes from sensitive RF and analog sections. All ground potentials must be DC coupled, and resistive drops should contribute no more than 50mV difference between the ground pins. A single-point analog ground ("star" ground point) should be established at the ground supply connection to the PC

board, separate from the active circuitry. Three ground planes should be established, connected at the star ground point. The three ground planes should be dedicated as follows: analog and RF ground plane, digital ground plane, and output ground plane. The various ground pins should be connected to this star ground network according to Table 2. The ground current return path for all supplies should be low impedance at frequencies of interest for each supply.

Table 2. Ground Plane Assignments

Ground Pin	Pin Number	Ground Plane
VGNDIF	94	analog
VGNDI	79	analog
VGNDQ	2	analog
VGND2	16	analog
VGNDAD	20, 21	analog
VGNDP	10	digital
VGNDC	66	digital
VGND D	34, 47	digital
VGND O	26, 30, 37, 43, 51, 55	output

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the MAX2101 package.

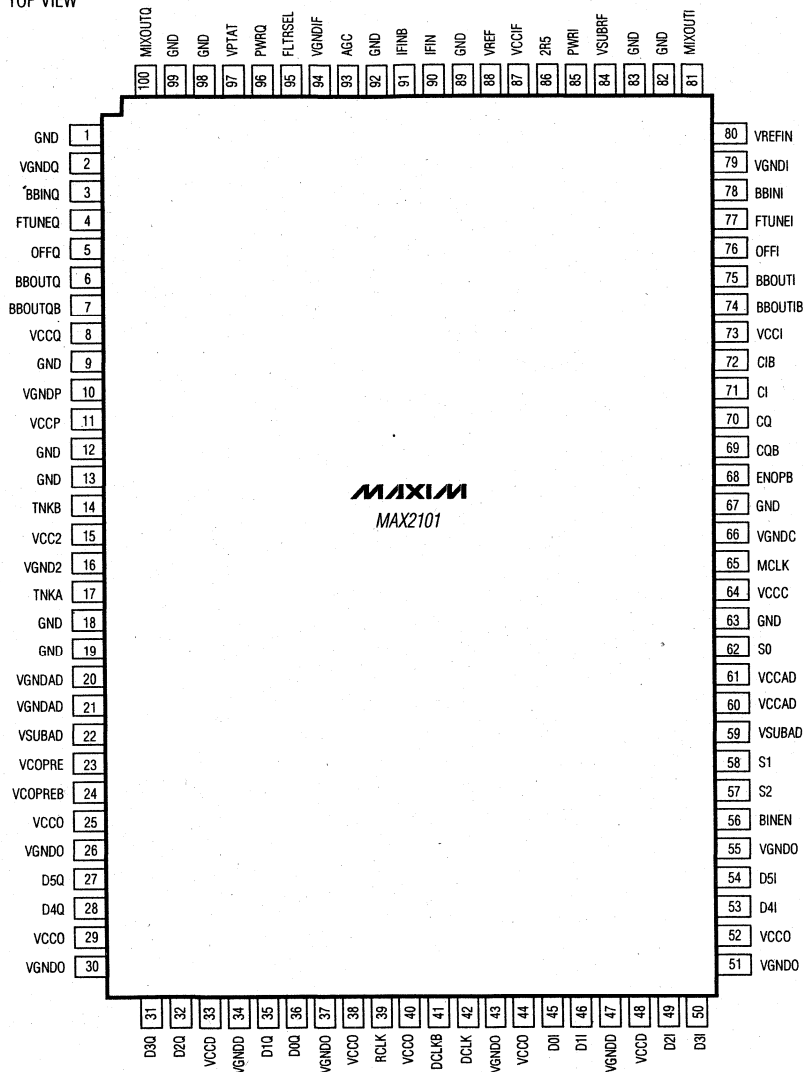
The MAX2101 requires +5V $\pm$ 5% for all supply pins. Bypass the supply pins with high-quality 0.1 μ F and 0.001 μ F ceramic capacitors located as close to the package as possible. The high-frequency supplies, VCCIF and VCC2, both require an additional ceramic surface-mount bypass capacitor nominally valued at 47pF. The baseband supplies (VCCI and VCCQ) need additional filtering to ensure sufficient channel-to-channel isolation. Place a small-value resistor, such as 5 Ω , between the supply and the pins to create a single-pole filter with the bypass capacitor. The DC IR drop across the resistor should not exceed 150mV. Alternatively, place an RF choke between the supply and the pins. The SRF of the selected choke must be high enough to block energy from the other baseband channel.

6-Bit Quadrature Digitizer

Pin Configuration

MAX2101

TOP VIEW



10

EVALUATION KIT
AVAILABLE**MAXIM**

800MHz to 1000MHz Transmitter

General Description

The MAX2402 transmitter integrates a double-balanced mixer, buffered local oscillator (LO) port, variable gain stage, and power amplifier into a single IC. It is intended for use in the 800MHz to 1000MHz band, and is compatible with both direct-sequence and frequency-hopping spread-spectrum designs in the 902MHz to 928MHz ISM band.

In a typical application, a digital baseband signal is mixed with a local oscillator signal to yield a BPSK-modulated carrier at the antenna. Alternatively, the baseband input may be grounded and an FSK-modulated LO signal applied directly to the LO port. The LO port consists of a limiting amplifier that can accept a single-ended or differential signal with input power between -6dBm and +6dBm in the frequency range of 800MHz to 1000MHz. The baseband modulation input is linear over a 2V range, and limits with larger signal levels within the supply range. The double-balanced mixer has been optimized for high carrier rejection. The variable gain stage offers typically 40dB of adjustment range. The power amplifier provides more than 20dBm output power and has a bias adjustment, which allows adjustment of efficiency and harmonic distortion.

A shutdown function reduces the current draw to less than 2 μ A in less than 10 μ s. The MAX2402 comes in a 20-pin SSOP package to minimize board area.

Applications

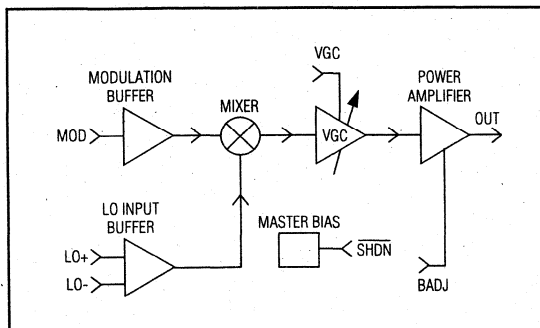
Direct-Sequence Spread-Spectrum Transmitter

Frequency-Hopping Spread-Spectrum Transmitter

FSK, GMSK, BPSK, and ASK Digital Transmitter

AM and FM Analog Transmitter

Functional Diagram



Features

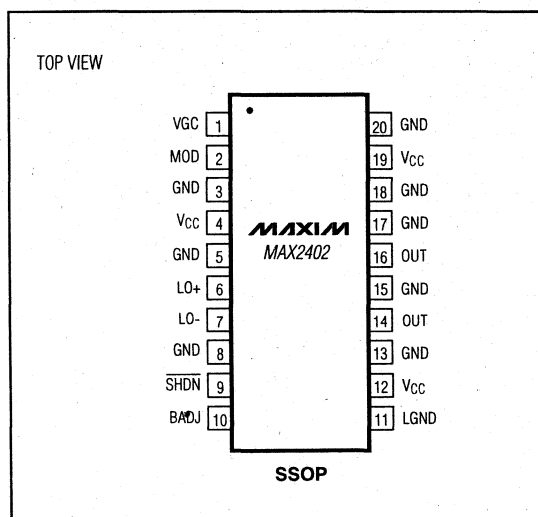
- ♦ Low-Cost, Flexible Transmitter
- ♦ More than 100mW of Output Power into 50 Ω
- ♦ Operates from 800MHz to 1000MHz
- ♦ Single +5V Supply
- ♦ 20-Pin SSOP Package
- ♦ Uses Less than 2 μ A in Power-Down
- ♦ More than 35dB of Power Adjustment Range
- ♦ LO Input Power Range from -6dBm to +6dBm
- ♦ 2V Linear Range on Modulation Input

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2402EAP*	-40°C to +85°C	20 SSOP

* An alternate marking, MAX2402CAP, has been identically tested.

Pin Configuration



MAX2402

10**MAXIM**

Maxim Integrated Products 10-33

Call toll free 1-800-998-8800 for free samples or literature.

800MHz to 1000MHz Transmitter

ABSOLUTE MAXIMUM RATINGS

V_{CC} -0.3V to +6.5V
 Continuous Power Dissipation (T_A = +70°C)
 SSOP (derate 16.7mW/°C above +70°C) 1330mW
 Operating Temperature Range -40°C to +85°C

Storage Temperature Range -65°C to +160°C
 Lead Temperature (soldering, 10sec) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V, BADJ = open, SHDN = V_{CC} - 0.5V, VGC = V_{CC}, MOD = open, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I _{CC}	Not transmitting		105		mA
Shutdown Supply Current	I _{CCPD}	SHDN = 0.5V		0.15	2	μA
Supply Voltage Range	V _{CC}		4.75		5.50	V
VGC Input Bias Current	I _{VGC}	VGC = V _{CC}			115	μA
MOD Bias Current	I _{MOD}	MOD = V _{CC}			325	μA
		MOD = 0V	-320			
SHDN Bias Current	I _{PD}	SHDN = V _{CC}			10.5	μA
SHDN Low Threshold	V _{SHDN} Low				0.5	V
SHDN High Threshold	V _{SHDN} High		V _{CC} - 0.5			V

AC ELECTRICAL CHARACTERISTICS

(MAX2402 evaluation kit, V_{CC} = 5.0V, BADJ = 2V, SHDN = V_{CC}, MOD = 0V, VGC = V_{CC}, R_{LOAD} = 35Ω, f_{LO} = 900MHz, LO power = -3dBm, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I _{CCAC}	P _{OUT} = 20dBm (including current to load)		165		mA
Maximum Output Power	P _{MAX}	(Note 1)		21		dBm
Minimum Output Power	P _{MIN}	VGC = 0V (Note 1)		-19		dBm
Power Gain from LO	P _{GAIN}			24		dB
LO Input Power Range	P _{LO}	For max power out (50Ω input term) (Note 2)	-6		6	dBm
LO Frequency Range	f _{LO}	(Note 2)	800		1000	MHz
MOD Usable Bandwidth	MODBW	(Note 2)			25	MHz
VGC Control Range	VGC	(Note 2)	1.0		2.5	V
Carrier Suppression	CS	MOD = 5Vp-p @ 100kHz		30		dBc
2nd Harmonic Suppression	HS2	(Note 1)		22		dBc
3rd Harmonic Suppression	HS3	(Note 1)		25		dBc
Output IP3 (BADJ = 1.0V)	IP3	f _{LO} = 900MHz + 901MHz		28.4		dBm

Note 1: See *Typical Operating Characteristics* graphs.

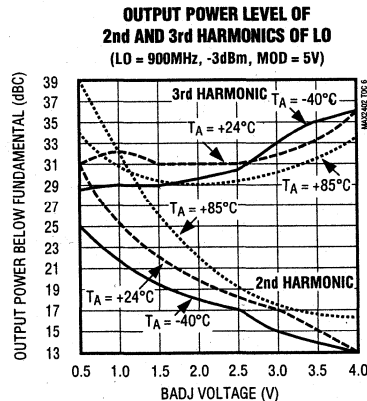
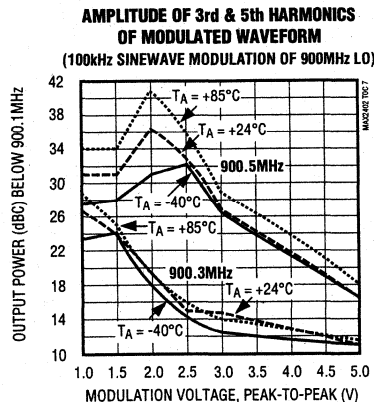
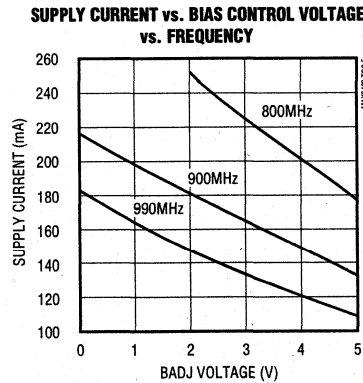
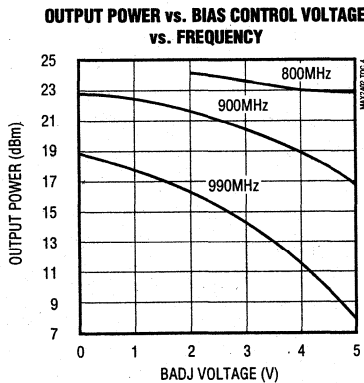
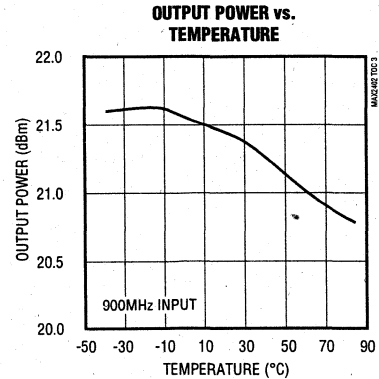
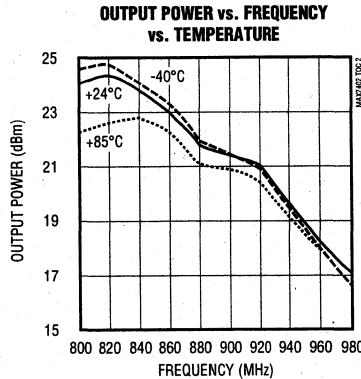
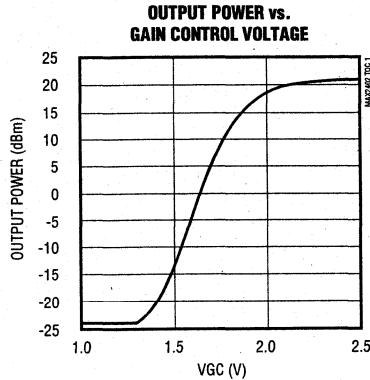
Note 2: Guaranteed by design.

800MHz to 1000MHz Transmitter

Typical Operating Characteristics

(MAX2402 evaluation kit, $V_{CC} = 5.0V$, $BADJ = 2V$, $SHDN = V_{CC}$, $MOD = 0V$, $VGC = V_{CC}$, $R_{LOAD} = 35\Omega$, $f_{LO} = 900MHz$, $LO\ power = -3dBm$)

MAX2402



800MHz to 1000MHz Transmitter

Pin Description

PIN	NAME	FUNCTION
1	VGC	Variable Gain Control Input. Connect to V _{CC} for maximum gain.
2	MOD	Baseband Modulation Input to mixer
3, 5, 8, 13, 15, 17, 18, 20	GND	Ground
4, 12, 19	V _{CC}	Supply Voltage, set between 4.75V and 5.5V
6	LO+	Local-Oscillator Positive Input
7	LO-	Local-Oscillator Negative Input
9	SHDN	Shutdown Control Input. Low level = off, high level = on.
10	BADJ	Bias Adjustment Control for power amplifier. Connect resistor from BADJ to V+ or GND (see Table 1).
11	LGND	Connect 27nH inductor from LGND to GND to maximize output power.
14, 16	OUT	Power-Amplifier Output

Detailed Description

The MAX2402 transmitter is a versatile design that integrates several RF functions on a single IC. It has a wide variety of applications in portable and stationary wireless designs. Each of the functional blocks (shown in the *Functional Diagram*) is described in detail in the following sections.

LO Inputs

The LO inputs are internally capacitively coupled and self biasing. The LO port can be driven differentially or single ended. When terminated at the LO inputs with 50 Ω , the transmitter will provide full output power for LO inputs from -6dBm to +6dBm with single-ended drive, and -12dBm to +6dBm with differential drive. Input power beyond this range may saturate the LO input buffer, while input power below this range may result in less output power. The limiter is two cascaded differential stages, which also isolates the LO input from the mixer. This will help reduce any frequency-pulling effects in an external LO due to mixer loading. The limiter output drives one port of a double-balanced Gilbert mixer.

MOD Input

The other port of the mixer, the MOD input, remains linear over a 2V range from about 1.5V to 3.5V at the input. When driven with digital modulation (0V to 5V) this port will completely limit, resulting in a hard BPSK-modulated signal. Since this input is self biasing, carrier suppression can be improved by externally capacitively coupling the signal into the port (the MOD input resistance is approximately 10k Ω). This would compensate for voltage offset or duty-cycle offset at this port, thus increasing carrier suppression. This MOD self bias is designed for very low on-chip offset, resulting in excellent carrier suppression. Since this port self biases when the signal is removed from MOD, the mixer will attenuate the output power by about 40dB, resulting in further attenuation past that attained from VGC control—a useful feature for ASK modulation.

VGC Stage

The mixer output drives the VGC stage. This stage attenuates through a multiplication technique that does not distort the signal with increased attenuation. VGC control is non-attenuating when connected to the V_{CC} supply. VGC will attenuate for voltages from 2.5V to 1.0V. Most attenuation occurs between 1V and 2V. Maximum attenuation is achieved below 0.8V. Typical maximum attenuation is 40dB. At or beyond 40dB of attenuation, the signal may be slightly non-monotonic. This means that there may be a slight upturn in the signal level at the low end of the VGC control range (typically about 1dB). Because of the stability implications, we suggest that the user not plan on attenuating past 35dB within a feedback loop.

Power Amplifier

The VGC stage passes the signal to the power amplifier. This class AB stage will produce at least 20dBm of output power for almost the complete transmit frequency range (with T_A = +25°C). See *Typical Operating Characteristics*.

BADJ Input

The BADJ input adjusts the bias of the output stage. Increasing this voltage decreases bias current in the output devices, which increases efficiency, but also increases harmonic distortion (since the stage will be pushed further toward class B operation). Decreasing BADJ's voltage will increase bias current in the output devices, resulting in higher output power and less harmonic distortion. The user will want to optimize BADJ for their application.

800MHz to 1000MHz Transmitter

BADJ can be left open or adjusted with a single pull-up or pull-down resistor to V_{CC} or GND, respectively. The value of this resistor will determine the amount of adjustment applied. A single resistor will result in no current flow at BADJ during power-down (whereas a resistor divider would always have current flowing through the resistors). Table 1 shows the approximate bias adjust voltage at the pin for different resistor values. At lower LO frequencies, where the transmitter gain and output power is the highest, setting BADJ to a low voltage (maximum bias current) will cause excessive current in the output and may cause unstable behavior in the IC. At lower LO frequencies (around 800MHz), more than 22dBm of power is easily obtained with BADJ set for 3V or more. If higher bias current and less distortion is desired in the 800MHz range, using a lower inductor value on LGND (pin 11) (see the *Typical Application Circuit*) may make the desired bias level stable. At higher frequencies (near 1000MHz), a lower bias level voltage will result in more power (see the Output Power vs. Bias Control Voltage vs. Frequency graph in the *Typical Operating Characteristics*).

Table 1. Bias-Adjust Voltage for Various Resistor Values

Resistor Value (Ω)	BADJ with Resistor Connected to GND (V)*	BADJ with Resistor Connected to V_{CC} (V)
10k	0.36	4.54
20k	0.63	4.27
30k	0.84	4.05
40k	1.00	3.89
50k	1.13	3.75
100k	1.54	3.34
200k	1.89	3.00
300k	2.05	2.85
400k	2.13	2.75
500k	2.20	2.68
1M	2.31	2.57

* Typical variation of BADJ over temperature and process is less than 5%.

Power Amplifier Output

The power amplifier has an open-collector output that can drive into a load of 30Ω to 50Ω , however maximum power transfer is obtained at about 35Ω . As shown in the *Typical Application Circuit*, 27nH to ground is recommended on LGND (pin 11). This inductor is used as a current source on the base of the output stage to pull stored charge out of the base.

SHDN Input

The SHDN input will completely shut down the current from the supply and all signal pins when switched below 0.5V. During normal operation, SHDN should remain above $V_{CC} - 0.5V$.

The shutdown control will shut down the total current to below 150nA (typ). Power-up will occur within 10 μ s.

Applications Information

The MAX2402 transmitter is designed to operate within the 800MHz to 1000MHz frequency range. Figure 1 shows a Typical Application Circuit. Additional applications information can be obtained from the MAX2402 evaluation kit manual.

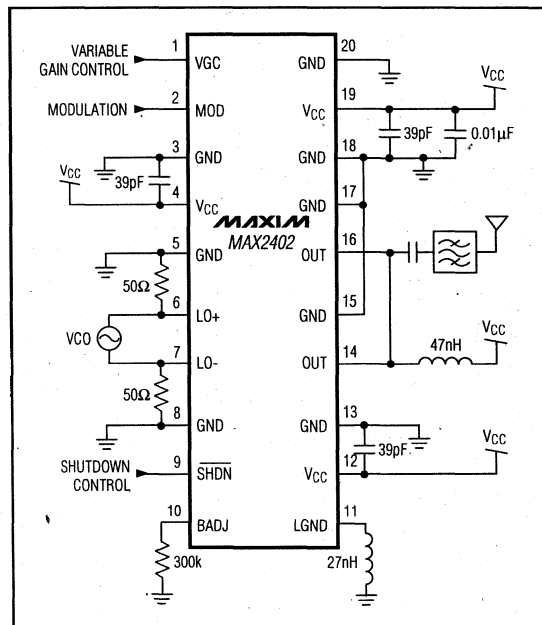


Figure 1. Typical Application Circuit

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

800MHz to 1000MHz Low-Voltage Power Amplifier/Predriver

General Description

The MAX2430 RF power amplifier operates from a 3V to 5V supply and delivers more than 100mW (20dBm) in the 800MHz to 1000MHz band. The MAX2430 consists of a large power transistor driven by a capacitively coupled driver stage. The input impedance is internally matched to 50Ω (VSWR < 1.5:1) and the overall power gain is guaranteed to be greater than 30dB.

To save power during the "idle slots" in time-division multiple-access (TDMA) transmissions, a TTL/CMOS-compatible command (EN pin low) can throttle the supply current to under 10μA in only 1μs. A power ramping feature allows the final stage on/off time to be controlled by a single external capacitor. Variable power-gain control of the final stage is also possible for use in a power control loop. The MAX2430 comes in a 16-pin narrow SO package.

Applications

Cordless Phones
Wireless LANs
Cellular Phones
915MHz ISM Band Applications

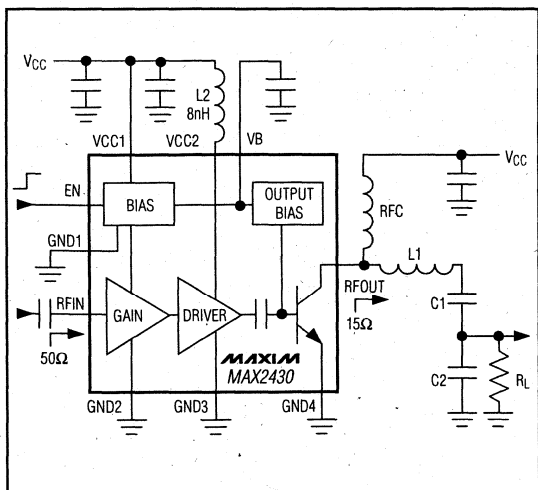
Features

- ♦ 3-Cell Battery Operation
- ♦ >100mW Output Power (at 3V)
- ♦ 30dB Power Gain
- ♦ Power Up/Down Ramp Time Controlled by External Capacitor
- ♦ Input Matched to 50Ω
- ♦ 10μA Power-Down Current
- ♦ Comes in 16-Pin Narrow SO

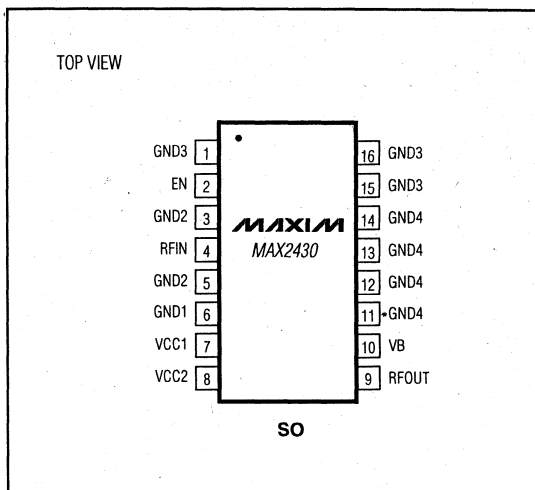
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2430CSE	0°C to +70°C	16 Narrow SO

Typical Operating Circuit



Pin Configuration



MAX2430

10

MAXIM

Maxim Integrated Products 10-39

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

70MHz Quadrature Modulator/Demodulator

MAX2450

General Description

The monolithic MAX2450 is a quadrature modulator and demodulator with supporting oscillator and divide-by-8 prescaler. It operates from a single +3V supply and draws less than 9mA. The modulator accepts 10MHz differential I and Q baseband signals with amplitudes up to 1.2Vp-p, and produces a 70MHz differential IF output. The demodulator circuitry provides 49dB of conversion gain, automatic cancellation of baseband offset, and a 400Ω input impedance for matching to an external IF filter.

A command to the CMOS-compatible power-down control lowers the supply current to less than 20μA. To minimize spurious feedback, the MAX2450's internal oscillator is set at 140MHz (twice the IF) via external tuning components. The oscillator and associated phase shifter produce differential signals exhibiting amplitudes within ±0.3dB, and a phase imbalance no greater than ±3°. The MAX2450 comes in a 20-pin SO package.

Applications

900MHz Digital Cordless Phones

GSM and North American Cellular Radios

Wireless LANs

VHF Transceivers

Digital Satellite Communications

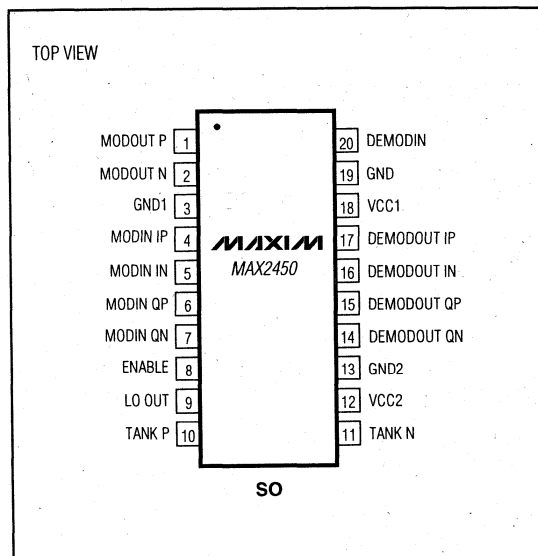
Features

- ♦ Quadrature Modulator and Demodulator on the Same IC
- ♦ On-Chip Oscillator with External Tuning Circuit
- ♦ Integrated Quadrature Phase Shifters
- ♦ On-Chip Divide-by-8 Prescaler
- ♦ Modulator Input Bandwidth up to 10MHz
- ♦ 49dB Demodulator Conversion Gain
- ♦ Draws <30mW from a Single +3V Power Supply
- ♦ CMOS-Compatible Control for Power Up/Down

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2450CWP	0°C to +70°C	20 SO

Pin Configuration



10

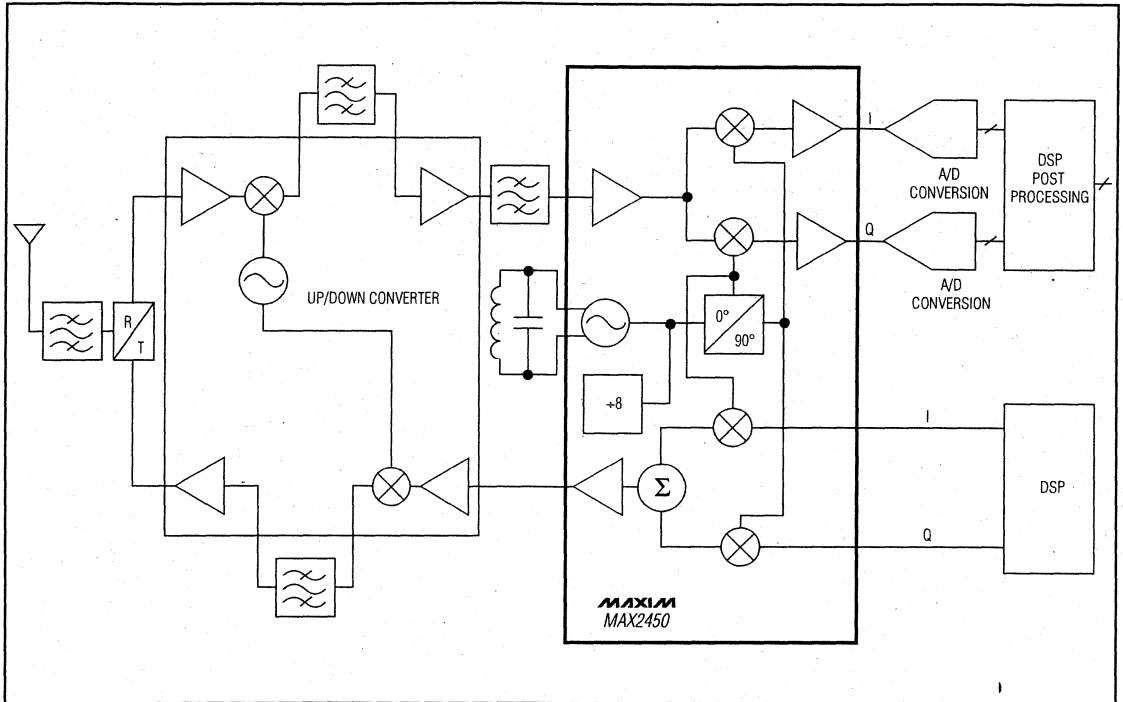
MAXIM

Maxim Integrated Products 10-41

Call toll free 1-800-998-8800 for free samples or literature.

70MHz Quadrature Modulator/Demodulator

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

70MHz Quadrature Demodulator

General Description

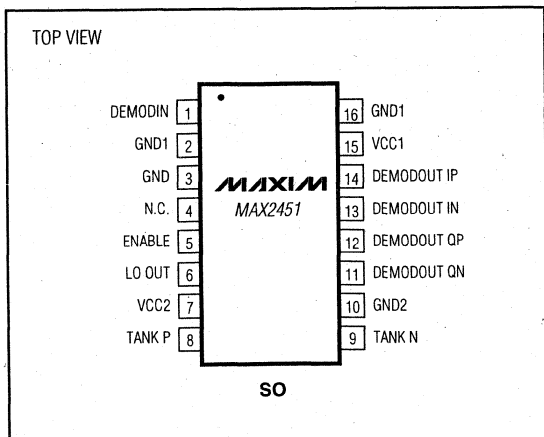
The monolithic MAX2451 is a quadrature demodulator with supporting oscillator and divide-by-8 prescaler. It operates from a single +3V supply and draws less than 8.5mA. The demodulator circuitry provides 49dB of conversion gain, automatic cancellation of baseband offset, and a 400Ω input impedance for matching to an external IF filter.

A command to the CMOS-compatible power-down control lowers the supply current to less than 20μA. To minimize spurious feedback, the MAX2451's internal oscillator is set at 140MHz (twice the IF) via external tuning components. The oscillator and associated phase shifter produce differential signals exhibiting amplitudes within ±0.3dB, and a phase imbalance no greater than ±3°. The MAX2451 comes in a 16-pin narrow SO package.

Applications

900MHz Digital Cordless Phones
GSM and North American Cellular Radios
HDTV Receivers
Video Set-Top Cable Boxes
Wireless LANs
GPS Receivers

Pin Configuration



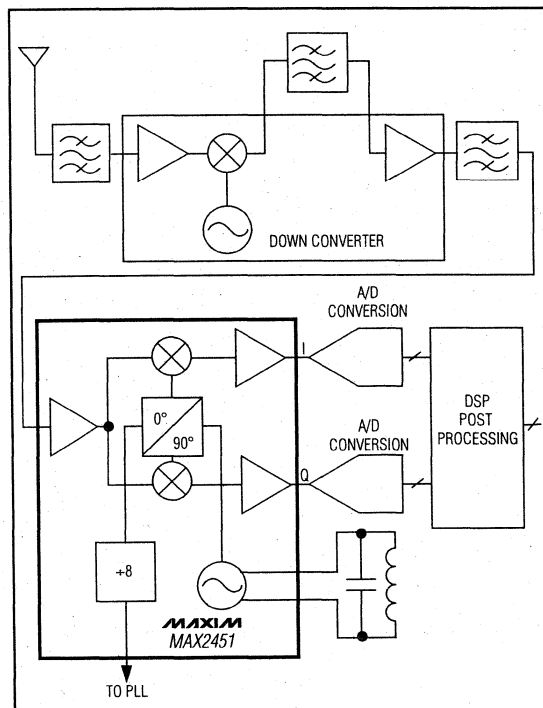
Features

- ◆ 49dB Conversion Gain
- ◆ On-Chip Oscillator with External Tuning Circuit
- ◆ On-Chip Divide-by-8 Prescaler
- ◆ Integrated Quadrature Phase Shifters
- ◆ Demodulator Output Bandwidth >7MHz
- ◆ Draws <30mW from a Single +3V Power Supply
- ◆ CMOS-Compatible Control for Power Up/Down

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2451CSE	0°C to +70°C	16 Narrow SO

Typical Operating Circuit



10

MAXIM

Maxim Integrated Products 10-43

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ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/95

MAXIM

70MHz Quadrature Modulator

MAX2452

General Description

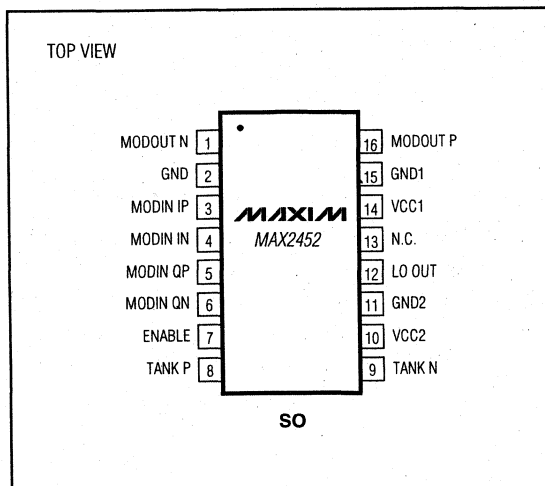
The monolithic MAX2452 is a quadrature modulator with supporting oscillator and divide-by-8 prescaler. It operates from a single +3V supply and draws less than 7.5mA. The modulator accepts 10MHz differential I and Q baseband signals with amplitudes up to 1.2Vp-p, and produces a 70MHz differential IF output.

A command to the CMOS-compatible power-down control lowers the supply current to less than 20µA. To minimize spurious feedback, the MAX2452's internal oscillator is set at 140MHz (twice the IF) via external tuning components. The oscillator and associated phase shifter produce differential signals exhibiting amplitudes within ±0.3dB, and a phase imbalance no greater than ±3°. The MAX2452 comes in a 16-pin narrow SO package.

Applications

- 900MHz Digital Cordless Phones
- GSM and North American Cellular Radios
- Wireless LANs
- Digital Satellite Communications

Pin Configuration



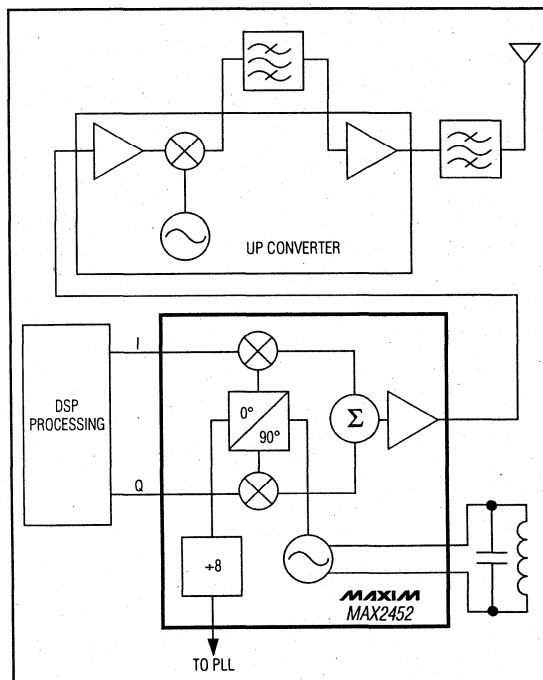
Features

- ♦ Input Bandwidth up to 10MHz
- ♦ On-Chip Oscillator with External Tuning Circuit
- ♦ On-Chip Divide-by-8 Prescaler
- ♦ Integrated Quadrature Phase Shifters
- ♦ Self-Biased Differential Baseband Inputs
- ♦ Single +3V Power Supply
- ♦ CMOS-Compatible Control for Power Up/Down

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2452CSE	0°C to +70°C	16 Narrow SO

Typical Operating Circuit



10

MAXIM

Maxim Integrated Products 10-45

Call toll free 1-800-998-8800 for free samples or literature.



Fiber/Cable Products

Fiber/Cable Products, Product Table	11-2
MAX3260 1GHz Transimpedance Preamplifier w/ 25dB Dynamic Range	11-3
MAX3261 1.2Gbps, 5V, Fully Integrated Laser Diode Driver	11-7
MAX3262 1Gbps, High-Speed Limiting Amp w/ Chatter-Free Loss-of-Signal Detection	11-19
MAX3263 155Mbps, 5V, Fully Integrated Laser Diode Driver*	11-27
MAX3270 155/622Mbps Clock Recovery and Data Retiming IC w/ Fully Integrated Phase/Frequency Detector	11-29

*Advance Information—first page of data sheet in preparation.

Fiber/Cable Communications Products

Fibre Channel Communications Products									
Part Number	Supply Voltage (V)	Analog Bandwidth (GHz)	Trans-Impedance (Ω)	Max Input (μA)	Input Noise (nA)	Pins- Package	Features	Applications	
TRANSIMPEDANCE PREAMPLIFIERS									
MAX3260	+5	1.0	2000	900	240	die only	Single supply, 25dB dynamic range, optimized for TO header	Fibre Channel, SDH/SONET	
Part Number	Supply Voltage (V)	Data Rate (Mbps)	Max Gain (dB)	Min LOS Sensitivity (mV)	Input Noise (μV)	Pins- Package	Features	Applications	
LIMITING POSTAMPLIFIERS									
MAX3262	+5	1063	48	9	80	24-SSOP	900MHz bandwidth, programmable LOS threshold, single supply	Fibre Channel, SDH/SONET	
Part Number	Supply Voltage (V)	Data Rate (Mbps)	Max Modulation Current (mA)	Max Bias Current (mA)	Pins- Package	Features	Applications		
LASER DIODE DRIVERS									
MAX3261	+5	1200	25	60	32-TQFP	Automatic power control, single supply, temperature-compensated reference voltage	Fibre Channel, SDH/SONET		
MAX3263†	+5	155	25	60	24-SSOP	Automatic power control, single supply, temperature-compensated reference voltage	Fibre Channel, ATM/SONET		
Part Number	Supply Voltage (V)	Data Rate (Mbps)	I/O Levels	Bellicore Jitter Tolerance	Pins- Package	Features	Applications		
CLOCK RECOVERY AND DATA RETIMING ICs									
MAX3270	+5 & -5	155 or 622	ECL	Surpasses specification	44-MQFP	Selectable data rate, fully integrated PLL, no external reference clock required	SDH/SONET, ATM/SONET		

† Future product—contact factory for pricing and availability. Specifications are preliminary.

MAXIM

1GHz Transimpedance Preamplifier with 25dB Dynamic Range

General Description

The MAX3260 high-speed transimpedance amplifier is ideally suited for Fibre Channel and SDH/SONET applications. An extended dynamic range makes the MAX3260 useful in optical receiver systems with as much as 25dB of input signal range. A DC-restore feedback network prevents amplifier saturation in all Fibre Channel applications by allowing input currents as high as 900 μ A to be amplified linearly. To reduce noise, the restore function is disabled at low input levels, allowing detection of signals as small as 2.4 μ A with a signal-to-noise ratio of 10.

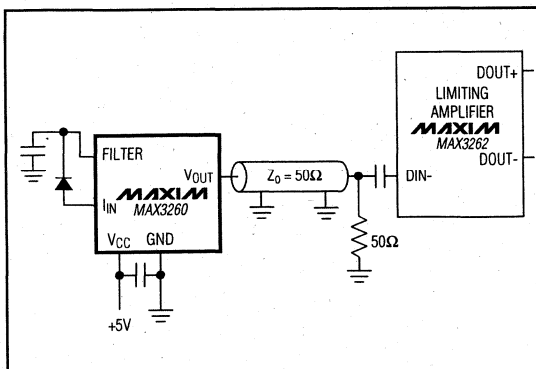
The filter output (FILTER) of the MAX3260 provides a convenient voltage source for a photodiode, especially when the circuit will be placed into a TO-style header with the photodiode. The filter output is connected to VCC through a 1k Ω on-chip resistor. In combination with a bypass capacitor, the filter function significantly reduces the amount of noise present at the cathode of the photodiode.

The MAX3260 operates from a single +5V supply consuming only 115mW of power when the output is AC coupled. With 50 Ω output termination, it consumes less than 300mW of power.

Applications

High-Speed Fiber Optics
531Mbps and 1062Mbps Fibre Channel
622Mbps SDH/SONET
Current-to-Voltage Converters
PIN-Preamp Headers

Typical Operating Circuit



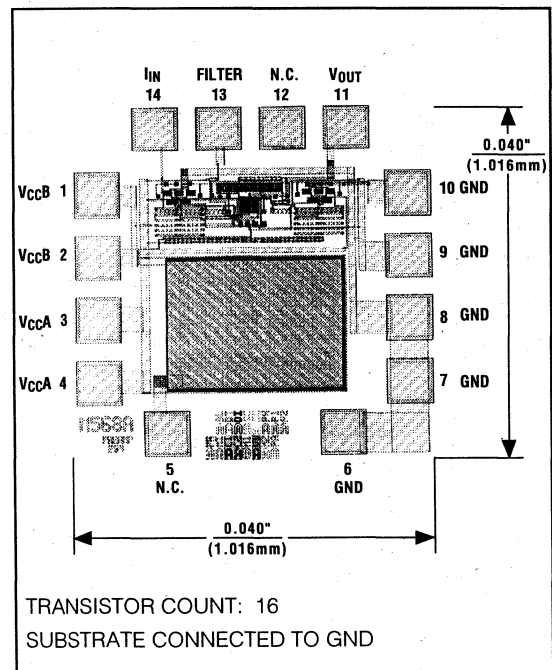
Features

- ◆ 1GHz Bandwidth
- ◆ Single 5V Supply
- ◆ 25dB Dynamic Range
- ◆ Optimized for TO-Style Header

Ordering Information

PART	T _J RANGE	PIN-PACKAGE
MAX3260C/D	0°C to +100°C	Dice

Chip Topography



MAX3260

11

MAXIM

Maxim Integrated Products 11-3

Call toll free 1-800-998-8800 for free samples or literature.

1GHz Transimpedance Preamplifier with 25dB Dynamic Range

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CCA} , V_{CCB} to GND0V, 6V
 Input Current, I_{IN} , FILTER1.5mA
 Input Bias Voltage, V_{IN} 0V, 6V

Output Voltage, V_{OUT} 0V, 6V
 Operating Junction Temperature-55°C to +150°C
 Processing Temperature.....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V$, output terminated with 50Ω to ground, 100% tested, $T_J = +27^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS						
Input Bias Voltage	V_{IN}			1.6		V
DC-Restore Time Constant	t_{DC}			1		μs
Filter Resistor Value	R_{FILTER}		750		1250	Ω
Supply Current	I_{VCC}	50Ω load to ground		56	70	mA
DC Transimpedance		$I_{IN} > 400\mu A$	-400			V/A
		$I_{IN} < 100\mu A$	-2400	-2000	-1600	
DC-Restore Activation Current	$I_{RESTORE}$			350		μA
AC SPECIFICATIONS (Not production tested)						
Small-Signal Transimpedance	GT		-2400	-2000	-1600	V/A
-3dB Bandwidth	BWU		0.8	1.0		GHz
Peak Input Current	I_{IN}				900	μA
Pulse-Width Distortion	PWD	(Notes 1, 2, 3)			100	ps
Input Referred Current Noise	I_{NRMS}	(Notes 2, 4)			240	nA
Power-Supply Rejection Ratio	PSRR			21		dB
Output Resistance	R_{OUT}			3		Ω

Note 1: Input is a square wave with 0.5GHz frequency and <200ps rise time.

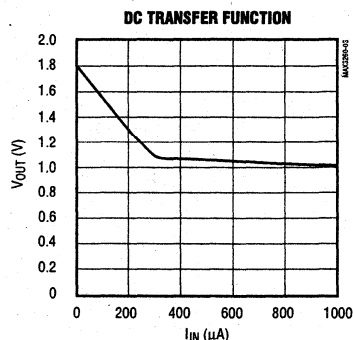
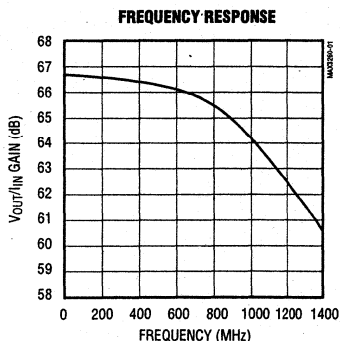
Note 2: External capacitance on the input $\leq 0.4pF$.

Note 3: Pulse-width distortion measured at the 50% level of the output pulses: Input is 900 μA , zero-peak.

Note 4: Output noise is measured through a four-pole Bessel filter with -3dB bandwidth of 800MHz.
 Noise is then referred to the input by dividing the DC transimpedance.

Typical Operating Characteristics

($T_J = +27^\circ C$, unless otherwise noted.)

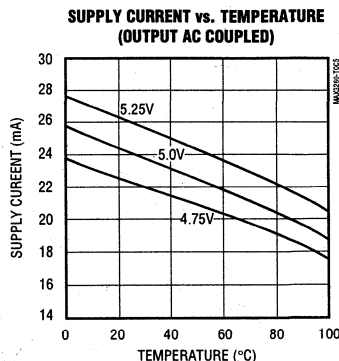
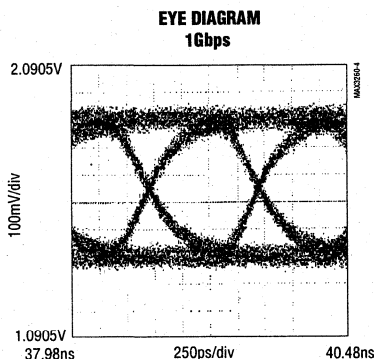


1GHz Transimpedance Preamplifier with 25dB Dynamic Range

Typical Operating Characteristics (continued)

($T_J = +27^\circ\text{C}$, unless otherwise noted.)

MAX3260



Detailed Description

The MAX3260 is a high-speed transimpedance amplifier, designed to accommodate input currents with a large dynamic range. This circuit is optimized to operate in a 1062Mbps Fibre Channel receiver, and is also suitable for use in 622Mbps SONET applications.

The MAX3260 employs shunt-shunt feedback around a bipolar amplifier. The resulting circuit provides an inverted current-to-voltage conversion. The conversion gain is nominally -2000V/A .

Modern fiber-optic communications systems place many requirements on transimpedance preamplifiers. Power budgets are important when considering a preamp, since the circuit will generally be placed into a small module or header, which limits the amount of heat dissipation. In addition, the signal presented to the preamp may carry an 18dB to 20dB dynamic range, which must be amplified linearly to prevent the addition of jitter. Finally, preamp noise generally determines the receiver sensitivity, and must be held to a minimum.

The MAX3260 employs several techniques to address the needs of fiber-optic preamplifiers. The output of the MAX3260 operates in the 1V to 2V range (depending

on the average input) to keep output standing current at a minimum. The reduced output voltage helps keep power consumption low, but also reduces the dynamic range of the output stage. Fiber communications transimpedance amplifiers commonly use dynamic control of the shunt-shunt feedback loop to vary the gain. The unwanted side-effect of this technique is a circuit bandwidth that varies with input current. To prevent output-stage saturation, the MAX3260 employs a DC-restore circuit. As input signal power increases, DC current is drawn away from the input node of the amplifier. This reduces the DC gain of the amplifier without affecting the small-signal performance. To prevent noise feedback at low signals, an integrated comparator senses the power level and disables the DC-restore function.

The MAX3260's filter output provides a convenient voltage source for a photodiode, especially when the circuit will be placed into a TO-style header with the photodiode. The filter output is connected to V_{CC} through an on-chip $1\text{k}\Omega$ resistor. In combination with a bypass capacitor, the filter function reduces the bandwidth at the anode of the photodiode, therefore significantly reducing the amount of noise at the cathode. The filter connection can be left unconnected if not used.

11

1GHz Transimpedance Preamplifier with 25dB Dynamic Range

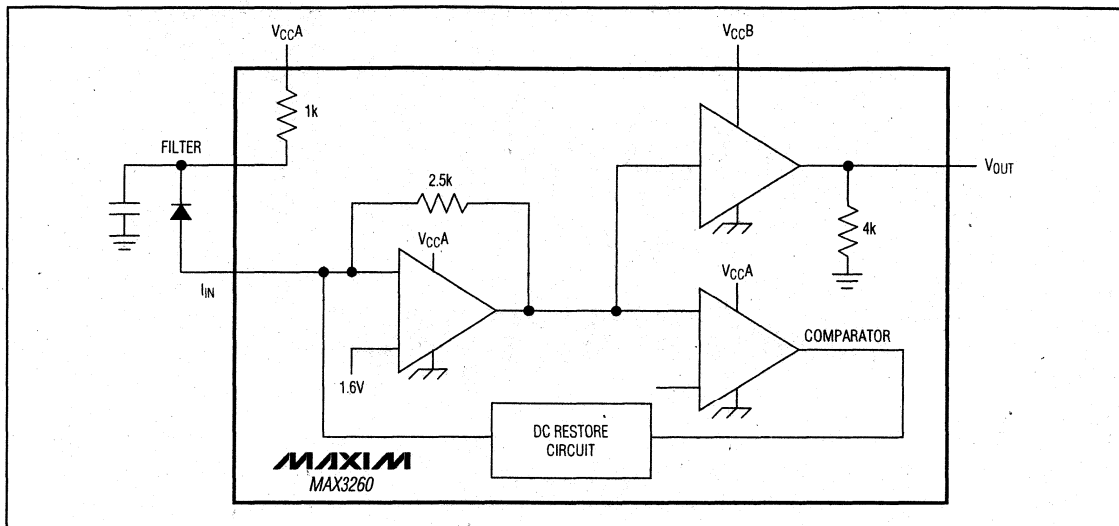


Figure 1. Functional Diagram

Wire Bonding

For high current density and reliable operation, the MAX3260 uses gold metallization. Connections to the die should be made with gold wire only, using ball bonding techniques. Wedge bonding is not recommended. Die pad size is 4 mils.

Design Procedure

The MAX3260 is a high-speed, high-gain component. Its performance is strongly affected by module design and layout. Improper design techniques can cause oscillations or ringing.

In fiber-optic receiver applications, it is highly recommended that the transimpedance preamplifier be placed close to the photodetector, in the same package or header if possible. This reduces parasitic inductance and improves static-discharge protection during manufacturing. An alternative layout is to assemble the preamplifier on a hybrid circuit board. In either case, the designer should ensure that power-supply runs to the VCCA and VCCB inputs are properly filtered. Keep ground connections to the MAX3260 short and minimize inductance. Multiple vias may be required when connecting to the ground plane on a circuit board, to reduce the ground inductance.

The MAX3260 will typically be connected to a limiting or post amplifier by means of a controlled-impedance transmission line. If a transmission line is used, it is important to end-terminate the line with the characteristic impedance to prevent reflections into the output of the MAX3260.

Applications Information

The MAX3260 consumes approximately 23mA of current with no output load. Typically, the majority of power used by the preamplifier is consumed in the output termination. The termination is needed at the end of the transmission line connecting MAX3260 to a limiting amplifier. The average output level is typically 1.6V, and is maintained at that level by the DC-restore function. A 50Ω termination to ground will consume 32mA of standing current. Power consumption can be reduced by terminating to higher resistance. A 75Ω transmission line and termination would consume only 22mA. Power consumption can be reduced dramatically by excluding the transmission line and termination, which requires very short distances between the MAX3260 and the following circuit.

MAXIM

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

General Description

The MAX3261 is a complete, easy-to-program, single +5V-powered, 1.2Gbps laser diode driver with complementary enable inputs and Automatic Power Control (APC). The MAX3261 accepts differential PECL inputs and provides complementary output currents. A temperature-stabilized reference voltage is provided to simplify laser current programming. This allows modulation current to be programmed from 5mA to 25mA and bias current to be programmed from 5mA to 60mA with two external resistors.

Complementary enable inputs allow the MAX3261 to interface with open-fiber-control architecture—a feature not found in other 1.2Gbps laser diode drivers.

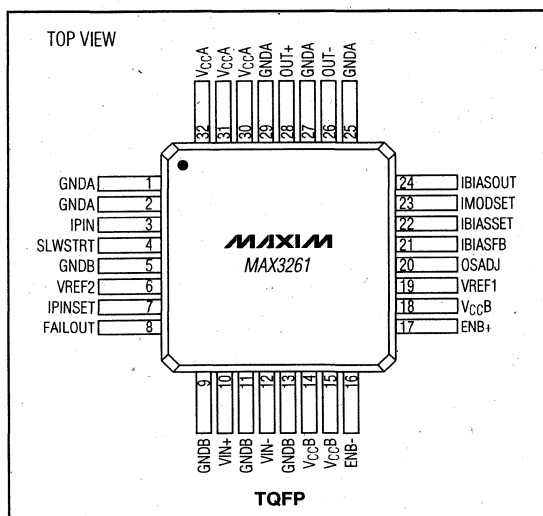
An APC circuit is provided to maintain constant laser power in transmitters that use a monitor photodiode. Only one external resistor is required to implement the APC function.

The MAX3261's fully integrated feature set includes a TTL-compatible laser failure indicator and a programmable slow-start circuit to prevent laser damage. The slow-start is preset to 50ns and can be extended by adding an external capacitor.

Applications

Laser Diode Transmitters
531Mbps and 1062Mbps Fibre Channel
622Mbps SDH/SONET

Pin Configuration



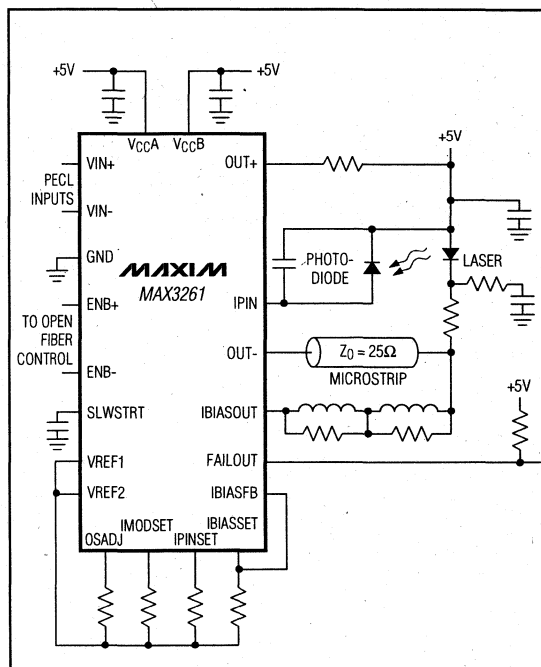
Features

- ◆ Rise Times Less than 250ps
- ◆ Differential PECL Inputs
- ◆ Single +5V Supply
- ◆ Automatic Power Control
- ◆ Temperature-Compensated Reference Voltage
- ◆ Complementary Enable Inputs

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3261CCJ	0°C to +70°C (T _A)	32 TQFP
MAX3261C/D	0°C to +100°C (T _J)	Dice

Typical Operating Circuit

**11****MAXIM**

Maxim Integrated Products 11-7

Call toll free 1-800-998-8800 for free samples or literature.

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

ABSOLUTE MAXIMUM RATINGS

(VCC = 5.0V, TA = +25°C, unless otherwise noted.)

Supply Voltages

VCCA, VCCB to GND	-0.3V, +6V
IPIN, IPINSET, IMODSET, IBIASET, OSADJ, IBIASFB	5mA
OUT+, OUT-, VREF1, VREF2	+6V
ENB+, ENB-	0V, VCC, -0.3V
FAILOUT	0V, VCC

SLWSTRT	+6V
IBIASOUT	90mA
Input Voltage Levels, VIN-, VIN+	0V, +6V
Operating Junction Temperature Range	-55°C to +175°C
Storage Temperature Range	-55°C to +175°C
Processing Temperature (Die)	+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V, TA = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Range of Programmable Laser Bias Current	IBIAS				60	mA
Reference Voltage	VREF		3.15	3.3	3.45	V
Available Reference Current	IREF			12		mA
Supply Current	IVCC	Failout loaded with 1kΩ to VCC, IBIAS = 0mA, IMOD = 0mA			60	mA
PECL Input High		Minimum swing is 550mV, TA = +25°C	VCC - 1.165			V
PECL Input Low		Minimum swing is 550mV, TA = +25°C		VCC - 1.475		V
TTL Low (Inputs/Outputs)					0.8	V
TTL High (Inputs/Outputs)			2.0			V

AC ELECTRICAL CHARACTERISTICS

(VCC = +5.0V, RLOAD = 25Ω to +5V, AC parameters are not tested, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Range of Programmable Modulation Current	IMOD	Minimum input swing is 550mV			25	mA
Modulation-Current Rise and Fall Time	tr, tf	IBIAS = 25mA, IMOD = 12mA, 8ns period, 10% to 90%			250	ps
Aberrations, Rising and Falling Edge	OS	IMOD = 12mA, MAX3261C/D		±10		%
		IMOD = 12mA, MAX3261CCJ		±15		
Modulation-Current Pulse-Width Distortion	PWD	IBIAS = 25mA, IMOD = 12mA, 8ns period			80	ps

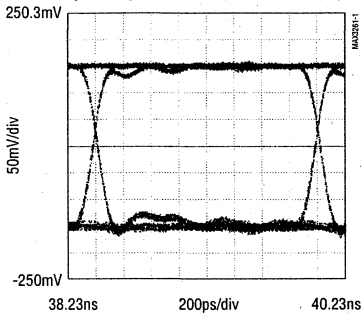
Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

Typical Operating Characteristics

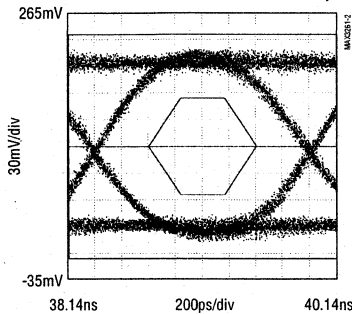
(MAX3261C/D, $R_L = 25\Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX3261

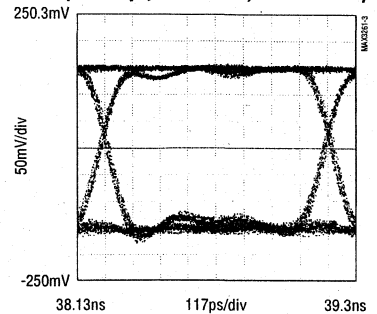
EYE DIAGRAM
(622Mbps, $R_L = 25\Omega$, NOT FILTERED)



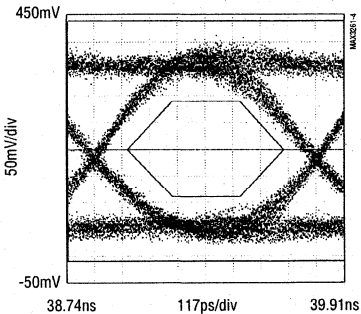
EYE DIAGRAM (622Mbps, LOAD = 1300nm LASER WITH 467MHz BESSEL FILTER)*



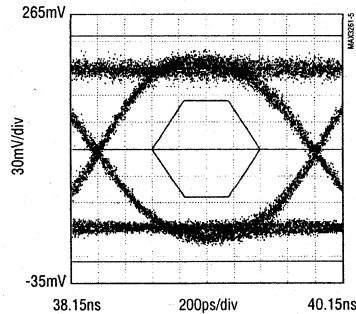
EYE DIAGRAM
(1062Mbps, LOAD = 25Ω , NOT FILTERED)



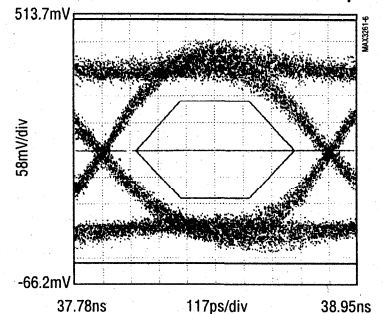
EYE DIAGRAM (1062Mbps, LOAD = 1300nm LASER WITH 800MHz BESSEL FILTER)*



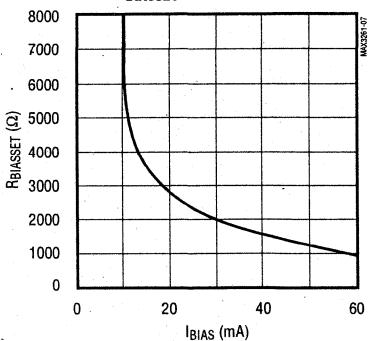
MAX3261CCJ
EYE DIAGRAM (622Mbps, LOAD = 1300nm LASER WITH 467MHz BESSEL FILTER)*



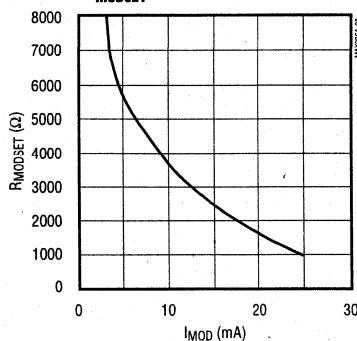
MAX3261CCJ
EYE DIAGRAM (1062Mbps, LOAD = 1300nm LASER WITH 800MHz BESSEL FILTER)*



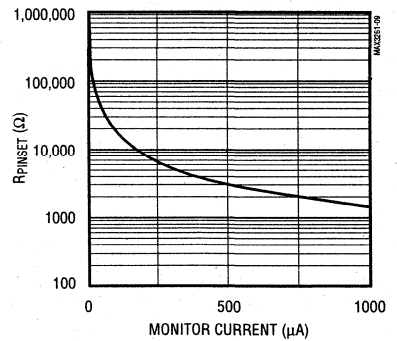
RBIASSET vs. BIAS CURRENT



RMODSET vs. MODULATION CURRENT



RPINSET vs. MONITOR CURRENT

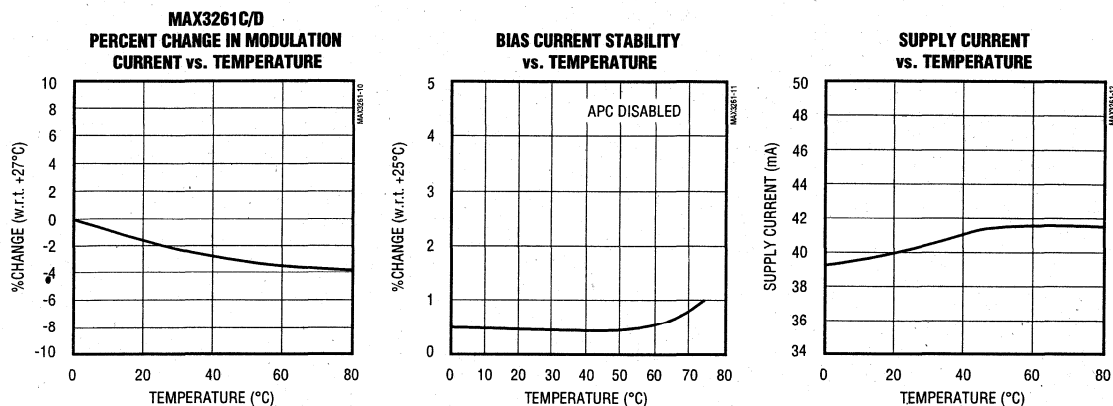


* EPITAXX EDL 1300RFC TO-STYLE HEADER

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

Typical Operating Characteristics (continued)

(MAX3216C/D, $R_L = 25\Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 2, 25, 27, 29	GNDA	Ground for Output and Bias Driver
3	IPIN	Current Source from Monitor Photodiode
4	SLWSTRT	Capacitor Port for Slow Start-Up. Turn-on time = $25.4\text{k} \times (\text{CSLWSTRT} + 2\text{pF})$.
5, 9, 11, 13	GNDB	Grounds for VREF and APC
6	VREF2	Temperature-Compensated Reference, 3.25V typical
7	IPINSET	Current Input for APC. Proportional to monitor-diode current.
8	FAILOUT	Active-Low Open-Collector TTL Output. Asserts when IPIN voltage drops below 2.6V.
10	VIN+	Positive PECL Inputs
12	VIN-	Negative PECL Inputs
14, 15, 18	VCCB	Positive Supplies for VREF and APC, +5V, $\pm 0.25\text{V}$
16, 17	ENB-, ENB+	Complementary TTL Input to Enable Output Currents
19	VREF1	Temperature-Compensated Reference, 3.25V typical
20	OSADJ	Overshoot Adjust, sets current for input stage. Connect to VREF with resistor.
21	IBIASFB	Output from APC Circuit, used to set laser bias current. Connect to IBIASSET terminal for APC operation.
22	IBIASSET	Sets Laser Bias Current. $\text{IBIASOUT} = 40 \times (\text{IBIASSET} + \text{IBIASFB})$.
23	IMODSET	Sets Laser Modulation Current. Modulation Current = $20 \times \text{IMODSET}$.
24	IBIASOUT	Laser Bias Output Current
26	OUT-	Primary Laser Modulation Outputs
28	OUT+	Secondary Laser Modulation Outputs
30, 31, 32	VCCA	Positive Supplies for Output and Bias Driver

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

Detailed Description

The MAX3261 laser driver has three main sections: a reference generator with temperature compensation, a laser bias block with automatic power control, and a high-speed modulation driver.

The reference generator provides temperature-compensated biasing and a voltage-reference output. The voltage reference is used to program the current levels of the high-speed modulation driver, laser diode, and PIN (p+, intrinsic, n-) monitor diode.

The laser bias block sets the bias current in the laser diode and maintains it above the threshold point. A current-controlled current source (current mirror) programs the bias, with IBIASSET as the input. The mirror's gain is approximately 40 over the MAX3261's input range. Keep the output voltage of the bias stage above 2.6V to prevent saturation.

The modulation driver consists of a high-speed input buffer and a common-emitter differential output stage. The modulation current mirror sets the laser modulation current in the output stage. This current is switched between the OUT+ and OUT- ports of the laser driver. The modulation current mirror has a gain of approximately 20.

MAX3261

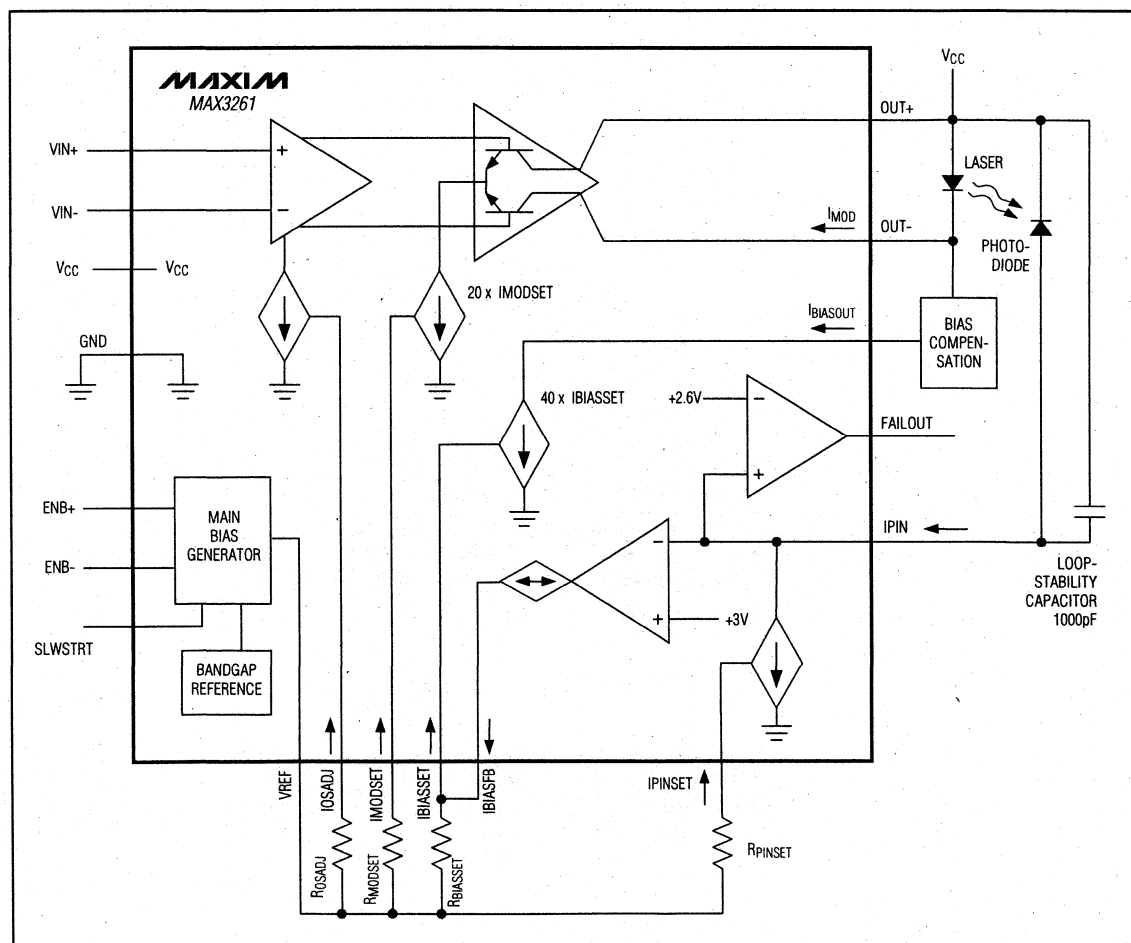


Figure 1. Block Diagram

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

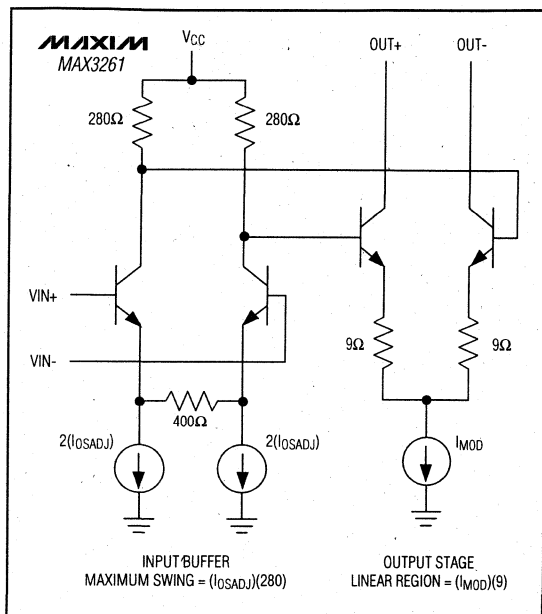


Figure 2. MAX3261 Modulation Driver (Simplified)

The overshoot mirror sets the bias in the input buffer stage. Reducing this current slows the input stage and reduces overshoot in the modulation signal. At the same time, the peak-to-peak output swing of the input buffer stage is reduced. Careful design must be used to ensure that the buffer stage can switch the output stage completely into the nonlinear region (Figure 3). For the output stage, the width of the linear region is a function of the desired modulation current. Increasing the modulation current increases the linear region. Therefore, increases in the modulation current requires larger output levels from the first stage. Table 1 shows the maximum allowable ROSADJ (to ensure complete switching) versus the laser modulation-current level.

Table 1. Optimum ROSADJ

I_{MOD} (mA)	Max ROSADJ (kΩ)
10	7.50
15	6.00
20	5.25
25	4.25
30	3.70

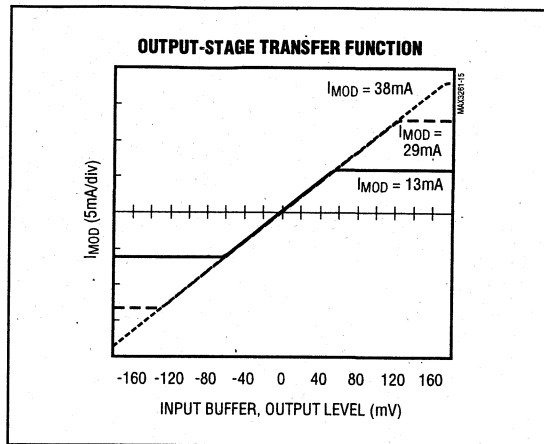


Figure 3. Output-Stage Transfer Function

Failure to ensure that the output stage switches completely results in a loss of modulation current (and extinction ratio). In addition, if the modulation port does not switch completely off, the modulation current will contribute to the bias current, and may complicate module assembly.

Automatic Power Control

The automatic power control (APC) feature allows an optical transmitter to maintain constant power, despite changes in laser efficiency with temperature or age. The APC requires the use of a monitor photodiode.

The APC circuit incorporates the laser diode, the monitor photodiode, the PIN set current mirror, a transconductance amplifier, the bias set current mirror, and the laser fail comparator (Figure 1). Light produced by the laser diode generates an average current in the monitor photodiode. This current flows into the MAX3261's IPIN input. The PIN set current mirror draws current away from the IPIN node. When the current into the IPIN node equals the current drawn away by IPINSET, the node voltage is set by the 3V reference of the transconductance amplifier. When the monitor current exceeds IPINSET, the IPIN node voltage will be forced higher. If the monitor current decreases, the IPIN node voltage is decreased. In either case, the voltage change is amplified by the transconductance amplifier, and results in a feedback current at the IBIASFB node. Under normal APC operation, IBIASFB is summed with IBIASSET, and the laser bias level is adjusted to maintain constant output power. This feedback process continues until the monitor-diode current equals IPINSET.

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

MAX3261

If the monitor-diode current is sufficiently less than IPINSET (i.e., the laser stops functioning), the voltage on the IPIN node will drop below 2.6V. This will trigger the failout comparator, which provides a TTL signal indicating laser failure. The FAILOUT output asserts only if the monitor-diode current is low, not in the reverse situation where the monitor current exceeds IPINSET.

The transconductance amplifier can output currents up to approximately 1mA. Since the laser bias generator has a gain of approximately 40, the APC function has a limit of approximately 40mA (up or down) from the initial set point. To take full advantage of this adjustment range, it may be prudent to program the laser bias current slightly higher than required for normal operation.

To maintain APC loop stability, a 1000pF bypass capacitor may be required across the photodiode. If the APC function is not used, disconnect the IBIASFB pad.

Enable Inputs

The MAX3261 provides complementary enable inputs (ENB+, ENB-) for interfacing with open-fiber-control architecture. Laser control is achieved by reducing the reference voltage outputs (VREF1, VREF2). Only one logic state will enable laser operation (Table 2).

Table 2. MAX3261 Truth Table

ENB-	ENB+	VREF
0	0	Off
0	1	Oh
1	0	Off
1	1	Off

The APC circuit requires a 1000pF capacitor between the IPIN input and ground for stability. With a 1000pF stability capacitor, the MAX3261 modulation and bias can be enabled and disabled within 5 μ s. This timing satisfies the requirements of the Open Fiber Control system used in Fibre Channel networks.

Temperature Considerations

The MAX3261 output currents are programmed by current mirrors. These mirrors each have a 2V_{BE} temperature coefficient. The reference voltage (VREF) is adjusted 2V_{BE} so these changes largely cancel, resulting in output currents that are very stable with respect to temperature (see *Typical Operating Characteristics*).

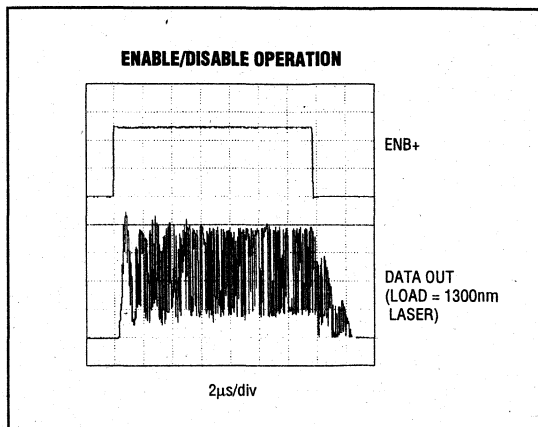


Figure 4. Enable/Disable Operation

Wire Bonding Die

For reliable operation, the MAX3261 has gold metallization. Make connections to the die with gold wire only, using ball bonding techniques. Wedge bonding is not recommended. Pad size is 4mils.

Design Procedure

Interfacing Suggestions

Use high-frequency design techniques for the board layout of the MAX3261 laser driver. High-speed interfaces often require fixed-impedance transmission lines (Figure 6). Adding some damping resistance in series with the laser raises the load impedance, making the

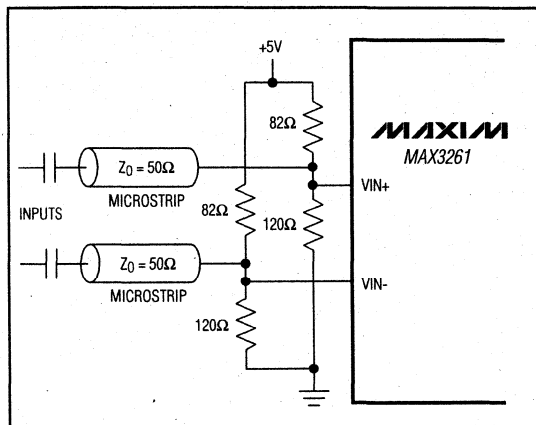


Figure 5. Typical Thevenin Equivalent Circuit, 50 Ω to 3V

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

transmission line more realizable, and it also helps reduce power consumption (see the section *Reducing Power Consumption*). Minimize any series inductance to the laser, and place a bypass capacitor as close to the laser's anode as possible.

Power connections labeled VCCA are used to supply the laser modulation and laser bias circuits. VCCB connections supply the bias-generator and automatic-power control circuits. For optimum operation, isolate these supplies from each other by independent bypass filtering.

VCCA, VCCB, and GND all have multiple connections provided. Even though only one connection is required for each of these supplies, proper use of the additional connections improves the MAX3261's high-frequency performance. Ground connections between signal lines (VIN+, VIN-, OUT+, OUT-) improve the quality of the signal path by reducing the impedance of the interconnect. Multiple connections, in general, reduce inductance in the signal path and improve the high-speed signal quality. GND pins should be tied to the ground plane with short runs and multiple vias. Avoid ground loops, since they are a source of high-frequency noise.

The MAX3261 inputs interface to PECL signal levels. If the incoming data stream has a 50% duty cycle (NRZ), the inputs can be AC coupled and connected to other differential logic levels. If logic levels other than PECL are used, it is important to bias the modulation inputs (VIN+, VIN-) with a circuit that provides a Thevenin equivalent of 50Ω to 3V (Figure 5).

Bias Network Compensation

When driving the laser diode with transmission lines, it is important to maintain a constant load impedance in order to minimize aberrations due to reflections. The inductive nature of laser packages will cause the laser impedance to increase with frequency, and the parasitic capacitance of the laser driver bias output (IBIASOUT) has some loading effects at high frequency. Of these two effects, the loading due to the laser lead inductance dominates. Impedance variation must be compensated for high-frequency operation. One possible approach is to use a shunt R-C network in parallel with the laser diode (Figure 6). Adding a two-stage R-L circuit in series with the bias output results in even better performance.

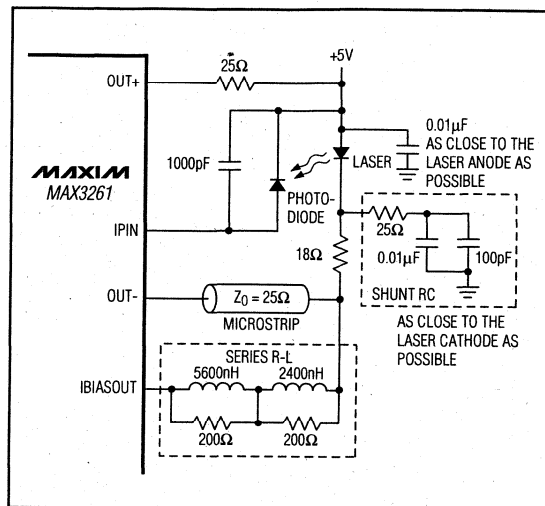


Figure 6. Typical Laser Interface with Bias Compensation

Reducing Power Consumption

The laser driver typically consumes 40mA of current for internal functions. Typical load currents, such as 12mA of modulation current and 20mA of bias current, bring the total current requirement to 72mA. If this were dissipated entirely in the laser driver, it would generate 360mW of heat. Fortunately, a substantial portion of this power is dissipated across the laser diode. A typical laser diode will drop approximately 1.6V when forward biased. This leaves 3.4V at the MAX3261's OUT- terminal. It is safe to reduce the output terminal voltage even further with a series damping resistor. Terminal voltage levels down to 2.2V can be used without degrading the laser driver's high-frequency performance. Power dissipation can be further reduced by adding a series resistor on the laser driver's OUT+ side. Select the series resistor so the OUT+ terminal voltage does not drop below 2.2V with the maximum modulation current.

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

MAX3261

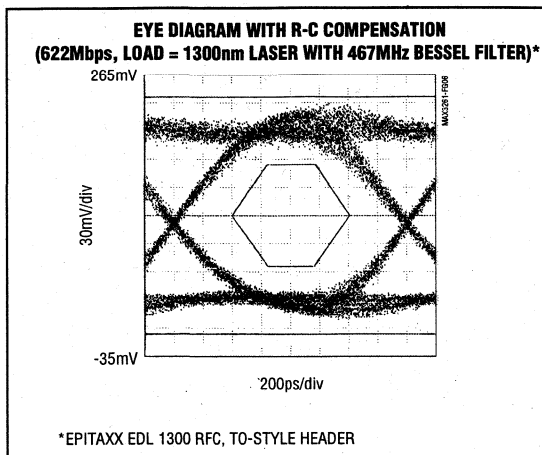


Figure 7. Eye Diagram with R-C Compensation ($R_L = 1300\text{nm}$ Laser)

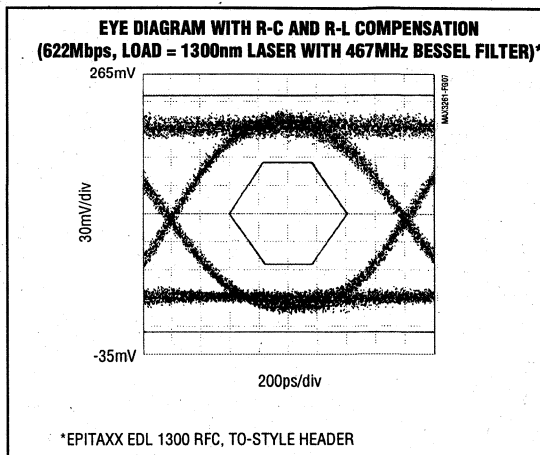


Figure 8. Eye Diagram with R-C and R-L Compensation ($R_L = 1300\text{nm}$ Laser)

Applications Information

Programming the MAX3261 Laser Driver

Programming the MAX3261 is best explained by an example. Assume the following laser diode characteristics:

Wavelength	λ	780nm
Threshold Current	I_{TH}	20mA at +25°C (+0.35mA/°C temperature variation)
Monitor Responsivity	ρ_{mon}	0.1A/W (monitor current / average optical power into the fiber)
Modulation Efficiency η		0.1mW/mA (worst case)

Now assume the communications system has the following requirements:

Average Power	P_{AVE}	0dBm (1mW)
Extinction Ratio	E_r	6dB ($E_r = 4$)
Temperature Range	T_r	0°C to +70°C

1) Determine the value of IPINSET:

The desired monitor-diode current is $(P_{AVE})(\rho_{mon}) = (1\text{mW})(0.1\text{A/W}) = 100\mu\text{A}$. The *Typical Operating Characteristics* show that R_{PINSET} should be 18k Ω .

2) Determine RMODSET:

The average power is defined as $(P_1 + P_0) / 2$, where P_1 is the average amplitude of a transmitted "one" and P_0 is the average amplitude of a transmitted "zero." The extinction ratio is P_1/P_0 . Combining these equa-

tions results in $P_1 = (2 \times P_{AVE} \times E_r) / (E_r + 1)$ and $P_0 = (2 \times P_{AVE}) / (E_r + 1)$. In this example, $P_1 = 1.6\text{mW}$ and $P_0 = 0.4\text{mW}$. The optical modulation is 1.2mW. The modulation current required to produce this output is $1.2\text{mW} / \eta = (1.2\text{mW}) / (0.1\text{mA/mW}) = 12\text{mA}$. The *Typical Operating Characteristics* show that $R_{MODSET} = 3\text{k}\Omega$ yields the desired modulation current.

3) Determine the value of ROSADJ:

Using Table 1, a 6.8k Ω resistor is chosen for 12mA of modulation current. The values given in Table 1 minimize aberrations in the waveform and ensure that the driver stage operates fully limited.

4) Determine the value of RBIASSET:

The automatic power control circuit can adjust the bias current 40mA from the initial setpoint. This feature makes the laser driver circuit reasonably insensitive to variations of laser threshold from lot to lot. The bias setting can be determined using one of two methods:

- Set the bias at the laser threshold.
- Set the bias at the midpoint of the highest and lowest expected threshold values.

Method A is straightforward. In the second method, it is assumed that the laser threshold will increase with age. The lowest threshold current occurs at 0°C, when the laser is new. The highest threshold current occurs at +70°C, at the end of the product's life. Assume the laser is near the end of life when its threshold reaches two-times its original value.

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

Lowest Bias Current:

$$I_{TH} + \Delta I_{TH} = 20\text{mA} + (0.35\text{mA}/^{\circ}\text{C})(-25^{\circ}\text{C}) = 11.25\text{mA}$$

Highest Bias Current:

$$2 \times I_{TH} + \Delta I_{TH} = 40\text{mA} + (0.35\text{mA}/^{\circ}\text{C})(+45^{\circ}\text{C}) = 55.8\text{mA}$$

In this case, set the initial bias value to 34mA (which is the midpoint of the two extremes). The 40mA adjustment range of the MAX3261 maintains the average laser power at either extreme.

The *Typical Operating Characteristics* show that $R_{BIASSET} = 1.8\text{k}\Omega$ delivers the required bias current.

End-of-Life Indicator

Some applications require a failout flag (end-of-life indicator) to be set when the laser bias current reaches two-times its original setting. A simple comparator circuit monitoring IBIASFB and IBIASSET can be implemented to provide this type of failout signal (Figure 9).

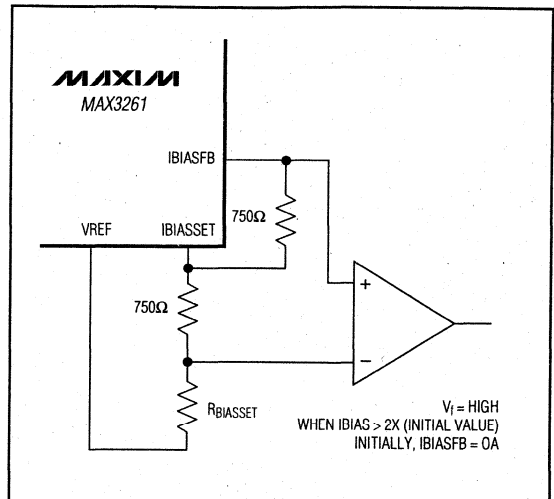
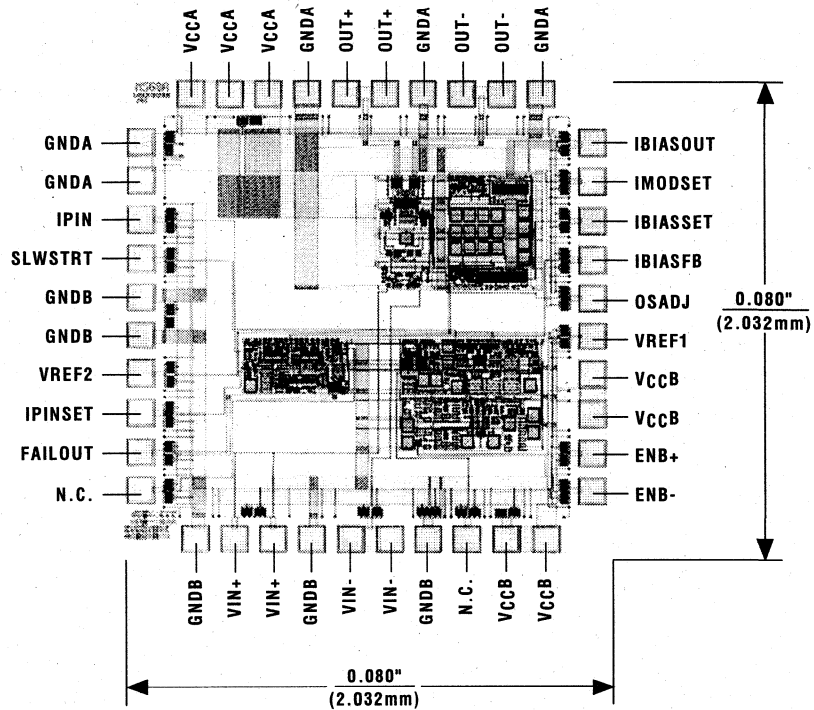


Figure 9. End-of-Life Indicator

Single +5V, Fully Integrated, 1.2Gbps Laser Diode Driver

Chip Topography

MAX3261



TRANSISTOR COUNT: 204
SUBSTRATE CONNECTED TO GNDA AND GNDB



1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

General Description

The MAX3262 limiting amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 1Gbps. The amplifier's gain can be adjusted between 33dB and 48dB. At maximum gain, signals as small as 6mVp-p can be amplified to drive devices with PECL inputs.

The MAX3262 has complementary loss-of-signal outputs for interfacing with open-fiber-control (OFC) circuitry. These outputs can be programmed to assert with input levels between 9mVp-p and 48mVp-p. LOS hysteresis for any programmed level is nominally 2.5dB, preserving a balance between noise immunity and dynamic range.

And, the MAX3262's offset correction function reduces pulse-width distortion.

Applications

531Mbps and 1062Mbps Fibre Channel

622Mbps SONET

High-Speed FM Limiting Amplifier

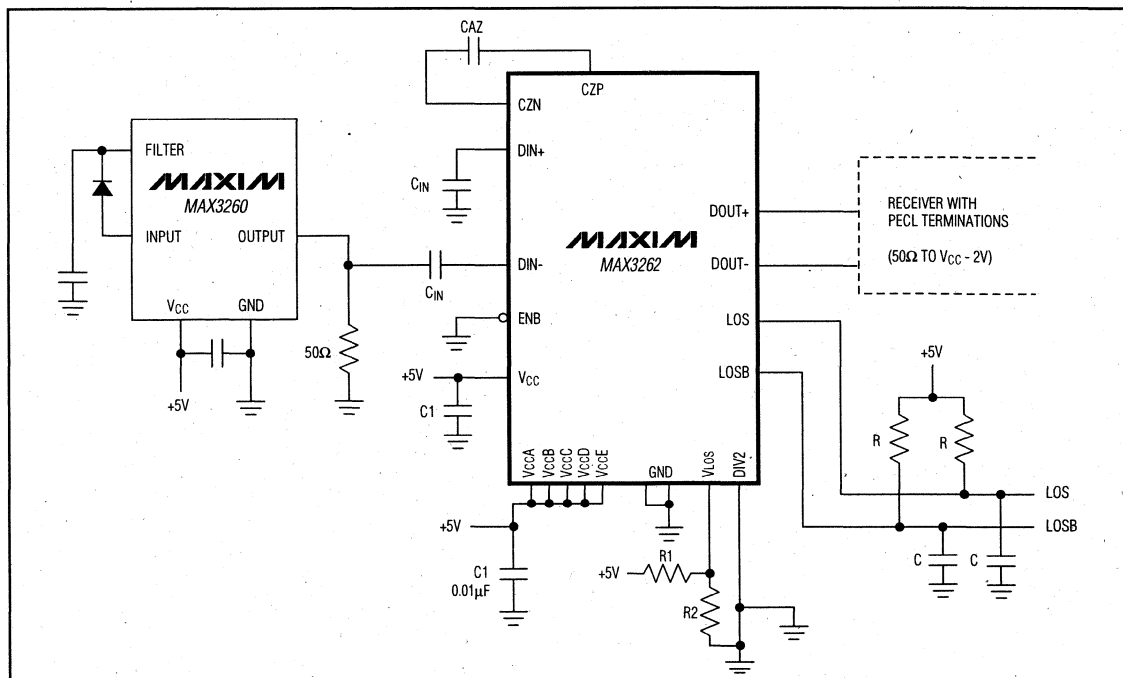
Features

- ◆ 900MHz Bandwidth
- ◆ Maximum Gain, 48dB
- ◆ Chatter-Free LOS
- ◆ Programmable LOS Threshold
- ◆ Single +5V Power Supply
- ◆ Fully Differential Architecture

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3262CAG	0°C to +70°C (T _A)	24 SSOP
MAX3262C/D	0°C to +100°C (T _J)	Dice

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

MAXIM**Maxim Integrated Products 11-19**

Call toll free 1-800-998-8800 for free samples or literature.

MAX3262

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1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply $V_{CC} - V_{EE}$	6.0V	Junction Operating Temperature	-55°C to +150°C
Input Voltage, $DIN+$, $DIN-$	6.0V	Storage Temperature Range	-55°C to +175°C
CZN, CZP, ENB, VLOS, DIV2, LOS+, LOS-	-0.3V, $V_{CC} + 0.3V$	Processing Temperature (Die)	+400°C
DOUT+, DOUT- (with 50 Ω load)	2.5V, $V_{CC} + 0.3V$		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V$, $R_{LOAD} = 50\Omega$ to 3V, $T_A = 0^\circ C$ to $+70^\circ C$, AC parameters are not tested, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS						
Power-Supply Current	I_{VCC}	No output load			60	mA
Enable Input Current	I_{ENB}				150	μA
VLOS Input Current	I_{LOS}			120		μA
Common-Mode Output Voltage			3.5	3.7	3.8	V
Open-Collector Outputs, LOS+, LOS-		$I_{OUT} = -1.0mA$			0.5	V
DIV2 Short-Circuit Current		DIV2 = 0V		0.5		mA
Differential Output Offset, DOUT+ to DOUT-					± 35	mV
Input Bias Voltage	V_{DIN}		2.5		3.0	V
AC SPECIFICATIONS (AC parameters are not tested.)						
Power-Supply Rejection Ratio	PSRR	Input referred, 55MHz		35		dB
LOS Release Time, Minimum Input	t_{OFFL}	(Note 1)	0.020		0.5	μs
LOS Release Time, Maximum Input	t_{OFFH}	(Note 2)			0.5	μs
LOS Assert Time	t_{ONL}	(Note 1)		0.2	0.5	μs
Input Voltage Range	V_{ID}	Peak-to-peak	0.006		1.8	V
LOS Sensitivity Range	V_{SR}	Differential inputs, peak-to-peak				mV
		MAX3262C/D	9		48	
		MAX3262CAG	10		48	
LOS Hysteresis	HYS		1.5	2.5	4.0	dB
Differential Input Noise	V_n	$V_{LOS} = 5V$, DIV2 = GND (Note 3)			80	μV
Pulse-Width Distortion	PWD	1Gbps, 8mVp-p input			40	ps
Output Edge Speed	t_R, t_F	$C_{LOAD} = 300fF$			250	ps
Differential Output Voltage Swing	V_{OD}		400	600	730	mV
Upper Small-Signal Bandwidth	BW_H	MAX3262C/D	800	925		MHz
		MAX3262CAG	750	810		

Note 1: Input is a 200MHz square wave, $t_R < 300ps$, 8mVp-p.

Note 2: Input is a 200MHz square wave, $t_R < 300ps$, 1.8Vp-p.

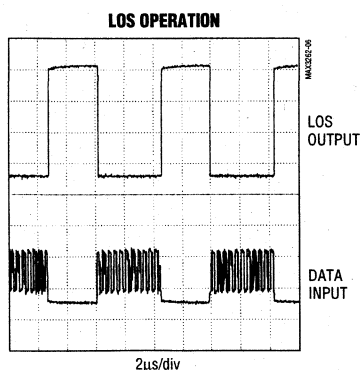
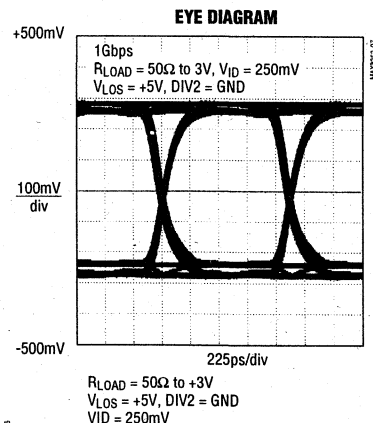
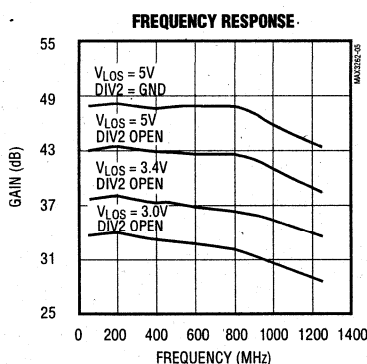
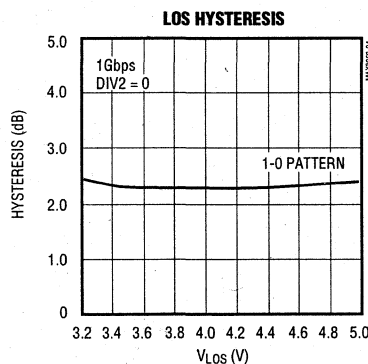
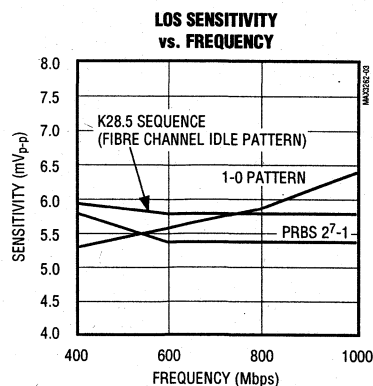
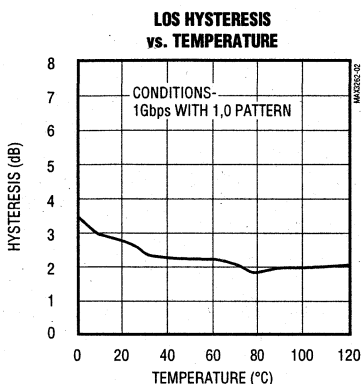
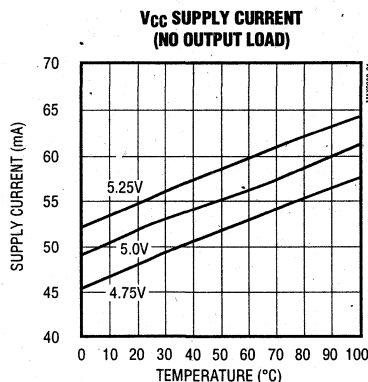
Note 3: Input referred noise = RMS output noise/low-frequency gain.

1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX3262



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1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

Pin Description

PIN	NAME	FUNCTION
1	V _{CCB}	Positive supply for internal gain stages
2	V _{LOS}	Power detect/LOS level set. Use this input to program the required threshold level for LOS assertion.
3	CZP	Offset-correction loop compensation capacitor. This pin should be connected to the CZN pin through a 100nF to 330nF capacitor, which provides the dominant pole for the offset-correction loop.
4	CZN	Offset-correction loop compensation capacitor. This pin should be connected to the CZP pin through a 100nF to 330nF capacitor, which provides the dominant pole for the offset-correction loop.
5	V _{CCA}	Power supply for the input stage amplifier
6	DIN+	Data Input
7	DIN-	Inverting Data Input
8	GND	Ground for the input stage amplifier
9	ENB	Output Enable. Internal gain stages are disabled and LOS is asserted when this input is brought to TTL high, and restored when this input is low.
10	DIV2	Input stage gain adjust. Grounding this pin forces the input stage gain to maximum (11dB) for applications where the LOS threshold level will be set for input signals in the 9mVp-p to 20mVp-p range. Leaving this pin open forces the gain of the input stage to be divided by two (6dB) for applications where the LOS threshold level will be set for input signal levels in the 15mVp-p to 48mVp-p range.
11	V _{TH}	Comparator threshold voltage for test only. Leave unconnected.
12	V _{CC} E	Positive supply for the power detect/LOS circuitry
13	GND	Ground for the power detect/LOS circuitry
14	GND	Ground for the LOS+/LOS- buffer circuitry
15	V _{CC} D	Positive supply for the LOS+/LOS- buffer circuitry
16	LOS-	Loss-of-Signal detect. This pin is asserted low when input power drops below the LOS threshold level.
17	LOS+	Loss-of-Signal detect. This pin is asserted high when input power drops below the LOS threshold level.
18	DOUT-	Inverting Data Output
19	DOUT+	Data Output
20	GND	Substrate Ground
21	V _{CC} C	Positive supply for bias generators
22	GND	Ground for bias generators
23	V _{CC}	Positive supply for output buffers
24	GND	Ground for internal gain stages

1 Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

MAX3262

Detailed Description

The MAX3262 is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical transimpedance amplifiers found within a fiber-optic link. The linear signal output from a transimpedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The MAX3262 limiting amplifier quantizes the signal, and outputs a voltage-limited waveform over a 48dB input dynamic range.

The MAX3262 provides an offset correction function that effectively reduces the offset voltage to negligible levels. In communications systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated by the transimpedance amplifier appears as input offset and is partially removed by the offset correction function. An external capacitor is required between CZP and CZN to compensate the offset correction loop, determining the lower 3dB point.

Loss-of-Signal Function

The MAX3262 incorporates a chatter-free loss-of-signal function, which is used to detect that the input signal has dropped below the level necessary for acceptable bit error rate performance, or to indicate an open-fiber condition. The loss-of-signal function is implemented with a rectifying peak detector, which samples the signal entering the output stage. The output from the peak detector is compared against an internally generated threshold, and is used to assert the LOS+ and LOS- outputs.

The loss-of-signal threshold is adjusted by varying the amplifier gain. The MAX3262 is configurable for gains between 33dB and 48dB, allowing LOS thresholds between 9mVp-p and 48mVp-p. Figure 2 shows the LOS threshold as a function of the DIV2 and VLOS pins. The DIV2 pin provides a coarse adjustment of 6dB of gain, while the VLOS pin provides a fine gain adjustment between 0dB and 11dB.

Level-detect hysteresis and a 200ns internal delay ensure chatter-free LOS outputs when the input signal level is close to the LOS threshold. The hysteresis for any programmed loss-of-signal level is nominally 2.5dB.

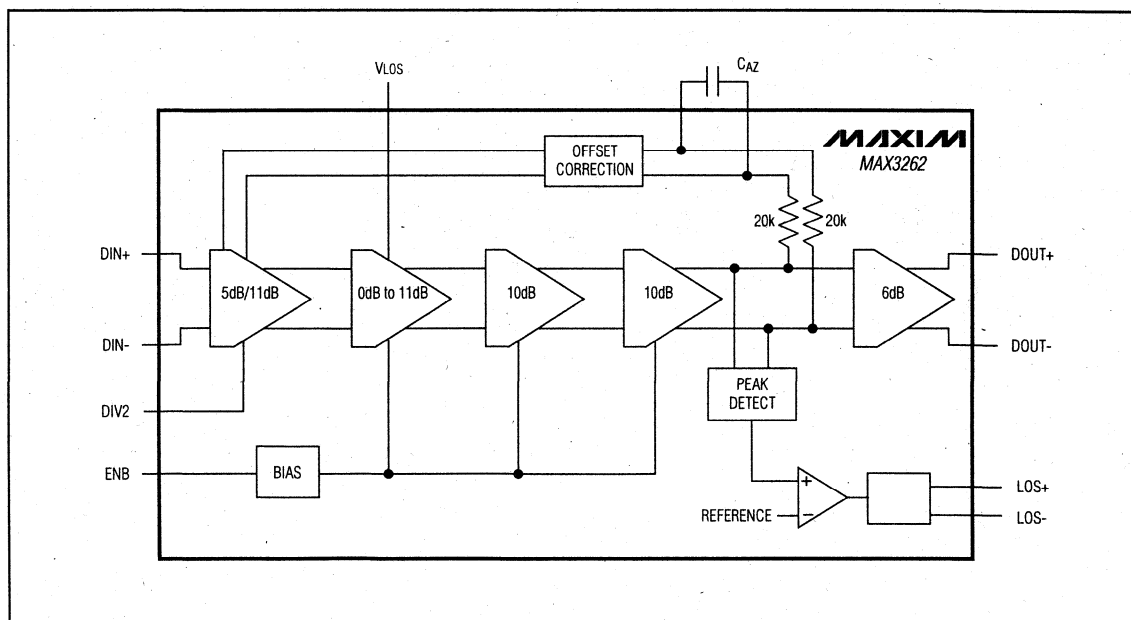


Figure 1. Functional Diagram

1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

The LOS+ and LOS- outputs are open-collector, Schottky-clamped transistors, that require pull-up resistors for proper operation (Figure 3). The loss-of-signal time constant is set externally with the appropriate pull-up resistor and shunt load capacitance.

The ENB pin allows the user to disable the output signal without removing the input signal.

Wire Bonding Die

For reliable operation, the MAX3262 has gold metallization. Connections to the die should be made with gold wire only, using ball bonding techniques. Wedge bonding is not recommended. Bond pad size is 4 mils.

Design Procedure

Determining Capacitor Values

The MAX3262 inputs must be AC coupled to allow proper operation of the offset correction function. Figure 4 shows the circuit's input stage. The circuit's lower -3dB point is determined by the input coupling capacitors. The lower -3dB frequency is $1 / [(2\pi)(1500\Omega)(C_{IN})]$ Hz.

C_{IN} should be large enough to not affect the signal quality, but small enough to not affect the LOS assert time. When an open-fiber condition occurs, the input coupling capacitors must discharge below the LOS threshold level before the LOS can assert. The worst-case discharge time would occur with the maximum

input signal and the minimum LOS threshold. In this case, the input capacitor must discharge from 0.9V to 4.5mV. The time required for this to occur is:

$$t = (1500)(C_{IN}) \ln(V_{max} / V_{THRESH}) \text{ seconds}$$

Example: If the MAX3262 is configured for 6mV sensitivity, $C_{IN} = 100\text{pF}$ results in a lower -3dB frequency of 1MHz, and a maximum LOS delay of about 1μs.

The offset correction capacitor (CAZ) must be greater than 100nF to ensure stable operation. This capacitor is in series with an internal 40kΩ of resistance. The -3dB point of the offset zeroing circuit is:

$$1 / [(2\pi)(CAZ)(40k\Omega)] \text{ Hz}$$

For CAZ = 180nF, the bandwidth of the offset correction circuit is 22Hz. Maxim's proprietary offset-correction architecture decouples the input coupling time constant from the offset correction time constant. This ensures there is no interaction between these two networks, eliminating an additional source of chatter on LOS.

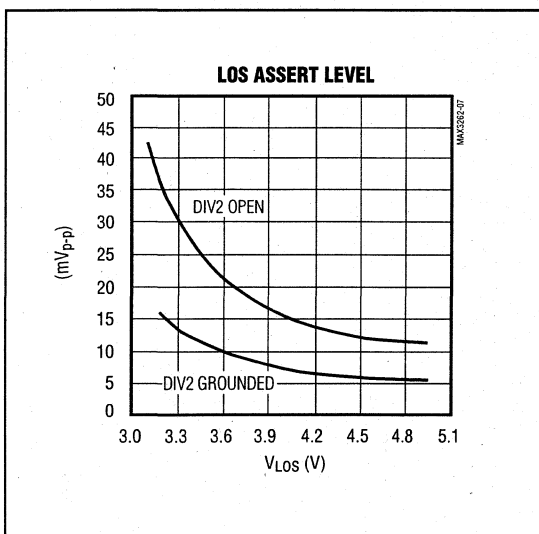


Figure 2. MAX3262 Sensitivity vs. V_{LOS} Setting

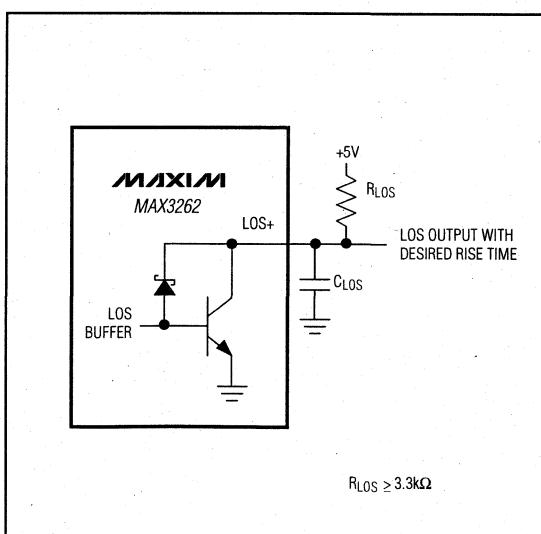


Figure 3. Setting the LOS Time Constant

1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

Output Termination

The MAX3262 outputs must be terminated with a 50Ω load to ($V_{CC} - 2V$), or a Thevenin equivalent. Figure 5 shows two possible output termination methods.

Layout and PCB Design

Since the MAX3262 is a high-frequency component, the circuit's performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via the power supply. Some fiber-optic limiting amplifiers suffer from LOS "chatter." The act of switching the LOS outputs on or off generates noise on the power supply, which can cause the LOS outputs to chatter. With proper board layout, the MAX3262 ensures chatter-free LOS operation.

The MAX3262 has five ground pins and a substrate connection. All of these should be connected to the circuit board's ground. Use multiple PCB vias close to the part to connect the grounds. Avoid long, inductive runs, which can degrade MAX3262 performance. The MAX3262's six V_{CC} supply pins must all be connected. $V_{CCA}-V_{CCE}$ can be collectively decoupled with one capacitor. V_{CC} (pin 23) should be decoupled separately (see the *Typical Operating Circuit*).

Applications Information

The loss-of-signal indicator, can be used as a DC loss-of-light indicator. If the input stimulus drops to a DC level, such as during a loss of light condition, the input capacitors discharge to a balanced steady-state, where the differential input voltage is 0V. The power detector

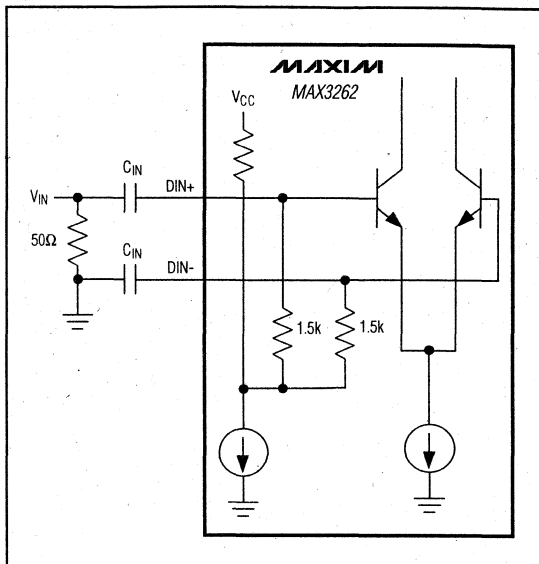


Figure 4. MAX3262 Equivalent Input Circuit

will detect no signal, and LOS will be asserted. The complementary LOS outputs meet the requirements for designs using the open-fiber-control safety feature.

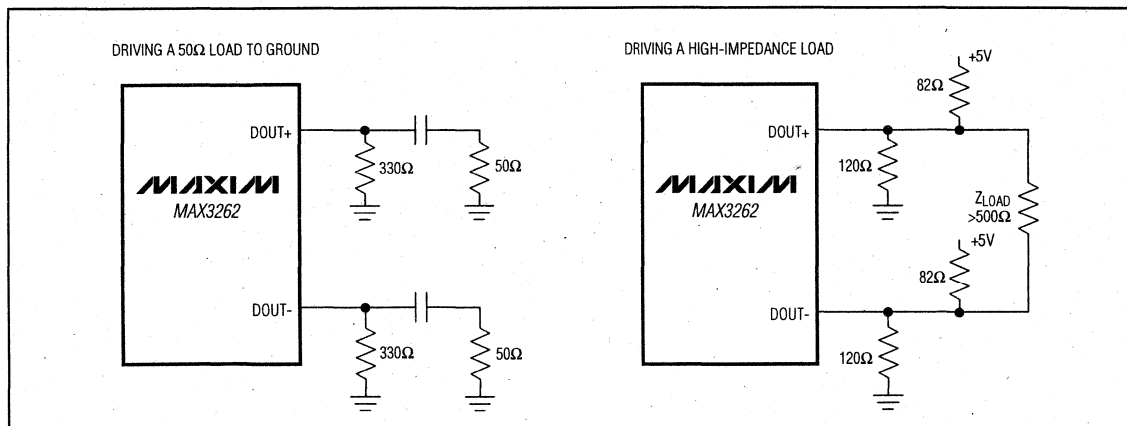
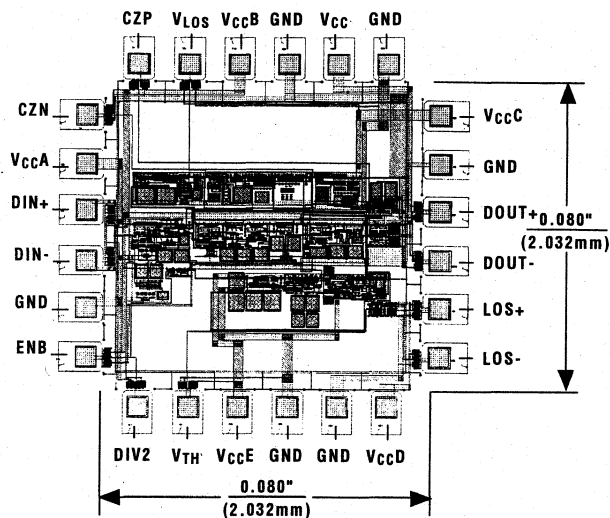
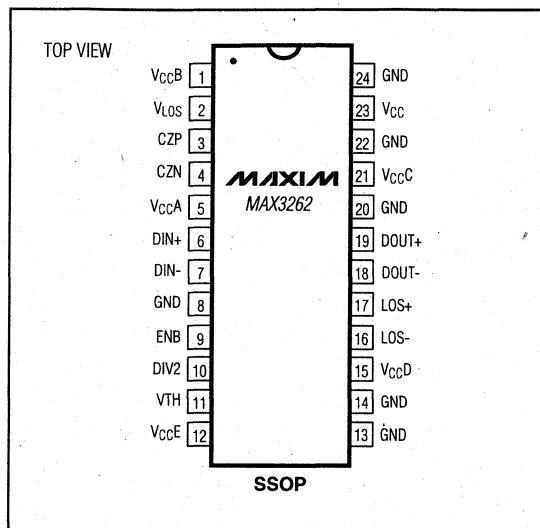


Figure 5. Output Termination Techniques

1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection

Pin Configuration

Chip Topography



TRANSISTOR COUNT: 200

SUBSTRATE CONNECTED TO GND PIN 17

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.
8/95

MAXIM

Single +5V, Fully Integrated, 155Mbps Laser Diode Driver

MAX3263

General Description

The MAX3263 is a complete, easy-to-program, single +5V-powered, 155Mbps laser diode driver with complementary enable inputs and Automatic Power Control (APC). The MAX3263 accepts differential PECL inputs and provides complementary output currents. A temperature-stabilized reference voltage is provided to simplify laser current programming. This allows modulation current to be programmed from 5mA to 25mA and bias current to be programmed from 5mA to 60mA with two external resistors.

An APC circuit is provided to maintain constant laser power in transmitters that use a monitor photodiode. Only one external resistor is required to implement the APC function.

The MAX3263's fully integrated feature set includes a TTL-compatible laser failure indicator and a programmable slow-start circuit to prevent laser damage. The slow-start is preset to 50ns and can be extended by adding an external capacitor.

Applications

Laser Diode Transmitters
155Mbps SDH/SONET

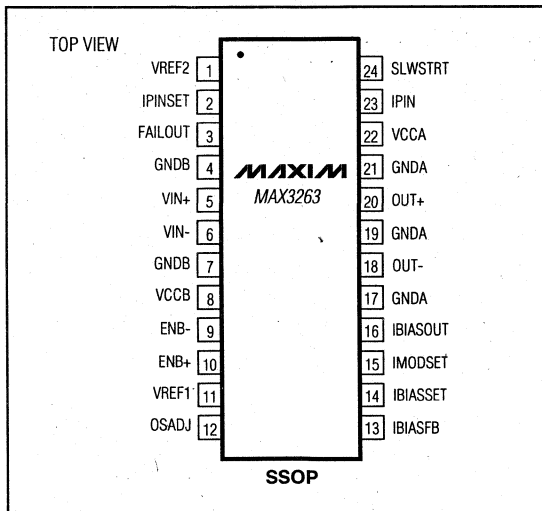
Features

- ♦ Rise Times Less than 1ns
- ♦ Differential PECL Inputs
- ♦ Single +5V Supply
- ♦ Automatic Power Control
- ♦ Temperature-Compensated Reference Voltage
- ♦ Complementary Enable Inputs

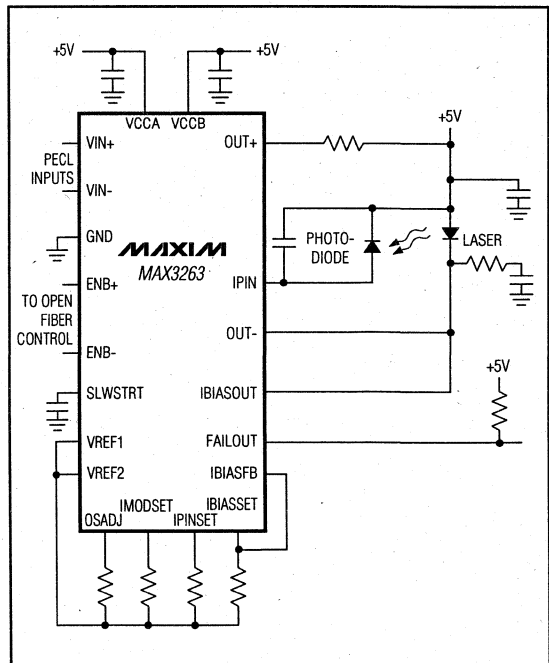
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3263CAG	0°C to +70°C (TA)	24 SSOP

Pin Configuration



Typical Operating Circuit



11

MAXIM

Maxim Integrated Products 11-27

Call toll free 1-800-998-8800 for free samples or literature.



155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

General Description

The MAX3270 is a complete Clock Recovery and Data Retiming IC for 155Mbps and 622Mbps SDH/SONET and ATM applications. The MAX3270 meets Bellcore and CCITT jitter tolerance specifications ensuring error-free data recovery. Recovered clock and data are phase aligned using a fully integrated phase-locked loop (PLL). An output frequency monitor (FM) is included to detect loss of PLL acquisition or a loss of input data.

The MAX3270 has differential ECL input and output interfaces, so it is less susceptible to noise in a high-frequency environment. The fully integrated PLL includes an integrated phase-frequency detector that eliminates the need for external references.

Applications

155Mbps (STM-1/OC-3)/622Mbps (STM-4/OC-12) SDH/SONET Transmission Systems
155Mbps/622Mbps ATM/SONET Access Nodes
Add/Drop Multiplexers
Cross-Connects

Features

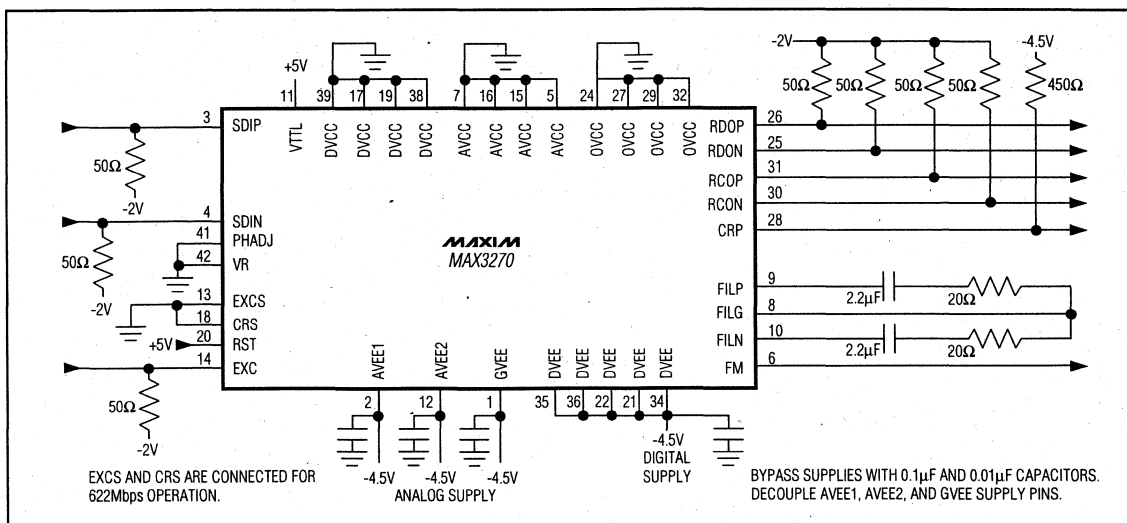
- ◆ Supports Both 155Mbps and 622Mbps Clock Recovery and Data Retiming
- ◆ Fully Integrated Phase/Frequency Detector
- ◆ Capable of Switching to an External Clock
- ◆ Differential 100K ECL Data and Clock I/Os
- ◆ Output Monitor Provides Lock Detection
- ◆ No External Reference Clock Required

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3270EMH	-40°C to +85°C	44 MQFP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



11

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltages		PHADJ, VR	-8.0V to +8.0V
VTTL to GND	-0.5V to +8.0V	FM	-8.0V to +8.0V
VCC to GND	-0.5V to +8.0V	Input Differential Voltage Level, SDIP, SDIN	+3.0V
VEE to GND	-8.0V to +0.5V	Continuous Power Dissipation (T _A = +85°C)	1.3W
SDIP, SDIN, EXC	-8.0V to +0.5V	Operating Temperature Range	-40°C to +85°C
RDOP, RDON, RCOP, RCON, CRP	-8.0V to +0.5V	Storage Temperature Range	-55°C to +150°C
EXCS, RST, CRS	-0.5V to +8.0V	Lead Temperature (soldering, 10sec)	+300°C
FILP, FILG, FILN	-8.0V to +0.5V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V ±5%, VTTL = 5V ±5%, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Voltage Supply (with respect to ground)	V _{TTL}		4.75	5.00	5.25	V
Negative Voltage Supply (with respect to ground)	V _{EE}		-4.725	-4.50	-4.275	V
Static Supply Current from VTTL	I _{TTL}			2.4	5	mA
Static Supply Current from VEE	I _{VEE}			150	210	mA
ECL INPUTS: EXC, SDIP, SDIN						
Input High Voltage	V _{IH}		-1165		-870	mV
Input Low Voltage	V _{IL}		-1830		-1475	mV
Input High Current	I _{IH}	V _{IN} = V _{OH} (typ)	0		100	μA
Input Low Current	I _{IL}	V _{IN} = V _{OL} (typ)	-100		100	nA
ECL OUTPUTS: RCOP, RCON, RDOP, RDON						
Output High Voltage	V _{OH}	Loaded with 50Ω to -2V	-1025	-955	-870	mV
Output Low Voltage	V _{OL}	Loaded with 50Ω to -2V	-1830	-1705	-1550	mV
LOW-POWER ECL OUTPUT: CRP						
Output High Voltage	V _{OH}	Loaded with 470Ω to V _{EE}	-1025	-955	-870	mV
Output Low Voltage	V _{OL}	Loaded with 470Ω to V _{EE}	-1830	-1705	-1620	mV
TTL INPUTS: CRS, RST, EXCS						
Input High Voltage	V _{IH}		2			V
Input Low Voltage	V _{IL}				0.8	V
Input High Current	I _{IH}	VTTL = 5.00V, V _{IN} = 2V	0		40	μA
Input Low Current	I _{IL}	VTTL = 5.00V, V _{IN} = 0.8V	0		40	μA
PHASE ADJUST INPUTS: PHADJ, VR						
Input Bias Current	I _{BIAS}	VR = PHADJ = 0, T _A = +25°C	0		10	μA

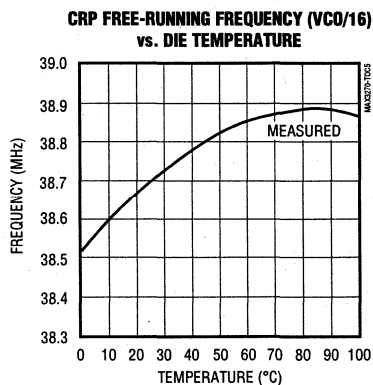
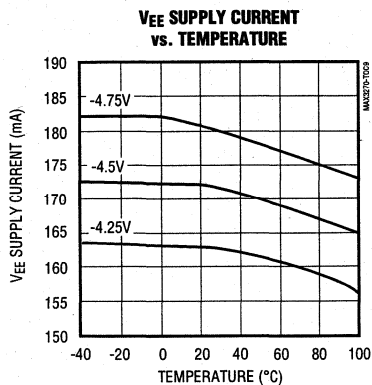
155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

AC ELECTRICAL CHARACTERISTICS (continued)

($V_{EE} = -4.5V$, $V_{TTL} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.)

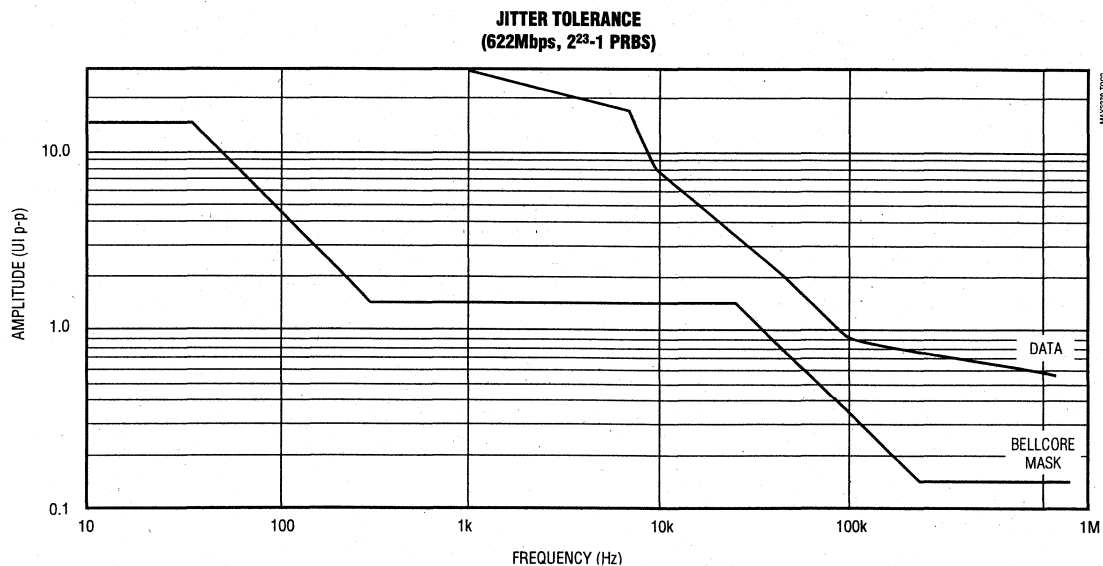
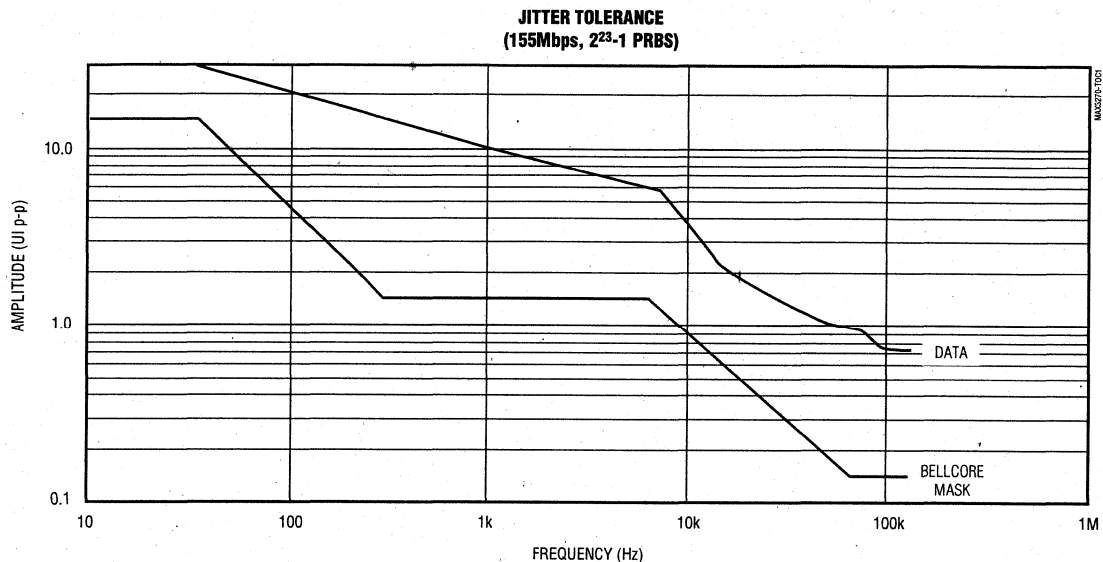
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ECL OUTPUTS: RDOP, RDON, RCOP, RCON						
Transition Time 20% to 80%	t_r, t_f	Loaded with 50Ω to -2V and 5pF to GND		600		ps
Time Difference between RDO and RCO	TD	Loaded with 50Ω to -2V and 5pF to GND		100		ps
PFD AND FILTER AMPLIFIER TEST LEVELS						
Output Offset Voltage of the Monitor Amplifier	V_O	PHADJ = 0, FILP and FILN shorted	-35		35	mV
Gain of the Monitor Amplifier	GFM	PHADJ = 0	0.95		1.05	V/V
Filter Amplifier Open-Loop Voltage Gain	GOL	FILP and FILN open	21	26		dB
VCO TEST PARAMETERS; CPR OUTPUT						
Center Frequency	F_O	FILP and FILN shorted, PFD = neutral state	38.00		39.50	MHz
Frequency Range	DF_O	FILP - FILN = 1.6V	6		10	MHz
Mean Frequency Sensitivity	K_O	FILP - FILN = 1.6V	3.75		6	MHz/V
Frequency Sensitivity to Power-Supply Voltage	K_{OV}	FILP and FILN shorted			550	kHz/V
PLL ELECTRICAL SPECIFICATIONS						
Frequency of VCO	F_O			622.08		MHz
Incremental Tuning Sensitivity (Incremental Slope, $\Delta f/\Delta V_t$)	K_O	$f_t = 622.08\text{MHz}$		75		MHz/V
Phase-Detector Gain	KD			192		mV/rad
Transconductance Gain of Filter Amplifier	Gm			1.25		mA/V
Phase Offset Sensitivity, $\Delta\Phi/\Delta\text{PHADJ}$	KPHADJ			2		rad/V

Typical Operating Characteristics



155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Typical Operating Characteristics

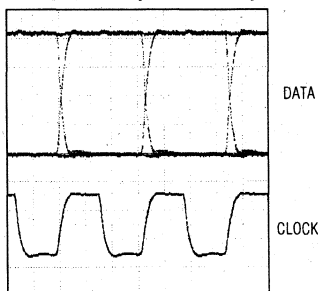


155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Typical Operating Characteristics

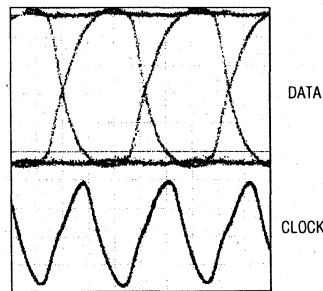
MAX3270

155Mbps RECOVERED CLOCK AND RETIMED DATA (SINGLE ENDED)



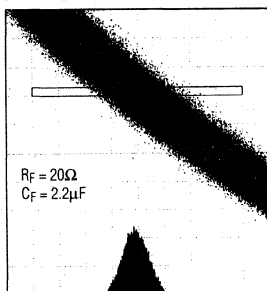
2ns/div

622Mbps RECOVERED CLOCK AND RETIMED DATA (SINGLE ENDED)



500ps/div

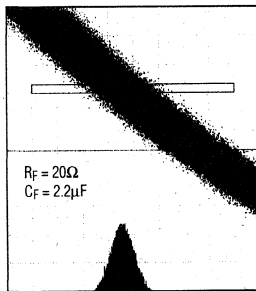
RECOVERED CLOCK JITTER
(155Mbps, 2⁷-1 PRBS, 5.1ps RMS)



10ps/div

Mean	40.61ns	$\mu \pm 1\sigma$	68.961%
RMSΔ	5.13ps	$\mu \pm 2\sigma$	95.844%
PkPk	45.6ps	$\mu \pm 3\sigma$	99.717%

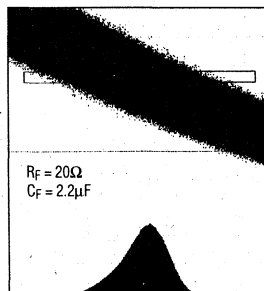
RECOVERED CLOCK JITTER
(155Mbps, 1-0 PATTERN, 4.7ps RMS)



10ps/div

Mean	40.65ns	$\mu \pm 1\sigma$	69.674%
RMSΔ	4.7ps	$\mu \pm 2\sigma$	95.558%
PkPk	38.4ps	$\mu \pm 3\sigma$	99.698%

RECOVERED CLOCK JITTER
(622Mbps 2⁷-1 PRBS 9.0ps RMS)



10ps/div

Mean	38.68ns	$\mu \pm 1\sigma$	69.747%
RMSΔ	9.049ps	$\mu \pm 2\sigma$	95.453%
PkPk	79.4ps	$\mu \pm 3\sigma$	99.582%

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155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Pin Description

PIN	NAME	FUNCTION
1	GVEE	Guard-Ring Negative Supply to Substrate: -4.5V
2	AVEE1	Negative Supply for Input Buffers: -4.5V
3	SDIP	Serial Data Input: 155Mbps or 622Mbps. Differential ECL Positive.
4	SDIN	Serial Data Input: 155Mbps or 622Mbps. Differential ECL Negative.
5	AVCC	Ground for Input Buffers: 0V
6	FM	Frequency Monitor Output. This pin monitors the input voltage to the VCO. When the PLL is locked, the pin will be $\approx 0V$.
7	AVCC	Guard-Ring Positive Supply to Epi: 0V
8	FILG	Loop Filter Ground. This pin connects to an external filter.
9	FILP	Loop Filter Positive. This pin connects to an external filter.
10	FILN	Loop Filter Negative. This pin connects to an external filter.
11	VTTL	TTL Positive Supply: +5.0V
12	AVEE2	Negative Supply for VCO: -4.5V
13	EXCS	External Clock-Select TTL Input. A logical high selects the external clock.
14	EXC	External Clock. Single-ended ECL input.
15, 16	AVCC	Ground for VCO: 0V
17, 19, 38, 39	DVCC	Digital Ground for Mux: 0V
18	CRS	Clock-Rate Select TTL Input. This selects the clock rate to be either 155Mbps or 622Mbps. A logic-high level selects the 622Mbps mode.
20	RST	Resets all digital flip-flops, TTL input. Reset is assert when low.
21, 22, 34, 35, 36	DVEE	Digital Negative Supply: -4.5V
23, 33, 37, 40, 43, 44	N.C.	No Connection
24, 27, 29, 32	OVCC	Output Driver Ground: 0V
25	RDON	Negative Recovered Data Output, differential ECL output: 155Mbps or 622Mbps.
26	RDOP	Positive Recovered Data Output, differential ECL output: 155Mbps or 622Mbps.
28	CRP	Clock-Reference Output Divide-by-4. ECL low-power single-ended: 38Mbps or 155Mbps.
30	RCON	Negative Recovered Clock Output, differential ECL output: 155Mbps or 622Mbps.
31	RCOP	Positive Recovered Clock Output, differential ECL output: 155Mbps or 622Mbps.
41	PHADJ	Phase Adjust. This is an analog adjustment that varies the static phase between the input data and the recovered clock. If not used, this input should be grounded. The range is from -1V to 1V.
42	VR	Phase Reference Voltage: 0V. The PHADJ pin compares to this voltage. Set to ground.

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

MAX3270

Detailed Description

The block diagram of Figure 1 shows the MAX3270's architecture. The phase-locked loop (PLL) consists of a phase/frequency detector (PFD), a loop filter amplifier, and a voltage-controlled oscillator (VCO).

Phase Detector

The phase detector produces a voltage proportional to the phase difference of the incoming data and the output of the recovered clock. Because of its feedback nature, the PLL will drive the error voltage to zero, making the phase difference zero and aligning the recovered clock to the incoming data. An external phase-adjustment pin (PHADJ) allows the user to vary phase alignment.

Frequency Detector

A frequency detector is also incorporated into the PLL. Frequency detection aids in the acquisition of the input data; this frequency-aided acquisition is necessary during start-up conditions, since the input data stream and VCO difference frequency may be outside the PLL

bandwidth. The input data stream is sampled by quadrature components of the VCO clock, generating a difference frequency. Depending on the rotation of the difference frequency, the PFD will drive the VCO so that the difference frequency is driven to zero. Once frequency acquisition is obtained, the frequency detector will return to a neutral state.

Loop Filter and VCO

The PLL is a second-order transfer function whose bandwidth is set by the loop filter. The VCO is integrated into the PLL and always operates at 622MHz. The center frequency is tightly controlled by laser trimming, limiting frequency drift when lock is lost. 155Mbps or 622Mbps mode is selected by the clock-rate select (CRS) pin. CRS selects the inputs to multiplexer MUX2.

The internal VCO can be bypassed with an external clock applied to the EXC input. The external clock select (EXCS) controls the input selections to multiplexers MUX1 and MUX2.

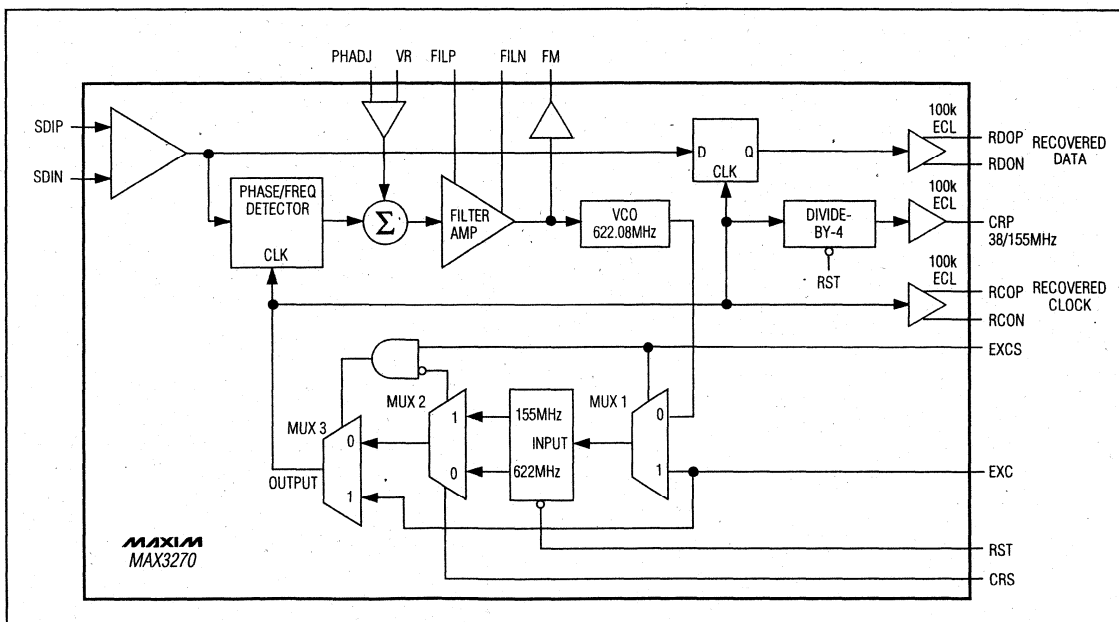


Figure 1. Block Diagram

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155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Design Procedure

Selecting the Data Rate

The MAX3270 is intended for use in SDH/SONET systems operating at 155.52Mbps or 622.08Mbps data rates. TTL inputs (CRS and EXCS) are provided for selecting the recovered clock rate (Table 1). It is also possible to switch to an externally supplied clock by enabling the EXC input. The EXC input is a high-speed single-ended ECL interface capable of handling serial clock rates of 155MHz and 622MHz.

Table 1. MAX3270 Logic Table

EXCS	CRS	RCOP/RCON	CRP
0	1	155.52Mbps	38.88Mbps
0	0	622.08Mbps	155.52Mbps
1	0	EXC	EXC/4
1	1	EXC/4	EXC/16

Setting the Loop Filter

The loop filter within the PLL consist of a transconductance amplifier and the external filter elements R_f and C_f (Figure 2). The closed-loop bandwidth of a PLL can be approximated by:

KD Ko Gm Rf

where K_D is the gain of the phase detector, K_O is the gain of the VCO, and G_m is the transconductance of the filter amplifier. Because this filter is an integrator, a zero in the open-loop gain is required for stability. This zero is set by the following equation:

$$W_7 = 1 / (R_f C_f)$$

where the recommended external values are $R_f = 20\Omega$ and $C_f = 2.2\mu F$. To decrease the PLL's closed-loop bandwidth, reduce the value of R_f . Decreasing this bandwidth will improve the MAX3270's jitter transfer performance but reduce jitter tolerance. The MAX3270 has been designed (using the recommended values of R_f and C_f) to meet the Bellcore and CCITT specifications for jitter tolerance of a Network Element. Carefully consider the application if a reduction in loop bandwidth is desired. By reducing R_f an order of magnitude, the PLL's bandwidth becomes more sensitive to the internal tolerances of the IC. As a result, the loop bandwidth may have a wider variation. If R_f is reduced, then C_f should also be increased to maintain loop stability and minimize jitter peaking.

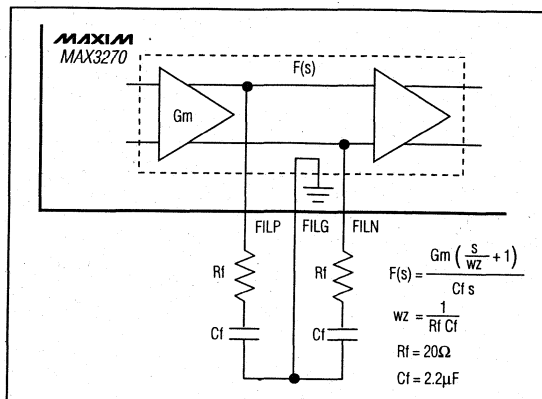


Figure 2. Loop Filter

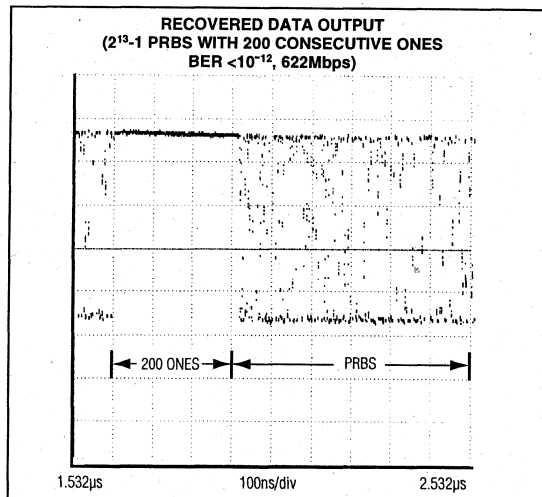


Figure 3. Recovered Data Output

The MAX3270 is optimally designed to acquire lock and to provide a bit-error rate (BER) of less than 10^{-12} for long strings of consecutive zeros or ones. Using the recommended external values for $R_f = 20\Omega$ and $C_f = 2.2\mu F$, measured results show that the MAX3270 can tolerate more than 200 consecutive ones or zeros. Figure 3 shows a bit stream of $2^{13} - 1$ PRBS with 200 consecutive ones.

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

MAX3270

Input and Output Termination

The MAX3270 data and clock I/Os (SDIP, SDIN, RDOP, RDON, RCOP, RCON, and EXC) are open emitters, designed to interface with ECL signal levels. It is important to bias these ports appropriately. A circuit that provides a Thevenin equivalent of 50Ω to $-2V$ should be used with fixed-impedance transmission lines for proper termination. Figure 4 shows some typical input and output termination methods.

The serial data input signals (SDIP and SDIN) are the differential inputs to an emitter coupled pair. As a result, the MAX3270 can accept differential input signal levels as low as $250mV$. The serial input (SDIP) can also be driven single-ended by externally biasing SDIN to the center of the voltage swing (approximately $-1.3V$). Make sure that the differential inputs and outputs each see the same termination impedance for balanced operation.

CRP is also an open-emitter ECL output, but it requires a termination resistor of 450Ω to $-4.5V$. If this output is not used, reduce power by connecting CRP to VEE through a resistor valued at $10k\Omega$ or more.

The MAX3270's performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductances and using fixed-impedance transmission lines on the data and clock signals. Power-

supply decoupling should be placed as close to the VEE and VTTL pins as possible. AVEE1, AVEE2 and GVEE should each have their own bypass/decoupling elements, independent of each other and any other $-4.5V$ supply. Make sure to isolate the inputs from the outputs to reduce feedthrough.

Applications Information

Lock Detection

The MAX3270 has an output (FM) that monitors the input voltage to the VCO. FM is an analog output that can be used as a flag to indicate that the PLL is locked. Under normal operation, the loop is locked and the FM output is approximately equal to $0V$. When the PLL is unlocked, the VCO will drift. The FM output monitors this drift and will equal approximately $\pm 1V$ in the limit.

Phase Adjust

In some applications, the optimum alignment point between the recovered clock and the serial data is not at the center of the eye diagram. The MAX3270 has a PHADJ input that can be used in these applications to introduce a phase difference between the recovered clock and the serial data. When no phase difference is desired, this input should be set to $0V$. The VR pin is the reference input for PHADJ and is normally tied to GND.

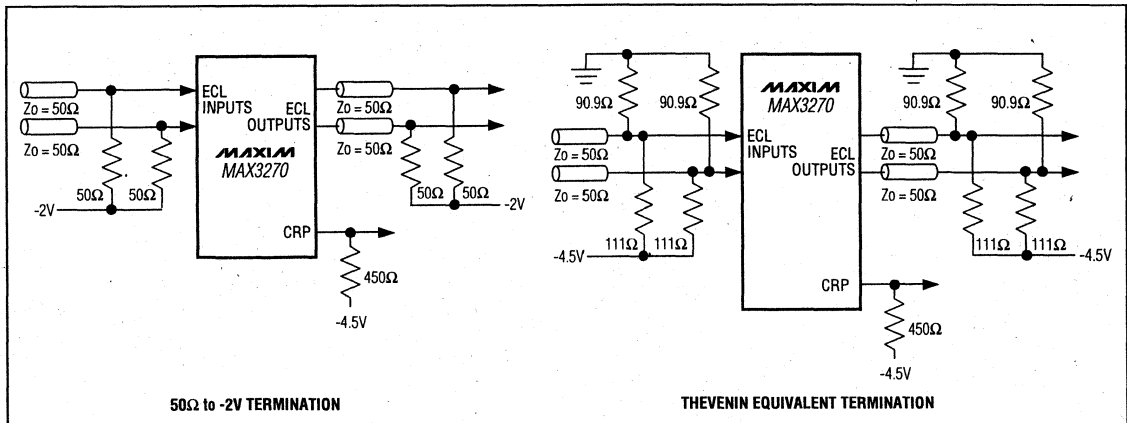
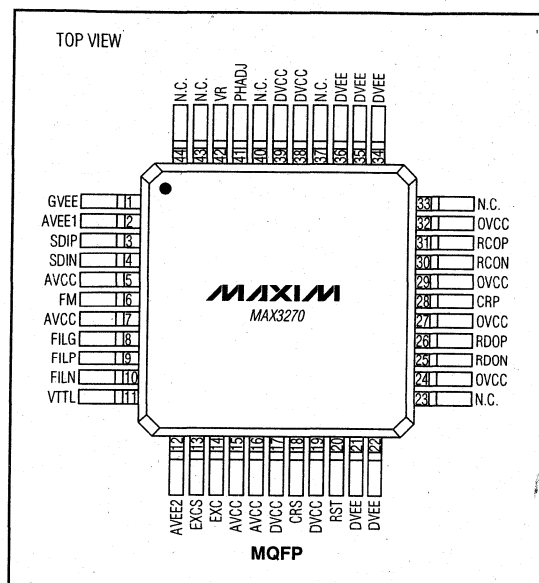


Figure 4. Typical Input and Output Terminations

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155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Pin Configuration





Appendix

Evaluation Kit Table	A-2
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Maxim's Military Program.....	A-11
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Package Information.....	A-13

Evaluation Kits

Part Number	EV Kit	Order Free Sample*	EV Kit Price† (\$)	Part Number	EV Kit	Order Free Sample*	EV Kit Price† (\$)
INTERFACE PRODUCTS							
MAX212	MAX212EVKIT-SO		38.00	MAX189	MAX187EVKIT-DIP	MAX189BCPA	55.00
A/D CONVERTERS							
MAX100	MAX100EVKIT		†††	MAX190	MAX187EVC16-DIP**	MAX189BCPA	150.00
MAX101	MAX101EVKIT		†††	MAX191	MAX190EVKIT-DIP**		95.00
MAX104	MAX104EVKIT		††	MAX194	MAX191EVKIT-DIP		55.00
MAX110	MAX110EVKIT-DIP		55.00	MAX195	MAX191EVSYS-DIP**		150.00
	MAX110EVC32-DIP**		150.00	MAX197	MAX194EVC16-DIP**		55.00
MAX111	MAX110EVKIT-DIP	MAX111CPE	55.00		MAX195EVC16-DIP**		150.00
MAX120	MAX110EVC32-DIP**	MAX111CPE	150.00	MAX199	MAX197EVKIT-DIP		55.00
MAX121	MAX120EVKIT-DIP		82.00		MAX197EVC16-DIP**		150.00
MAX122	MAX121EVKIT-DIP		85.00		MAX197EVC32-DIP**		150.00
MAX132	MAX120EVKIT-DIP	MAX122BCNG	82.00		MAX197EVC32-DIP**		150.00
MAX133	MAX132EVKIT-DIP**		95.00		MAX197EVC32-DIP**		150.00
MAX134	MAX134EVBKD-DIP	MAX133CPL	125.00		MAX197EVC32-DIP**		150.00
MAX152	MAX152EVKIT-DIP		65.00		MAX197EVC32-DIP**		150.00
MAX153	MAX152EVKIT-DIP	MAX153CPP	65.00		MAX197EVC32-DIP**		150.00
MAX155	MAX155EVKIT-DIP**		95.00		MAX197EVC32-DIP**		150.00
MAX176	MAX176EVKIT-DIP		82.00		MAX197EVC32-DIP**		150.00
MAX180	MAX180EVKIT-DIP**		95.00		MAX197EVC32-DIP**		150.00
MAX181	MAX180EVKIT-DIP**	MAX181CCPL	95.00		MAX197EVC32-DIP**		150.00
MAX186	MAX186EVKIT-DIP		55.00		MAX197EVC32-DIP**		150.00
	MAX186EVSYS-DIP**		150.00		MAX197EVC32-DIP**		150.00
MAX187	MAX187EVKIT-DIP		55.00		MAX197EVC32-DIP**		150.00
	MAX187EVC16-DIP**		150.00		MAX197EVC32-DIP**		150.00
MAX188	MAX188EVKIT-DIP	MAX188DCPP	55.00		MAX197EVC32-DIP**		150.00
	MAX188EVSYS-DIP**	MAX188DCPP	150.00		MAX197EVC32-DIP**		150.00

* Some kits are used to evaluate more than one device. In these cases, order the indicated EV kit and a free sample of the device you wish to evaluate.
† Future product—contact factory for pricing and availability.
†† Includes microcontroller

††† Future EV kit—contact factory for pricing and availability.

Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
††† Contact factory for pricing.

Evaluation Kit Tables

Evaluation Kit Tables

Part Number	EV Kit	Order Free Sample*	EV Kit Price† (\$)	Part Number	EV Kit	Order Free Sample*	EV Kit Price† (\$)
MAX607‡	MAX606EVKIT-MM	MAX606CUA	††	MAX737	MAX739EVKIT-DIP	MAX737CPD	20.00
MAX608‡	MAX608EVKIT-SO		††	MAX738A	MAX738EVKIT-DIP	MAX738ACPA	20.00
MAX619	MAX619EVKIT-SO		25.00		MAX738EVKIT-SO	MAX738ACWE	20.00
MAX639	MAX639EVKIT-DIP		20.00	MAX739	MAX739EVKIT-DIP		20.00
	MAX639EVKIT-SO		20.00	MAX742	MAX742EVKIT-SO		50.00
MAX640	MAX639EVKIT-DIP	MAX640CPA	20.00	MAX743	MAX743EVKIT-DIP		20.00
	MAX639EVKIT-SO	MAX640CSA	20.00	MAX744A	MAX738EVKIT-DIP	MAX744ACPA	20.00
MAX649	MAX649EVKIT-SO		35.00		MAX738EVKIT-SO	MAX744ACWE	20.00
MAX651	MAX649EVKIT-SO	MAX651CSA	35.00	MAX747	MAX747EVKIT-SO		45.00
MAX652	MAX649EVKIT-SO	MAX652CSA	35.00	MAX748A	MAX738EVKIT-DIP	MAX748ACPA	20.00
MAX653	MAX639EVKIT-DIP	MAX653CPA	20.00		MAX738EVKIT-SO	MAX748ACWE	20.00
	MAX639EVKIT-SO	MAX653CSA	20.00	MAX749	MAX749EVKIT-SO		20.00
MAX662A	MAX662EVKIT-SO	MAX662ACSA	20.00	MAX750A	MAX758EVKIT-DIP	MAX750ACPA	20.00
MAX688	MAX688EVKIT-SO		60.00		MAX758EVKIT-SO	MAX750ACSA	20.00
	MAX688EVKIT-4A		††	MAX752	MAX752EVKIT-DIP		20.00
MAX689	MAX688EVKIT-SO	MAX689CSA	60.00	MAX756	MAX756EVKIT-SO		25.00
	MAX688EVKIT-4A	MAX689CSA	††	MAX757	MAX756EVKIT-SO	MAX757CSA	25.00
MAX712	MAX712EVKIT-DIP		60.00	MAX758A	MAX758EVKIT-DIP	MAX758ACPA	20.00
MAX713	MAX712EVKIT-DIP	MAX713CPE	60.00		MAX758EVKIT-SO	MAX758ACWE	20.00
	MAX713SWEVKIT		60.00	MAX759	MAX759LCKKIT-SO		30.00
MAX716	MAX716EVKIT-SO		50.00		MAX739EVKIT-DIP	MAX759CPD	20.00
MAX717	MAX718EVKIT-SO	MAX717CSE	30.00	MAX761	MAX761EVKIT-SO		25.00
MAX718	MAX718EVKIT-SO		30.00	MAX762	MAX761EVKIT-SO	MAX762CSA	25.00
MAX719	MAX718EVKIT-SO	MAX719CSE	30.00	MAX763A	MAX738EVKIT-DIP	MAX763ACPA	20.00
MAX722	MAX722EVKIT-SO		30.00		MAX738EVKIT-SO	MAX763ACSA	20.00
MAX723	MAX722EVKIT-SO	MAX723CSE	30.00	MAX764	MAX764EVKIT-SO		35.00
MAX730A	MAX738EVKIT-DIP	MAX730ACPA	20.00	MAX765	MAX764EVKIT-SO	MAX765CSA	35.00
	MAX738EVKIT-SO	MAX730ACSA	20.00	MAX766	MAX764EVKIT-SO	MAX766CSA	35.00
MAX731	MAX731EVKIT-DIP		20.00	MAX767	MAX767EVKIT-SO		60.00
MAX732	MAX752EVKIT-DIP	MAX732CPA	20.00	MAX770	MAX770EVKIT-SO		35.00
	MAX732EVKIT-SO		20.00	MAX771	MAX770EVKIT-SO	MAX771CSA	35.00
MAX733	MAX752EVKIT-DIP	MAX733CPA	20.00	MAX772	MAX770EVKIT-SO	MAX772CSA	35.00
MAX734	MAX734EVKIT-SO		20.00	MAX774	MAX774EVKIT-SO		35.00
MAX736	MAX739EVKIT-DIP	MAX736CPD	20.00	MAX775	MAX774EVKIT-SO	MAX775CSA	35.00

* Some kits are used to evaluate more than one device. In these cases, order the indicated EV kit and a free sample of the device you wish to evaluate.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

‡ Future product—contact factory for pricing and availability.

†† Future EV kit—contact factory for pricing and availability.

Evaluation Kits (continued)

Part Number	EV Kit	Order Free Sample*	EV Kit Price† (\$)	Part Number	EV Kit	Order Free Sample*	EV Kit Price† (\$)
MAX776	MAX774EVKIT-SO	MAX776CSA	35.00	MAX859	MAX856EVKIT-MM	MAX859CUA	35.00
MAX777	MAX778EVKIT-SO	MAX777CSA	25.00	MAX863‡	MAX863EVKIT-SO		††
MAX778	MAX778EVKIT-SO		25.00	MAX866	MAX866EVKIT-MM		35.00
MAX779	MAX778EVKIT-SO	MAX779CSA	25.00	MAX867	MAX866EVKIT-MM	MAX867CUA	35.00
MAX781	MAX781EVKIT-SO		95.00	MAX877	MAX877EVKIT-SO		25.00
MAX782	MAX782EVKIT-SO		95.00	MAX878	MAX877EVKIT-SO	MAX878CSA	25.00
MAX783	MAX783EVKIT-SO		95.00	MAX879	MAX877EVKIT-SO	MAX879CSA	25.00
MAX786	MAX786EVKIT-SO		95.00	OP AMPS			
MAX796	MAX796EVKIT-SO		60.00	MAX476‡	MAX476EVKIT-SO		††
MAX797	MAX797EVKIT-SO		60.00	VIDEO PRODUCTS			
MAX799	MAX796EVKIT-SO	MAX799CSE	60.00	MAX4111	MAX4121EVKIT-SO		††
MAX830	MAX831EVKIT-SO	MAX830CWE	††	MAX4121	MAX4121EVKIT-SO	MAX4111CSA	††
MAX831	MAX831EVKIT-SO		††	MAX4221	MAX4221EVKIT-SO		††
MAX832	MAX831EVKIT-SO	MAX832CWE	††	MAX4141	MAX4141EVKIT-SO		††
MAX833	MAX831EVKIT-SO	MAX833CWE	††	MAX458	MAX459EVKIT-DIP	MAX458CPL	72.00
MAX840	MAX840EVKIT-SO		35.00	MAX459	MAX459EVKIT-DIP		72.00
MAX843	MAX840EVKIT-SO	MAX843ISA	35.00	MAX464	MAX466EVKIT-SO	MAX464CWI	67.00
MAX844	MAX840EVKIT-SO	MAX844ISA	35.00	MAX466	MAX466EVKIT-SO		67.00
MAX845	MAX845EVKIT-MM		35.00	MAX496‡	MAX497EVKIT-SO	MAX496CPE	††
MAX850	MAX850EVKIT-SO		35.00	MAX497‡	MAX497EVKIT-SO		††
MAX851	MAX850EVKIT-SO	MAX851CSA	35.00	WIRELESS PRODUCTS (High Frequency)			
MAX852	MAX850EVKIT-SO	MAX852CSA	35.00	MAX2101	MAX2101EVKIT-SO		†††
MAX853	MAX850EVKIT-SO	MAX853CSA	35.00	MAX2402	MAX2402EVKIT-SO		†††
MAX856	MAX856EVKIT-MM		35.00	MAX2430	MAX2430EVKIT-SO		††
MAX857	MAX856EVKIT-MM	MAX857CUA	35.00				
MAX858	MAX856EVKIT-MM	MAX858CUA	35.00				

Design Software

Part Number	Description	Price† (\$)	Description	Price† (\$)
MAX260SOFT	Filter design software for MAX260-MAX268	20.00	Op-Amp/Comparator P-Spice Models	FREE
MAX274SOFT	Filter design software for MAX274/MAX275	5.00		

* Some kits are used to evaluate more than one device. In these cases, order the indicated EV kit and a free sample of the device you wish to evaluate.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

‡ Future product—contact factory for pricing and availability.

†† Future EV kit—contact factory for pricing and availability.

††† Contact factory for pricing.

Wafer Inspection

All wafers are fabricated using standard processes with extremely tight control. Each wafer must pass numerous in-process checkpoints for oxide thickness, critical dimensions, pin-hole densities, and other requirements. And, each must comply with Maxim's demanding electrical and physical specifications.

Finished wafers are optically inspected for physical defects. Then they are parametrically tested to ensure full conformity to Maxim's specifications. Our precision parametric measurement capability ensures reliability and reproducibility in analog circuits. We believe this quality-control technology to be the best in the industry, capable of resolving current levels below 1pA and capacitance less than 1pF. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface-state density, and other parameters that are crucial to predicting long-term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.

Testing

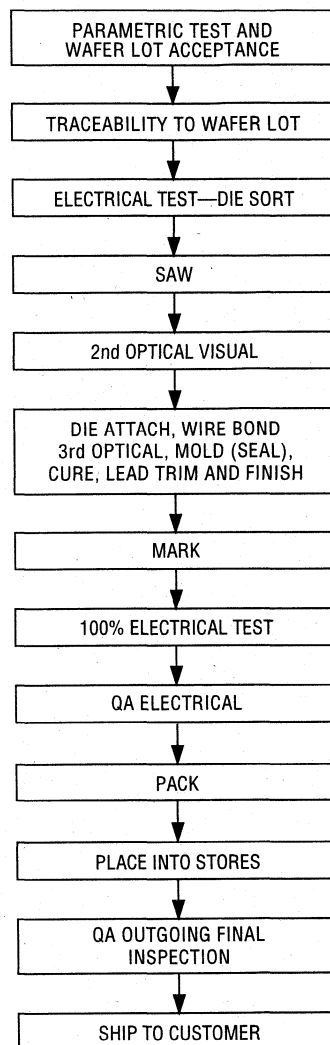
Once assembled, units are tested over temperature. This is not a common practice in the industry. Maxim uses the latest high-speed automatic handling equipment, which allows us to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data-acquisition products. Maxim's analog test capability is a significant improvement in accuracy, noise performance, and speed compared to current industry standards. This provides our customers with assurance that they will receive the part they paid for every time, without fail.

Product Conditioning and Qualification

Maxim also runs parts through qualification cycles, including accelerated life tests equivalent to 20 million operating hours and pressure/humidity cycles (85°C/85%).

Packaged Unit Process Flow



Surface-Mount Products

Maxim is committed to providing high-quality, high-reliability 8-pin to 160-pin plastic surface-mount products. Nearly every monolithic device is offered in a surface-mount package. Except for 100% burn-in and cold test, they are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels. They receive the same product conditioning and lot qualification as the DIPs. Maxim assures lot reliability by subjecting a sample from each lot to a long-term life test prior to shipment.

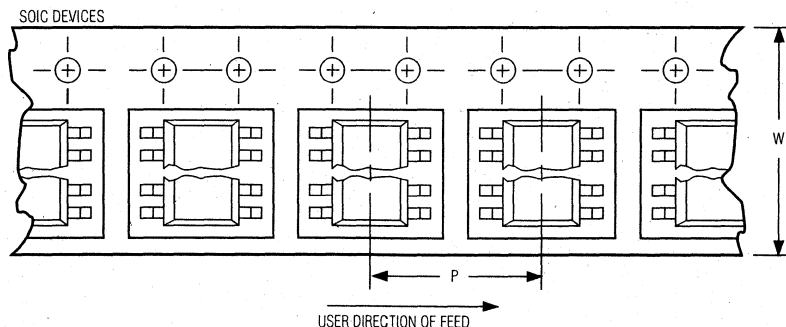
Surface-Mount Packages in Reeled Tape

Maxim surface-mount packages are shipped in anti-static plastic rails. For customers using automatic placement systems, parts also come mounted in pockets on embossed tape. The tape is wound and shipped on reels.

The table and diagram on this page indicate the tape sizes used for various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow," the standard that ensures lot quality and reliability.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
Package	Pins		
SOIC	8	12	8
	14	16	8
	16	16	8
SOIC	16	16	12
	18	24	12
	20	24	12
	24	24	12
	28	24	12
PLCC	28	24	16
	44	32	24
QFP	44	24	16
SOT	3	8	4
	4	8	4
SSOP	20	16	12
	24	16	12
	28	16	12
QFP	8	12	8



Die and Wafer Products

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet's +25°C worst-case limits.

Generally, the parameters or parameter limits listed in the product data sheets are tested during electrical probe. However, some parameters are impossible to test, or to test with absolute accuracy on unassembled product. Information regarding any of these parameters or parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	VALUE	UNITS
Chip Thickness Backlapped Wafers	15 ± 1	mils
Die Length/Width Tolerance	±1	mils
Bonding Pad Dimensions (minimum)	typical min = 3.5 x 3.5	mils
Bonding Pad and Interconnect Material Thickness	10 to 12	kÅ
Storage Temperature	-40 to +150	°C
Operating Temperature	0 to +70	°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010, Condition B, with modifications reflecting CMOS requirements.

Each die surface is protected by a passivation layer, except for bonding pads and scribe lines. Surface passivation is removed from bonding pad areas by plasma etching. The bonding pads may appear discolored at low magnification due to the aluminum's surface roughness after the etching process.

Maxim guarantees die and wafer AQL levels as follows:

Visual	1.0%
Functional Electrical Testing	0.65%
Parametric DC Testing	2.5%
Untested Parameters	6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry environment—preferably an inert gas such as nitrogen. Extreme care should be taken when handling die. An unclean environment or mishandling may result in electrical and visual failure.

Die Attach

For eutectic die attach, we recommend using a 98% gold/2% silicon preform, at a die attach temperature between 385°C and 435°C. To prevent oxidation, die attach should be done in a gaseous nitrogen ambient atmosphere. For epoxy die attach, the epoxy cure temperature should not exceed 150°C.

Bonding

When thermosonic or thermocompression gold ball bonding, use 1.0 or 1.3 mil diameter, 99.99% pure gold wire. When ultrasonic bonding, use 1.0 or 1.25 mil diameter, 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Figures 1 and 2 show how die and wafers are packaged for shipping:

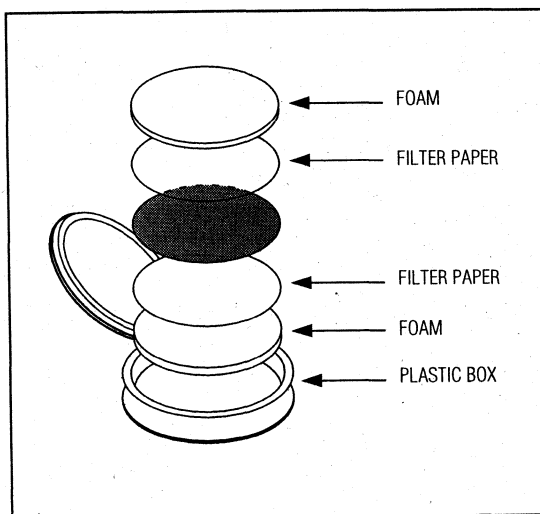


Figure 1. Wafer Carrier Package

A

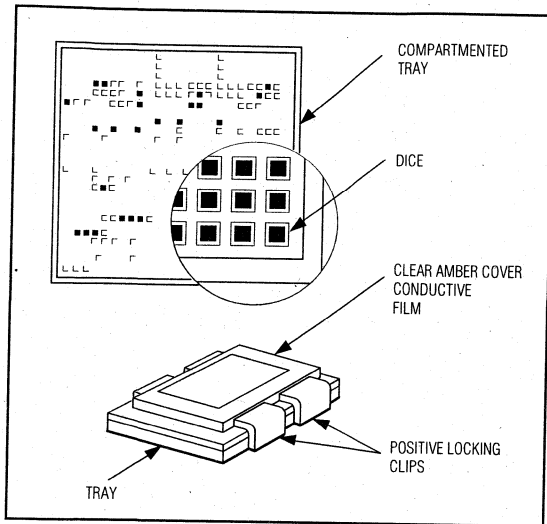


Figure 2. Die Carrier Package

Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Though these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

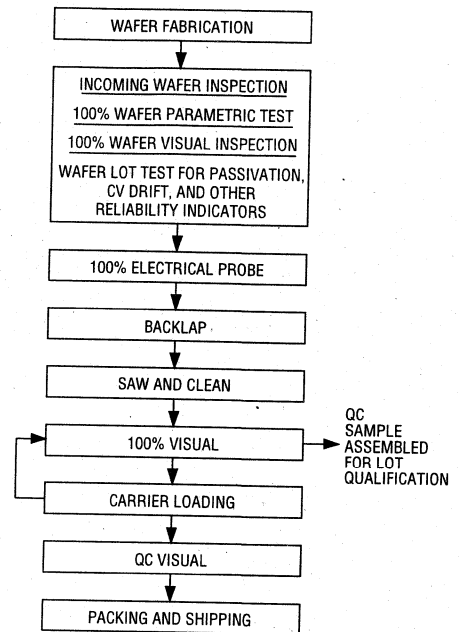
Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the date the die is shipped to the user. Maxim assumes no responsibility for the die after 75 days or after further user processing such as, but not limited to, die attach or wire bonding.

Ordering Information

Die orders are identified by a "/D" suffix. Example: ICL7109C/D.

When ordering dice as wafers, replace the "D" with a "W" in the part number. Example: MAX7231C/D die = MAX7231C/W wafer.

Die Process Flow

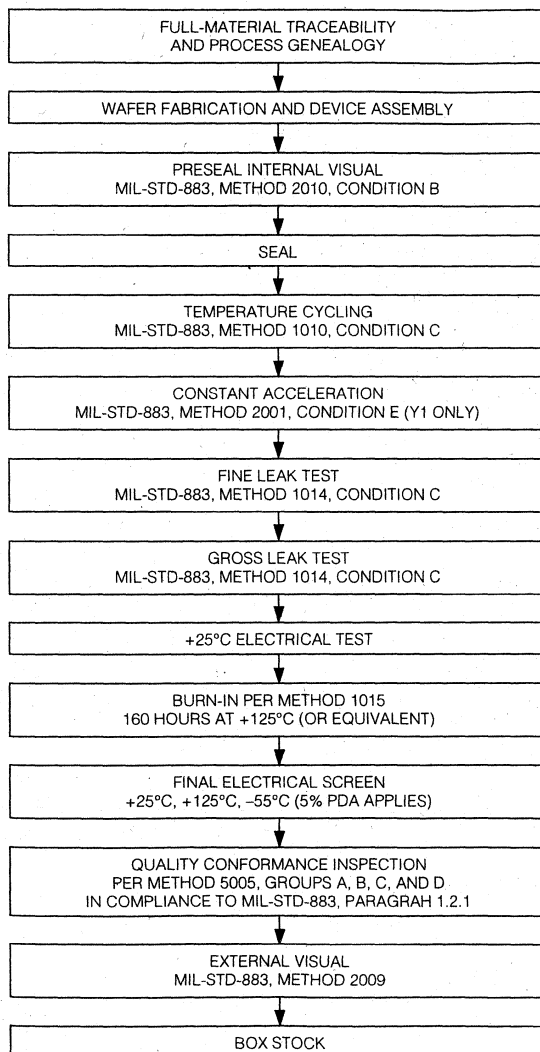


Maxim's /883 and High-Reliability Program

/883 Flow

Maxim's /883 program is fully compliant to MIL-STD-883, paragraph 1.2.1. Environmental and electrical screening are performed per Method 5004, Class B of MIL-STD-883. Quality conformance inspection is performed per method 5005 (Groups A, B, C, and D).

/883B Process Flow



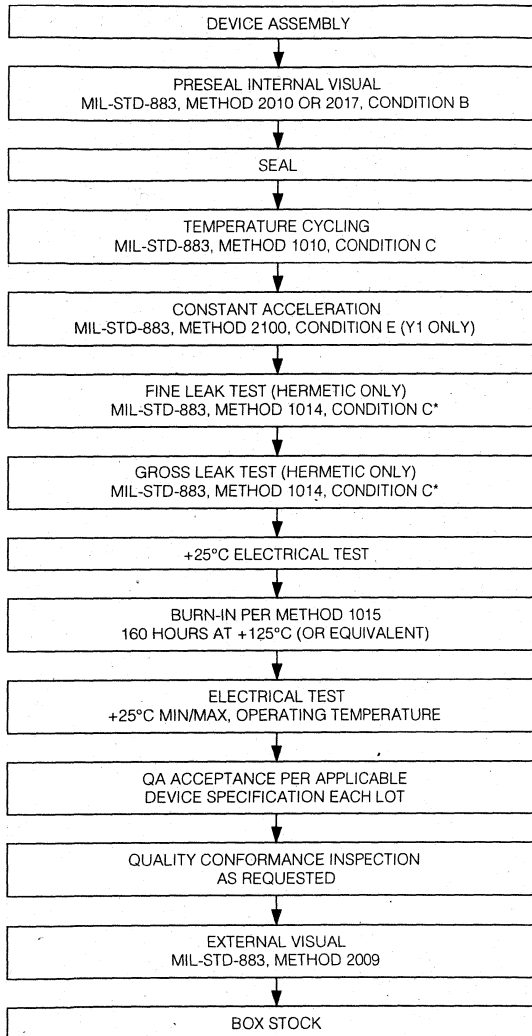
/HR Flow

Maxim's High Reliability (/HR) flow is offered for hybrid products as well as for products that have not yet been fully certified compliant to MIL-STD-883, and are therefore non-compliant. The /HR flow will not be offered for parts certified to MIL-STD-883. As seen by the adjacent flow chart, the /HR flow follows the steps and requirements of the MIL-STD-883 flow closely. Product processed to this flow is not documented in as much detail, nor does it have to adhere to the operating temperature range required by MIL-STD-883. Product may follow this flow but be tested over the commercial (0°C to +70°C) or extended (-40°C to +85°C) temperature ranges. This flow applies to hermetic packaged product only. It is Maxim's experience that this flow is desired by companies having older government projects or projects requiring an inherently higher reliability screening for critical application environments. Full QCI testing will be performed when requested. Only Group A will be performed per each inspection lot.

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Maxim's /883 and High-Reliability Program

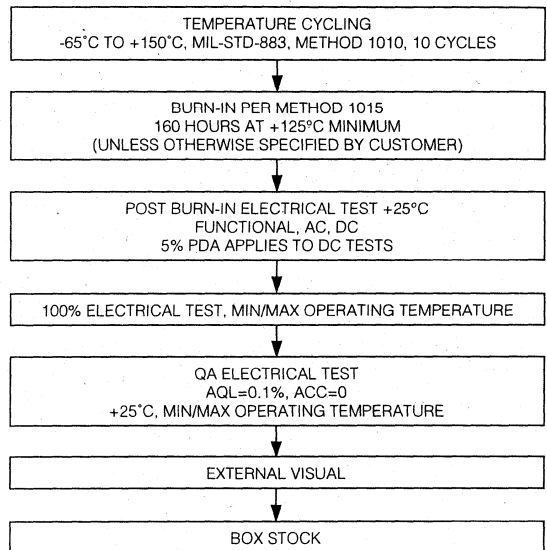
/HR Process Flow



Rugged Plastic Flow

In addition to the /883B and /HR screening flows, Maxim offers an extended rugged-plastic screening flow for plastic-encapsulated packages including SOIC package types. Products screened to this flow can be used in high-reliability applications when hermetically sealed devices screened to MIL-STD-883 may not be justified. SOICs with full burn-in and screening not only offer excellent reliability, but also save valuable PC board space. Customers should contact the factory for availability of the specific device types currently offered.

Rugged-Plastic Process Flow



* If seal perimeter is greater than 2.0 inches, Condition A applies.

Maxim's Military Program

DESC Approved Devices to Standard Military Drawings (SMDs) Currently Available

MAXIM P/N	SMD NUMBER	MAXIM P/N	SMD NUMBER	MAXIM P/N	SMD NUMBER
MAX1044	5962-38707	MAX680	5962-93120	MX7824/7828	5962-88764
MAX1232	5962-94514	MAX690/692/694	5962-90712	MXL1062	5962-91595
MAX1259	5962-93264	MAX691/693/695	5962-90711	DG201A	77053
MAX220/22/ 32A/42/43	5962-94565	MAX696/697	5962-93125	DG403	5962-89763
MAX230/1/2/4/6-9	5962-89877	MAX705-708	5962-93267	DG405	5962-89961
MAX280	5962-91595	MAX731/732/733	5962-94621	DG408/409	5962-92042
MAX310/311	5962-94556	MAX738	5962-93121	DG411/412/413	5962-90731
MAX333	5962-93180	MAX813L	5962-93267	DG417/418/419	5962-90737
MAX358	77052	MAX8211/8212	5962-90811	DG441/442	5962-92041
MAX359	5962-85131	MX536A	5962-89805	DG506A/7A/9A	5962-85131
MAX4420/4429	5962-88770	MX574A	5962-85127	DG508A	77052
MAX452-455	5962-94512	MX580	5962-86861	DG528	5962-87689
MAX500	5962-94527	MX584	5962-38128	HI-201	77053
MAX502	5962-88767	MX7226	5962-87802	ICL7660A	5962-38707
MAX543	5962-92345	MX7524	5962-87700	ICL7667	5962-87660
MAX630	5962-94540	MX7528	5962-87701	IH5040-5045	81006
MAX631/632/633	5962-92141	MX7537	5962-87763	IH5047	81006
MAX634	5962-92124	MX7541	5962-89481	IH5140-5145	81006
MAX638	5962-92127	MX7545	5962-87702	IH5148/5149	81006
MAX660	5962-94632	MX7547	5962-89657	REF01	5962-89581
MAX663/4/6/7	5962-92126	MX7572	5962-87591	REF02	85514
MAX674	5962-94681	MX7574	5962-89616	TSC426/427/428	5962-88503
		MX7820	5962-88650		

Parts Currently /883 Compliant

MAX1044	MAX280	MAX663/4/6/7	MX7225/7226	DG441/442
MAX122	MAX291	MAX674	MX7501/2/3	DG506A-509A
MAX1232	MAX310/311	MAX680	MX7520/1/4/8	DG528/529
MAX1259	MAX333	MAX690-697	MX7533/7537	HI-201/201HS
MAX154/158	MAX358/359	MAX690A/692A	MX7541/2/3/5/7	ICL7660A/7667
MAX160/161	MAX378/379	MAX691A/693A	MX7572/7574	IH5040-5049
MAX170/172	MAX4420/4426-9	MAX705-708	MX7624/7628	IH5050/5051
MAX176	MAX452-455	MAX730-733	MX7820/1/4/8	IH5140-5145
MAX180/181	MAX481/483/485	MAX738	MXL1062	IH5147/5148/5151
MAX186/188	MAX500	MAX805L	DG200A/201A/202	IH5341/5352
MAX220/222	MAX502	MAX813L	DG300A-309	OP07
MAX230/231/232	MAX516	MAX8211/8212	DG381A/4A/7A	REF01/02
MAX232A	MAX526/527	MX536A	DG390A	TSC426/427/428
MAX234	MAX543	MX565	DG401/403/405	
MAX236-239	MAX626/627/628	MX574A	DG406-409	
MAX242/243	MAX630-634/638	MX580/581/584	DG411/412/413	
MAX274	MAX660	MX674A	DG417/418/419	

A

Product Numbering Systems

Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped into categories, according to their functions. Maxim currently adds a "MAX" prefix to the part's unique number. The categories are as follows (with some exceptions):

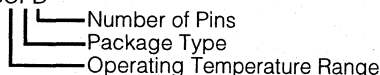
MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface Products and Analog Filters
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op Amps, Buffers, and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power-Supply Circuits and Voltage Ref.
MAX700-799	μ P Peripherals and Display Drivers
MAX800-899	μ P Supervisory
MAX900-999	Comparators

Within each category, blocks of numbers are reserved for subgroups.

3-Letter Suffixes

EXAMPLE:

MAX358CPD



4-Letter Suffixes

When a part has a four-letter suffix, the first letter of the suffix denotes product grade. For example, the first "A" in MAX631ACPA indicates 5% output accuracy; the remaining three letters denote temperature range, package type, and number of pins. Therefore, the MAX631ACPA has 5% output accuracy, operates over the 0°C to +70°C range, comes in a plastic DIP package, and has eight pins.

Temperature Ranges

"C"	0°C to +70°C	"E"	-40°C to +85°C
"I"	-20°C to +85°C	"M"	-55°C to +125°C

Package Type

"A"	SSOP (Shrink Small-Outline Package)
"B"	CERQUAD
"C"	TO-220, TQFP (Thin Quad Flat Pack)
"D"	Ceramic Sidebrazed
"E"	QSOP (Quarter Small-Outline Package)
"F"	Ceramic Flat Pack
"H"	Module
"J"	CERDIP Dual-In-Line
"K"	TO-3, PPGA
"L"	LCC (Leadless Ceramic Chip Carrier)
"M"	Plastic Quad Flat Pack

"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	PLCC (Plastic Leaded Chip Carrier)
"R"	Narrow CERDIP (300 mil)
"S"	Small Outline (150 mil)
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-99, TO-100)
"U"	TSSOP, μ MAX, SOT
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"X"	J Leaded Ceramic Chip Carrier (JLCC)
"Y"	Narrow Sidebrazed (300 mil)
"Z"	TO-92, MQAD
"D"	Dice
"PR"	Rugged Plastic
"W"	Wafer

Number of Pins

"A"	8	"N"	18
"B"	10, 64	"P"	20
"C"	12	"Q"	2, 100
"D"	14	"R"	3, 84
"E"	16	"S"	4, 180
"F"	22	"T"	6, 160
"G"	24	"U"	60
"H"	44	"V"	8 (0.200" pin circle, isolated case)
"I"	28	"W"	10 (0.230" pin circle, isolated case)
"J"	32	"X"	36
"K"	5, 68	"Y"	8 (0.200" pin circle, isolated case)
"L"	40	"Z"	10 (0.230" pin circle, isolated case)
"M"	48, 7		

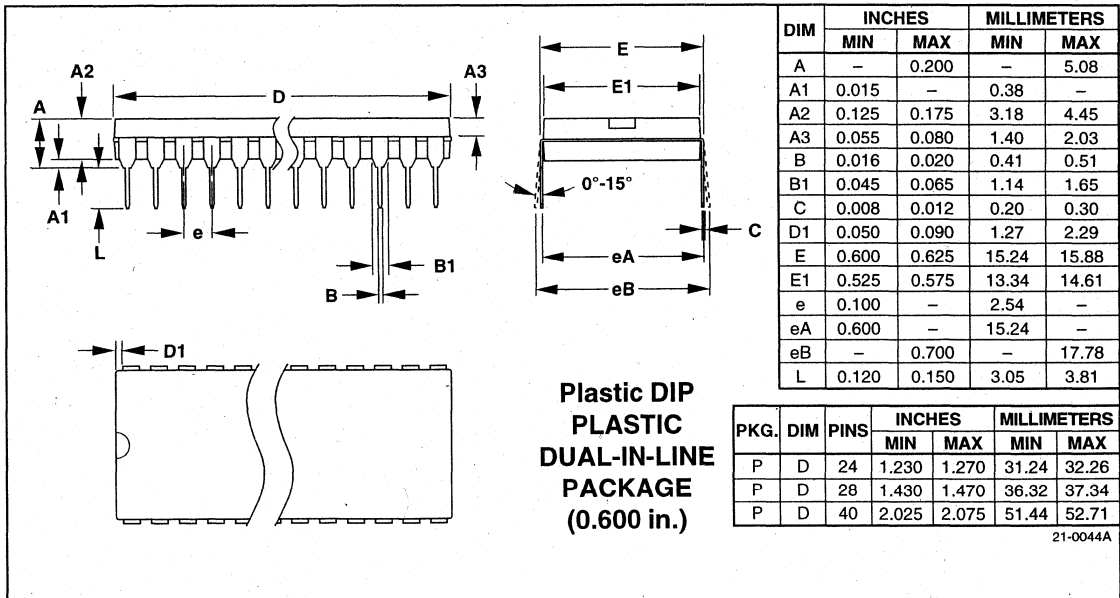
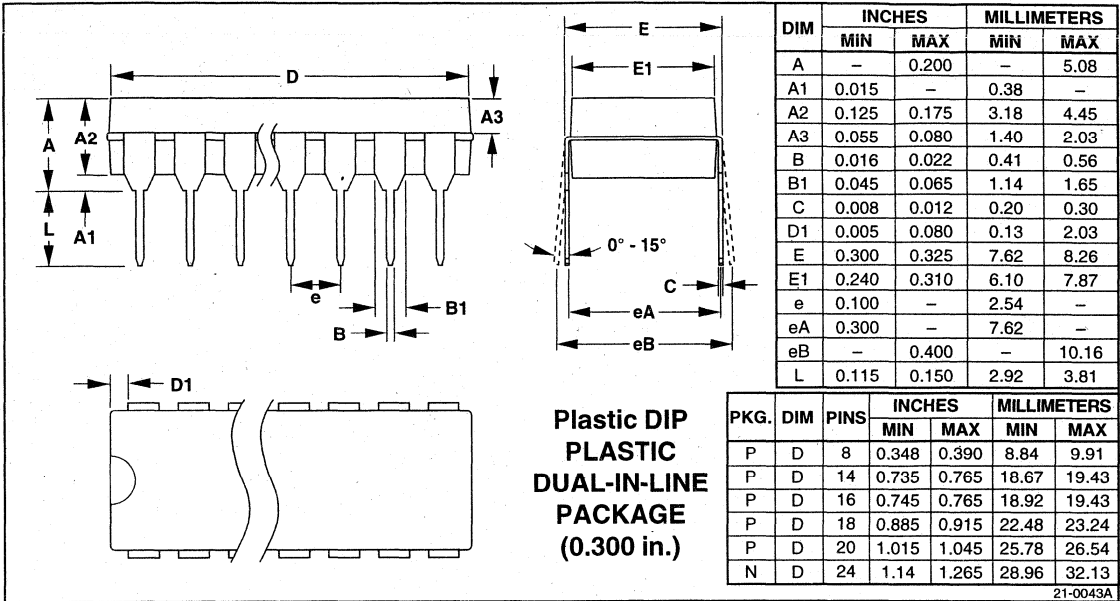
Second-Source Numbering System

In most cases, Maxim's part number for a second-source product follows the industry's most widely accepted numbering system for that particular part, rather than our own convention. This includes the most commonly recognized prefix as well as the original designators for product grade, temperature range, package type, and number of pins.

Maxim frequently supplies second-source products in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, these devices are given a part number that follows the original numbering convention.

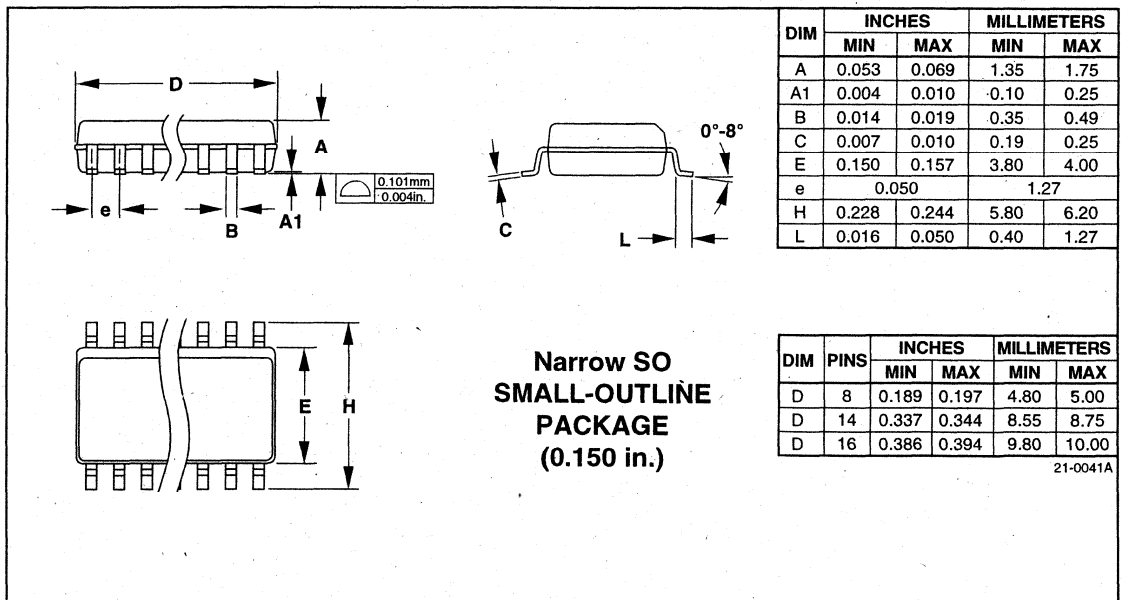
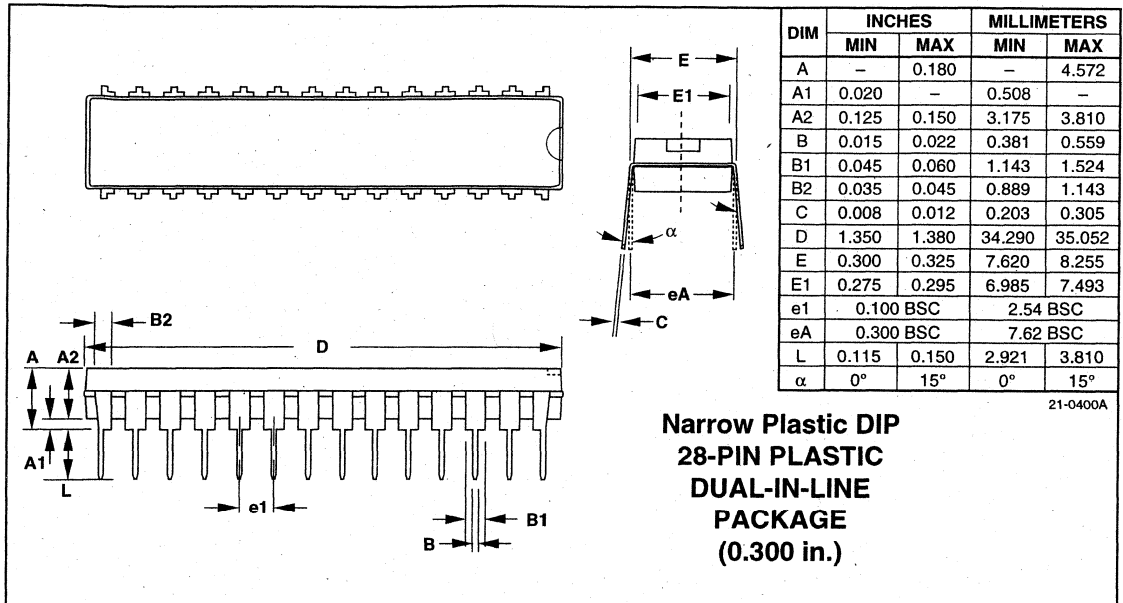
Package Information

This section contains physical dimensions for all packages currently supplied by Maxim.

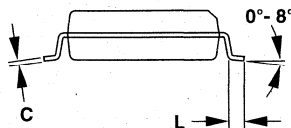
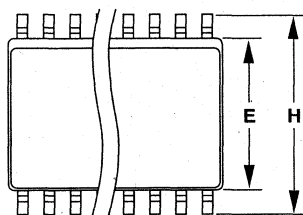
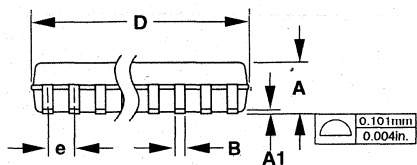


A

Package Information



Package Information

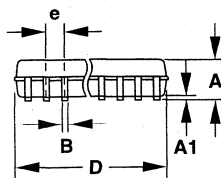
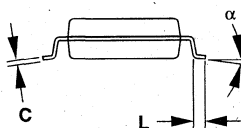
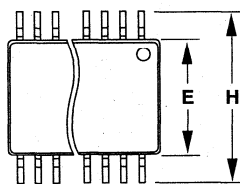


**Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

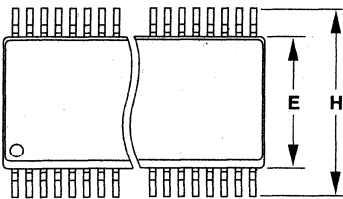
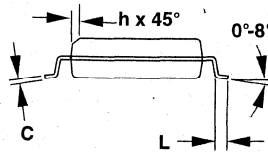
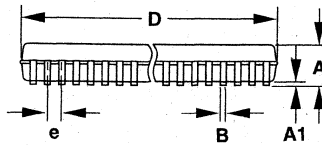


**SSOP
SHRINK
SMALL-OUTLINE
PACKAGE**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

21-0056A

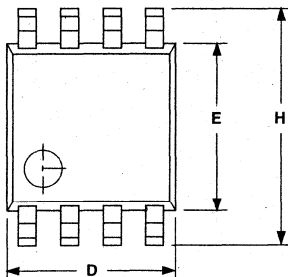
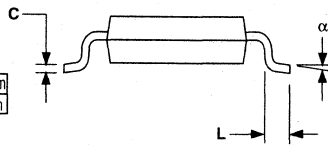
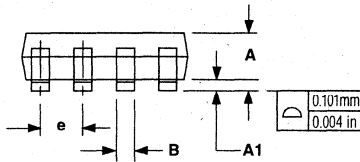


**SSOP
SHRINK SMALL-OUTLINE
PACKAGE**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
D	SEE VARIATIONS			
E	0.292	0.298	7.42	7.57
e	0.0315		0.800	
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	36	0.604	0.610	15.34	15.49
D	44	0.702	0.708	17.83	17.98

21-0040A

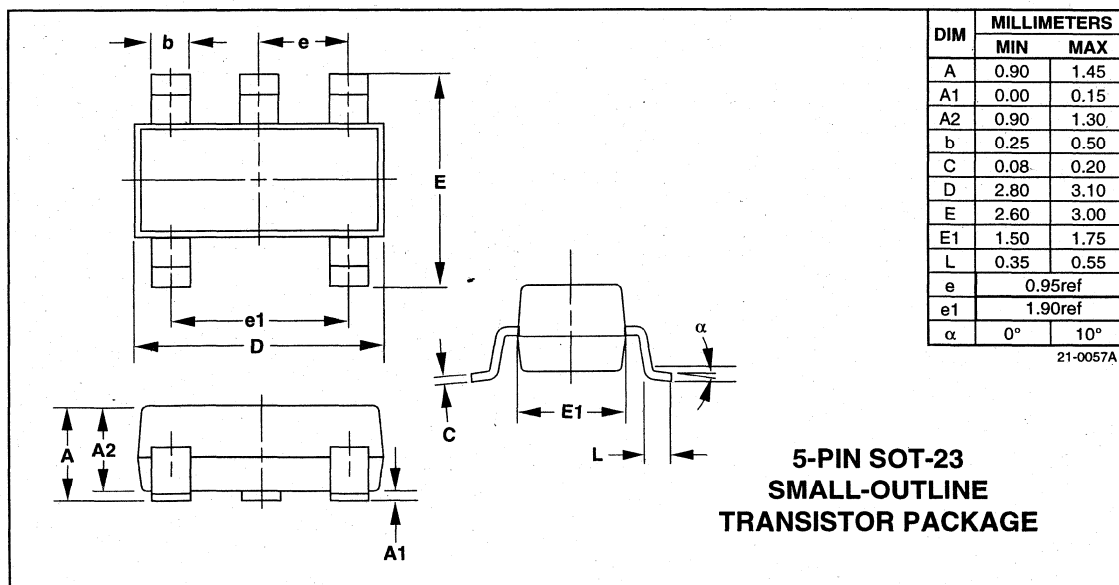
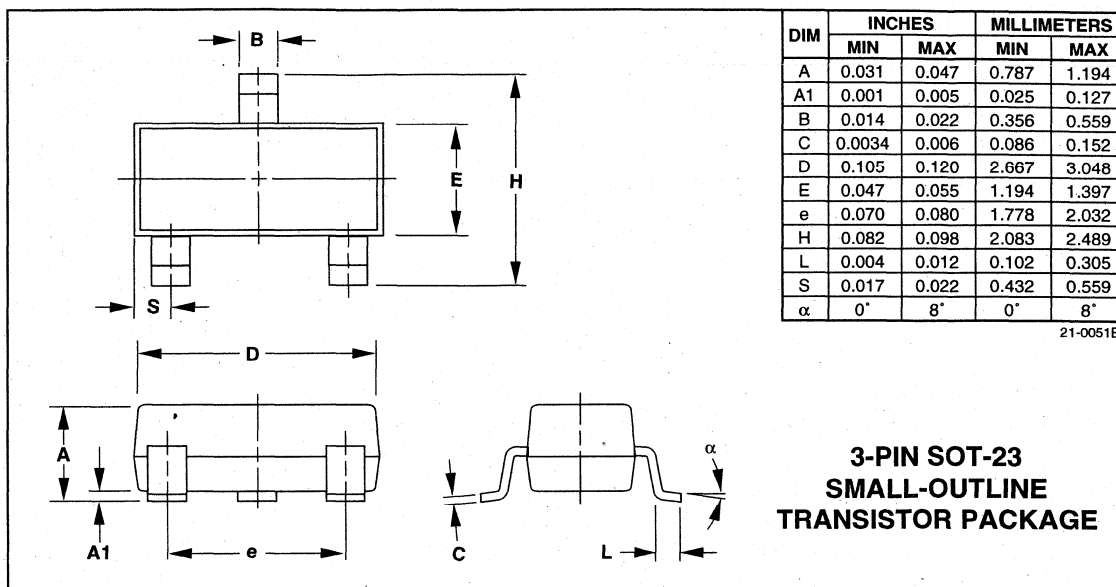


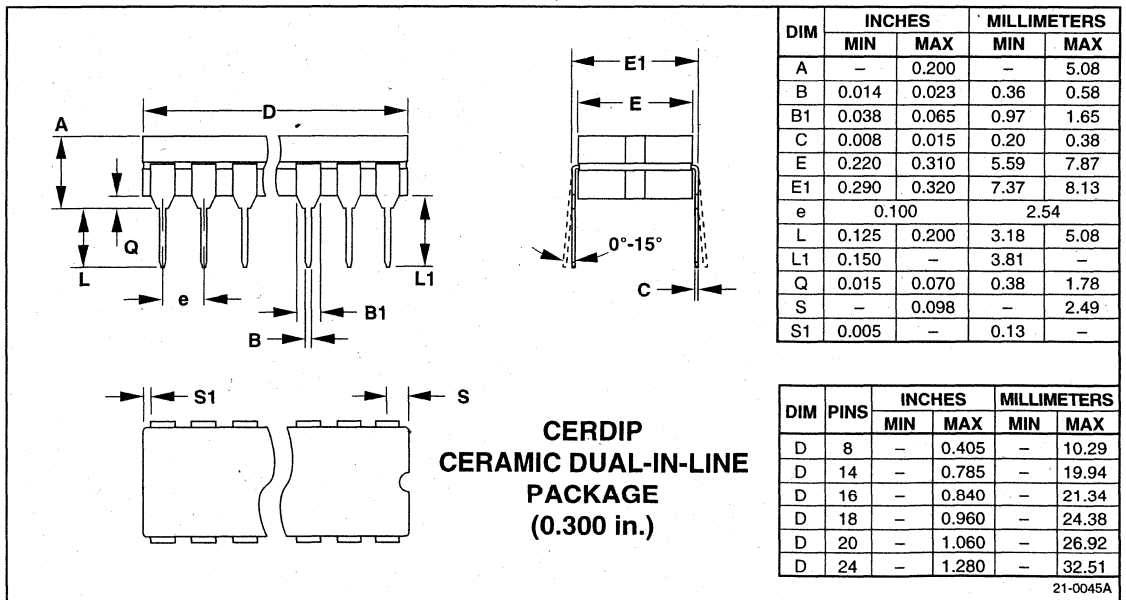
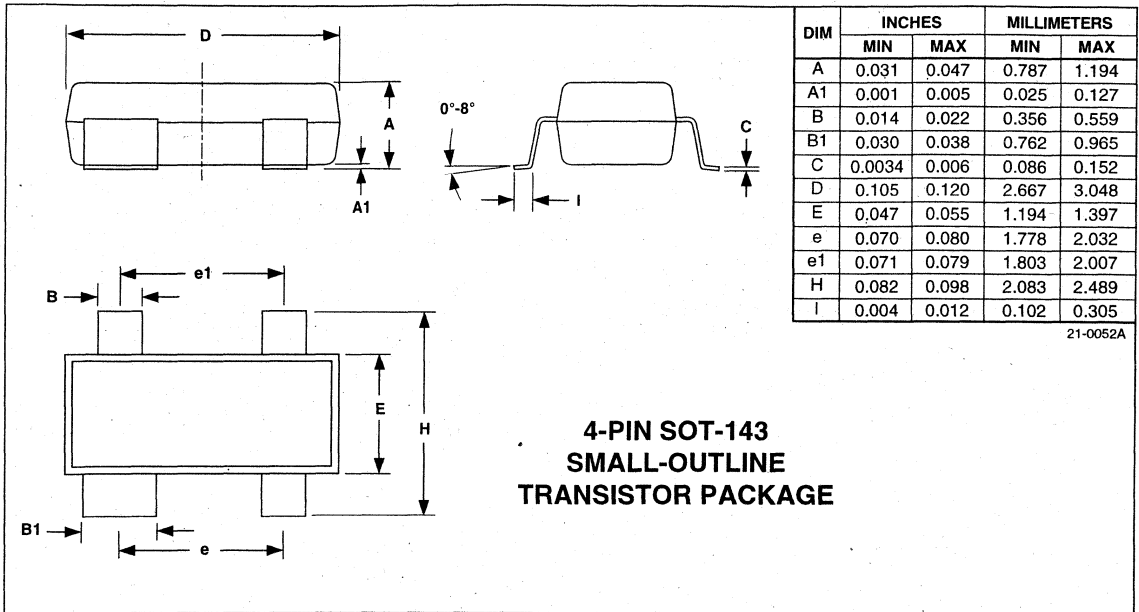
**8-PIN μMAX
MICROMAX SMALL-OUTLINE
PACKAGE**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

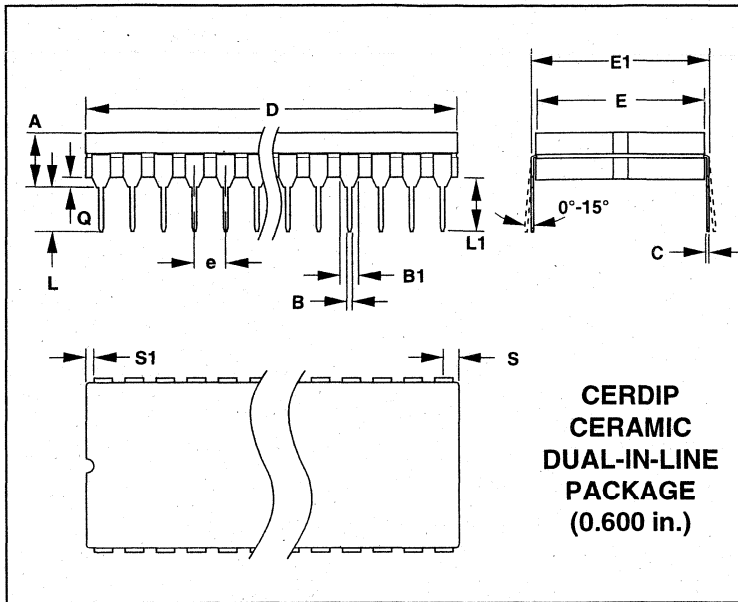
21-0036D

Package Information





Package Information

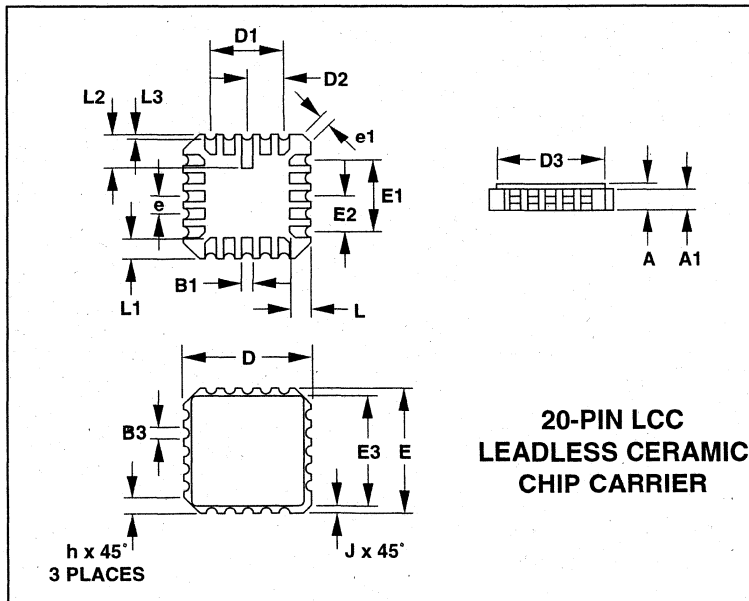


**CERDIP
CERAMIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.232	—	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.500	0.620	12.70	15.75
E1	0.590	0.630	14.99	16.00
e	0.100		2.54	
L	0.120	0.200	3.05	5.08
L1	0.150	—	3.81	—
Q	0.015	0.075	0.38	1.91
S	—	0.100	—	2.54
S1	0.005	—	0.13	—

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	—	1.290	—	32.77
D	28	—	1.490	—	37.85
D	40	—	2.096	—	53.24

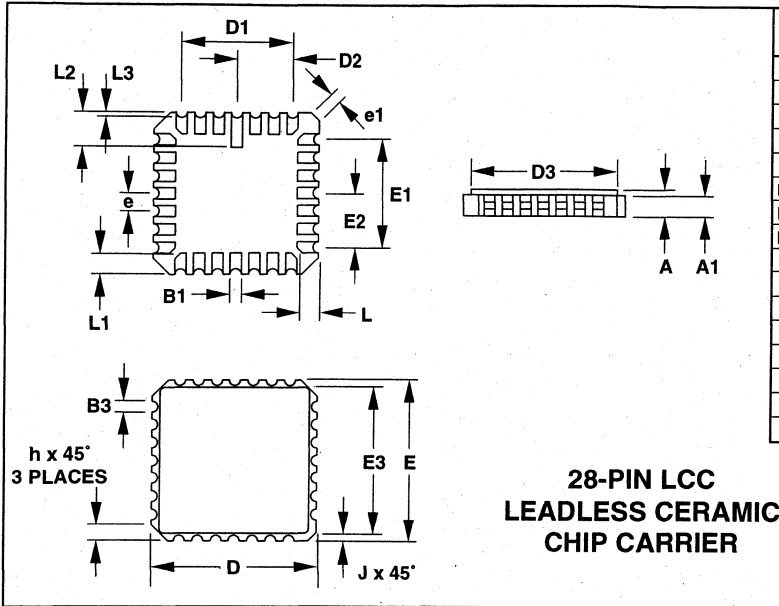
21-0046A



**20-PIN LCC
LEADLESS CERAMIC
CHIP CARRIER**

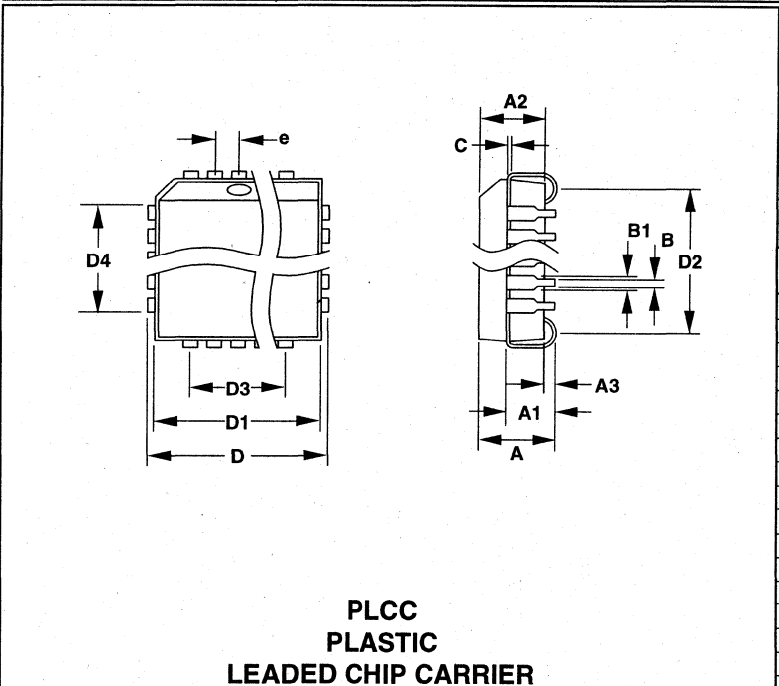
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.342	0.358	8.69	9.09
D1/E1	0.200 BSC		5.08 BSC	
D2/E2	0.100 BSC		2.54 BSC	
D3/E3	—	0.350	—	9.09
e	0.050 BSC		1.27 BSC	
e1	0.015	—	0.38	—
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

21-658A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300		7.62	
D2/E2	0.150		3.81	
D3/E3	—	0.460	—	11.68
e	0.050		1.27	
e1	0.015	—	0.38	—
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

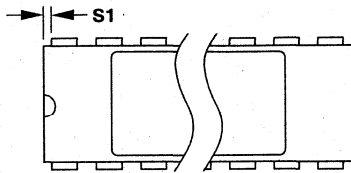
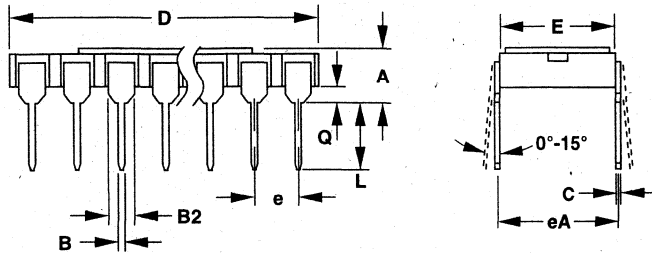
21-4497A



DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
A		0.165	0.180	4.19	4.57
A1		0.090	0.120	2.29	3.05
A2		0.145	0.156	3.68	3.96
A3		0.020	—	0.51	—
B		0.013	0.021	0.33	0.53
B1		0.026	0.032	0.66	0.81
C		0.009	0.011	0.23	0.28
e		0.050		1.27	
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3	28	0.200	REF	5.08	REF
D		0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2	44	0.390	0.430	9.91	10.92
D3		0.300	REF	7.62	REF
D4		0.300	—	7.62	—
D	68	0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2		0.590	0.630	14.99	16.00
D3	88	0.500	REF	12.70	REF
D4		0.470	—	11.94	—
D		0.985	0.995	25.02	25.27
D1	108	0.950	0.958	24.13	24.33
D2		0.890	0.930	22.61	23.62
D3		0.800	REF	20.32	REF
D4	128	0.625	—	15.87	—

21-0049B

Package Information

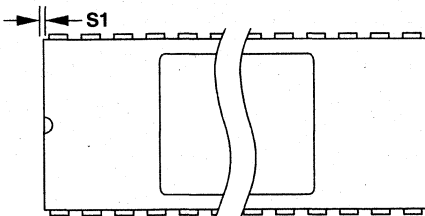
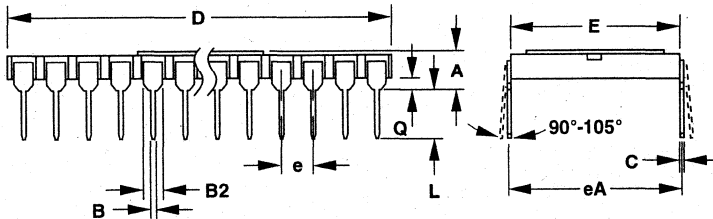


**Ceramic SB
CERAMIC SIDEBRAZE
PACKAGE
(0.300 in.)**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
eA	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	—	0.13	—

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	—	0.550	—	13.97
D	14	—	0.785	—	19.94
D	16	—	0.840	—	21.34
D	18	—	0.960	—	24.38
D	20	—	1.060	—	26.92
D	24	—	1.280	—	32.51

21-0047A



**Ceramic SB
CERAMIC SIDEBRAZE
PACKAGE
(0.600 in.)**

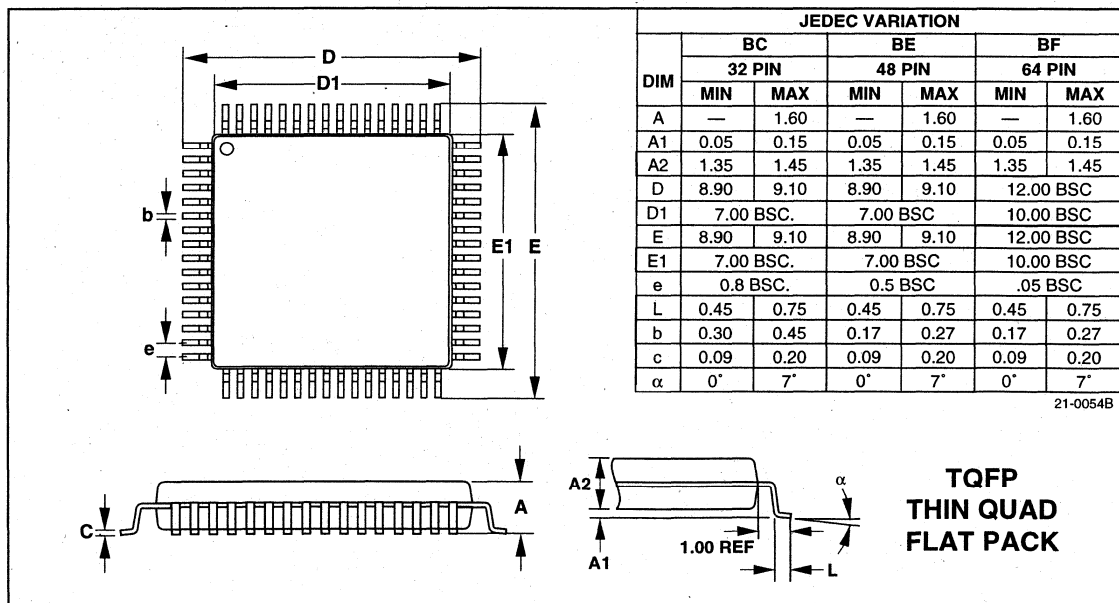
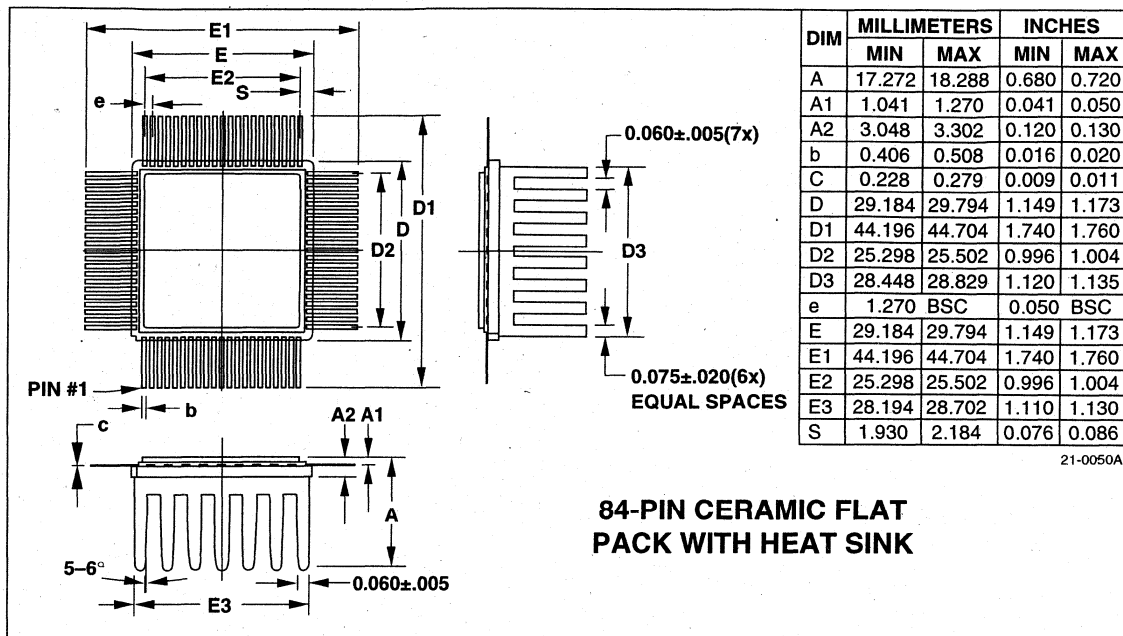
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.510	0.610	12.95	15.49
eA	0.600		15.24	
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	—	0.13	—

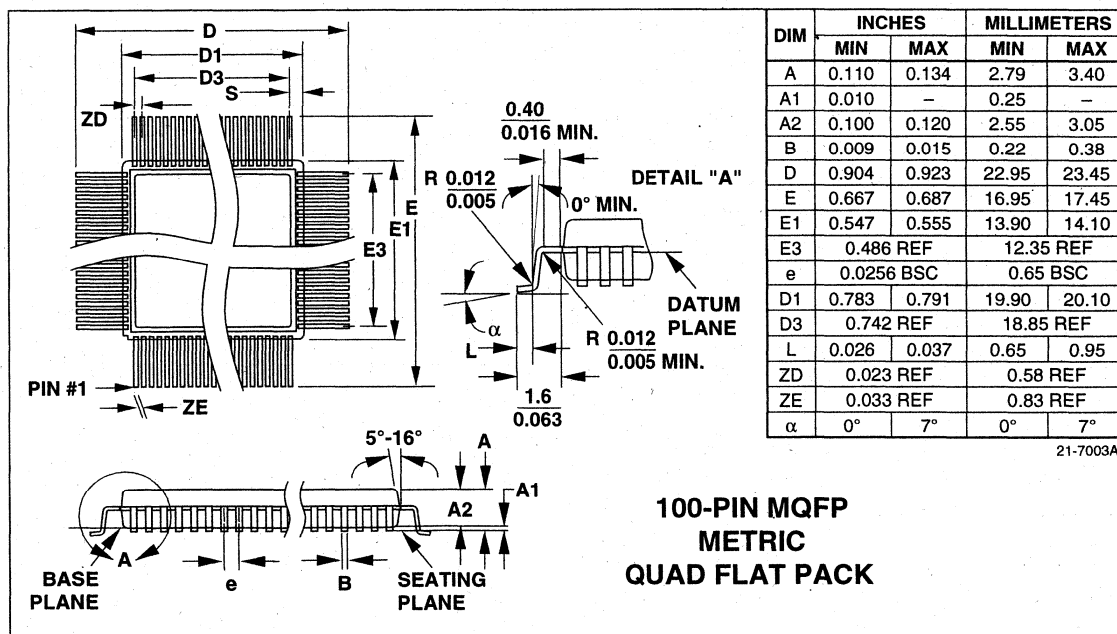
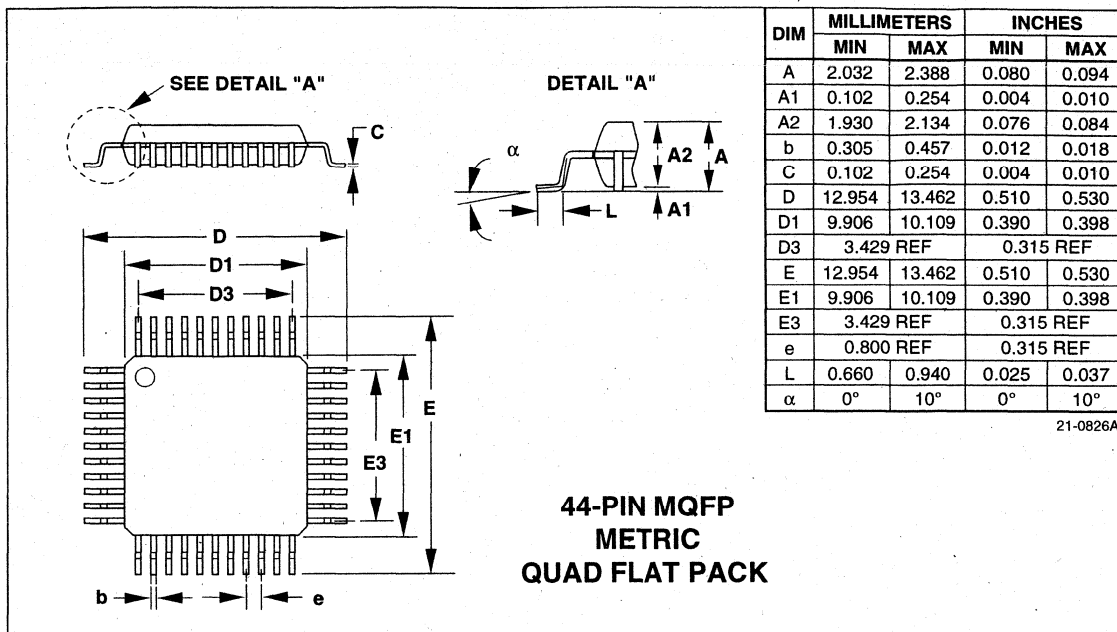
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	—	1.29	—	32.77
D	28	—	1.49	—	37.85
D	40	—	2.096	—	53.24

21-0048A

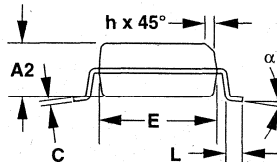
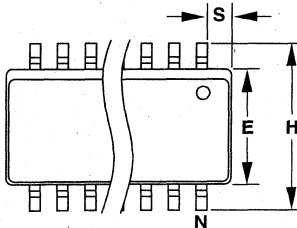
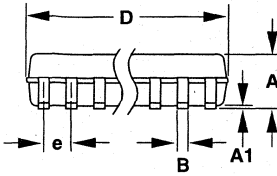
A

Package Information





Package Information

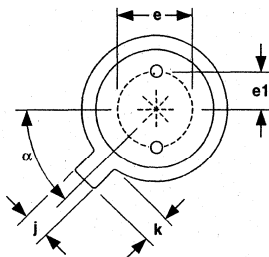
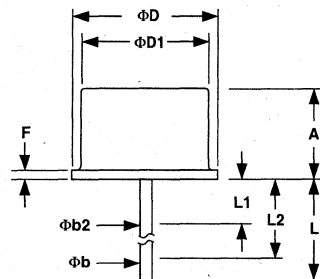


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.127	0.25
A2	0.055	0.061	1.40	1.55
B	0.008	0.012	0.20	0.31
C	0.0075	0.0098	0.19	0.25
D	SEE VARIATIONS			
E	0.150	0.157	3.81	3.99
e	0.25 BSC		0.635 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.189	0.196	4.80	4.98
S	16	0.0020	0.0070	0.05	0.18
D	20	0.337	0.344	8.56	8.74
S	20	0.0500	0.0550	1.27	1.40
D	24	0.337	0.344	8.56	8.74
S	24	0.0250	0.0300	0.64	0.76
D	28	0.386	0.393	9.80	9.98
S	28	0.0250	0.0300	0.64	0.76

21-0055A

QSOP QUARTER SMALL-OUTLINE PACKAGE

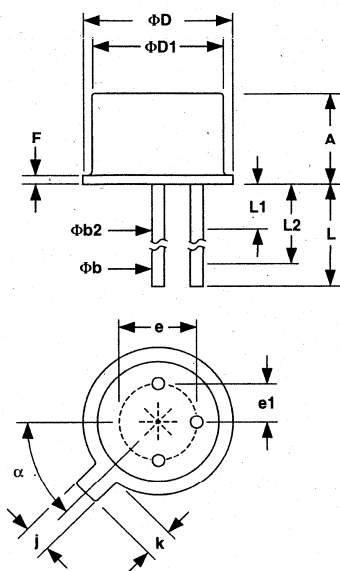


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.115	0.150	2.92	3.81
Φb	—	0.021	—	0.533
Φb2	0.016	0.019	0.406	0.483
ΦD	0.209	0.230	5.31	5.84
ΦD1	0.178	0.195	4.52	4.95
e	0.100		2.54	
e1	0.050		1.27	
F	—	0.030	—	0.762
j	0.036	0.046	0.914	1.17
k	0.028	0.048	0.711	1.22
L	0.500	—	12.70	—
L1	—	0.050	—	1.27
L2	0.250	—	6.35	—
α	45°		45°	

21-0020A

2-PIN TO-52 PACKAGE

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.115	0.150	2.92	3.81
Φb	—	0.021	—	0.533
$\Phi b2$	0.016	0.019	0.406	0.483
ΦD	0.209	0.230	5.31	5.84
$\Phi D1$	0.178	0.195	4.52	4.95
e	0.100		2.54	
e1	0.050		1.27	
F	—	0.030	—	0.762
j	0.036	0.046	0.914	1.17
k	0.028	0.048	0.711	1.22
L	0.500	—	12.70	—
L1	—	0.050	—	1.27
L2	0.250	—	6.35	—
α	45°		45°	

21-0019A

**3-PIN TO-52
PACKAGE**

A

